Design and Simulation of a "Traffic Light Simulator" Using 5-bit Counter and Decoder

Overview

This project simulates a **4-way traffic light controller** using **T Flip-Flops** as a counter and a **5-to-32 line decoder**.
The counter generates sequential binary states, and the decoder activates one output line per state.
Logic gates combine these outputs to control **Red, Yellow, and Green lights** for each road direction.

Apparatus Required:

- 5 × T Flip-Flops (for 5-bit counter)
- 5-to-32 Decoder
- Logic Gates (OR)
- LED Indicators (Red, Yellow, Green)
- Clock Pulse Generator
- Logisim software

Theory:

A traffic light controller can be designed using **sequential logic circuits**.

- The **T Flip-Flop counter** acts as a timer that cycles through 32 states (0–31).
- The **Decoder** ensures that exactly one line is HIGH for each state.
- The **Logic Network** assigns specific output combinations to control the lights:
    - States 0–7 → North = Green
    - States 8–9 → North = Yellow
    - States 10–17 → East = Green
    - States 18–19 → East = Yellow

- States 20–27 → South = Green
- States 28–29 → South = Yellow
- States 30–31 → West = Green

Each set of outputs turns ON/OFF the corresponding LEDs.

Working:

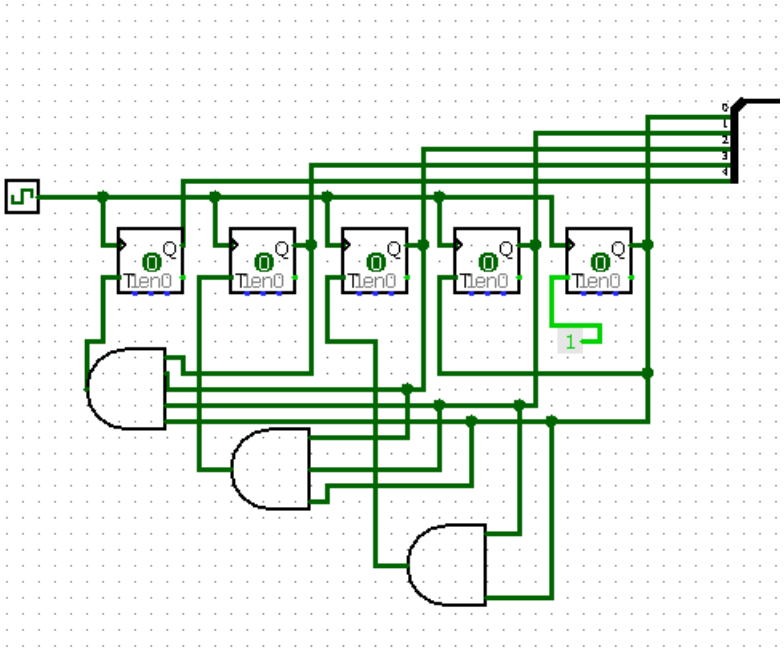
1. The counter advances on each clock pulse.
2. Decoder activates a unique output line.
3. The logic gates interpret these lines to drive traffic lights in the correct sequence.
4. The pattern repeats continuously, simulating a real-world traffic signal cycle.

Truth Table:

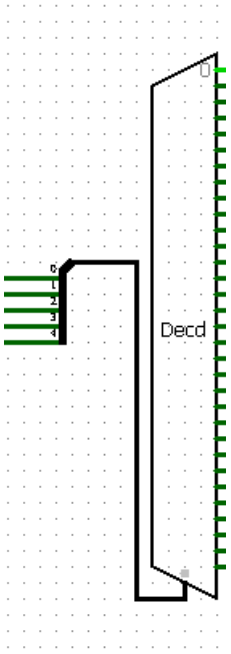
State (Binary)	Active Output (Decoder)	North	East	South	West
00000–00111	D0–D7	Green	Red	Red	Red
01000–01001	D8–D9	Yellow	Red	Red	Red
01010–10001	D10–D17	Red	Green	Red	Red
10010–10011	D18–D19	Red	Yellow	Red	Red
10100–11011	D20–D27	Red	Red	Green	Red
11100–11101	D28–D29	Red	Red	Yellow	Red
11110–11111	D30–D31	Red	Red	Red	Green

Circuit Diagram:

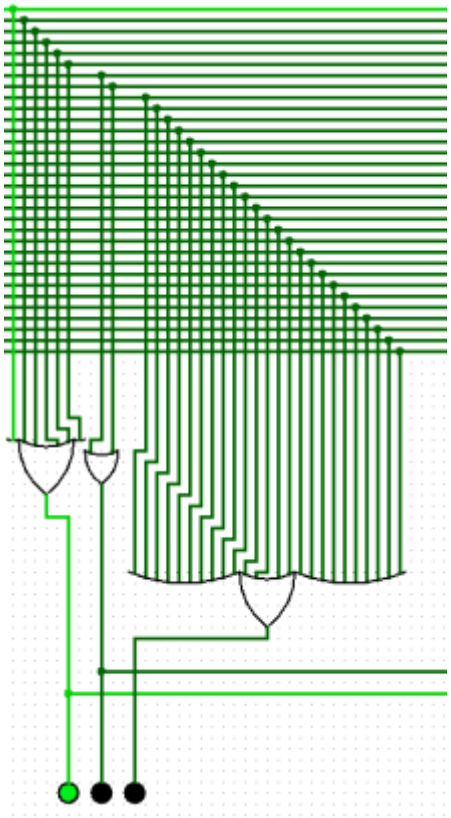
- Counter circuit:



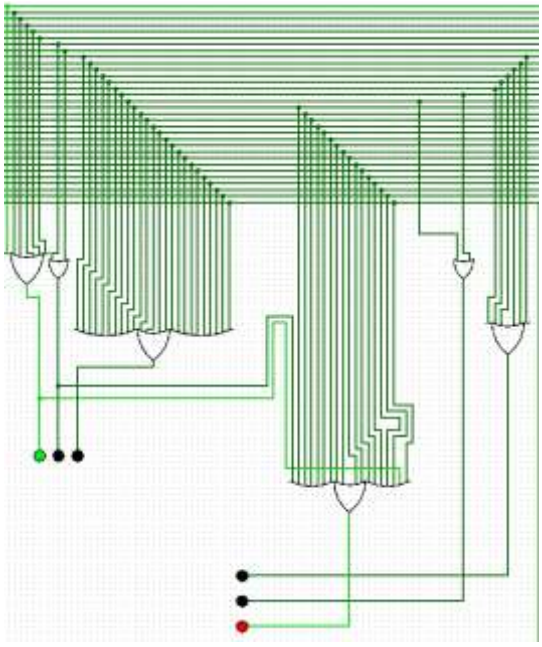
- Decoder circuit:



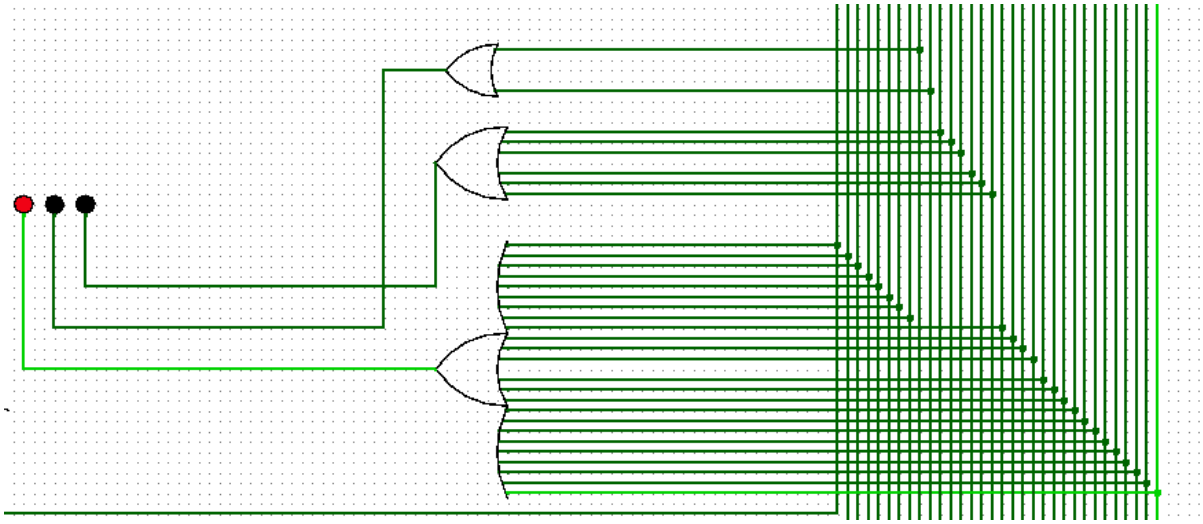
- Logic for North Direction:



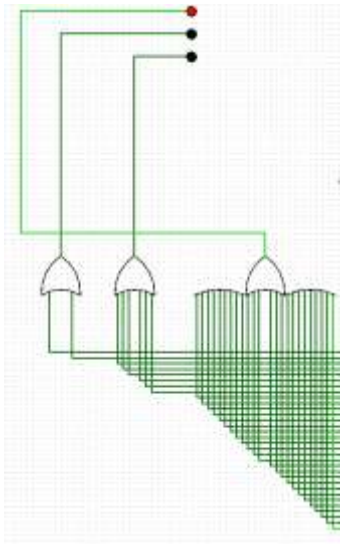
- Logic for East Direction:



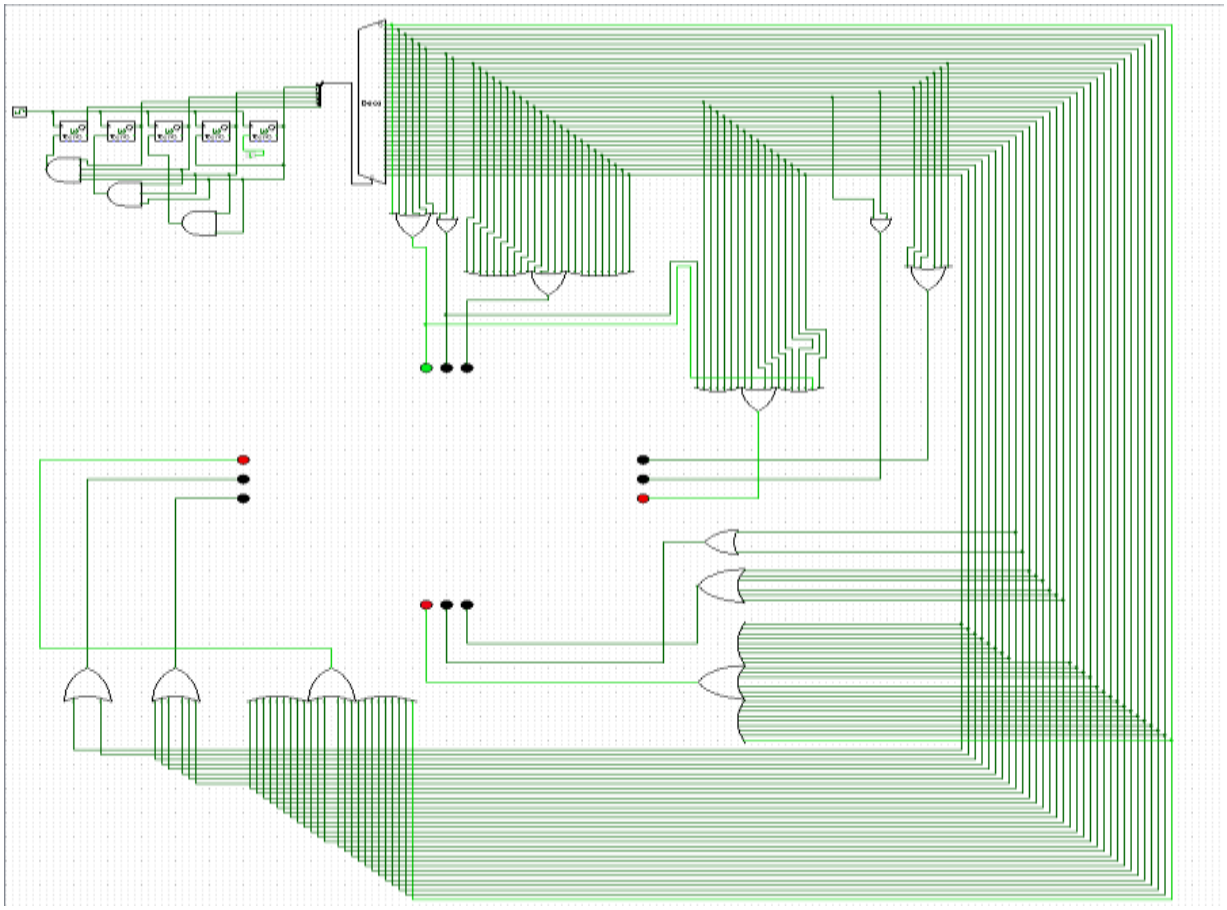
- Logic for South Direction:



- Logic for West Direction:



- Entire circuit:



Applications:

- Real-time traffic control systems.
- Embedded systems or microcontroller interfacing.
- Sequential logic learning and simulation.
- FPGA implementation for smart intersections.

Conclusion:

The project successfully demonstrates how **sequential (flip-flop counter)** and **combinational logic (decoder and gates)** can be combined to design an automatic traffic signal control system.
It serves as a foundation for advanced real-time embedded traffic systems.

By,

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