ESC201: Lecture 16

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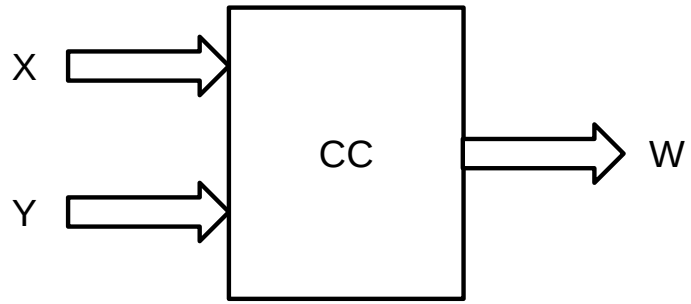
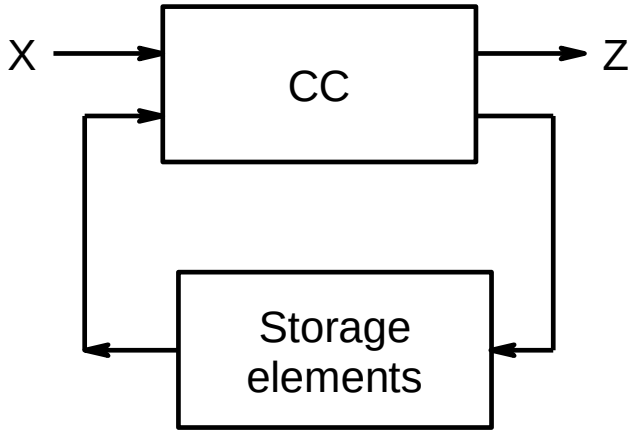
Digital Circuits

Combinational Circuits

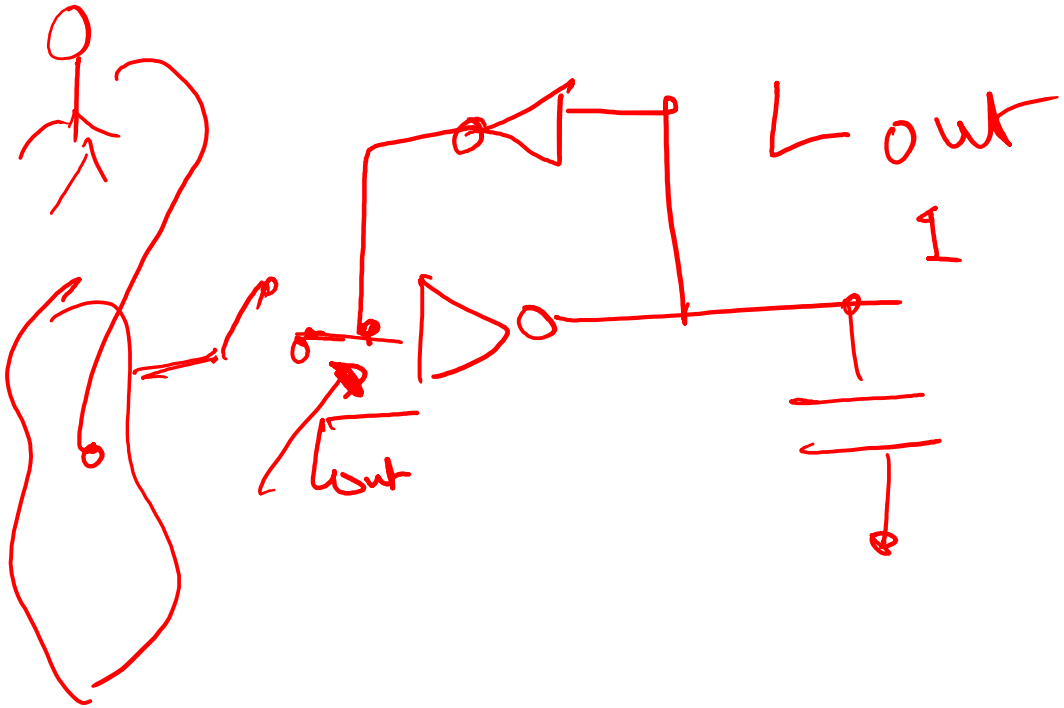


Output is determined by current values of inputs only.

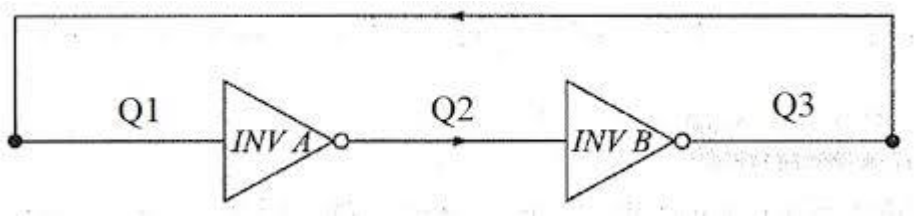
Sequential Circuits



Output is determined in general by current values of inputs and past values of inputs/outputs as well.

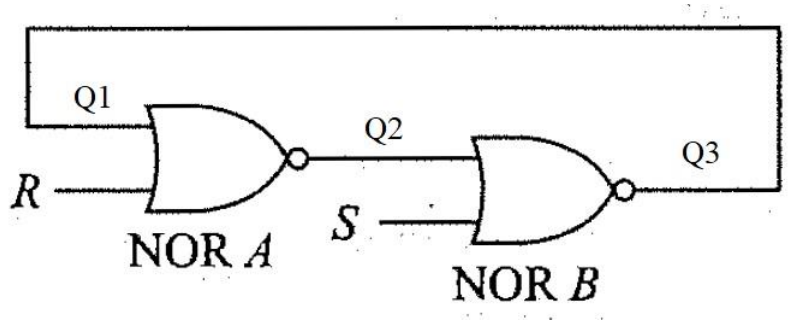

Lout
1
Lout

Memory with Set/Reset Knob

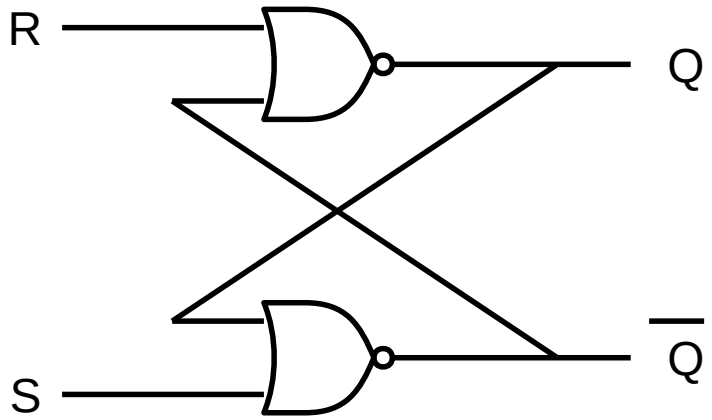


Two memory states are possible:
1. Q1=Q3=0 (Low), Q2=1 (High)
2. Q1=Q3= 1 (High), Q2= 0 (Low)

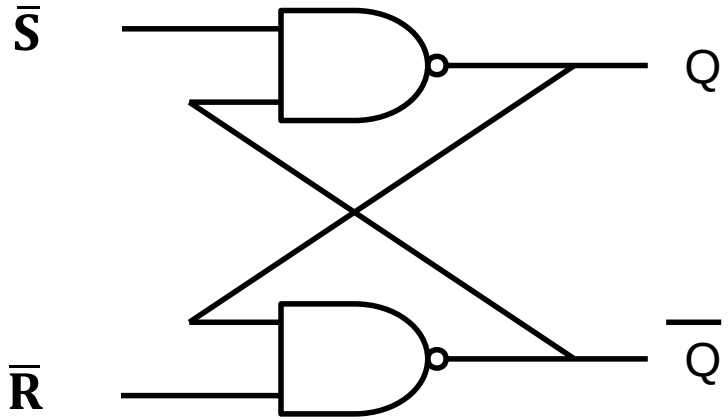
But how will one change the state?



We need at least 2 i/p logic gates
- NOR gate behave like INV if one i/p is 0
- NAND behaves like INV if one i/p is 1

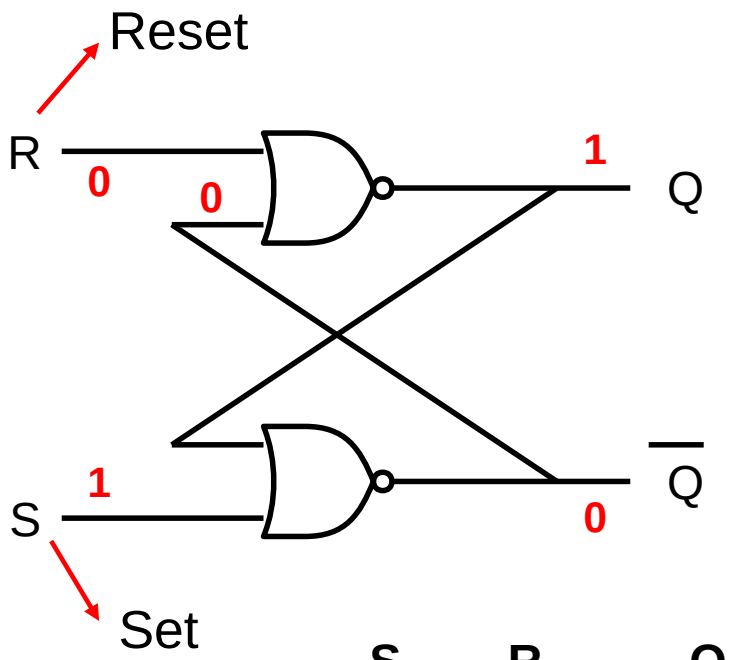


NOR-based SR Latch



NAND-based SR Latch

Set-Reset (SR) Latch: Set State



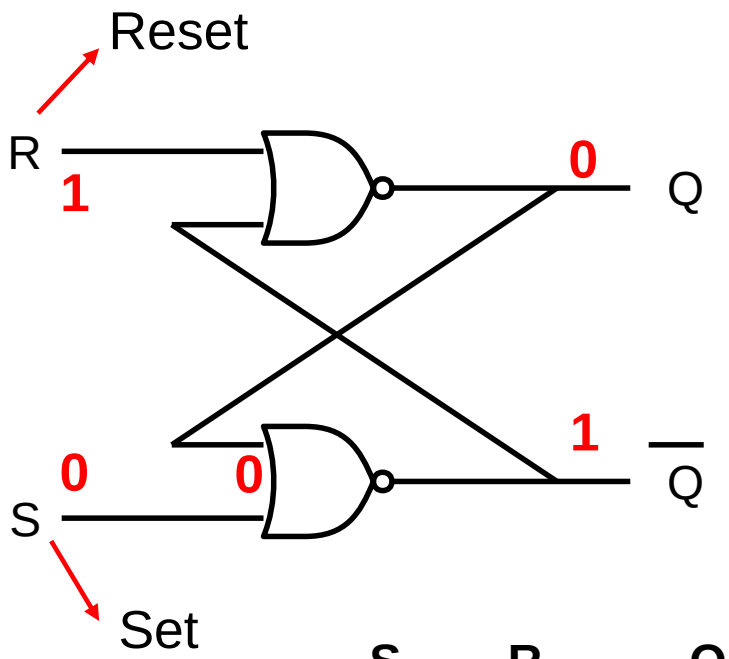
$$Q = 1; \overline{Q} = 0 \quad \text{Set State}$$

$$Q = 0; \overline{Q} = 1 \quad \text{Re set State}$$

$$\overline{1 + Q} = 0$$

S	R	Q	$\overline{Q}$	State
1	0	1	0	SET

Set-Reset (SR) Latch: Reset State



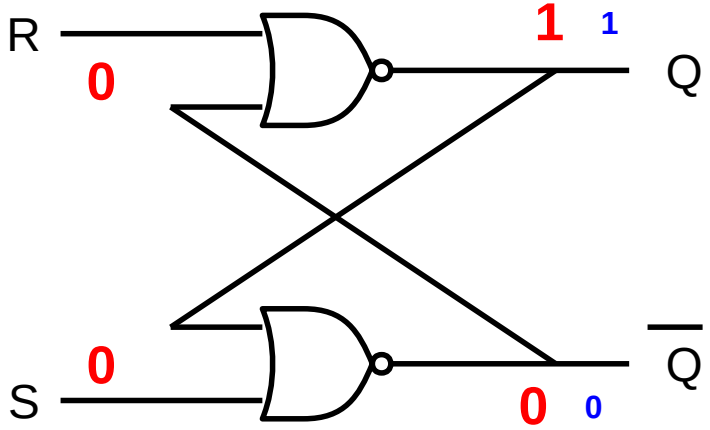
$Q = 1; \overline{Q} = 0$ Set State

$Q = 0; \overline{Q} = 1$ Re set State

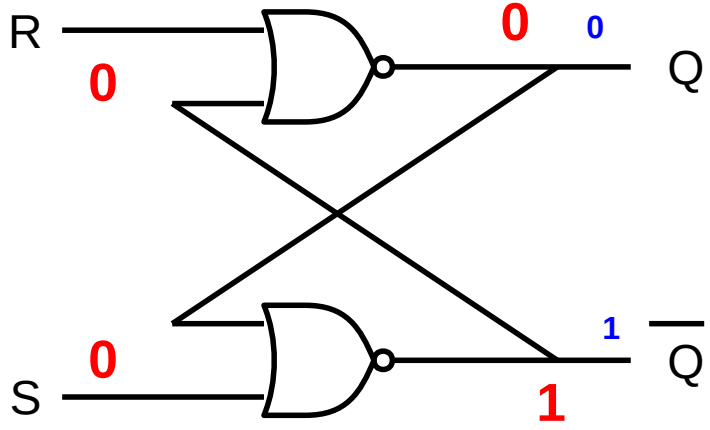
$$\overline{1 + \bar{Q}} = 0$$

S	R	Q	$\overline{Q}$	State
1	0	1	0	SET
0	1	0	1	RESET

SR Latch: 'Hold' (memory)

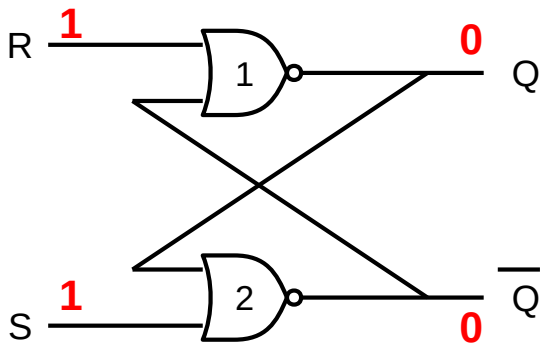


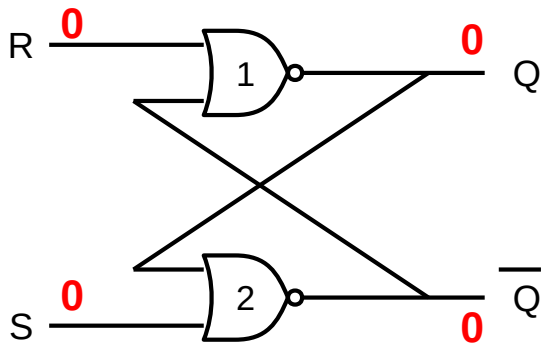
S	R	Q	$\overline{Q}$	State
1	0	1	0	SET
0	0	1	0	HOLD

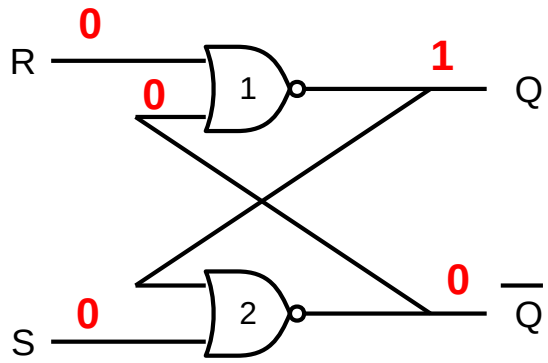


S	R	Q	$\overline{Q}$	State
1	0	1	0	SET
0	0	1	0	HOLD
0	1	0	1	RESET
0	0	0	1	HOLD

SR Latch: Invalid Input and Gate Delays



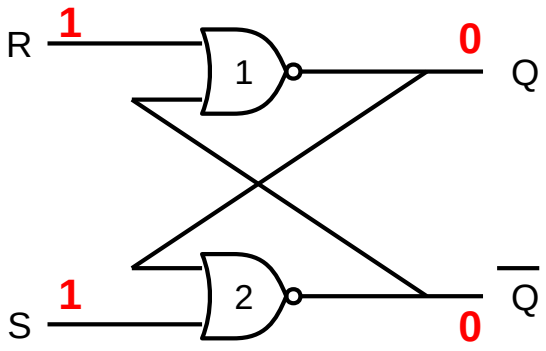


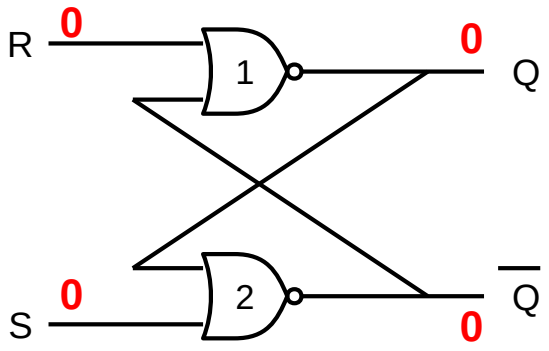


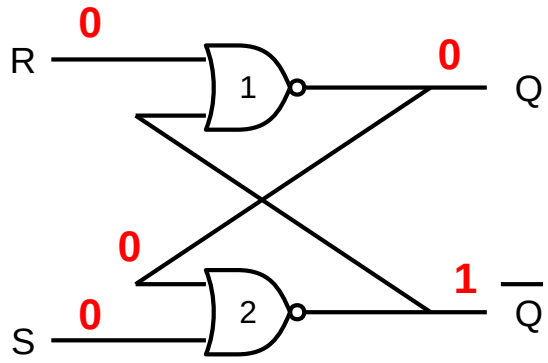
Suppose gate-1 is faster

Q = 1

On the other hand suppose that gate-2 is faster.

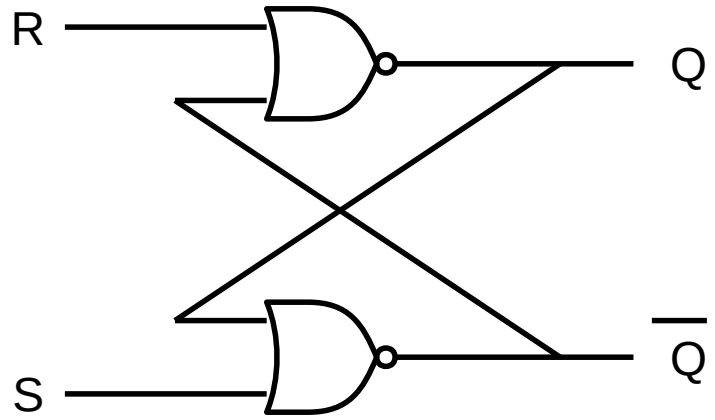




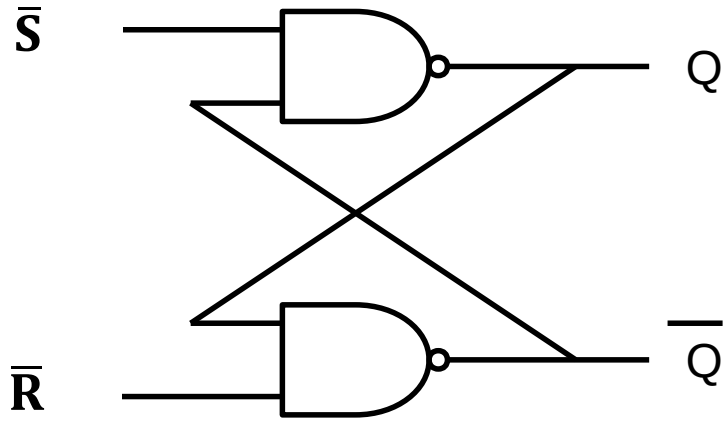


Again the output is unpredictable in general

NOR-based vs NAND-based SR Latch

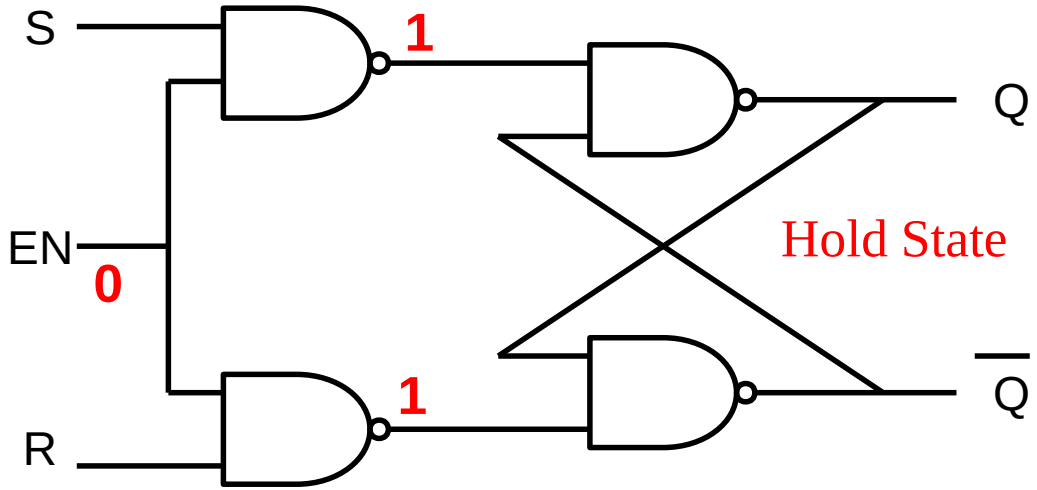


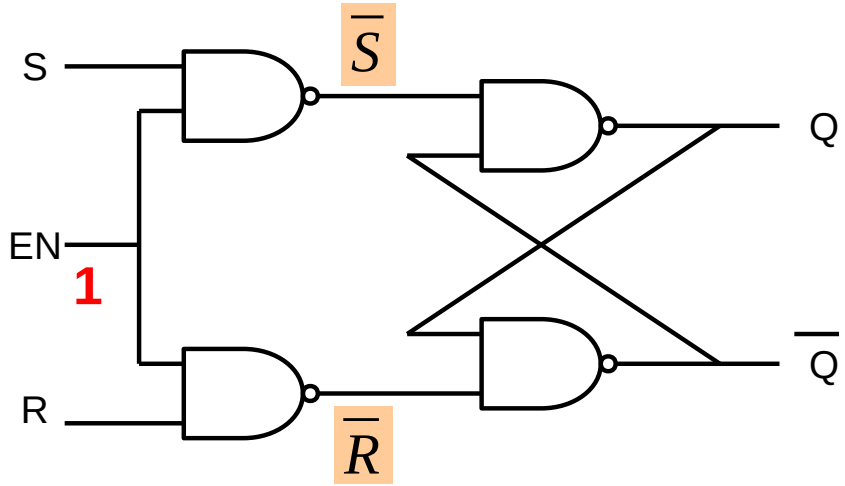
S	R	Q	$\overline{Q}$	State
1	0	1	0	SET
0	1	0	1	RESET
0	0	Q	$\overline{Q}$	HOLD
1	1	0	0	INVALID



$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	State
0	1	1	0	SET
1	0	0	1	RESET
1	1	Q	$\overline{Q}$	HOLD
0	0	1	1	INVALID

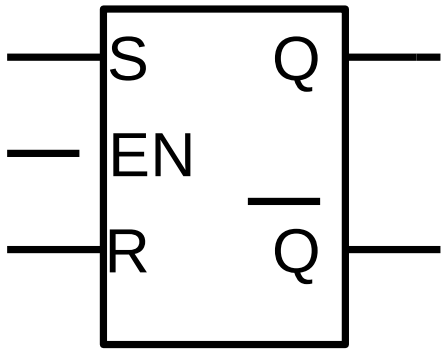
NAND-based SR Latch with Enable

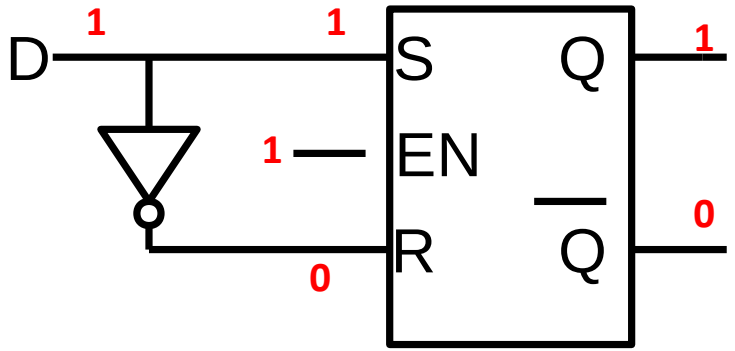




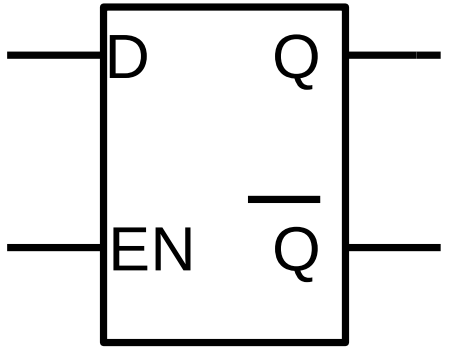
Enable	S	R	Q	$\overline{Q}$	State
0	x	x	Q	$\overline{Q}$	Hold
1	1	0	1	0	Set
1	0	1	0	1	Reset
1	0	0	Q	$\overline{Q}$	Hold
1	1	1	0	0	Invalid

D latch





Enable	S	R	Q	$\overline{Q}$	State
0	x	x	Q	$\overline{Q}$	Hold
1	1	0	1	0	Set
1	0	1	0	1	Reset
1	0	0	Q	$\overline{Q}$	Hold
1	1	1	0	0	Invalid



If EN = 1 then Q = D otherwise the latch is in Hold state

Synchronous Sequential Circuits