DD Assignment Group-68

Topic 12

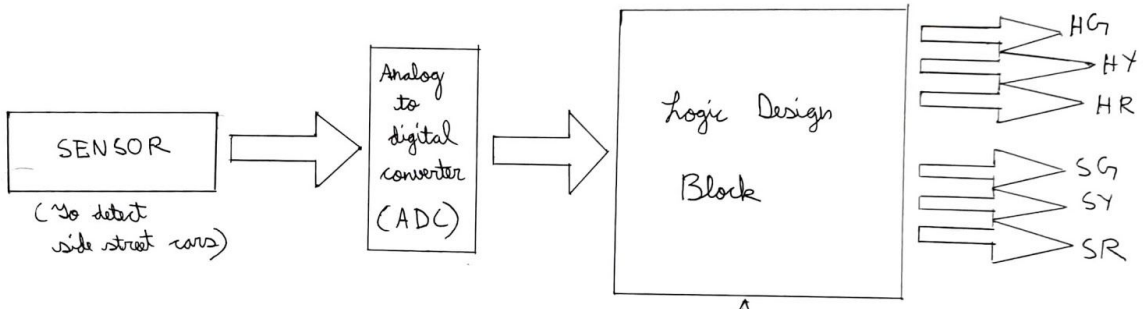
Prepared by:

2019AAPS0230G - RAHUL PETER
2019AAPS0235G - AGRAWAL KRISHI AJAYKUMAR
2019AAPS0242G - NEELAREDDY SIDDARTHA REDDY
2019AAPS0247G - SARTHAK CHAKRABARTI
2019AAPS0250G - SAYAN DUTTA PRAMANIK
2019AAPS0257G - SARVESHWAR MAHAPATRO

Index:

Question: Design a traffic signal system at a junction of 2 roads, a highway and a side street. The signal system should be designed in such a way so as to not impede traffic on the highway. The signal must switch only when a car shows up on the side street.

Top level block diagram:



SR NO.	Legend	
1.	SENSOR	Sensor detecting cars on side street
2.	CLK	Periodic clock signal
3.	HG	Highway green light
4.	HY	Highway yellow light
5.	HR	Highway red light
6.	SG	Side street green light
7.	SY	Side street yellow light
8.	SR	Side street red light

Assumptions(Strategy):

1. In the initial state, the highway lights must be Green (state HG) and the side road light must be Red (state SR). The lights must remain at this state for at least 3 clock cycles before any change of lights can occur.

2. When a car is detected on the side road approaching the junction, the highway lights should cycle from Green (HG) to Red (state HR) through Yellow (state HY) , and the side road light should be Green (state SG) during this duration. Cycling to and from state HY should take one clock cycle each.
3. The side road lights are to remain Green (SG) only while the car sensor signal(SENSOR) remains high, but no longer than for 2 clock cycles.

4. The side road lights are then to cycle through Yellow (SY) to Red (SR), at which point the highway lights should turn Green (HG).

5. Cycling to or from side road Yellow (state SY) should also take one clock cycle. Upon returning to the initial state (HG/SR), the highway lights are not to be interrupted again for at least 3 clock cycles.

6. The durations for which the highway green, highway yellow and highway red lights are on are in the ratio **3:1:2**.

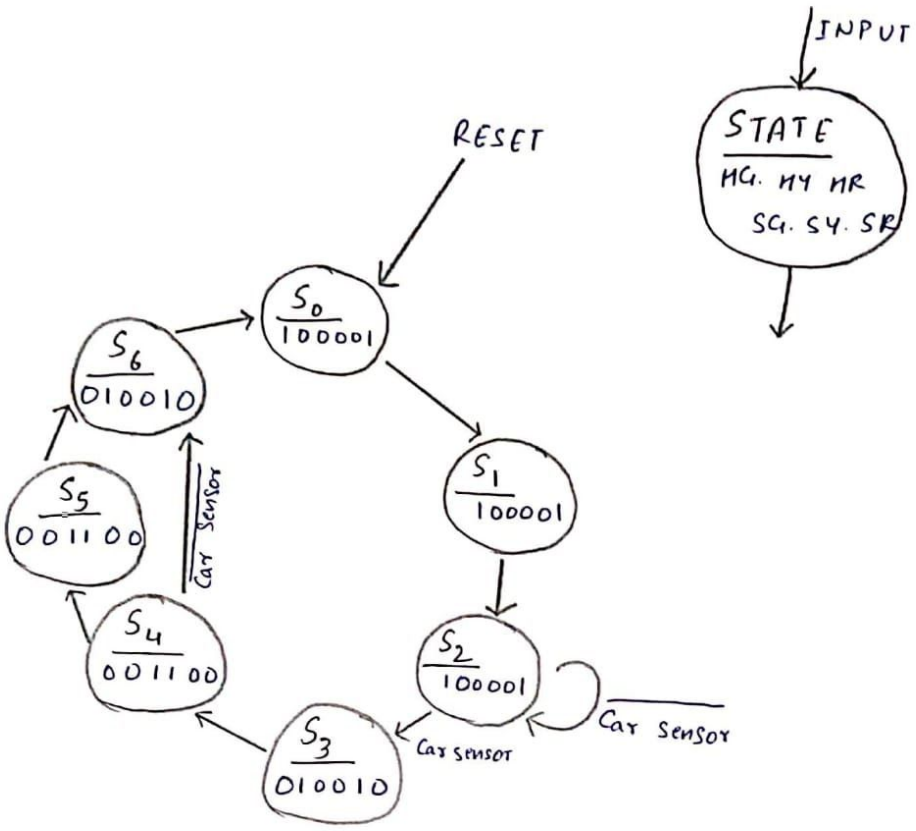
7. The clock period is taken to be 10 seconds.

8. If a car is not detected on the side street, then instead of completing the time duration of 20 sec , the highway traffic signal will automatically turn yellow and then green.
9. When the light on one road is green, the light on the other road must not be the same.

INPUTS: The Traffic Light Controller circuit has one primary input, the value of which depends on whether a car is detected on the side street or not. We denote this input by the label SENSOR. The design also utilizes a periodic clock signal (CLK).

OUTPUTS: The circuit should have six traffic light outputs: three for the highway lights (HG, HY, HR) and three for the side road lights (FG, FY, FR). These signals are to be derived directly from the state registers (suggesting that we will need a Moore machine for our implementation).

STATE DIAGRAM:



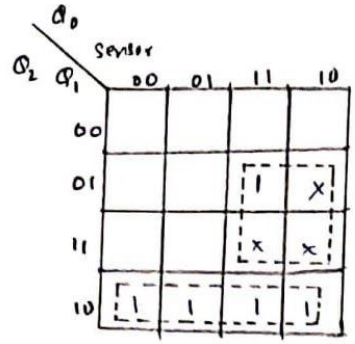
MOORE STATE MACHINE

STATE TABLE:

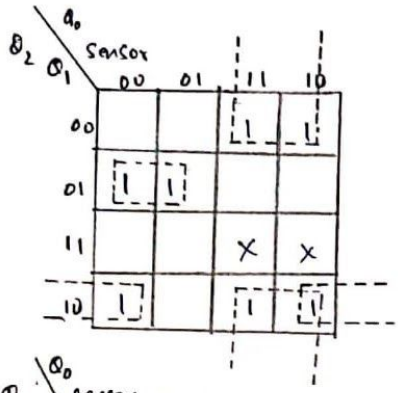
STATE	Present State			Input	Next State			OUTPUT					
	Q2(t)	Q1(t)	Q0(t)	sensor	Q2(t+1)	Q1(t+1)	Q0(t+1)	HG	HY	HR	SG	SY	SR
S0	0	0	0	0	0	0	1	1	0	0	0	0	1
	0	0	0	1	0	0	1	1	0	0	0	0	1
S1	0	0	1	0	0	1	0	1	0	0	0	0	1
	0	0	1	1	0	1	0	1	0	0	0	0	1
S2	0	1	0	0	0	1	0	1	0	0	0	0	1
	0	1	0	1	0	1	1	1	0	0	0	0	1
S3	0	1	1	0	1	0	0	0	1	0	0	1	0
	0	1	1	1	1	0	0	0	1	0	0	1	0
S4	1	0	0	0	1	1	0	0	0	1	1	0	0
	1	0	0	1	1	0	1	0	0	1	1	0	0
S5	1	0	1	0	1	1	0	0	0	1	1	0	0
	1	0	1	1	1	1	0	0	0	1	1	0	0
S6	1	1	0	0	0	0	0	0	1	0	0	1	0
	1	1	0	1	0	0	0	0	1	0	0	1	0
Unused state	1	1	1	0	X	X	X	X	X	X	X	X	X
	1	1	1	1	X	X	X	X	X	X	X	X	X

NOTE: We have used positively edge trigerred D-Flipflops in our circuit implementation.

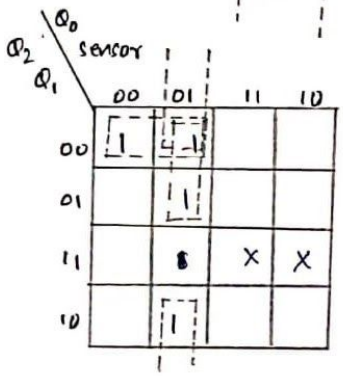
K-MAP Simplifications:



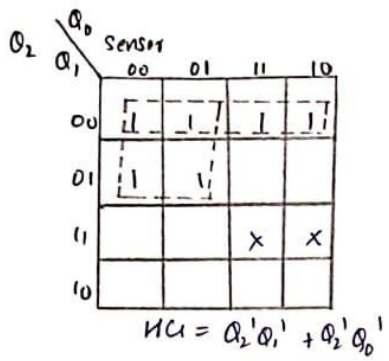
$$Q_2(t+1) = D_2 = Q_2 Q_1' + Q_1 Q_0$$



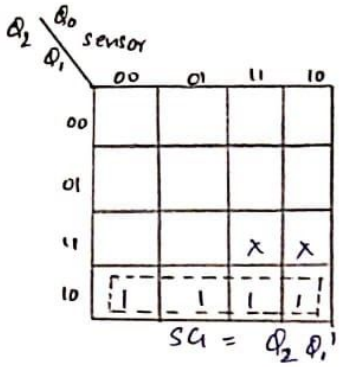
$$Q_1(t+1) = D_1 = Q_1' Q_0 + Q_2' Q_1 Q_0' + Q_2 Q_1' \text{ sensor}'$$



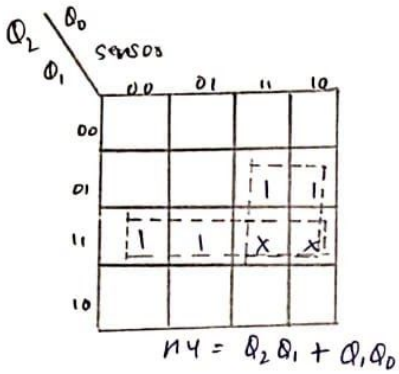
$$Q_0(t+1) = D_0 = Q_2' Q_1' Q_0 + Q_2' Q_0' \text{ sensor} + Q_1' Q_0' \text{ sensor}$$



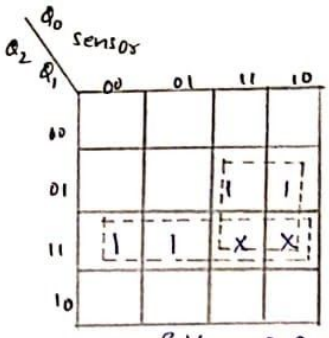
$MC = Q_2'Q_1' + Q_2'Q_0'$



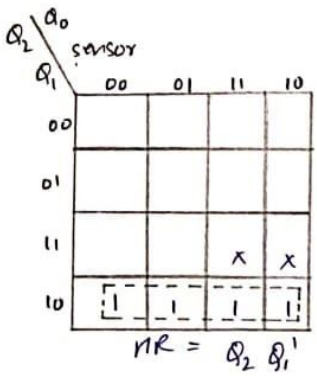
$SC = Q_2 Q_1'$



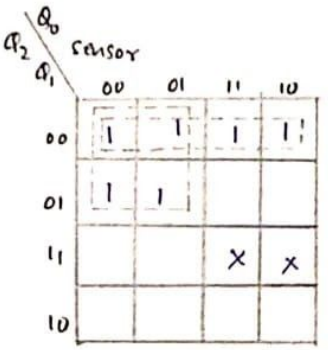
$MY = Q_2 Q_1 + Q_1 Q_0$



$SY = Q_2 Q_1 + Q_1 Q_0$

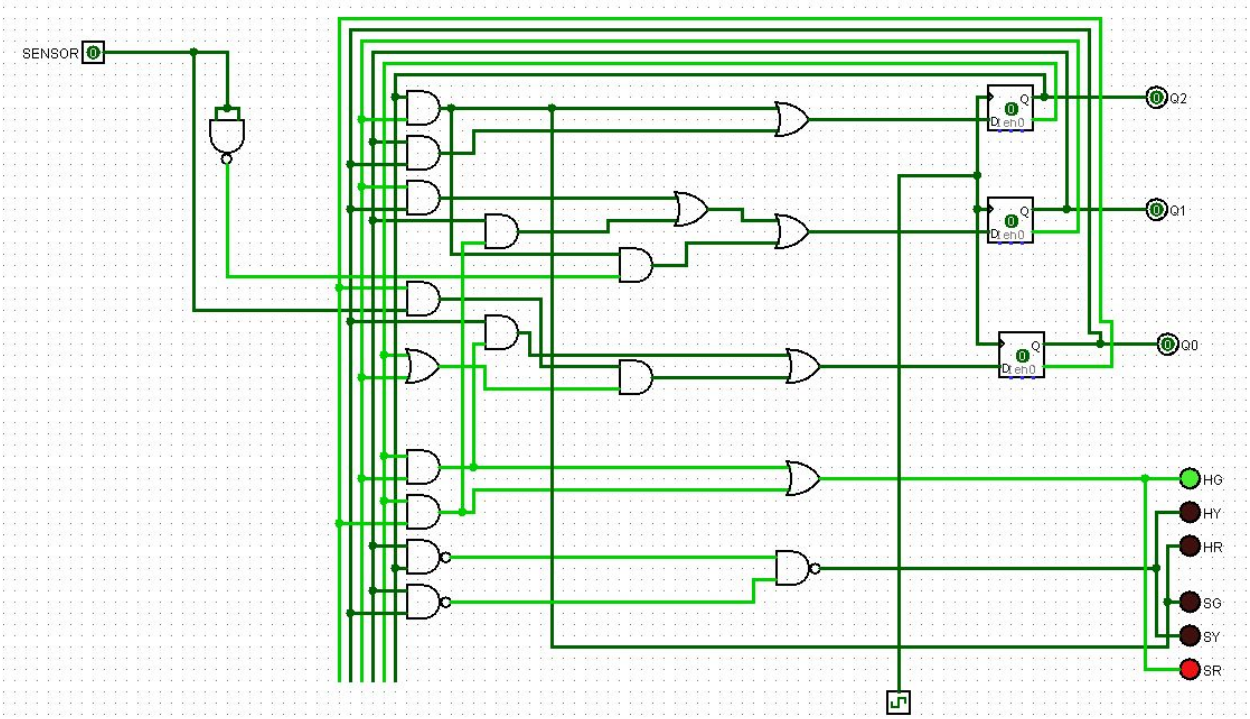


$MR = Q_2 Q_1'$



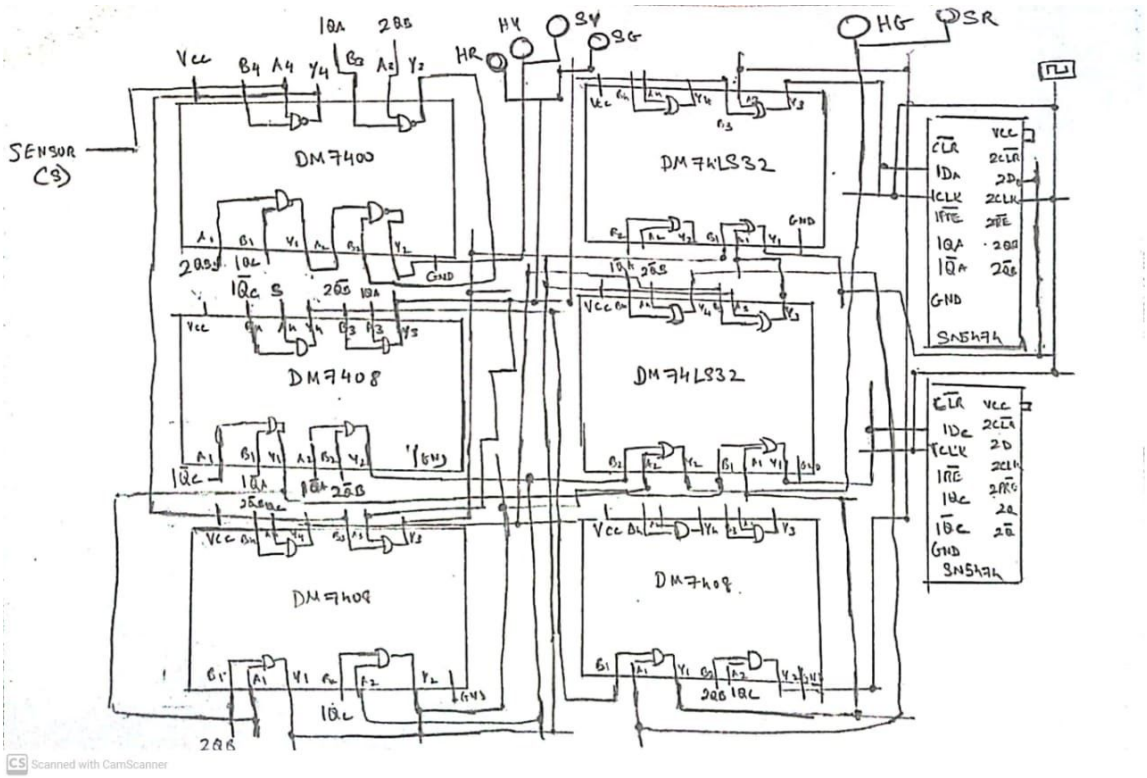
$SR = Q_2'Q_1' + Q_2'Q_0'$

Circuit Diagram in Logisim:

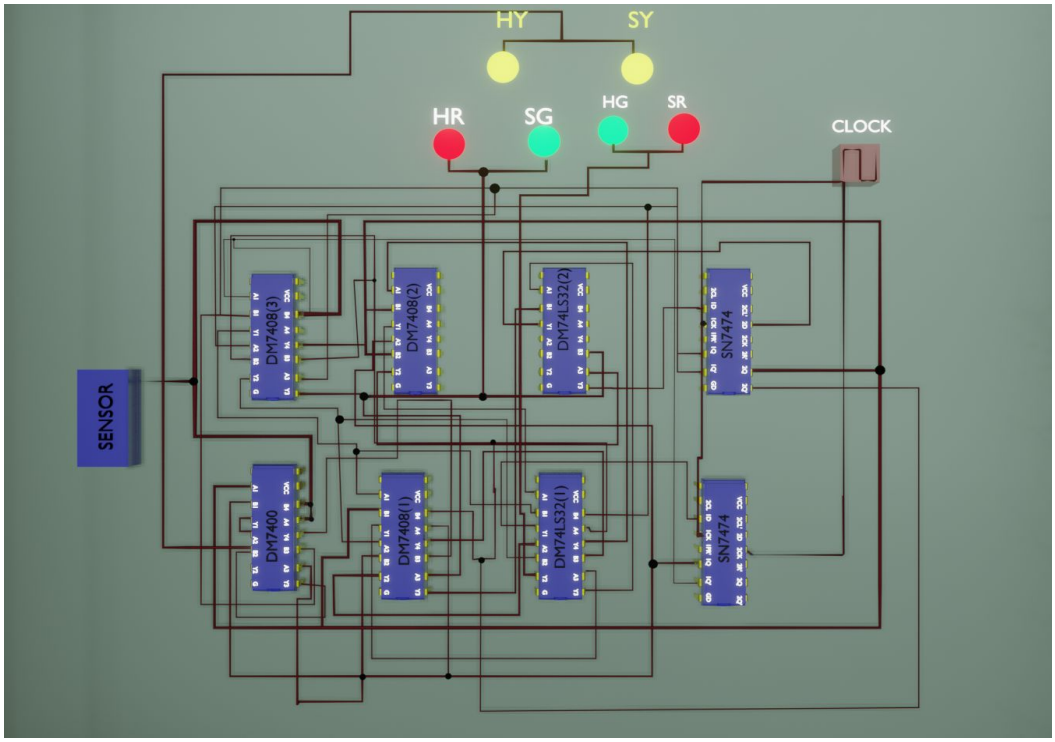


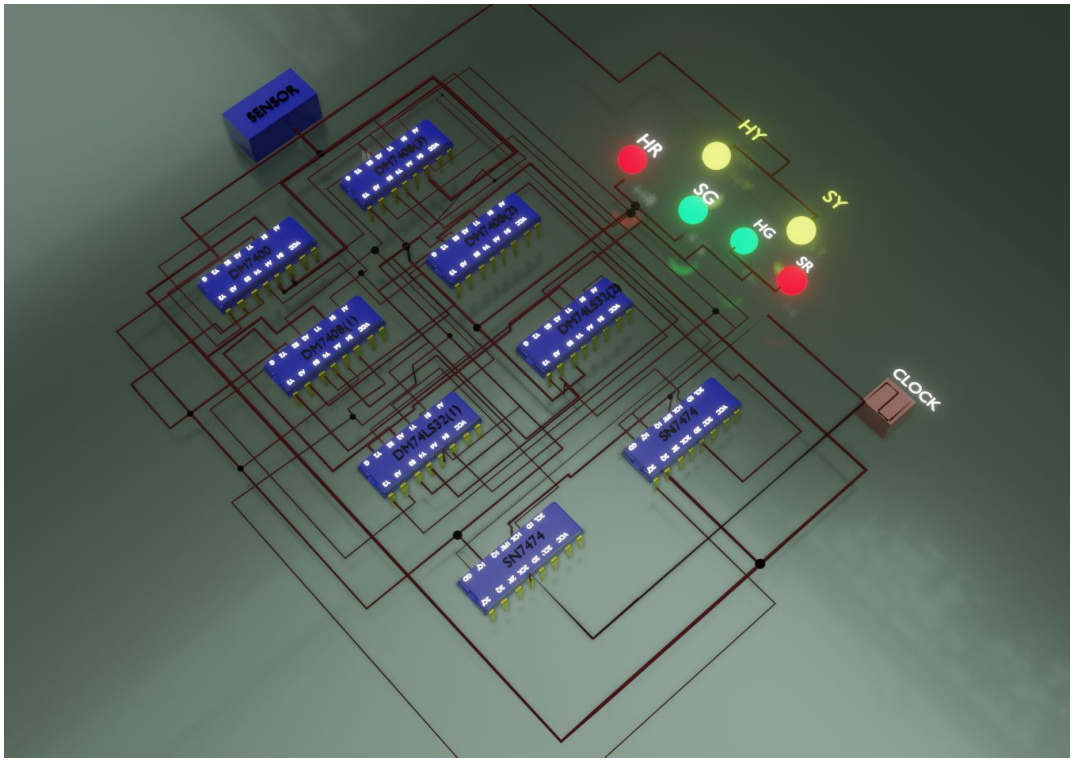
We have used positively edge triggered D flip flop.

Pin-Out Diagram:

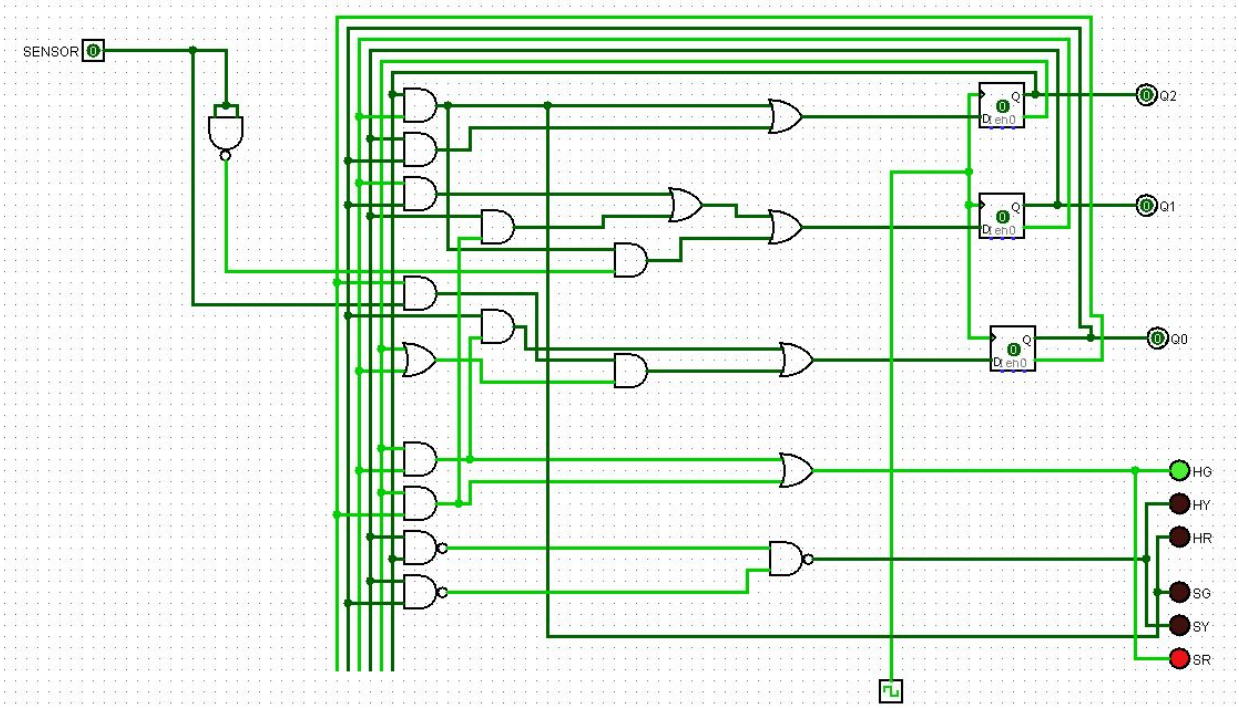


Pin-Out diagram using software:





Sample Input/Output Combination:



Full sample output summary with the steps is in the Logisim Input/Output folder of zipped folder.

Additional Functionality:

When a vehicle is detected on the side street, the signal system is activated, and the traffic lights facing the highway cycle from green to red via yellow, and then back to green via yellow again, after which point the system is reset and waits until another vehicle is detected on the side street. The same holds true for the side street traffic lights. This is to ensure smooth traffic movement.

Bill of materials(All prices in Rupees)

Name	Description	Quantity	Price	Total
Dm 7408	Quad 2 input AND gates	3	16.00	48.00
Ref: https://www.electronicscomp.com/74hc08-quad-2-input-and-gate-ic				
Dm 7432	Quad 2 input OR gates	2	11.00	22.00
Ref: https://www.findchips.com/search/dm74ls32				
Dm 7400	Quad 2 input NAND gates	1	15.00	15.00
Ref: https://www.electronicscomp.com/74hc00-quad-2-input-nand-gate-ic				
DM 7474	D-Flip Flop	2	50.00	100.00
Ref: https://www.amazon.in/INVENTO-74HCT74D-Flip-Flop-Complementary-Positive/dp/B081FC42PS/ref=sr_1_1?crid=PQFZOJFZMA8A&dchild=1&keywords=7474+ic&qid=1605704968&sprefix=7474+%2Caps%2C311&sr=8-1				

Total cost is : **185** (as per the prices of ICs today 18/11/2020)

APPENDIX:

Dm 7400 Quad 2 input NAND gates
https://drive.google.com/file/d/1_E44asfnYAr_IOmdUpDTixt4gVELj_QB/view

Dm 7408 Quad 2 input AND gates
https://drive.google.com/file/d/1kJHP73Vyfl8Eqibz20ARs0_9CepxtLhn/view?usp=sharing
Dm 7432 Quad 2 input OR gates
https://drive.google.com/file/d/1GE7JFVNRSvsBobxPrha8TJdR1viRUv0Q/view?usp=sharing
DM 7474 D-Flip Flop
https://drive.google.com/file/d/1q2Sd9FHkZwbE4ZgOdNpqCoMXI3uyr9WO/view?usp=sharing