KALAM: toolKit for Automating high-Level synthesis of Analog computing systeMs

Ankita Nandi, Krishil Gandhi, Mahendra Pratap Singh, Shantanu Chakrabartty, and Chetan Singh Thakur

Abstract—Diverse computing paradigms have emerged to meet the growing needs for intelligent energy-efficient systems. The Margin Propagation (MP) framework, being one such initiative in the analog computing domain, stands out due to its scalability across biasing conditions, temperatures, and diminishing process technology nodes. However, the lack of digital-like automation tools for designing analog systems (including that of MP analog) hinders their adoption for designing large systems. The inherent scalability and modularity of MP systems present a unique opportunity in this regard. This paper introduces KALAM (toolKit for Automating high-Level synthesis of Analog computing systeMs), which leverages factor graphs as the foundational paradigm for synthesizing MP-based analog computing systems. Factor graphs are the basis of various signal processing tasks and, when coupled with MP, can be used to design scalable and energy-efficient analog signal processors. Using Python scripting language, the KALAM automation flow translates an input factor graph to its equivalent SPICE-compatible circuit netlist that can be used to validate the intended functionality. KALAM also allows the integration of design optimization strategies such as precision tuning, variable elimination, and mathematical simplification. We demonstrate KALAM's versatility for tasks such as Bayesian inference, Low-Density Parity Check (LDPC) decoding, and Artificial Neural Networks (ANN). Simulation results of the netlists align closely with software implementations, affirming the efficacy of our proposed automation tool.

Index Terms—Margin Propagation, SPICE automation, analog computing, Bayesian inference, LDPC decoder, ANN.

I. INTRODUCTION

Rising energy and performance demands have curated the need for advancements in analog hardware to create smarter machine interfaces with data compression and the development of new computing paradigms [1]. In this regard, the Margin Propagation (MP) circuits offer a promising solution as a versatile analog computing framework, successfully demonstrated on hardware for signal processing (SP) and machine learning (MP) processors [2], [3], [4]. MP allows energy efficient, accuracy tunable modular implementation of any non-linear monotonic function using piece-wise linear splines. MP analog designs can be pre-characterized and are scalable across temperature, biasing regimes, and process technology nodes, thus making MP a favorable analog standard cell [5].

However, despite its versatility and efficient implementations of ML and SP processors, MP analog systems lack

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popularity due to the absence of a digital-like automation framework for quick design synthesis and validation. Hence, in this work, we leverage the advantages of MP and propose an automation tool, KALAM. KALAM utilizes factor graphs to represent the system to be implemented while generating a SPICE-compatible netlist for design validation. Factor graphs can model various signal processing tasks, such as Kalman filters and stochastic models [6]. When combined with MP, they create a powerful platform for designing analog signal processors. In this paper, we demonstrate KALAM's capabilities by designing Bayesian networks, LDPC decoders, and an ANN. The key contributions of this paper are:

- An automation tool to synthesize MP analog computing circuits using input factor graphs to produce SPICE netlists.
- Implementation of Bayesian inference for different networks with varying nodes and features. The accuracy of KALAM-generated circuits corresponds to software accuracy.
- Implementation of an MP-based LDPC decoder proposed in [2] for $32-$bit, $64-$bit and $96-$bit codelengths using KALAM. The netlist-derived Bit and Frame Error Rate plots strongly correlate with software results.
- Implementation of an ANN on the IRIS dataset. The netlist-derived accuracy strongly correlates with software results.

The rest of the paper is organized as follows: Section II delves into the factor graph-based systems to be implemented. Section III describes the proposed tool KALAM, and Section IV delves into the results. A detailed discussion is presented in Section V, and Section VI concludes the work.

II. FACTOR GRAPHS

Factor graphs are bipartite graphs consisting of two distinct sets of nodes. Variable nodes denoted by $\mathcal{V} = \{v_1, v_2, \cdots, v_N\}$, represent the random variables in the system. Factor nodes denoted as $\mathcal{F} = \{f_1, f_2, \cdots, f_M\}$, represent functions that constrain the probability distribution over the connected random variables. Each factor node (representing a function) f_i connects to a set of variable nodes ($\mathcal{X}_i$) by edges. The joint probability distribution of the factor graph is given by (1), where Z is a normalization constant that ensures the probability distribution sums (or integrates) to 1.

$$p(v_1, v_2, \cdots, v_N) = \frac{1}{Z} \prod_{i=1}^{M} f_i(\mathcal{X}_i) \qquad (1)$$

This factorization allows efficient inference algorithms to be applied to the model. In this work, we discuss the following examples of factor graphs:
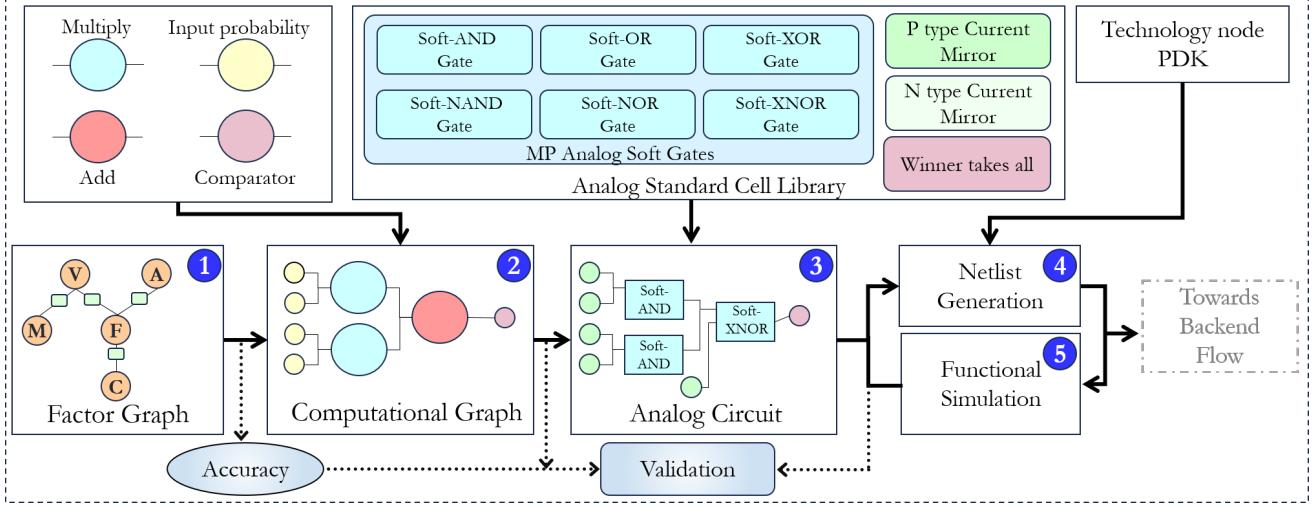
Fig. 1. This figure shows the proposed flow of KALAM for synthesizing analog MP-based systems. The associated figures in each stage refer to the design of a Bayesian network for illustration. *Stage* 1 of this figure shows the factor graph representation to be synthesized. This factor graph is translated into a computational graph in *Stage* 2, which is then mapped onto analog circuits in *Stage* 3. The MP-based analog standard cell library is input at *Stage* 3. Finally, the corresponding netlist is then generated in *Stage* 4 and validated for accuracy through functional simulation in *Stage* 5.

1) Bayesian Networks (BN) as Factor Graphs: Bayesian networks are represented as Directed Acyclic Graphs (DAGs) that reflect the conditional probability distributions of each node v_i given its parents as shown in (1), such that $f_i(\mathcal{X}_i) \equiv p(v_i|parents(v_i))$ and $Z = 1$. Each factor node can be implemented using probabilistic soft gates, which in this case are MP analog soft gates [7].

2) Message Passing Decoders as Factor Graphs: Probabilistic message passing between factor and variable nodes uses the Sum-Product Algorithm (SPA) [2], which is an iterative decoding mechanism for LDPC codes. The primary functions governing v_i and f_j are defined as under [8]:

- Message from v_i to f_j is given by (2) where $(\mathcal{N}_{v \to f})$ shows all connected factor nodes to v_i:

$$m_{v_i \to f_j} = \prod_{f_k \in \mathcal{N}_{v \to f} \forall k \neq j} m_{f_k \to v_i} \qquad (2)$$

- Message from f_j to v_i such that all connected variable nodes are written as $(\mathcal{X}_{f \to v})$, can be calculated as:

$$m_{f_j \to v_i} = \prod_{v_k \in \mathcal{X}_{f \to v} \forall k \neq i} m_{v_k \to f_j} \qquad (3)$$

In this work, we leverage KALAM to implement the MP-based LDPC decoder proposed in [2].

3) Artificial Neural Network (ANN) as Factor Graphs: In an ANN, the neurons typically represent the variable nodes. The factor nodes correspond to activation functions (e.g., sigmoid, ReLU) applied to the weighted sum of inputs to a neuron (also known as the Multiply-Accumulate (MAC) operation). In this work, we demonstrate KALAM for ANN inference by using the MP MAC and MP activation functions proposed in [3].

The focus of this manuscript is to propose an automation framework for the design of MP-based analog processors like inference engines and decoders. Hence we refrain from discussing upon the merits of using MP designs.

III. KALAM: PROPOSED AUTOMATION FRAMEWORK

This section presents the proposed automation flow, segmented into five stages as shown in Fig. 1. We also present an example Bayesian network implementation towards the end of this section.

A. Factor Graph Generation: Defining the system

The process begins by defining the system as an equivalent factor graph. KALAM offers two functionalities:

- **User-Provided Factor Graph**: If a factor graph already exists, the user can directly input it into the framework. For example, when designing LDPC decoders, we can leverage the factor graph given by the code's parity-check matrix.
- **Factor Graph Construction**: Alternatively, KALAM can construct a factor graph based on the user's input, such as a Bayesian network represented as a DAG.

B. Computational Graph Generation: Mapping Operations

Building upon the factor graph from *Stage* 1 in Fig. 1, *Stage* 2 generates the computational graph. This graph depicts the crucial mathematical operations required at each factor node by using the following flow:

- **Analyzing the factor graph** to determine the number of inputs for each operation and the respective connections.
- **Computational optimization** eliminates redundant variables using variable elimination algorithms. It also implements mathematical and boolean simplifications if any.
- **Graph generation** by Graphviz Python package [9] and **validation** against software implementation.

C. Analog Circuit Mapping: From Graph to Circuits

Stage 3 translates the computations in the computational graph into practical analog circuits. This involves:
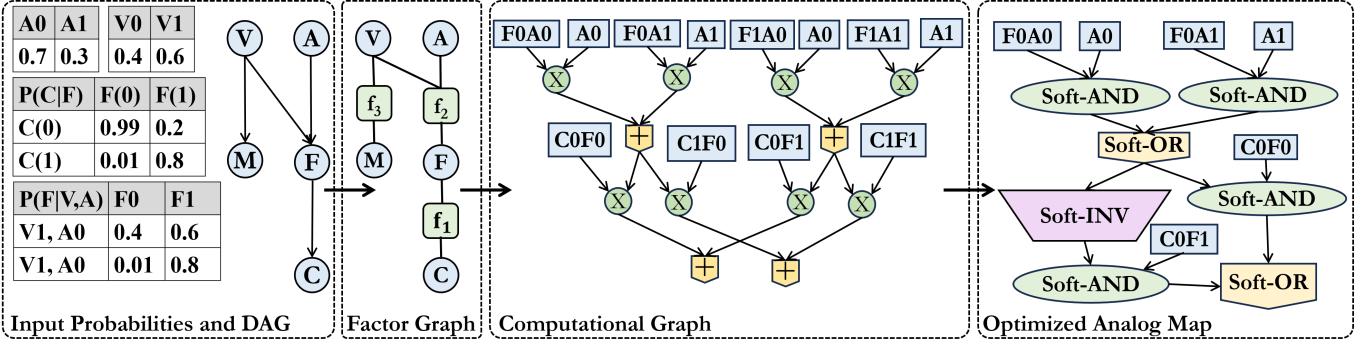
Fig. 2. This figure is an example illustration of the different synthesis stages for a Bayesian DAG using its input probabilities. It is first translated into a factor graph. A computational graph is then generated with respect to the computations of each factor node after variable elimination. Optimization strategies such as Boolean simplification and precision tuning are employed before generating the final optimized analog map.
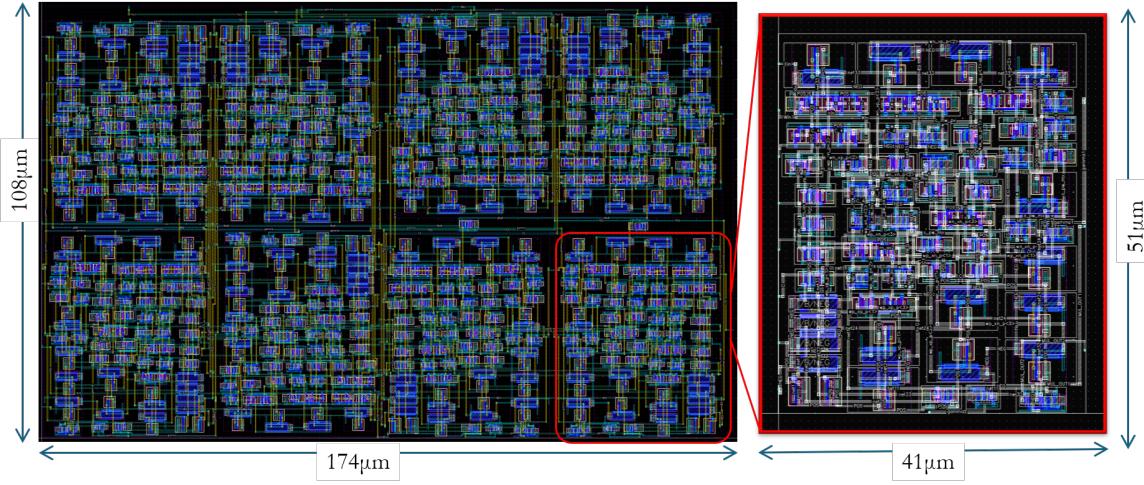

Fig. 3. Layout for the KALAM-generated netlist corresponding to the Computational Graph in Fig. 2 consisting of eight Soft-AND gates (each mapped to a multiplier), using the place-and-route options offered by Cadence Layout GXL. The inset figure zooms into the layout of a single Soft-AND gate.

- **Optimizing computations** with corresponding standard cells from a pre-defined analog standard cell library implemented for varying accuracy, precision, power, and area budget. This is done by implementing the behavioural model design based on the computational graph for varying splines. Increasing splines increases the accuracy but a penatlty of area overhead is to be paid [4]. Given that MP is modular, projecting the area overhead is feasible. A power-delay projection is made based on the operation regime. The weak inversion regime serves as a power saver mode while the strong inversion regime is the high performance mode [5].
- **Functionally validating** this stage using software tools.

D. Netlist Generation: Building the circuit

The analog circuit map from *Stage* 3 serves as the blueprint for netlist generation. Netlist contains the components and their interconnections, which are essential for circuit simulation. KALAM approaches netlist generation by:

- **Pre-defined Standard cells:** Synthesis of the standard cells involves computational mapping and transistor sizing using established techniques [7], [10].
- **Final netlist** is generated based on the analog circuit map by instantiating the implemented standard cells from the library using Python scripts for subsequent simulation.

TABLE I
ACCURACY AND RUNTIME OF DIFFERENT BAYESIAN NETWORKS

Model	#Variable Nodes	Software Accuracy (%)	Netlist Accuracy (%)	Synthesis Runtime (ms)
Airplane	22	82.38	82.27	6.1
Titanic	8	77.99	77.91	5.8
Pistachio	17	77.12	77.12	5.9
Thyroid	15	95.3	95.3	5.9
Drought	19	97.93	97.93	6

E. Functional Simulation and Validation

The generated netlists undergo validation using SPICE tools. We leverage *Cadence virtuoso* for visual inspection and *Cadence Spectre* for functional validation of the designs. Further, similar to digital synthesis the layout can be generated by using this schematic on *Cadence Layout GXL* through the automatic place and route features of the standard analog cells.

Example Design of a Bayesian network Using KALAM

To demonstrate the capabilities of KALAM, we illustrate various stages of the tool using an example involving the design and analysis of a simple Bayesian network to infer prey catching [11], as shown in Fig. 2. It starts by factorizing the probabilities to convert them to a factor graph. Thus, the
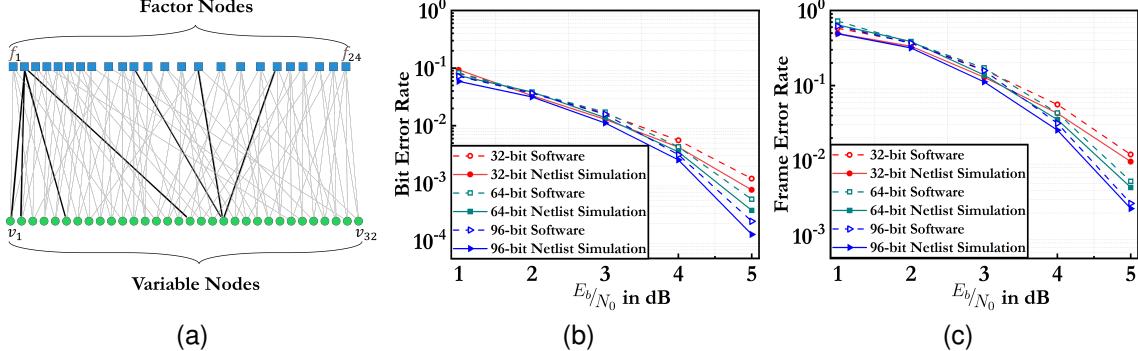
Fig. 4. (a) Tanner Graph for a (32,8) LDPC Decoder; (b) Bit Error Rate (BER) and (c) Frame Error Rate (FER) of the simulated netlist w.r.t. the software implementation for code lengths $32-$bit (synthesis runtime$= 32ms$), $64-$bit (synthesis runtime$= 39ms$) and $96-$bit (synthesis runtime$= 51ms$).

TABLE II
SUMMARY OF ANALOG DESIGN AUTOMATION FRAMEWORKS FOR SYNTHESIS

Work	Methodology	Flow Automated	Example Design Automated
[12]	Franz Lisp	Sizing and Netlist generation	Comparator Topology
[13]	Signal Flow Graph Transformation	Structural synthesis using Transfer function	Summing Circuit
[14]	Equation based Optimisation	Sizing	CMOS Op-Amps
[15]	ODAE Model, VHDL-AMS, Java	Structural synthesis using VHDL-AMS	Oscillator
[16]	Adaptive Genetic Algorithm, C++	Topology	OpAmp, Oscillator
[17]	Differential Evolution	Architectural selection and Sizing	CMOS OpAmp
LASER [18]	Tcl/Tk, C++, CPLEX	Netlist Synthesis and Layout	CMOS OpAmp
AutoCkt [19]	Reinforcement learning	Sizing	CMOS Two-stage OpAmp, OTA, TIA
[20]	Reinforcement learning: GCN	Sizing (Width & Fingers)	Two-stage OpAmp; GaN RF PA
OPAMP-Generator[21]	VGAE, Bayesian optimisation	Sizing and Netlist generation	CMOS OpAmp, Three-stage OpAmp
[22]	Aritificial Neural Networks, SIMSIDES [23]	Size and performance optimization	$\Sigma\Delta$ Modulators, OTA
KALAM (This Work)	Factor Graphs, Margin Propagation	Software to Netlist generation	Bayesian networks, LDPC Decoders

factor nodes are $f_1 = p(C|F)$, $f_2 = p(F|A, V)$. It can be observed that $f_3 = p(M|V)$ is unrelated to node **C**. For a small network such as this, we can visually eliminate unrelated variable nodes, but for large networks, this is not feasible. Thus, we need the computational graph. For the next stage, factor nodes are unrolled to represent computations in the computational graph, which is, in turn, used to make the analog map. The analog map is then transformed into a SPICE netlist. For SPICE validation, the input magnitudes have been mapped as a multiple of $1\mu A$ current for each input, which can be tuned based on the power budget. The final output of the BN, seen as the output current of the Soft-OR, was found to be $0.524\mu A$, corresponding closely to the expected mathematical output $p(C = 1/V = 1) = 0.555$.

In Fig. 3, we use the netlist which is generated using the computational graph with eight multipliers and two adders (prior to the optimization of the analog map). These multipliers are mapped to a Soft-AND operation and the adders are showcased by addition of currents (by Kirchoff's current conservation). Thus the corresponding layout has eight Soft-AND gates as seen in Fig. 3 with a zoomed inset of a single Soft-AND.

IV. RESULTS

We evaluate the tool's efficacy by validating the functionality of the KALAM-generated Bayesian Networks, LDPC decoders, and ANN circuits.

A. Bayesian networks

We used five different Bayesian networks from datasets found in Kaggle [24]. The *pgmpy* [25] Python library is used to obtain the ground truth software accuracy. The runtime of KALAM to generate the netlists, the software accuracy and the inference accuracy obtained through DC analyses of these netlists on *Cadence Spectre* is reported in Table I.

B. LDPC Decoder

We implement $32-$bit regular LDPC code having a $4-$degree factor node and a $3-$degree variable node as presented in Fig. 4a. The design in [2] comprises both MP and non-MP designs easily integrated by the tool. The runtime to generate the netlist is mentioned in Fig. 4. Further, we expand the $32-$bit code to $64-$bit and $96-$bit codelengths using the prototraph technique [26] of code construction. The Bit and Frame Error plots in Fig. 4b and Fig. 4c show the netlist simulation. The netlist simulation results conform with the software accuracy, demonstrating the efficacy of our tool.

C. Artificial Neural Network (ANN)

We demonstrate the design of an ANN using a network comprising of 4 input nodes, 8 hidden nodes, and 3 output nodes. The network consists of a MAC operation and ReLU activation function. For a training accuracy of 92%, the software testing accuracy was found to be 90.5% for an IRIS dataset using MP computational modules. The simulation of the KALAM-generated netlist also provided a 90% accuracy.

V. Discussion

Table I shows a negligible drop in the accuracy of the KALAM-generated netlists compared to their software counterpart for both Bayesian networks. Fig. 4b and Fig. 4c show that the bit and the frame error rates of the netlist simulations comply with the software implementation of the decoding algorithm. The difference in the software and the implemented SPICE results is an artifact also reported in the design in [2], which the authors of [2] explain as the effect of continuous-time analog simulations. The similarity of the implemented results with the baseline design reported in [2] is a testament to the tool's efficacy in implementing and integrating both MP and non-MP modules. The ANN has a software inference accuracy of 90.5% while a netlist accuracy of 90%. The runtime to generate the netlists of all the designs implemented by KALAM is observed to be $< 1s$ for an *Intel i7* processor, which is manifold compared to manual implementation considering the scale of the system being implemented.

Table II shows that while significant efforts have been dedicated to optimizing fundamental analog circuits, the automation required for designing large scalable analog circuits is less explored. The ability of MP-based designs to be pre-characterized, modular, and robust like digital designs, makes them suitable for automating large analog computing systems.

VI. Conclusion

In conclusion, this work introduces KALAM, an innovative automated synthesis flow for designing analog computing systems using the MP framework. KALAM handles the full design process, from high-level descriptions using factor graphs to SPICE-compatible netlist generation. It further supports the integration of non-MP modules, which is evidence that KALAM can be used for non-MP designs. Validation against custom designs demonstrates its potential for scalable and practical applications. Future versions will explore the synthesis of other graphical models and various machine-learning architectures for both MP and non-MP analog computing.

Acknowledgments

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