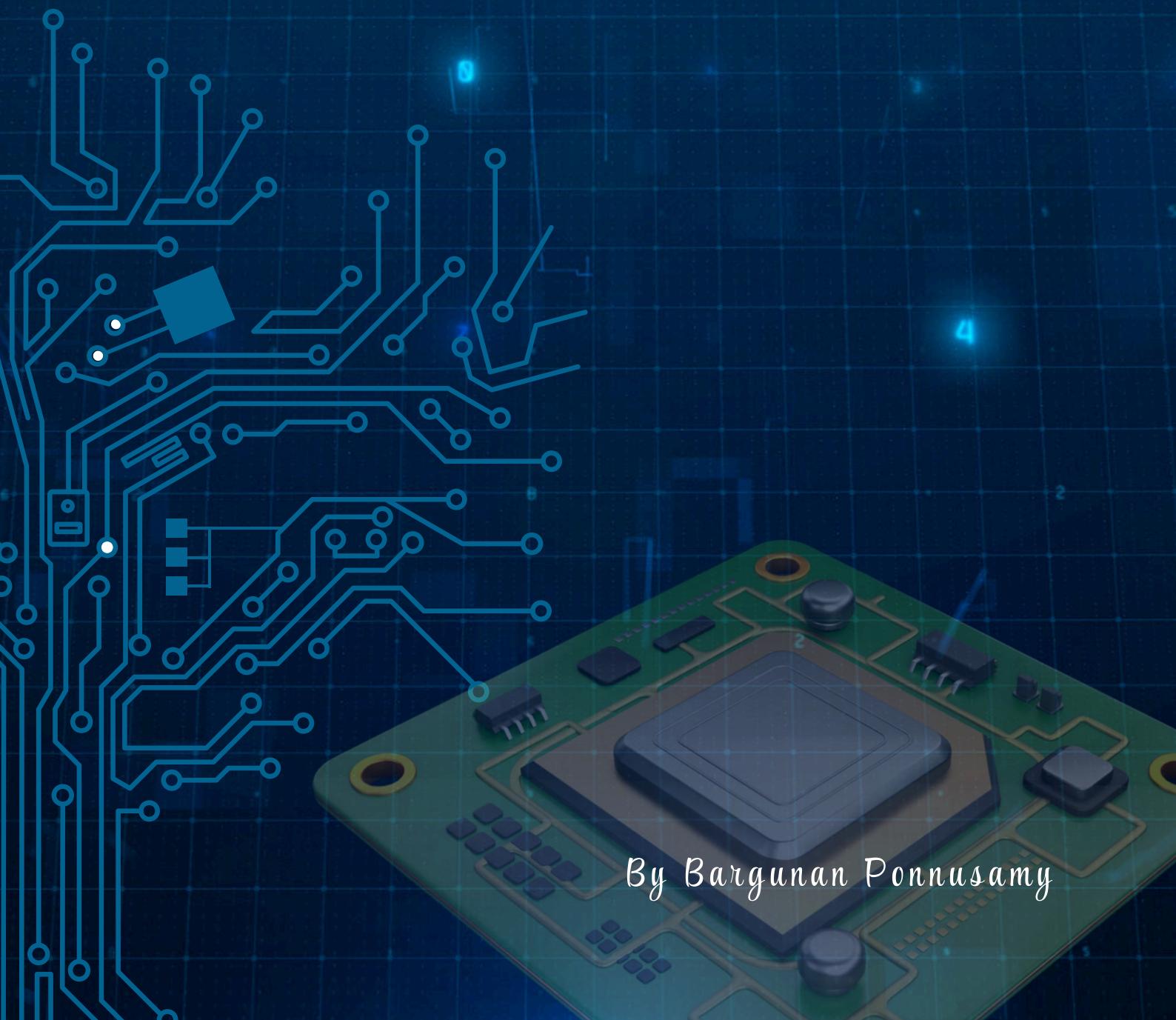


PCB DESIGN GUIDE



By Bargunan Ponnusamy

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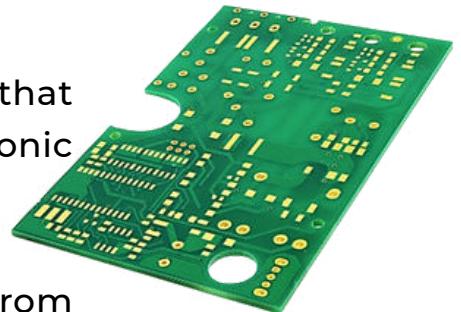
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FUNDAMENTALS OF PCB DESIGN

Basics

What is a PCB Board?

A Printed Circuit Board (PCB) is a flat board that mechanically supports and electrically connects electronic components using copper tracks instead of wires.



It acts as the backbone of all electronic devices — from mobile phones to computers and industrial machines.

What Does a PCB Contain?

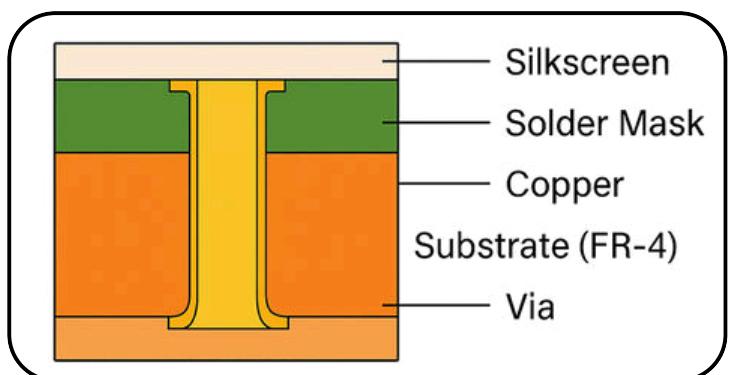
A typical PCB is made up of layers and materials:

- **Copper Foil** – Thin conductive layer that forms the circuit traces.
- **Substrate/Core (FR-4)** – Insulating base material (usually fiberglass epoxy).
- **Prepreg (insulating adhesive)** – Bonds copper layers together in multilayer PCBs.
- **Solder Mask** – Protective colored coating (green, blue, red) that prevents shorts.
- **Silkscreen** – White text/labels showing component positions (RefDes, logos).
- **Vias** – Small plated holes that connect traces between layers.
- **Surface Finish** – Coating on copper pads (ENIG, HASL) for solderability.

Simple Analogy:

Think of a PCB as a layered sandwich:

- Bread = Substrate (FR-4 core)
- Butter = Copper foil (traces)
- Plastic wrap = Solder mask
- Labels = Silkscreen



In short:

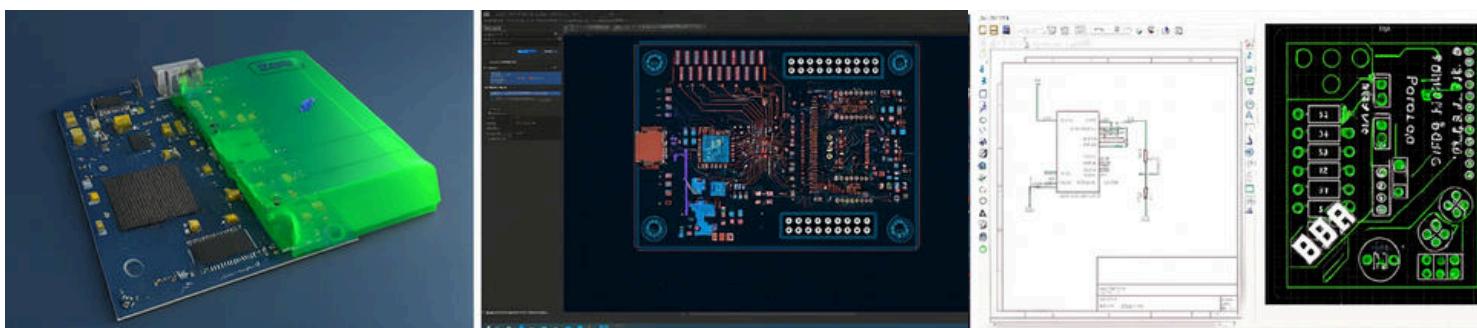
A PCB is a sandwich of **copper** and **insulating** materials, protected by **coatings**, with **holes (vias)** and **finishes** to allow reliable **soldering** and **electrical connectivity**.

FUNDAMENTALS OF PCB DESIGN

CAD Tools

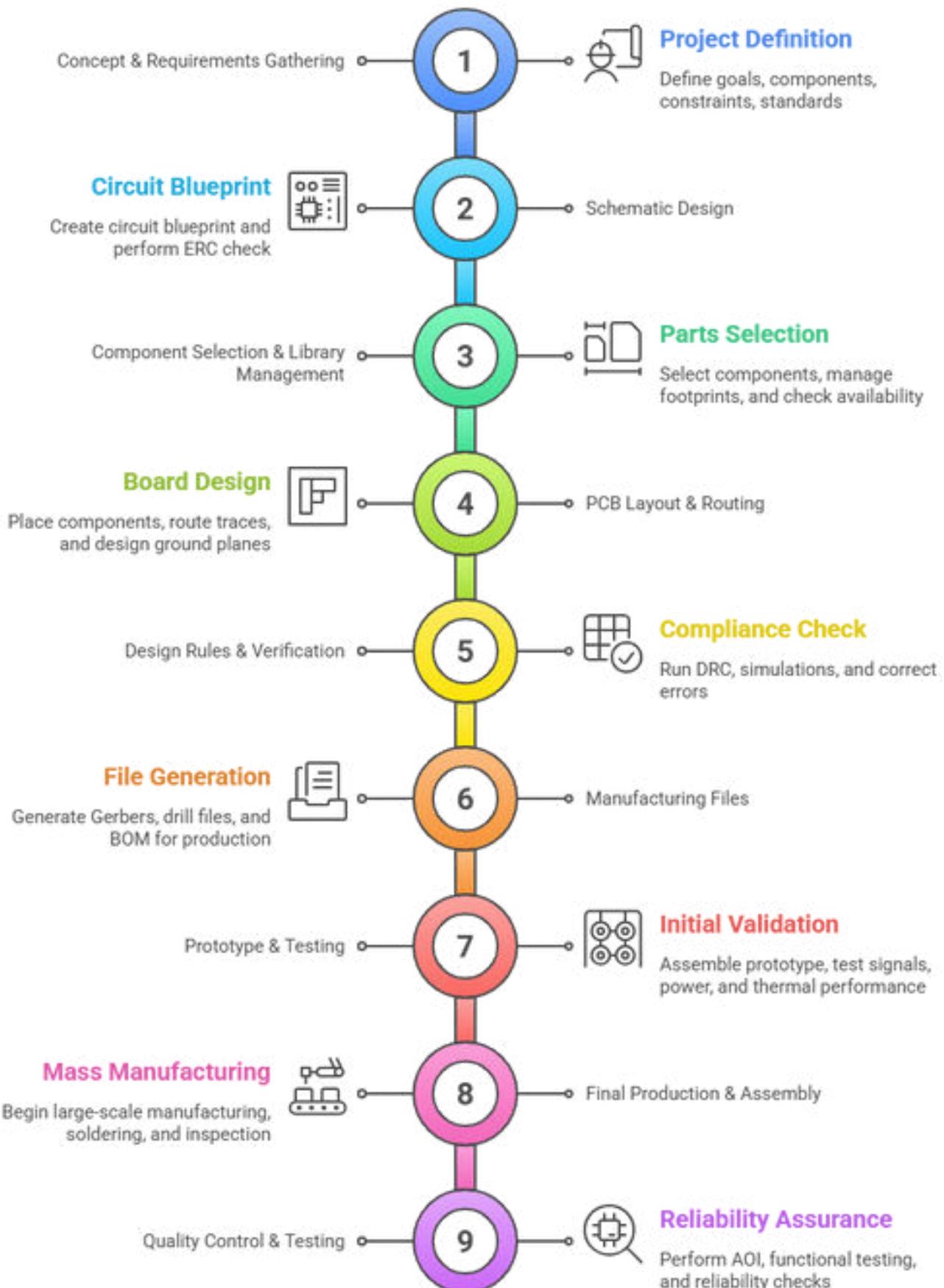
Today's PCB design relies on advanced CAD tools that provide schematic capture, layout, simulation, and manufacturing support.

Tool	Best For	Pros	Cons
Altium Designer	Professionals, mid-high designs	3D, libraries, integration	Expensive, heavy
Cadence Allegro	Enterprise, high-speed	Advanced SI/PI, DDR, PCIe	Steep learning, costly
Siemens Xpedition PCB	Large companies, cutting-edge designs	Enterprise features, collaboration, SI/PI, PLM integration	Very expensive, steepest learning
Siemens PADS	Mid-level pro	Strong verification, simpler than Xpedition	Outdated UI, cost
Eagle	Hobby/startup	Fusion 360 integration, affordable	Limited high-speed capability
KiCad	Students, open-source	Free, community support	Lacks enterprise-grade tools
Proteus	Embedded/teaching	MCU sim + PCB	Weak PCB features
EasyEDA	Beginners, quick fab	Free, browser-based, JLCPCB link	Limited for complex designs



FUNDAMENTALS OF PCB DESIGN

PCB Design Process Flow



FUNDAMENTALS OF PCB DESIGN

Inputs to Start a PCB design

1. General Inputs

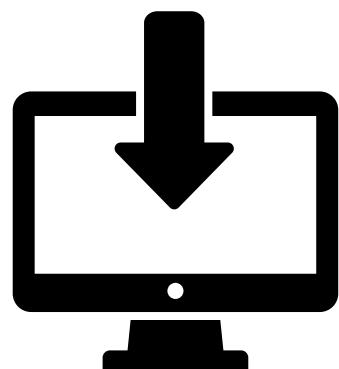
- **Bill of Materials (BOM)** – Complete list of components with part numbers, values, packages, and sourcing.
- **Schematic Diagram** – Defines logical interconnections between components.
- **Datasheets & Reference Designs** – Electrical, thermal, and recommended footprints.
- **Design Standards & Requirements** – IPC, UL, customer specs, reliability targets.

2. Mechanical Inputs

- **Board Outline & Dimensions** – Shape, size, cutouts, keep-outs.
- **Height Restrictions** – For enclosures and connectors.
- **Mounting Features** – Holes, slots, mechanical support areas.
- **Connector Placement & Orientation** – Defined by system integration.

3. Electrical Inputs

- Operating Voltages & Currents
- Power Supply Requirements
- Ambient Temperature & Thermal Limits
- Plane Split Requirements (for multilayer boards)
- **Feature Constraints:**
 - Trace-to-trace, trace-to-via, pad spacing
 - Trace length restrictions, impedance control
 - Copper thickness for high-current nets



4. Manufacturing Inputs

- **Fabrication Constraints** – Min trace width/spacing, via size, drill-to-copper clearance.
- **Copper Thickness Options** – For power vs. signal layers.
- **Material Selection** – FR-4, Polyimide, Rogers, etc.
- **Panelization Guidelines** – V-scoring, breakaway tabs.
- **Surface Finish Requirements** – HASL, ENIG, OSP, etc.

FUNDAMENTALS OF PCB DESIGN

5. Assembly Inputs

- **Assembly Process Review** – SMT, through-hole, mixed assembly.
- **Handling System Limitations** – Component size, placement restrictions.
- **Fiducials** – Local and global for pick-and-place alignment.
- **Component Spacing** – For rework, testability, and heat dissipation.
- **Coating Requirements** – Conformal coating for humidity/harsh environments.

7. Software Inputs

EDA Tool Inputs

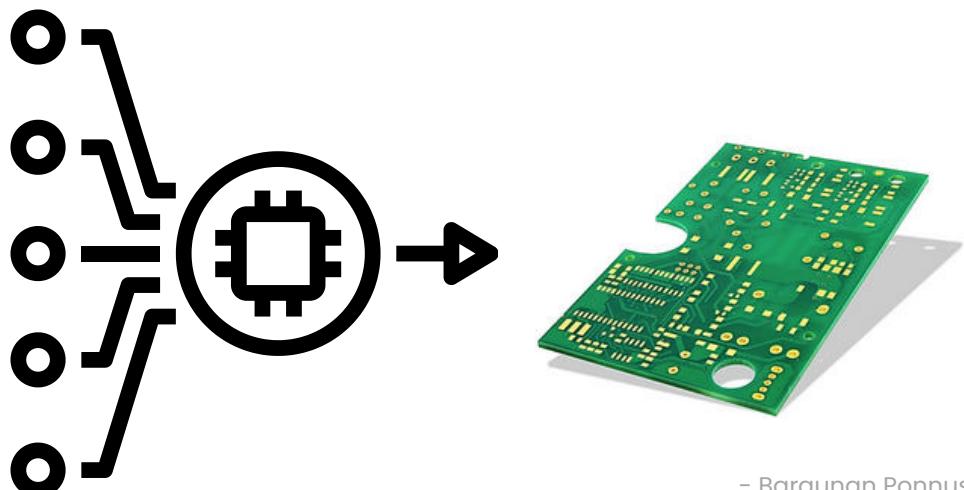
- CAD tool selection (Altium, Allegro, Xpedition, KiCad)
- Verified libraries (symbols, footprints, 3D models)
- DRC/ERC rule definitions
- Simulation models (SI/PI, thermal, EMI)

Firmware / Coding Inputs

- **Pin mapping** – Align MCU/FPGA I/Os with PCB routing feasibility
- **Clocks & reset** – Proper oscillator and reset placement
- **Power sequencing** – Meet device boot requirements
- **Programming/debug ports** – JTAG, SWD, UART access
- **Memory & bootloader needs** – Flash/SRAM support, stable routing
- **Peripheral interfaces** – USB, CAN, Ethernet connectors and terminations

8. Regulatory & Reliability Inputs (Additional)

- **Safety Standards** – IPC-2221, UL 796, IEC standards.
- **Reliability Requirements** – Thermal cycles, shock/vibration tolerance.
- **EMI/EMC Compliance** – Shielding, grounding, spacing guidelines.



FUNDAMENTALS OF PCB DESIGN

Copper Foil

Copper foil is a thin conductive layer of copper laminated onto the substrate (FR-4 or other base material) of a printed circuit board. It is the key material that gets etched or patterned to form traces, pads, and planes, which electrically connect all components on the PCB.

Function:

- Provides **electrical pathways** (traces) between components.
- Forms **power planes and ground planes** in multilayer PCBs.
- Handles **signal transmission** with low resistance.
- Distributes **current and voltage** across the board.
- Plays a role in **heat dissipation** in power and high-current designs.

Types of Copper Foil

- **Electro-Deposited (ED) Copper**
 - Made by electroplating, lower cost, commonly used in rigid PCBs.
 - Surface is rougher → good adhesion but higher signal loss at high frequencies.
- **Rolled-Annealed (RA) Copper**
 - Made by rolling copper into thin sheets and annealing.
 - Smoother surface → better for flexible PCBs and high-frequency RF circuits.
 - More expensive than ED copper.

Thickness (Copper Weight)

Copper thickness is usually defined by copper weight, measured in ounces per square foot (oz/ft²):

Copper Weight	Thickness (µm)	Typical Use Case
0.5 oz	~17 µm	Fine-pitch signal layers, HDI
1 oz	~35 µm	Standard signal & power
2 oz	~70 µm	Power layers, motor drivers
3 oz+	~105 µm+	High-current circuits, power electronics

Rule of Thumb: 1 oz copper = 35 µm thick ≈ carries ~1.6 A per 1 mm trace width (outer layer, 10°C rise).

FUNDAMENTALS OF PCB DESIGN



Applications

- **Signal Traces:** Carry low-current signals between ICs.
- **Power Distribution:** Supply rails, voltage planes, ground planes.
- **Thermal Management:** Dissipates heat through copper pours and thermal vias.
- **High-Power PCBs:** Used in automotive, industrial, and power electronics.
- **High-Frequency Designs:** RA copper preferred for RF & microwave circuits.

Design Considerations

- **Trace Width & Thickness:** Must be calculated (using IPC-2152) to handle required current.
- **Copper Roughness:** Affects high-frequency signal integrity.
- **Thermal Expansion:** Thick copper layers increase stress during soldering/lamination.
- **Etching Limitations:** Very thick copper (3–6 oz) requires wider clearances and larger pads.
- **Cost Factor:** More copper = higher cost of fabrication.

Surface Treatment

Before applying solder mask or finishes, copper is often treated to improve adhesion and protect from oxidation:

- **OSP (Organic Solderability Preservatives)**
- **ENIG (Electroless Nickel Immersion Gold)**
- **HASL (Hot Air Solder Leveling)**

Copper foil is the **heart of a PCB**, forming the conductive paths that connect all components. Its thickness, type, and quality directly affect the PCB's **electrical performance, thermal management, reliability, and cost**.

FUNDAMENTALS OF PCB DESIGN

Substrate / Core (FR-4)

The substrate (core) is the insulating base material of a PCB that provides mechanical strength and electrical insulation between copper layers.

The most widely used substrate material is FR-4 – a fiberglass-reinforced epoxy laminate.

Function:

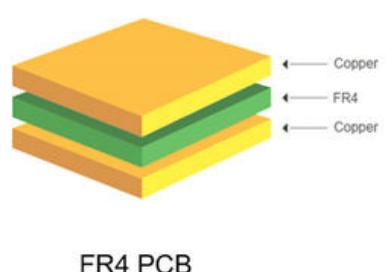
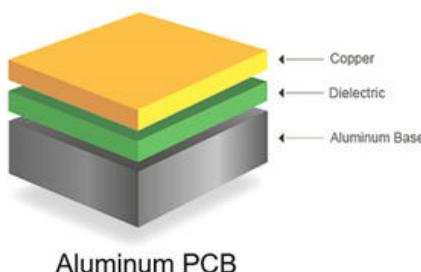
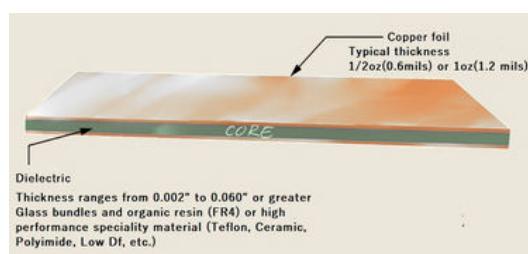
- Provides structural support for the PCB.
- Electrically insulates copper layers from each other.
- Ensures dimensional stability during manufacturing and operation.
- Defines key PCB properties: dielectric constant (D_k), loss tangent, and thermal expansion.

FR-4 Properties

- **Material:** Woven fiberglass cloth + epoxy resin.
- **Flame Retardant:** The "FR" stands for Flame Retardant, ensuring self-extinguishing properties.
- **Operating Temperature:** ~130°C to 140°C Tg (glass transition temperature).
- **Electrical Properties:**
 - Dielectric constant (D_k): ~4.2–4.8
 - Low moisture absorption (<0.15%)
 - Good electrical insulation at high voltages.

Common Substrate Types

- **FR-4 (Standard):** General-purpose, used in consumer & industrial electronics.
- **High-Tg FR-4:** Improved thermal performance (~170°C Tg), used in automotive, LED lighting, and high-power boards.
- **Polyimide:** Flexible and high-temperature (~260°C), used in aerospace & flex PCBs.
- **Rogers / PTFE:** Low-loss substrates for RF/microwave applications.



FUNDAMENTALS OF PCB DESIGN

Thickness

- Typical PCB thickness = 1.6 mm (0.062 inch) (standard).
- Can range from 0.4 mm to 4.75 mm depending on layers and applications.
- Core layers are sandwiched between copper foils, bonded with prepreg (epoxy sheets).

Applications

- **FR-4 Standard:** Consumer electronics, computers, IoT, industrial devices.
- **High-Tg FR-4:** Automotive, LED lighting, power boards.
- **Rigid PCBs:** Majority of commercial electronics.
- **As Core in Multilayer PCBs:** Supports stack-up with alternating prepreg and copper layers.

Design Considerations

- Choose FR-4 grade based on operating temperature (Std vs. High-Tg).
- Ensure dielectric thickness matches impedance control requirements.
- Watch for warpage in large or high-layer-count boards.
- Not ideal for RF/microwave → use low-loss substrates (Rogers, PTFE).

FR-4 vs Polyimide vs Rogers

Property	FR-4 (Glass Epoxy)	Polyimide	Rogers (PTFE / Hydrocarbon)
Dielectric Constant (Dk)	~4.2–4.8	~3.5–4.0	2.2–3.5 (very stable)
Dissipation Factor (Df)	~0.015–0.02	~0.01–0.015	0.0009–0.004 (ultra-low loss)
Glass Transition Temp. (Tg)	130–180 °C (Std/High-Tg)	200–260 °C	280–400 °C
Thermal Stability	Moderate	Excellent	Excellent
Flexibility	Rigid only	Flexible (ideal for Flex/Rigid)	Rigid
Moisture Absorption	0.10–0.20%	<0.15%	<0.05% (very low)
Thermal Conductivity	~0.3 W/m·K	~0.4 W/m·K	~0.6 W/m·K
Cost	Low (cheapest)	Medium–High	High
Typical Uses	General electronics, consumer devices,	Flexible PCBs, aerospace,	RF/Microwave, high-frequency circuits, 5G, satellite, radar
Strengths	Cost-effective, widely available, good	Excellent flexibility, high-	Best electrical properties, stable Dk/Df, very low loss
Limitations	Not suitable for high-frequency >3 GHz, higher	Expensive, higher moisture	Expensive, limited availability, harder to process

FUNDAMENTALS OF PCB DESIGN

Prepreg (Insulating Adhesive)

Prepreg (short for pre-impregnated) is a sheet of fiberglass cloth pre-impregnated with epoxy resin that is partially cured.

In PCB manufacturing, it is used as the insulating adhesive layer that bonds together copper foils and core (FR-4) layers during lamination.

Function:

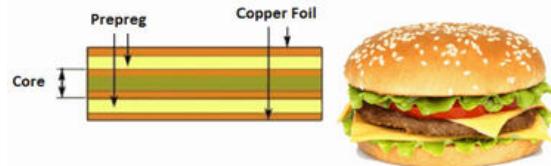
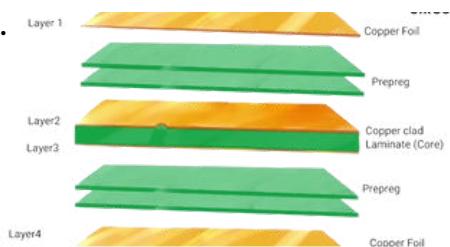
- Acts as an insulator between copper layers.
- Bonds multiple layers together in multilayer PCBs.
- Ensures mechanical stability of the board.
- Maintains dielectric spacing for impedance control.
- Provides adhesion strength during lamination under heat and pressure.

FR-4 Properties

- **Material:** Woven fiberglass cloth with epoxy resin (like FR-4 but uncured).
- **State:** "B-stage" resin – partially cured (solid, tacky), fully cures under heat.
- **Dielectric Constant (Dk):** Similar to FR-4, ~4.2–4.8.
- **Thickness Options:** 2–8 mil (0.05–0.2 mm), used in stacks to achieve required spacing.
- **Thermal Behavior:** Melts, flows, and hardens during lamination → bonds layers.

Role in PCB Stack-Up

- In 2-layer PCBs → Not required (just copper + core).
- In Multilayer PCBs → Placed between copper-clad cores to build up the stack.
- Example (4-layer PCB): Copper foil – Prepreg – Core (FR-4) – Prepreg – Copper foil.



Design Considerations

- Prepreg thickness affects impedance and capacitance of signal traces.
- Must be chosen carefully to meet stack-up requirements from the manufacturer. Excess resin flow can cause voids or shorts.
- Overuse of prepreg may cause warpage in high-layer count boards.

FUNDAMENTALS OF PCB DESIGN

Solder Mask

A Solder Mask is the protective colored coating applied over the copper traces of a PCB. It insulates the copper, prevents oxidation, and stops accidental solder bridges during assembly. **Common colors: Green (industry standard), but also red, blue, black, white, and matte finishes.**

Function:

- **Prevents Short Circuits** – Stops solder bridges between fine-pitch pads.
- **Protects Copper** – Guards against oxidation, corrosion, and environmental damage.
- **Improves Insulation** – Adds an extra dielectric layer between conductors.
- **Aids Assembly** – Leaves only pads exposed, ensuring solder sticks where needed.
- **Improves Aesthetics** – Gives the PCB its clean, colored finish.

Types of Solder Mask

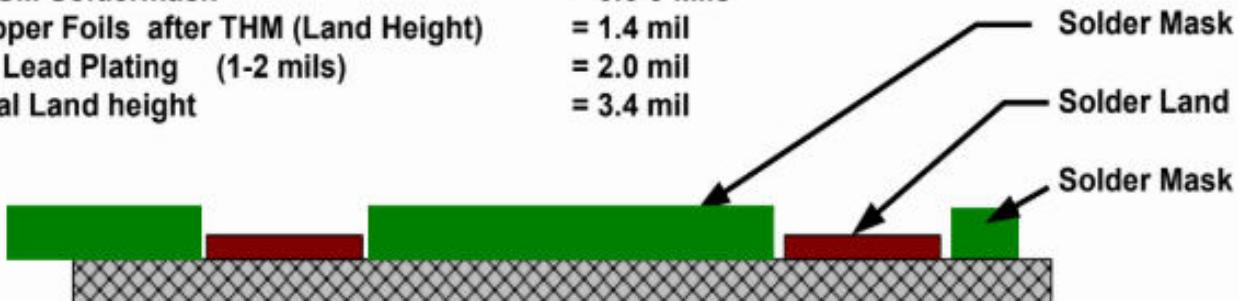
- **Liquid Photoimageable (LPI)**: Most common, applied as liquid → exposed with UV → developed to leave pad openings.
- **Dry Film**: Sheet-based, laminated and patterned. Used in some high-reliability or fine-line boards.
- **Epoxy Liquid**: Silkscreen-applied, cheaper, mostly used for simple boards.

Thickness

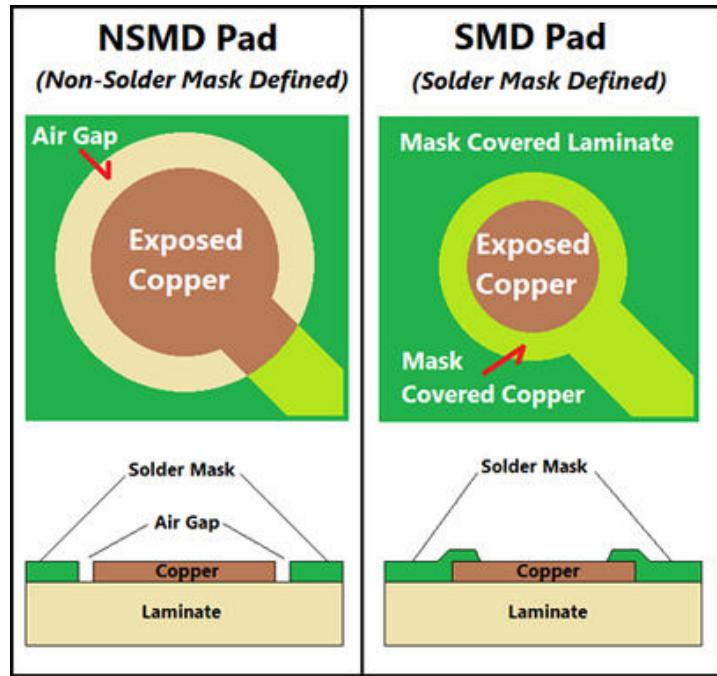
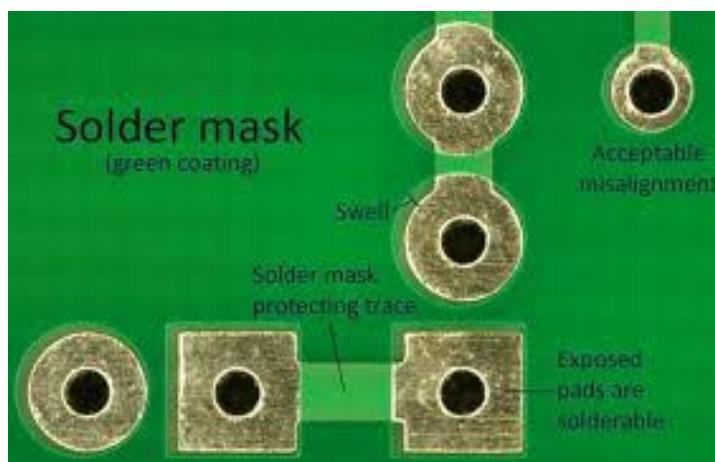
- Typically 0.5 – 1.2 mil (12 – 30 µm).
- Enough to protect copper while keeping pads accessible for soldering.

Solder mask thickness Limit is: 4- 6 mil

Dry Film Soldermask	= 3 - 4 Mils
LPISM Soldermask	= 0.6-9 Mils
Copper Foils after THM (Land Height)	= 1.4 mil
Tin Lead Plating (1-2 mils)	= 2.0 mil
Total Land height	= 3.4 mil



FUNDAMENTALS OF PCB DESIGN



Applications

- Used in all modern PCBs except bare copper RF/microwave boards.
- Critical for fine-pitch components (QFN, BGA, QFP).
- Prevents bridging in SMT reflow soldering.
- Essential in automotive, consumer, and industrial PCBs for long-term reliability.

Design Considerations

- Solder Mask Opening (SMO): Must be aligned with pads → too small = soldering issues, too big = risk of shorts.
- Solder Mask Defined (SMD) Pads: Mask defines the pad size (used in BGAs).
- Non-Solder Mask Defined (NSMD) Pads: Copper defines the pad, mask is slightly larger (better for reliability).
- Clearances: Typically 3–4 mil (75–100 µm) between copper features.
- Color Choice: Dark colors absorb more heat (affects IR reflow slightly). White solder mask is harder to inspect visually.

The **solder mask** is the thin protective layer that covers PCB copper traces, leaving pads exposed for soldering. It ensures **electrical insulation, corrosion protection, and assembly reliability**, while also giving the PCB its **distinctive color and professional finish**.

FUNDAMENTALS OF PCB DESIGN

Silkscreen

The silkscreen is the printed text and graphics layer on a PCB.

It is applied over the solder mask (usually in white ink, but also available in yellow, black, or other colors) to provide labels, component identifiers, and symbols that help in assembly, testing, and repair.

Function:

- Component Identification – Reference designators (R1, C5, U3, etc.).
- Orientation Marks – Pin 1 markers, polarity indicators (+/-).
- Assembly Guidance – Connector labels, test point IDs, switch settings.
- Branding – Company logos, product IDs, version numbers.
- Warnings & Instructions – Voltage ratings, safety marks, handling notes.

Methods

- Screen Printing – Traditional method, lower resolution, used for simple boards.
- Liquid Photoimageable (LPI) Ink – UV cured, higher accuracy, most common today.
- Direct Legend Printing (DLP) – Inkjet printing, high precision, used in modern fabs.

Typical Specifications

- Ink Color: White (most common), Yellow (dark boards), Black (light boards).
- Line Width: Minimum 0.15 mm (6 mils) for legibility.
- Text Height: 1.0 mm minimum recommended.
- Placement: Avoid pads and vias → silkscreen on copper pads can cause soldering issues.



FUNDAMENTALS OF PCB DESIGN

Applications

- Used in all PCBs for ease of assembly, testing, and maintenance.
- Crucial for manual soldering, debugging, and repair.
- Helps avoid assembly errors by providing clear markings.

Design Considerations

- Keep silkscreen off exposed copper pads.
- Ensure text size is readable after fabrication.
- Place pin 1 indicators near ICs for orientation.
- Use silkscreen to mark critical signals (e.g., GND, VCC).
- Include board name, revision, and date code for traceability
- Place Component legend outside part outlines
- Text height = 0.040"(1.00mm)
- Stroke thickness =0.006"(0.15mm)
- Position Polarity indicators correctly
 - Should not come next to adjacent component
 - Use chamfers on outlines to show polarity
- Identify Pin 1 of all IC's either with ● or "1"
- Add pin numbers at regular intervals for high pin components (except BGA)
- Keep all silk screen legend clear of solderable points by minimum of 0.015"(0.4mm)
- Clip all legend outlines

*The silkscreen is the printed labeling layer on a PCB that provides **component identifiers, orientation marks, and instructions**, making assembly, debugging, and maintenance much easier.*

FUNDAMENTALS OF PCB DESIGN

Surface Finish

The surface finish is the protective coating applied to exposed copper pads on a PCB. It preserves solderability, prevents oxidation, and ensures reliable component assembly.

Function:

- Protects exposed copper pads from oxidation & corrosion.
- Provides a solderable surface for component assembly.
- Ensures good electrical contact for connectors and test points.
- Improves reliability and shelf life of the PCB.

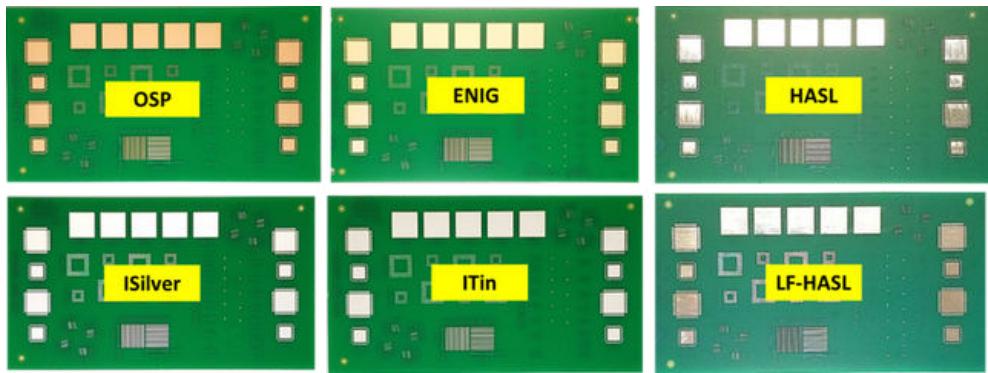
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Common Types of Surface Finish

Finish	Full Form	Features	Pros	Cons
HASL	Hot Air Solder Leveling	Pads coated with molten solder, leveled with hot air	Low-cost, widely used, long shelf life	Not flat (bad for BGAs), not RoHS if leaded
ENIG	Electroless Nickel Immersion Gold	Nickel barrier with thin gold layer	Flat, great for BGAs, RoHS, excellent shelf life	Expensive, risk of "black pad" defect
OSP	Organic Solderability Preservative	Organic layer protecting copper	Flat, low-cost, RoHS compliant	Limited shelf life, sensitive to handling
Immersion Tin	Cu coated with thin tin layer	Good solderability, flat	RoHS, inexpensive	Short shelf life, whisker risk
Immersion Silver	Cu coated with thin silver	Excellent conductivity, flat	RoHS, good for RF	Tarnishes easily, sensitive to storage
Hard Gold	Electroplated thick gold	High durability for edge connectors	Very durable, good wear resistance	Very expensive, overkill for normal pads

FUNDAMENTALS OF PCB DESIGN



Thickness

- HASL: ~1–40 µm solder
- ENIG: 3–6 µm nickel + 0.05–0.1 µm gold
- OSP: 0.2–0.5 µm organic layer
- Immersion Silver: 0.1–0.4 µm
- Immersion Tin: 0.8–1.2 µm
- Hard Gold: 30–50 µm gold plating

Applications

- HASL: Consumer, industrial boards with larger pitch components.
- ENIG: High-density BGAs, fine-pitch ICs, high-reliability boards.
- OSP: Low-cost mass production (mobile, consumer).
- Immersion Silver: RF/microwave, high-frequency designs.
- Hard Gold: Edge connectors, wear surfaces.

Applications

- Select finish based on component pitch (BGAs require flat finishes).
- Consider cost vs. reliability trade-off.
- RoHS compliance may rule out leaded HASL.
- Shelf life differs (OSP < 6 months, ENIG > 1 year).

A surface finish is the protective and solderable coating applied to PCB pads. The choice (HASL, ENIG, OSP, silver, tin, hard gold) depends on **cost, reliability, pitch size, and application**.

BASICS ELEMENTS IN PCB DESIGN

Vias in PCB

A via is a plated hole in a PCB that provides an electrical connection between different layers of the board.

It is filled or hollow, lined with copper, and allows signals, power, or ground to travel vertically between layers.

Function of Vias

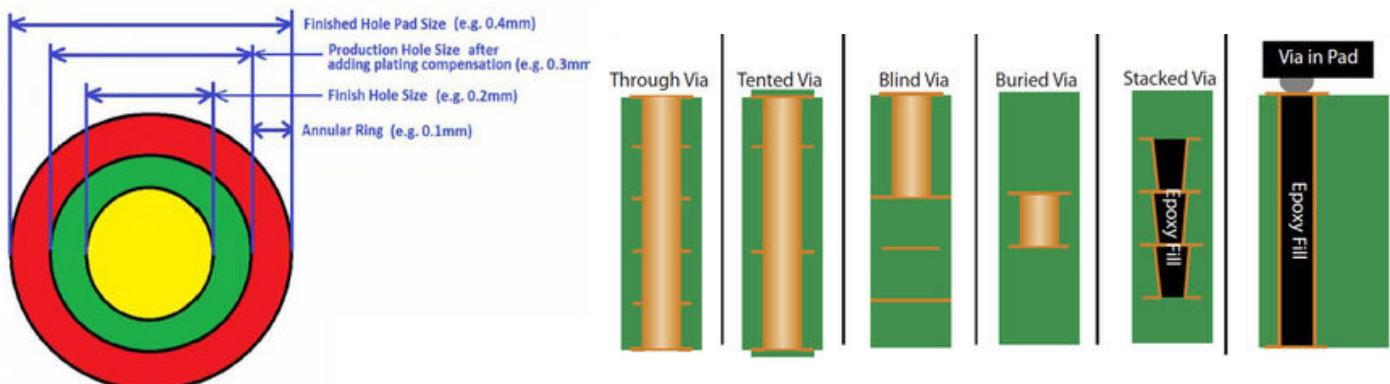
- Connect traces between layers in multilayer PCBs.
- Provide power and ground distribution through multiple layers.
- Support thermal management (thermal vias under power devices).
- Allow dense routing in high-pin-count packages (BGA, QFN, QFP).

Via Structure

- Drilled Hole – mechanical or laser-drilled.
- Plated Copper Barrel – provides conductivity.
- Annular Ring – copper pad around the via hole.
- Aspect Ratio – ratio of hole depth to diameter (typically $\leq 8:1$ for reliable plating).

Via Sizing

- Minimum size: Determined by PCB manufacturer capabilities, typically 0.2–0.3 mm drill diameter.
- Aspect ratio: Ensure via depth-to-diameter ratio supports reliable plating (commonly $\leq 8:1$).
- Current capacity: Select via size based on required current (multiple vias for high-current paths).
- Signal Integrity: Avoid placing vias in high-speed signal paths unless necessary, minimize stubs.
- Clearance: Maintain adequate spacing between vias and other features to prevent



BASICS ELEMENTS IN PCB DESIGN

Types of Vias

- Through-Hole Via
 - Drilled through the entire board.
 - Most common and cost-effective.
- Blind Via
 - Connects an outer layer to one or more inner layers (but doesn't go through the board).
 - Saves space in high-density designs.
- Buried Via
 - Connects only inner layers, not visible on outer layers.
 - Used in advanced multilayer boards.
- Microvia
 - Very small laser-drilled vias.
 - Used in HDI (High Density Interconnect) PCBs for smartphones, DDR, high-speed.
- Via-in-Pad
 - Placed directly on component pads (BGA escape routing).
 - Usually filled and plated flat to allow soldering.

Design Considerations

- Size: Standard via: 0.2–0.3 mm drill diameter. & Microvia: 0.05–0.15 mm.
- Current Capacity: Larger or multiple vias needed for power distribution.
- Thermal Relief: Multiple vias under hot components improve heat dissipation.
- Signal Integrity: High-speed signals require careful via design to minimize stub effect.
- Cost: Blind, buried, and microvias increase fabrication cost.

Applications

- Signal Vias: Connect traces across layers.
- Power Vias: Carry high current between planes.
- Thermal Vias: Dissipate heat from ICs, regulators, or MOSFETs.
- Escape Routing: Used under BGAs for breaking out dense pin grids.

A via is a plated hole in a PCB that connects copper layers vertically. They are essential for **multilayer routing, power delivery, and thermal management**, with different types (through, blind, buried, microvia) used depending on design complexity.

BASICS ELEMENTS IN PCB DESIGN

PAD in PCB

A pad in PCB design is the exposed area of copper (often covered with surface finish) where an electronic component's lead, pin, or ball makes an electrical and mechanical connection to the board.

Pads are essential for soldering components and for creating electrical contact points.

Function of Pads

- Provide soldering area for SMT and through-hole components.
- Ensure electrical connectivity between component pins and PCB traces.
- Serve as test points for debugging or manufacturing tests.
- Distribute heat during soldering, affecting solder joint quality.

Types of Pads

A. Based on Component Mounting

- **Through-Hole Pads:** Circular or oval pads with drilled holes, used for DIP, connectors, pin headers.
- **Surface-Mount Pads (SMD):** Flat exposed copper areas for SMD parts (resistors, capacitors, ICs).

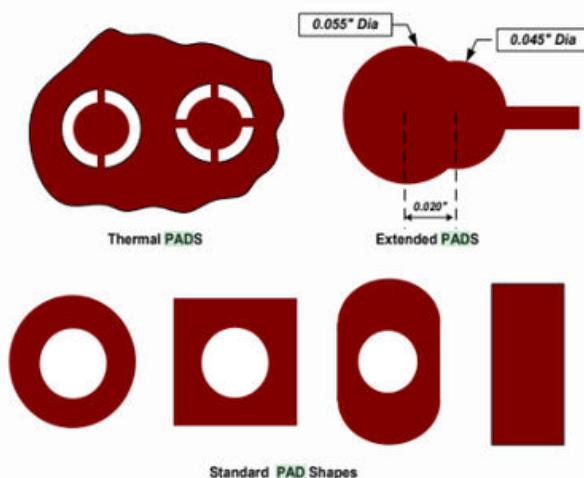
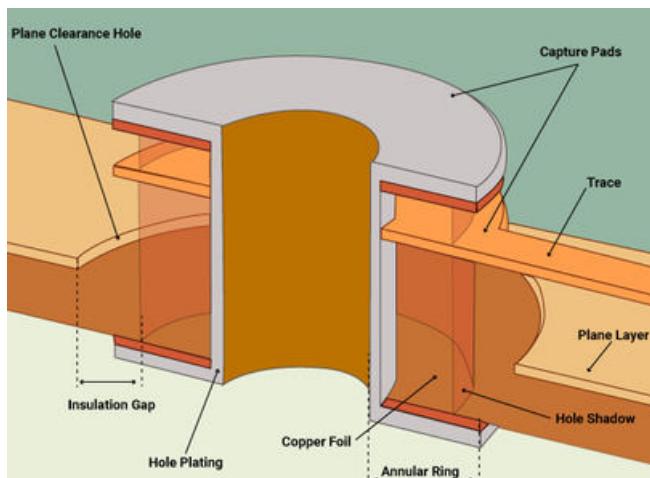
B. Based on Function

- **Single Pad** – For individual components or test points.
- **SMD Pad Array** – For QFP, QFN, or BGA packages.
- **Thermal Pad** – Large exposed copper pad under power ICs (for heat dissipation).
- **Via Pad** – Copper pad connected to vias for layer transition.

C. Special Pad Designs

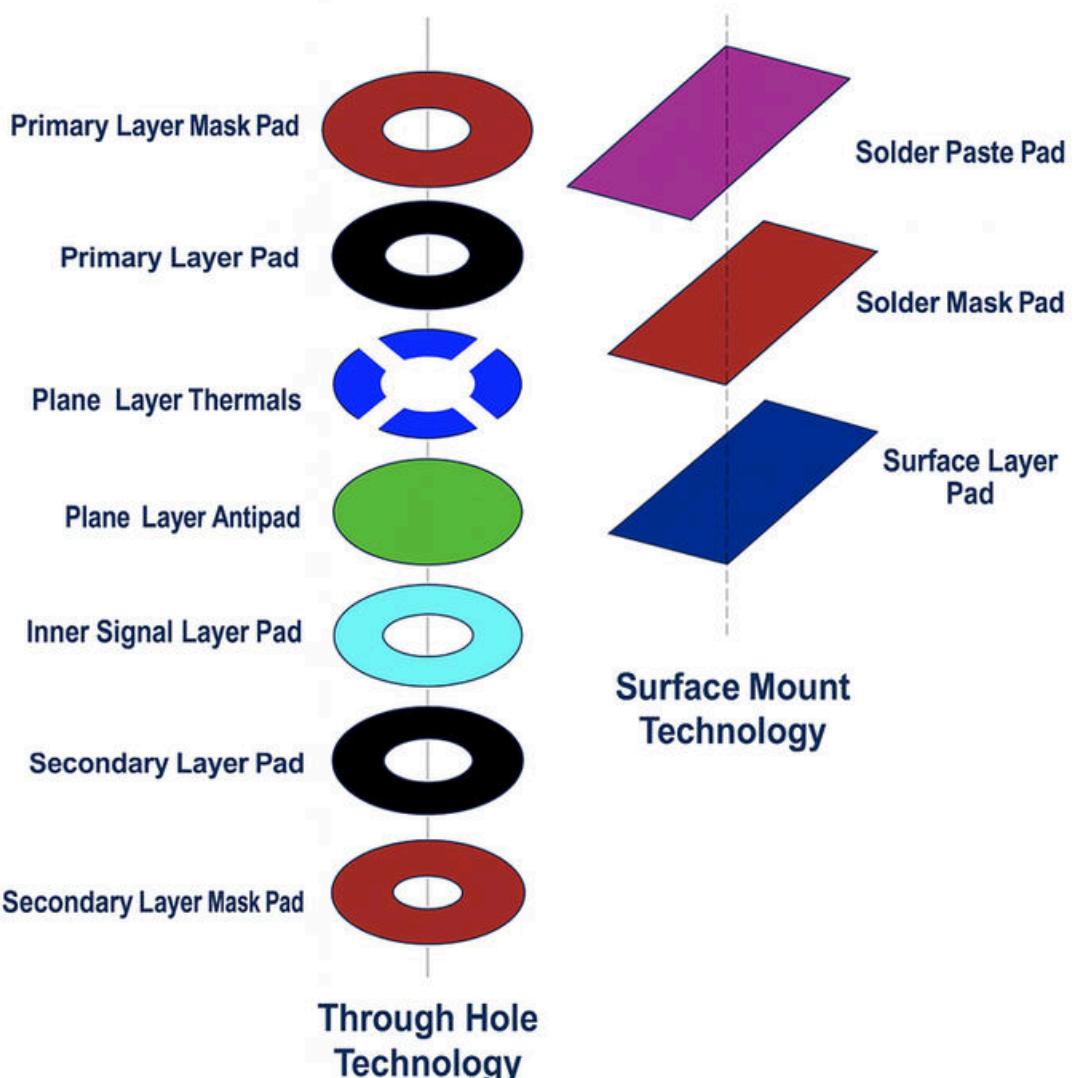
- **Round Pad** – Standard for through-hole and many SMT parts.
- **Oval Pad** – Provides more solder area, stronger adhesion.
- **Rectangular Pad** – Common for chip resistors, capacitors.
- **Thermal Relief Pad** – Pad with spokes to make soldering easier (on planes).

BASICS ELEMENTS IN PCB DESIGN



Pad Stack

- A pad stack defines all pad shapes and sizes across PCB layers, including:
- Top Pad (copper + finish)
- Inner Layer Pad (for multilayer connections)
- Bottom Pad
- Drill/Via hole (if applicable)
- Solder mask opening (clearance around pad)



BASICS ELEMENTS IN PCB DESIGN

Design Considerations

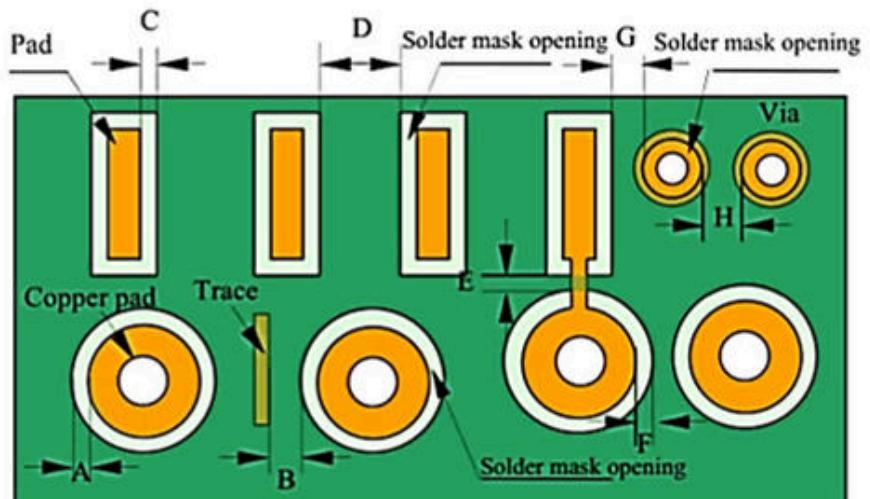
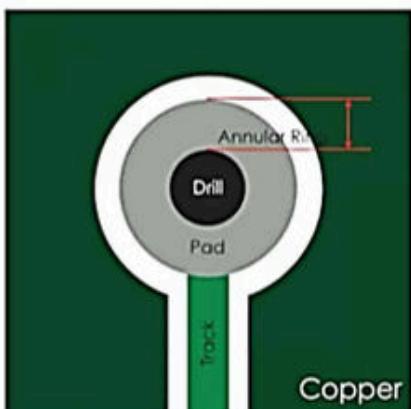
- Pad Size & Shape: Must follow IPC-7351 standards.
- Annular Ring: Minimum copper around drill hole (for through-hole pads).
- Solder Mask Clearance: Opening must be slightly larger than pad.
- Pitch & Spacing: Critical for fine-pitch ICs (QFN, BGA).
- Thermal Relief: Prevents soldering issues on large copper pours.
- Via-in-Pad: Used in HDI/BGA escape routing (requires filling & plating).

Applications

- Mounting and soldering all components.
- Providing test and debugging points.
- Creating thermal pads under ICs (e.g., power regulators, MOSFETs).
- Supporting mechanical strength of solder joints.

A **pad** is an exposed copper area on a PCB that allows components to be soldered and connected electrically. Pads come in many types (through-hole, SMD, thermal, test pads), and their design (size, shape, clearance) directly impacts **solderability, reliability, and manufacturability**.

Important Basic Elements



BASICS ELEMENTS IN PCB DESIGN

Units and Measurements in PCB

Common Units Used

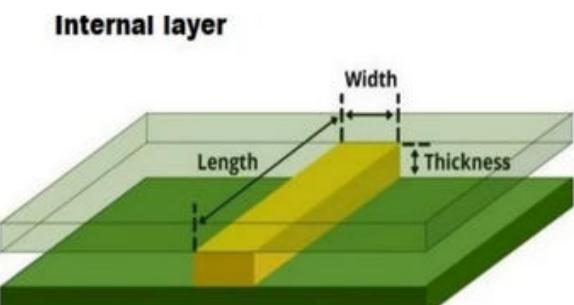
PCB design uses both imperial and metric units:

Unit	Definition	Equivalent	Usage
Mil	1/1000 inch (0.001 in)	1 mil = 25.4 µm = 0.0254 mm	Trace width, spacing, drill sizes
Millimeter (mm)	1/1000 meter	1 mm = 39.37 mils	Board dimensions, component pitch
Micrometer (µm)	1/1,000,000 meter	1 µm = 0.039 mil = 0.001 mm	Copper thickness, precision spacing
Inch	Standard imperial unit	1 in = 25.4 mm = 1000 mils	Connector spacing, mechanical outlines

Key PCB Measurements

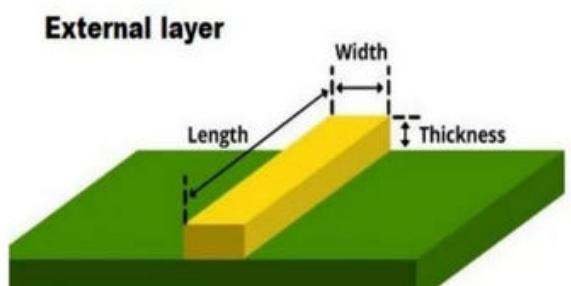
A. Trace Width

- Defines how wide a copper track is.
- Typical:
 - Signal traces: 4–8 mil (0.1–0.2 mm).
 - Power traces: 20–80 mil (0.5–2 mm), depending on current.
- Calculated using IPC-2152 (current vs. width).



B. Clearance (Spacing)

- Distance between two copper features.
- Standard: 4–6 mil (0.1–0.15 mm).
- High-voltage PCBs require larger clearances per IPC-2221.



C. Drill Sizes

- For vias and through-hole components.
- Typical via drill: 0.2–0.3 mm.
- Component holes: 0.6–1.2 mm depending on lead diameter.
- Aspect Ratio Rule: Depth-to-diameter $\leq 8:1$ for reliable plating.

D. Copper Thickness (Copper Weight)

- Defined in oz/ft² → equivalent thickness in microns.
- Standard:
 - 0.5 oz = 17 µm | 1 oz = 35 µm | 2 oz = 70 µm
- Heavier copper used for power electronics.

BASICS ELEMENTS IN PCB DESIGN

E. PCB Thickness

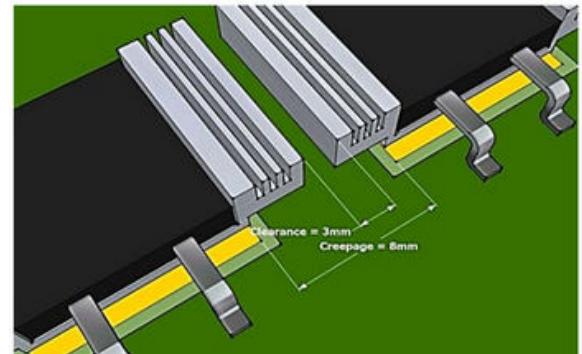
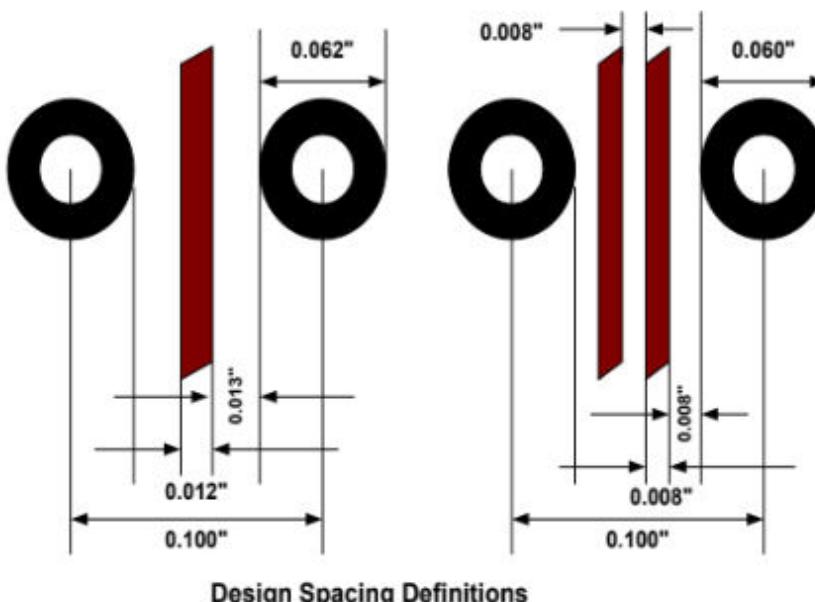
- Standard: 1.6 mm (0.062 in).
- Range: 0.4 mm – 4.75 mm (depends on layers & application).
- Flex PCBs can be as thin as 0.05 mm.

F. Component Pitch

- Distance between pins or balls in IC packages.
- Common:
 - SOIC: 1.27 mm
 - QFP: 0.8 mm
 - QFN/BGA: 0.5–0.8 mm
 - Advanced BGAs: down to 0.3–0.4 mm

Standard Design Rules (Typical)

- Trace-to-Trace Clearance: \geq 4 mil (0.1 mm).
- Via-to-Trace Clearance: \geq 2 mil (0.05 mm).
- Pad-to-Pad Clearance: \geq 4 mil (0.1 mm).
- Board Edge Clearance: \geq 20–40 mil (0.5–1.0 mm).



PCB design uses **mils, mm, μm , and oz/ft²** as core units.

Critical measurements include **trace width, spacing, drill size, copper thickness, board thickness, and component pitch** – all of which affect **signal integrity, current capacity, manufacturability, and reliability**.

BASICS ELEMENTS IN PCB DESIGN

Electronic Packaging

Common Units Used

Electronic packaging refers to the way electronic components are enclosed, mounted, and connected to a PCB.

It determines how components fit on the board, how signals are routed, and how heat is managed.

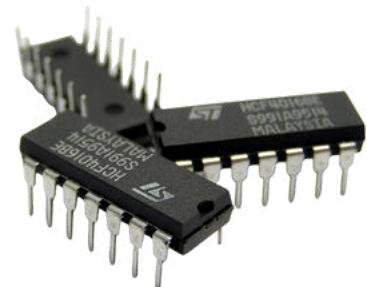
Importance in PCB Design

- Directly affects component placement and routing complexity.
- Defines pad design, footprint size, and soldering method.
- Influences mechanical constraints (board area, thickness, height restrictions).
- Impacts thermal dissipation, reliability, and assembly yield.

Major Packaging Types

A. Through-Hole Packages

- Leads go through drilled holes in the PCB.
- Examples: DIP (Dual In-line Package), Pin Headers, Connectors.
- Pros: Strong mechanical bond, easy prototyping, suitable for connectors/high power.
- Cons: Requires drilling, larger board area, limits routing density.



B. Surface Mount Packages (SMT)

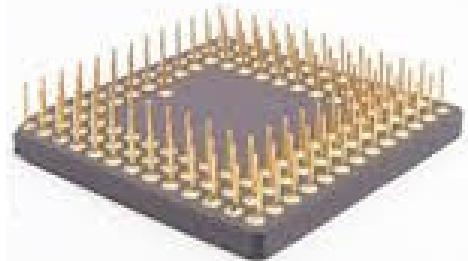
- Components soldered directly on PCB pads, no drilled holes.
- Examples: SOIC, QFP, QFN, BGA, chip resistors/capacitors.
- Pros: Smaller size, higher density, both sides of PCB usable.
- Cons: Requires precise placement, harder to rework manually.



BASICS ELEMENTS IN PCB DESIGN

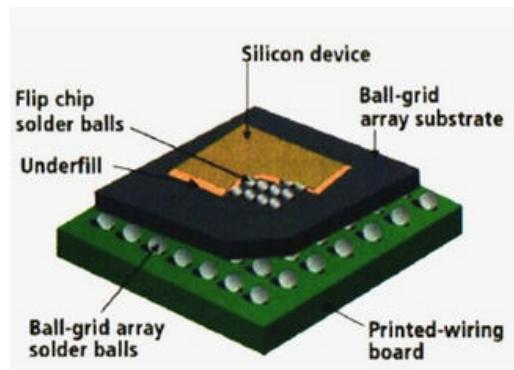
C. Grid Array Packages

- Pins/balls arranged in a grid under the component.
- Examples: BGA (Ball Grid Array), LGA (Land Grid Array).
- Pros: Very high I/O count, compact size, excellent electrical performance.
- Cons: Complex routing (needs microvias, multilayer PCBs), difficult inspection.



D. Chip-Scale & Advanced Packages

- CSP (Chip Scale Package): Package almost same size as die.
- Flip-Chip: Die bonded directly with bumps → best performance.
- 3D Packaging (SiP, PoP): Multiple dies stacked (used in mobile, IoT, high-performance CPUs).
- Pros: High performance, space-saving.
- Cons: Very expensive, complex assembly.



PCB Design Considerations for Packaging

- Pad & Footprint Design – must follow IPC-7351 standards.
- Routing Strategy – through-hole vs. surface mount vs. BGA escape.
- Thermal Design – large thermal pads/vias for power packages.
- Assembly Method – hand soldering, reflow, wave soldering.
- Inspection & Testing – BGAs need X-ray inspection.
- Board Density – fine-pitch SMT and BGAs need more PCB layers.

Package Pitch & Layout Difficulty

Package Type	Typical Pitch	Layout Difficulty	Thermal Performance
SOIC	1.27 mm	Low	Good
QFP	0.8 mm	Medium	Fair
QFN	0.5 mm	Medium	Excellent (thermal pad)
BGA	0.5–1.0 mm	High	Excellent

BASICS ELEMENTS IN PCB DESIGN

Key Calculations in PCB Design

1. Trace Width Calculation

- Purpose: Ensure the copper trace can carry the required current without overheating.
- Standard: IPC-2152.
- Formula (approx.): $W = \frac{I}{k \times (\Delta T)^b \times (H^c)}$

$$\text{External Layers Area} = \frac{I}{(0.0647 \times (\Delta T)^{0.4281})^{1/0.6732}}$$
$$\text{Internal Layers Area} = \frac{I}{(0.0150 \times (\Delta T)^{0.5453})^{1/0.7349}}$$

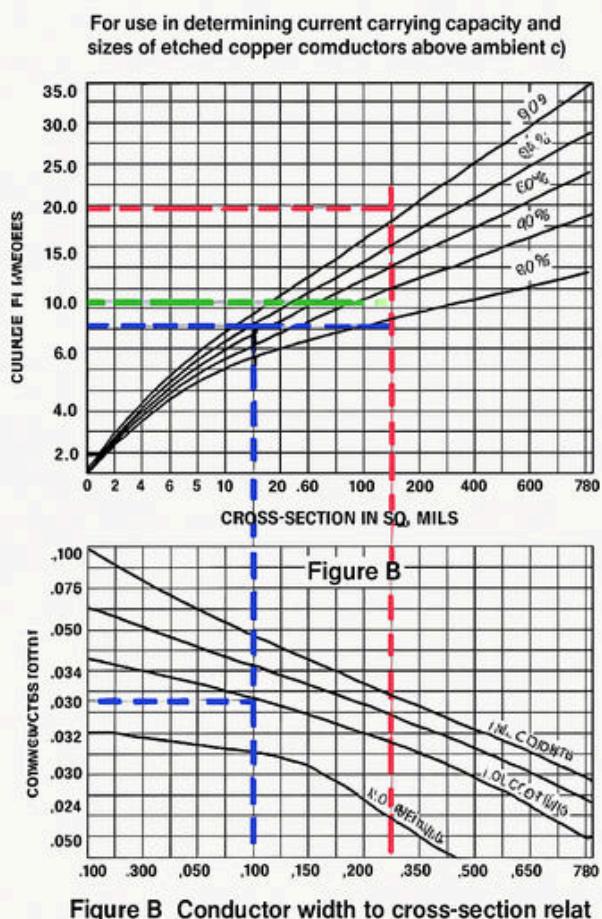
ΔT = Temperature rise over ambient in °C

I = Current carrying capacity of conductor

Where:

- W = Trace width
- I = Current (A)
- ΔT = Allowed temperature rise (°C)
- H = Copper thickness (μm)
- k, b, c = Constants (different for internal/external layers).

- Example1: 1 A on external 1 oz copper (35 μm), 10°C rise → ~0.25 mm width.
- Example2:



Let us compute trace width for:

Current rating = 5A
Temp, Rise acceptable : 30°C
Copper Clad Laminate = 1Oz (35)

- Figure A- draw a line at 5A Current
- Find intersection to curve 30°C
- Draw vertical line from this to Figure B to intersect 1oz line. This gives a cross section of 80 sq. mils.
- At this intersection draw a line to the Y axis that find the conductor width. You find that trace width = 0,055"

You will find for that if the conductor was interrial conductor, the trace width required a 170 sq. mils.

Trace width
= 0,055"

BASICS ELEMENTS IN PCB DESIGN

2. Impedance Calculation

- **Purpose:** For high-speed signals (USB, DDR, PCIe, HDMI), controlled impedance is critical.
- **Standard:** IPC-2141, field solver tools.
- **Formulas (simplified):**

- Microstrip (surface trace): $Z_0 \approx \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln \left(\frac{5.98h}{0.8W + t} \right)$

- Stripline (internal trace): $Z_0 \approx \frac{60}{\sqrt{\epsilon_r}} \ln \left(\frac{4h}{0.67(\pi(W + t))} \right)$

Common values:

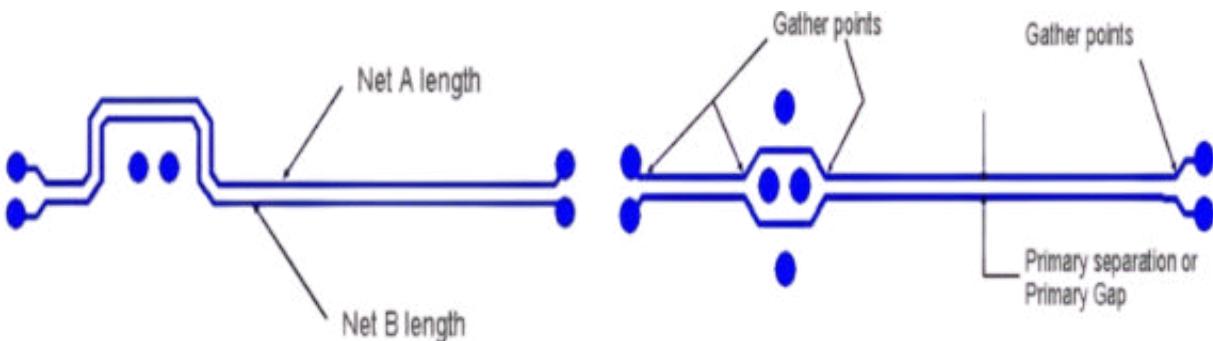
- Single-ended: 50 Ω
- Differential: 90–100 Ω

Where:

- Z_0 = Impedance (Ω), ϵ_r = Dielectric constant,
- h = height of dielectric, W = trace width, t = copper thickness.

3. Differential Pair Length Matching

- Purpose: Ensure signal pairs (USB, Ethernet, DDR, PCIe) arrive at the same time.
- **Calculation:**
- Skew tolerance depends on protocol.
- Example:
 - USB 2.0 requires ±150 mils (3.8 mm) matching;
 - DDR4 requires ±10 ps (~0.06 in).



4. Via Aspect Ratio

- Purpose: Ensure via plating reliability.
- Formula:
 - Aspect Ratio = $\frac{\text{Board Thickness}}{\text{Via Drill Diameter}}$
- Rule of Thumb: Aspect ratio ≤ 8:1 (e.g., 1.6 mm PCB → min via = 0.2 mm drill).

BASICS ELEMENTS IN PCB DESIGN

5. Thermal Calculations

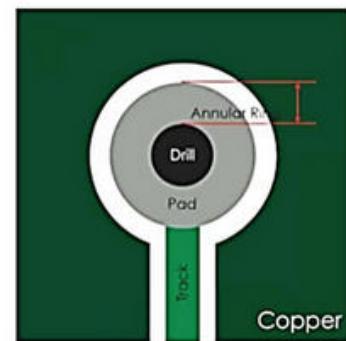
- Purpose: Estimate heat dissipation in copper planes and vias.
- Formula (thermal resistance): $R_{th} = \frac{\Delta T}{P}$
- Via Thermal Resistance: $\sim 70^{\circ}\text{C}/\text{W}$ for 0.3 mm plated via.
- Multiple vias in parallel reduce thermal resistance.

6. Creepage & Clearance

- Purpose: Ensure high-voltage safety (per IPC-2221 / IEC-60950).
- Clearance: Minimum air gap between conductors.
- Creepage: Minimum distance along surface of insulation.
- Rule Example:
 - 0–30 V \rightarrow 0.1 mm clearance
 - 30–150 V \rightarrow 0.2–1.0 mm
 - 600 V \rightarrow ≥ 5.0 mm

7. Annular Ring Calculation

- Purpose: Ensure sufficient copper around via drill.
- Formula:
$$\text{Annular Ring} = \frac{\text{Pad Diameter} - \text{Drill Diameter}}{2}$$
- Rule of Thumb: ≥ 4 mil (0.1 mm).



8. Power Plane Current Density

- Formula:
$$J = \frac{I}{A}$$
- External layer max: 35 A/mm²; Internal layer max: 17.5 A/mm² (per IPC-2221).

9. Stack-Up Thickness Control

- Purpose: Ensure signal impedance and mechanical stability.
- Calculate dielectric thickness between copper layers to control impedance.
- Typical: 3–5 mil (75–125 μm) prepreg between signal and plane.

10. Mechanical Calculations

- PCB Thickness – standard 1.6 mm, but check for rigidity vs. flexibility.
- Bend Radius (for Flex PCB): $\geq 10 \times$ thickness for repeated bends.
- Panelization & V-Scoring: Calculate spacing (typically 2–3 mm).

BASICS ELEMENTS IN PCB DESIGN

Important IPC Standards

The IPC publishes global standards for PCB design, fabrication, assembly, testing, and reliability. Below are the most relevant ones for PCB engineers:

1. PCB Design Standards

- IPC-2221 → Generic Standard on Printed Board Design
 - Covers basic PCB design rules (trace width, spacing, creepage, clearance).
- IPC-2222 → Sectional Design Standard for Rigid Organic Printed Boards.
- IPC-2223 → Sectional Design Standard for Flexible Printed Boards.
- IPC-2226 → HDI (High Density Interconnect) PCB design standard.

2. Fabrication Standards

- IPC-6011 → Generic Performance Specification for PCBs.
- IPC-6012 → Qualification and Performance Specification for Rigid PCBs.
- IPC-6013 → Performance Specification for Flexible PCBs.
- IPC-6018 → High-Frequency PCB Performance Specification (microwave/RF boards).

3. Acceptability Standards (Quality & Inspection)

- IPC-A-600 → Acceptability of Printed Boards
 - Defines visual quality standards for PCB fabrication (defects, plating, annular rings).
- IPC-A-610 → Acceptability of Electronic Assemblies
 - Gold standard for assembly inspection (solder joints, cleanliness, workmanship).

4. Assembly & Soldering

- J-STD-001 (IPC J-STD-001) → Requirements for Soldered Electrical and Electronic Assemblies
 - Defines soldering process requirements, flux types, cleanliness.
- IPC-7351 → Generic Requirements for Surface Mount Design and Land Pattern Standard
 - Defines footprints (pads) for SMD components.
- IPC-7711/7721 → Rework, Modification, and Repair of Electronic Assemblies.

BASICS ELEMENTS IN PCB DESIGN

5. Materials & Reliability

- IPC-4101 → Specification for Base Materials (laminates, FR-4, etc.).
- IPC-4562 → Specification for Copper Foil for PCBs.
- IPC-9592 → Requirements for Power Conversion Devices (power supplies).
- IPC-9701 → Reliability Qualification Testing for Surface Mount Attachments.

6. Testing & Verification

- IPC-TM-650 → Test Methods Manual (lab test methods for PCB reliability).
- IPC-9252 → Requirements for Electrical Testing of Unpopulated PCBs.

7. Classification Standards

- IPC-6011/6012 → Define PCB Classes (1, 2, 3).
- IPC-2615 → PCB Dimensioning and Tolerancing Standard.

PCB IPC Classification

PCB Classification – Based on Usage

- **Performance Class – IPC Classification**
 - **Class 1 : General Electronic Products**
 - Consumer electronics, Toys, Non-critical systems
 - **Class 2 : Dedicated Service Products**
 - Professional Systems, Computers, Communication Systems
 - **Class 3 : High Reliability Products**
 - Life Support systems, Radar's, Weapon systems, Satellite Communication equipment,

PCB Classification – Based on Yield

- **Producibility – IPC Classification**
 - Level A: General Design Complexity
 - Level B : Moderate Design Complexity
 - Level C : High Design Complexity

PCB Classification – Build

- **Construction – IPC Classification**
 - TYPE – 1 Single Sided Printed Board
 - TYPE – 2 Double-Sided Printed Board
 - TYPE – 3 Multilayer Board without Blind & Buried via
 - TYPE – 4 Multilayer Board with Blind & Buried via
 - TYPE – 5 Metal core Board without Blind & Buried via
 - TYPE – 6 Metal core Board with Blind & Buried via

DESIGN PREPARATION

Schematic Analysis

Schematic analysis is the process of reviewing and verifying the circuit diagram before moving to PCB layout.

It ensures that the schematic is logically correct, electrically valid, and ready for implementation.

Key Steps in Schematic Analysis

A. Net Connectivity Checks

- Ensure no floating pins or unconnected nets.
- Cross-check net labels (e.g., "GND" vs "Ground").
- Run ERC (Electrical Rule Check) to detect shorted nets or conflicts.

B. Power & Ground Verification

- Verify correct voltage assignment to each device.
- Add decoupling capacitors close to ICs.
- Check reset & enable pins are tied properly.

C. Component Validation

- Compare each symbol's pin mapping with datasheet pinout.
- Verify package & footprint assignments.
- Double-check orientation (e.g., diodes, polarized caps).

D. Critical Signal Identification

- Mark high-speed nets (USB, DDR, PCIe).
- Define differential pairs (TX+/TX-).
- Identify analog signals that need isolation.

E. Documentation & Annotation

- Proper reference designators (R1, C5, U3).
- Consistent naming conventions.
- Add notes for test points, jumpers, or optional components.

Schematic analysis ensures the **circuit diagram is complete, correct, and manufacturable** before moving to PCB layout. It involves **net verification, power checks, component validation, and marking critical signals** to avoid costly redesigns.

DESIGN PREPARATION

Component Selection

Choosing the right electronic parts for your circuit so that it works reliably, is easy to manufacture, and stays cost-effective.

Key Steps in Schematic Analysis

- Electrical Needs → Voltage, current, frequency, tolerance.
- Package Type → DIP, SOIC, QFN, BGA (must match PCB footprint).
- Availability → Prefer parts that are in stock and not obsolete.
- Cost → Balance performance vs budget.
- Thermal Rating → Can it handle the heat and power?
- Compliance → RoHS, automotive grade, medical grade (if needed).

Tips

- Place decoupling capacitors close to IC power pins.
- Choose standard resistor/capacitor values (easy to source).
- For critical ICs (CPU, FPGA), always plan second-source options.
- Avoid parts with long lead times unless absolutely necessary.

PACKAGE	PITCH	LAYOUT DIFFICULTY	THERMAL PERFORMANCE
SOIC	1.27MM	LOW	GOOD
QFP	0.8MM	MEDIUM	FAIR
BGA	0.5-1.0MM	HIGH	EXCELLENT
QFN	0.5MM	MEDIUM	EXCELLENT

Component selection is about picking the right part with the right ratings, package, availability, and cost. Good choices make your PCB easier to build, reliable, and cost-effective.

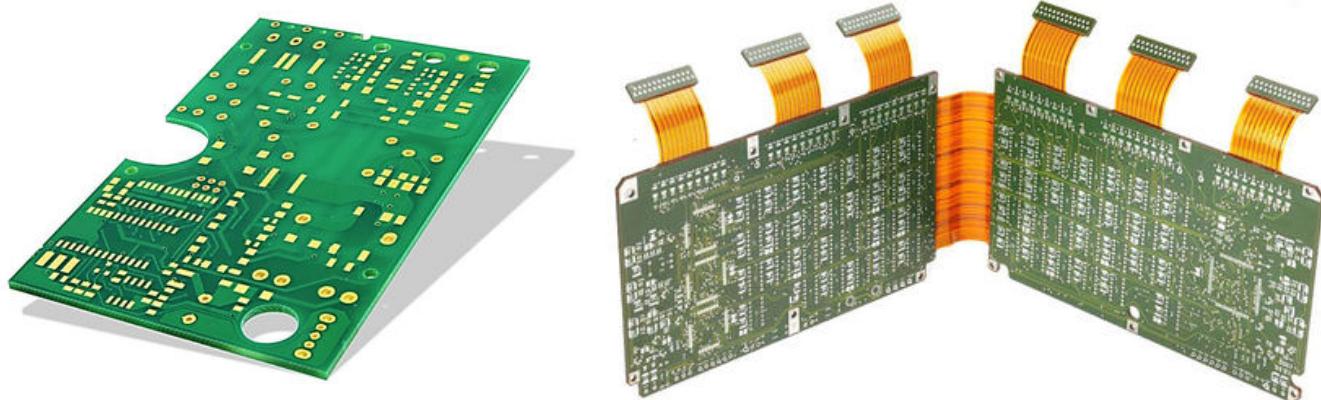
DESIGN PREPARATION

Material Selection for PCBs

The material of a PCB decides how well it handles signals, heat, strength, and cost.

Main Materials

- **FR-4 (Fiberglass Epoxy)** – Most common, low cost, general electronics.
- **Polyimide** – Flexible, high-temperature, used in flex/rigid-flex boards.
- **PTFE / Rogers** – Very low signal loss, used in RF and microwave boards.
- **Metal Core (Aluminum/Copper)** – Excellent heat dissipation, used in LED and power boards.
- **Ceramic** – High thermal conductivity, used in aerospace, medical, and high-frequency circuits.



Key Properties to Consider

- **Electrical** → Dielectric Constant (Dk), Loss Factor (Df).
- **Thermal** → Glass Transition Temp (Tg), Heat conduction.
- **Mechanical** → Flexibility, Strength, Thickness.
- **Reliability** → Moisture resistance, Chemical resistance.
- **Cost** → FR-4 cheapest, Rogers & Ceramic most expensive.

Choose PCB material based on electrical performance, thermal needs, mechanical strength, reliability, and cost.

- Use FR-4 for general use,
- Polyimide for flexible/high-temp,
- Rogers/PTFE for RF,
- Metal Core for power/LED,
- Ceramic for high-reliability.

DESIGN PREPARATION

PCB Stackup

PCB Stackup = The arrangement of copper layers (signal, power, ground) and insulating layers (dielectric) inside a PCB.

It decides how signals flow, how power is delivered, and how stable the board will be.

Why It's Important

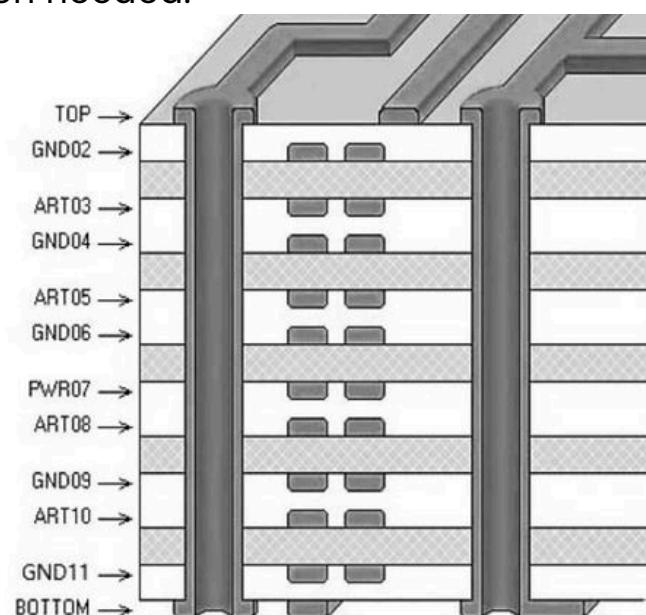
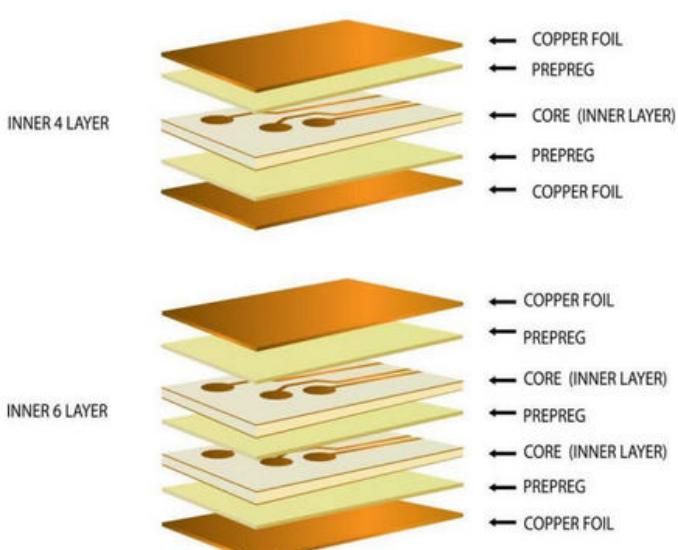
- Controls signal integrity (impedance, reflections).
- Ensures power integrity (clean power delivery).
- Reduces EMI/EMC issues.
- Provides mechanical balance (avoids warping).
- Affects cost (more layers = higher cost).

Common Types

- 2-Layer → Simple, low-cost boards (hobby, basic circuits).
- 4-Layer → Adds ground & power planes (better for high-speed, mid-complexity).
- 6-Layer → More signal layers + solid planes (DDR, USB, PCIe).
- 8+ Layers → High-speed, dense designs (servers, telecom, aerospace).

General Rules for Good Stackup

- Place ground planes next to signal layers (for return paths).
- Keep power & ground planes close (acts like a capacitor, improves decoupling).
- Use symmetrical stackups (top half = bottom half) to prevent warping.
- Route critical high-speed signals inside (between planes → stripline).
- Separate analog, digital, and RF zones when needed.



DESIGN PREPARATION

Board Planning

Board planning is the process of deciding the size, shape, layers, and component zones of the PCB before layout starts.

It acts as the blueprint for placement, routing, and manufacturing.

Why It's Important

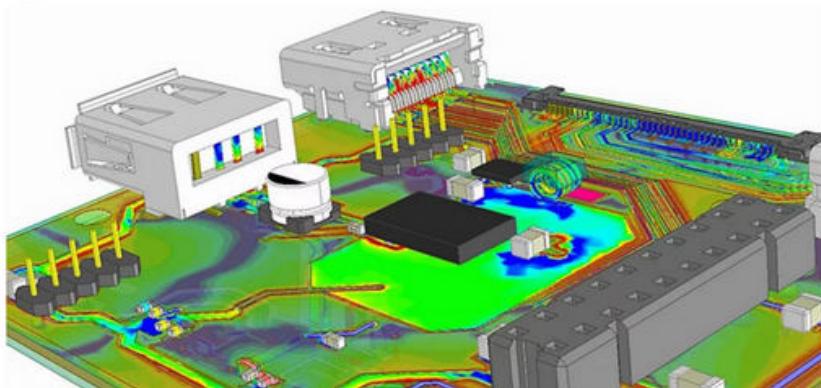
- Ensures the PCB fits inside the enclosure.
- Defines zones for analog, digital, RF, and power.
- Reduces layout rework and mistakes.
- Helps achieve signal integrity, thermal balance, and manufacturability.

Key Things to Define

- Board Outline & Size → based on enclosure or mechanical model.
- Mounting Holes & Keep-Outs → screws, connectors, and edges.
- Layer Count & Stackup → 2L, 4L, 6L, etc.
- Component Placement Zones:
 - Connectors → edges.
 - Power → one corner/side.
 - High-speed ICs → center with short routes.
 - Analog/RF → isolated from digital noise.
- Clearances → copper-to-edge, high-voltage creepage, thermal spacing.
- Test & Assembly Access → test pads, fiducials, rework space.

Example Planning Steps

- Import mechanical outline (DXF/STEP).
- Fix connectors, switches, LEDs at board edges.
- Place mounting holes & mechanical features.
- Assign zones for power, analog, digital, RF.
- Plan heat flow → power devices near edges, add thermal vias.
- Finalize stackup with manufacturer.

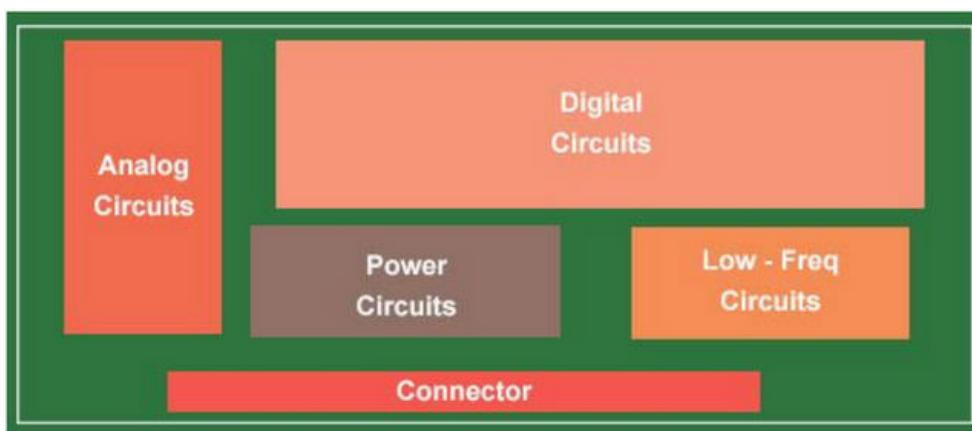


LAYOUT STRATEGIES

Layout strategies are the set of rules and best practices used to place components and route signals in a way that ensures the PCB is functional, reliable, and manufacturable.

Why It's Important

- Good layout = fewer errors, better performance.
- Helps maintain signal integrity, power integrity, and thermal balance.
- Reduces EMI/EMC issues.
- Makes manufacturing and testing easier.

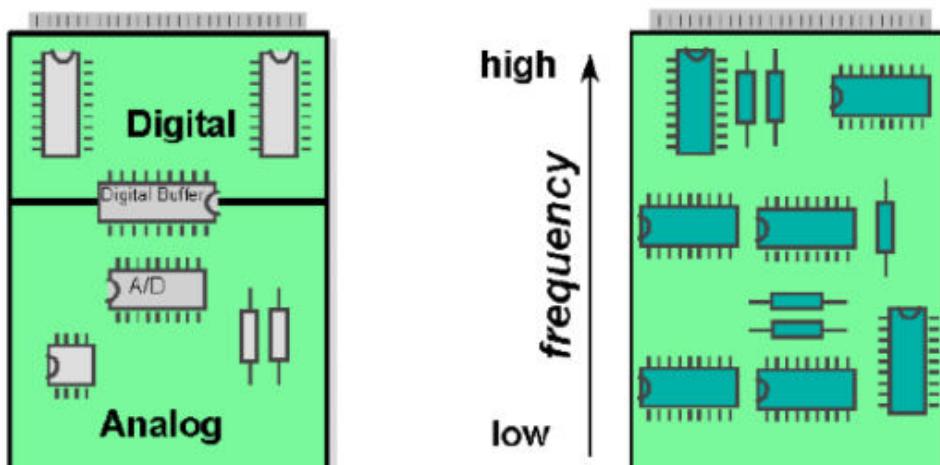


Component Placement

Component placement is the process of arranging electronic parts on the PCB in a way that makes the circuit functional, reliable, manufacturable, and easy to test. It's the first step in PCB layout before routing signals.

Why It's Important

- Determines signal flow efficiency.
- Affects heat dissipation.
- Controls noise and interference.
- Impacts manufacturability and testing.



LAYOUT STRATEGIES

Placement Guidelines

A. Mechanical & Edge Components

- Place connectors, switches, buttons, LEDs at board edges for accessibility.
- Reserve keep-out zones near mounting holes.

B. Functional Grouping

- Group parts by function:
 - Power section (regulators, MOSFETs, inductors) → one corner/edge.
 - High-speed ICs (CPU, DDR, FPGA) → center for short routes.
 - Analog circuits → isolated from digital noise.
 - RF sections → near antenna with clear keep-out areas.

C. Critical Components

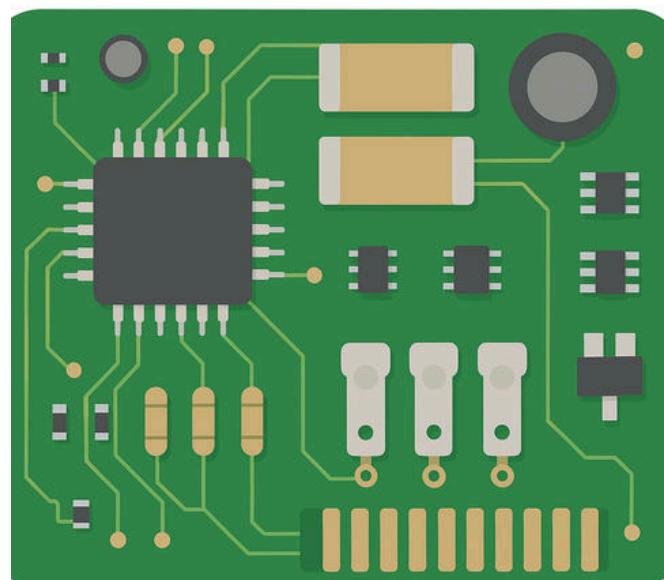
- Place decoupling capacitors as close as possible to IC power pins.
- Orient polarized parts (diodes, electrolytics, IC Pin 1) consistently to reduce errors.
- Keep sensitive parts away from heat sources.

D. Thermal Considerations

- Spread out hot components.
- Place high-power parts near board edges or heatsinks.
- Use copper pours & thermal vias under power devices.

E. Manufacturability & Testing

- Align parts in uniform orientation for easy assembly.
- Leave rework space around BGAs, QFNs, and connectors.
- Add test pads in accessible areas.



Component placement sets the foundation of PCB layout. By **placing mechanical parts, grouping functions, positioning critical ICs, and considering thermal and test requirements**, you make routing easier, improve reliability, and simplify manufacturing.

LAYOUT STRATEGIES

Signal Routing

Signal routing is the process of drawing copper traces that connect components on the PCB according to the schematic.

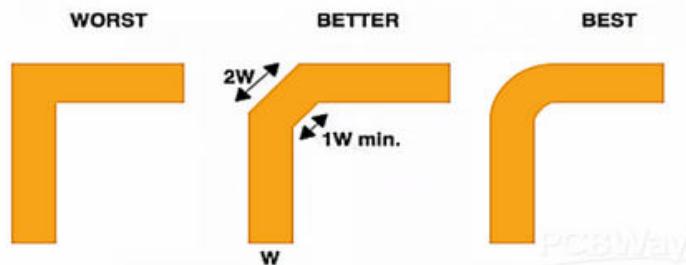
It decides how fast, clean, and reliable signals move across the board.

Why It's Important

- Poor routing → noise, reflections, EMI, crosstalk.
- Good routing → stable signals, high-speed reliability, manufacturable PCB.

General Routing Rules

- Keep traces short and direct.
- Use 45° bends (avoid 90° corners).
- Match trace width to current and impedance needs.
- Minimize via count → every via adds inductance & delay.
- Keep clearance per design rules (4–6 mil typical).



High-Speed Routing

- Controlled Impedance: Maintain 50Ω (single-ended), $90\text{--}100 \Omega$ (differential).
- Differential Pairs: Keep parallel, equal length, constant spacing.
- Length Matching: Match data and clock lines (DDR, USB, PCIe).
- Return Paths: Always route signals over a solid ground plane.
- Crosstalk Control: Apply 3W rule (space = $3 \times$ trace width).

Power & Sensitive Signal Routing

- Keep analog signals away from digital/high-speed.
- Route noisy power traces separately from signals.
- Use guard traces or shielding for sensitive analog nets.

Layer Usage Strategy

- Top/Bottom Layers: Component placement, short signal routes.
- Inner Layers: High-speed signals, stripline routing.
- Dedicated Planes: Power and ground for stability.

LAYOUT STRATEGIES

Power & Ground

- Power planes/traces distribute voltage to components.
- Ground planes/traces provide the return path for current.
- Together they form the Power Distribution Network (PDN) of the PCB

Why It's Important

- Stable power delivery ensures ICs function correctly.
- Solid ground return paths reduce noise and EMI.
- Poor design leads to voltage drops, ground bounce, unstable circuits.

Power Design Rules

- Use wide traces or copper pours for power rails (low resistance).
- For high-current paths, use 2 oz copper or more.
- Place decoupling capacitors close to IC power pins.
- Separate analog and digital power zones if needed.
- Use ferrite beads/filters between noisy and sensitive rails.

Ground Design Rules

- Use a solid ground plane (not broken or split).
- Stitch ground with multiple vias (near signal vias & ICs).
- Avoid routing signals across plane splits (causes noise).
- For mixed-signal boards → use separate analog and digital grounds, joined at a single point.
- Add thermal vias under power devices for heat sinking.

Layer Usage Strategy

- In 4-layer PCBs: dedicate one full layer to GND, one to PWR.
- In 6+ layer PCBs: multiple GND planes shield signal layers.
- Place power plane adjacent to ground plane → acts as a capacitor (improves decoupling).

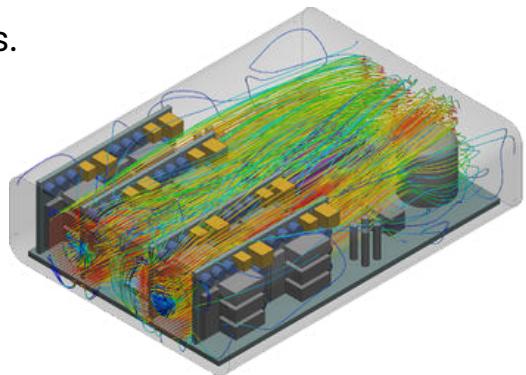
LAYOUT STRATEGIES

Thermal Management

Thermal management is the practice of controlling how heat is generated, spread, and dissipated in a PCB so that components work within safe temperature limits.

Why It's Important

- Prevents overheating & failure of components.
- Improves reliability & lifetime of the PCB.
- Ensures stable performance under load.



Sources of Heat in PCBs

- Power devices (MOSFETs, regulators, CPUs).
- High-current traces and planes.
- LEDs and high-power resistors.
- Dense ICs (FPGAs, GPUs, DDR).

Thermal Management Techniques

- Copper Pours & Wide Traces → Spread heat over large copper areas.
- Thermal Vias → Transfer heat from top to inner/bottom copper planes.
- Heatsinks & Heat Spreaders → Attach to hot components.
- Component Placement → Keep hot parts near board edges or in airflow path.
- Board Material → Use high-Tg FR-4, Metal Core PCBs, or Polyimide for high-temp designs.
- Thermal Relief Pads → Balance solderability with heat dissipation.
- Active Cooling → Fans or forced airflow in high-power boards.

Design Guidelines

- Place power-hungry parts away from sensitive analog/ICs.
- Add keep-out areas for heatsinks and airflow.
- Use multiple vias under power devices (array of thermal vias).
- Spread current evenly across multiple planes.
- For LEDs & power boards, consider MCPCBs (Metal Core).

LAYOUT STRATEGIES

EMI / Noise Control in PCB Design

Electromagnetic Interference (EMI) is unwanted noise that can affect PCB performance or nearby devices.

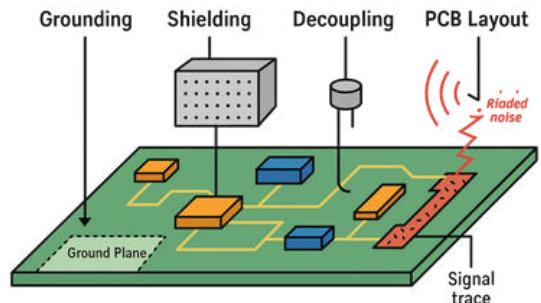
Noise control means designing the PCB so that it doesn't generate excessive EMI and is immune to external interference.

Why It's Important

- Prevents signal errors in high-speed designs.
- Ensures compliance with EMI/EMC standards.
- Reduces product failures and field issues.

Main Causes of EMI in PCBs

- Fast switching signals (clocks, high-speed buses).
- Large current loops in power circuits.
- Crosstalk between closely-routed signals.
- Poor grounding and return paths.
- Unshielded high-frequency circuits.



Main Causes of EMI in PCBs

- Ground Plane → Use solid, continuous ground planes.
- Short Return Paths → Keep signal loops small by routing over ground.
- Decoupling Capacitors → Place close to IC power pins to reduce noise.
- Trace Spacing → Follow 3W rule to minimize crosstalk.
- Shielding → Use guard traces, ground fills, or metal cans for sensitive circuits.
- Filter Components → Add ferrite beads, LC filters on noisy power rails.
- Differential Signals → Prefer differential pairs (USB, Ethernet, PCIe) for noise immunity.
- Avoid Split Planes → Don't route high-speed signals across ground/power splits.

Layout Guidelines

- Keep high-speed signals short and direct.
- Place crystals, oscillators near ICs, shield if needed.
- Isolate analog, digital, and RF zones.
- Route noisy signals away from sensitive analog circuits.
- Add stitching vias along ground fills for shielding.

LAYOUT STRATEGIES

DFM / Testing

- DFM (Design for Manufacturability): Designing the PCB so it can be easily fabricated and assembled with high yield and low cost.
- Testing: Ensuring the PCB can be easily inspected, probed, and verified during production and debugging

Why It's Important

- Reduces fabrication/assembly errors.
- Lowers production costs.
- Speeds up debugging and validation.
- Improves product reliability.

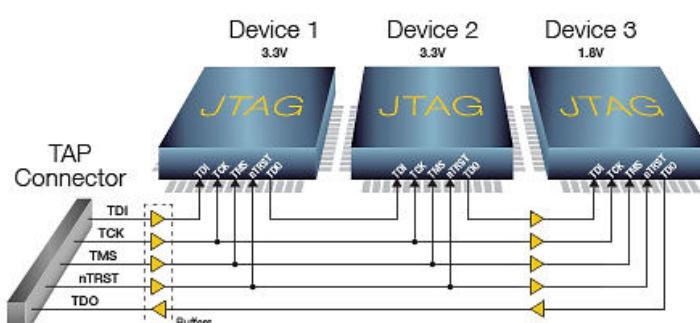


DFM Guidelines

- Clearances: Follow manufacturer's min trace width/spacing (e.g., 4–6 mil standard).
- Vias: Use manufacturable drill sizes ($\geq 0.2\text{--}0.3$ mm) and proper annular rings.
- Pads: Avoid vias on pads (unless filled).
- Panelization: Define breakaway tabs/v-scoring for volume builds.
- Fiducials: Add global & local fiducials for pick-and-place alignment.
- Silkscreen: Keep off pads; label reference designators clearly.
- Component Spacing: Leave room for assembly tools & rework.

Testing Guidelines

- Test Points: Add on power rails, clocks, high-speed nets, and key signals.
- Accessibility: Place test pads on one side for probe access.
- Bed-of-Nails Testing: Ensure uniform pad spacing if ICT is required.
- Boundary Scan / JTAG: For complex digital boards.
- Inspection: Provide space for AOI (Automated Optical Inspection) cameras.
- Debugging: Reserve headers/jumpers for firmware flashing & signal probing.



HIGH SPEED LAYOUT STRATEGIES

USB Design



USB interfaces (2.0, 3.x, 4.0) require careful impedance control, length matching, and EMI management for reliable high-speed performance.

USB 2.0 (High Speed – 480 Mbps)

- Differential Impedance: $90\Omega \pm 15\%$
- Trace Length Matching: ± 0.1 mm between D+ and D-
- Maximum Trace Length: 1500 mm
- EMI Filtering: Place common-mode chokes near connector
- Routing: Keep traces short, direct, and away from noisy power lines

USB 3.0 / 3.1 (SuperSpeed – 5 Gbps / 10 Gbps)

- Differential Impedance: $90\Omega \pm 7\Omega$
- Length Matching: ± 50 μm (very strict)
- Via Usage: Minimize vias in high-speed lanes (adds loss/discontinuity)
- Shielding: Enhanced requirements; avoid coupling with other high-speed nets
- Pair Routing: Keep differential pairs parallel and tightly coupled

USB 4.0 (SuperSpeed+ – 20–40 Gbps)

- Differential Impedance: $90\Omega \pm 7\Omega$
- Length Matching: ± 12 μm
- SI Analysis: Perform advanced signal integrity checks
- Via Control: Strict control of via stubs and layer transitions
- Reference Planes: Continuous GND planes required for return paths

General USB Routing Rules

- Route D+/D- or SuperSpeed pairs together, same length, same layer
- Avoid 90° bends (use 45° or arcs)
- Place ESD protection diodes close to the connector
- Keep USB connector shield tied to chassis/ground for EMI reduction
- Place decoupling capacitors near USB ICs

HIGH SPEED LAYOUT STRATEGIES

PCI Express (PCIe)

PCIe is a high-speed serial interface (Gen1 → 2.5 Gbps, Gen2 → 5 Gbps, Gen3 → 8 Gbps, Gen4 → 16 Gbps, Gen5 → 32 Gbps). It requires strict impedance control, length matching, and SI practices for reliable operation.

Electrical Requirements

- Differential Impedance: $85\Omega \pm 7\Omega$ (all generations)
- Intra-pair skew: <5 ps (~0.8 mm)
- Inter-pair skew: <100 ps (~15 mm)
- Reference Clock: Must meet jitter and skew requirements for synchronization

Signal Integrity Requirements

- Via Stub Elimination: Back-drill or use blind vias above 8 GHz
- Continuous Reference Planes: Route signals over solid GND planes
- AC Coupling Capacitors: Place close to the transmitter side
- Trace Length Matching: Maintain within skew budget for reliable link training
- Termination: Built-in at receivers, no external termination required

Routing Guidelines

- Keep differential pairs tightly coupled and parallel
- Avoid 90° bends → use 45° or arcs
- Minimize vias in high-speed lanes (each via adds loss & reflection)
- Separate PCIe lanes from noisy power/clock lines
- Use short, direct traces between controller and slot/device

Routing Guidelines

- Use dedicated power islands for PCIe reference voltages if required
- Stitch ground vias near PCIe signal vias for strong return paths
- Decouple PCIe power rails with low-ESR capacitors close to the device

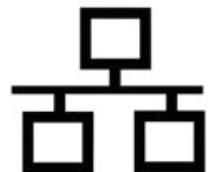
Design by Generation

- Gen1/Gen2 (2.5–5 Gbps): Standard FR-4 is sufficient
- Gen3 (8 Gbps): Careful loss budgeting, via optimization required
- Gen4 (16 Gbps): Use low-loss materials (Megtron, Isola, etc.)
- Gen5 (32 Gbps): Very strict SI control, requires simulation and advanced materials

HIGH SPEED LAYOUT STRATEGIES

Ethernet

Ethernet (Fast Ethernet, Gigabit, 10 Gigabit, etc.) requires precise impedance control, length matching, and EMI isolation for reliable high-speed communication.



Electrical Requirements

- Differential Impedance: $100\Omega \pm 10\%$ (standard for Ethernet)
- Pair Matching: All four twisted pairs must be length-matched
- Crosstalk Control: Maintain spacing between pairs, follow the 3W rule

Gigabit Ethernet (1 Gbps)

- Impedance: $100\Omega \pm 10\%$
- Length Matching: All four pairs matched within 50 mm
- Bend Radius: $\geq 2 \times$ trace width for controlled impedance
- Isolation: Requires magnetic isolation transformers near RJ45 connector
- Shielding: Place ESD protection near the connector, keep ground reference stable

10 Gigabit Ethernet (10GBASE-T)

- Impedance: $100\Omega \pm 5\%$ (tighter control)
- Length Matching: Stricter than Gigabit, sub-25 mm difference recommended
- Crosstalk Management: Enhanced isolation between pairs, keep pairs away from noisy circuits
- Backplane Considerations: Perform loss budgeting for long traces
- Equalization: Advanced equalization and DSP tuning required at PHY level

Layout Guidelines

- Route differential pairs together: same length, same layer, equal spacing
- Avoid stubs and unnecessary vias (adds reflections and loss)
- Keep Ethernet traces away from high-speed clock sources and power regulators
- Place RJ45 connector close to PHY to minimize trace length
- Use flooded ground areas under Ethernet section for noise shielding

EMI/EMC Considerations

- Add common-mode chokes near the connector
- Use ESD suppressors/TVS diodes at RJ45 input
- Ensure connector shield is properly tied to chassis ground
- Maintain isolation gap between Ethernet PHY and connector magnetics

HIGH SPEED LAYOUT STRATEGIES



DDR

DDR interfaces (DDR3, DDR4, DDR5) are very high-speed parallel buses. They require tight timing, impedance control, and careful layout for stable operation.

Electrical Requirements

- Single-Ended Impedance: $40\text{--}60\Omega \pm 10\%$ (data, address, control lines)
- Differential Impedance: $100\Omega \pm 7\Omega$ (clocks, DQS signals)
- Termination: On-die termination (ODT) used in DDR3 and later
- Power Noise: <30 mV ripple on VDDQ rails

Routing Guidelines

- Length Matching:
 - Data lines ($\text{DQ} \leftrightarrow \text{DQS}$): ± 5 mils (0.127 mm)
 - Address/Control/Command: ± 25 mils (0.635 mm)
- Differential Pairs:
 - Clock & DQS pairs tightly coupled, matched in length
- Via Usage:
 - ≤ 2 vias per net (to minimize reflections & stubs)
- Topology:
 - DDR3: T-branch (tree) possible
 - DDR4/DDR5: Fly-by topology for address/command/control

Layout Rules

- Place DRAMs close to the controller to minimize trace length
- Route data byte lanes together as groups
- Maintain solid reference planes (continuous GND under DDR signals)
- Use serpentine traces for length tuning (avoid sharp turns)
- Avoid routing DDR signals across plane splits
- Place decoupling capacitors close to DDR power pins

DDR Versions – Key Differences

- DDR3: 800–2133 Mbps, relaxed timing, T-topology acceptable
- DDR4: 1600–3200 Mbps, tighter skew control, fly-by topology mandatory
- DDR5: 3200–6400 Mbps, extremely tight timing, requires simulation & equalization

FLEX & RIGID-FLEX LAYOUT STRATEGIES

Flexible Fundamentals

A flexible PCB (flex circuit) is built on a bendable base material (usually polyimide or LCP).

It allows the circuit to bend, fold, or twist while maintaining electrical connectivity.

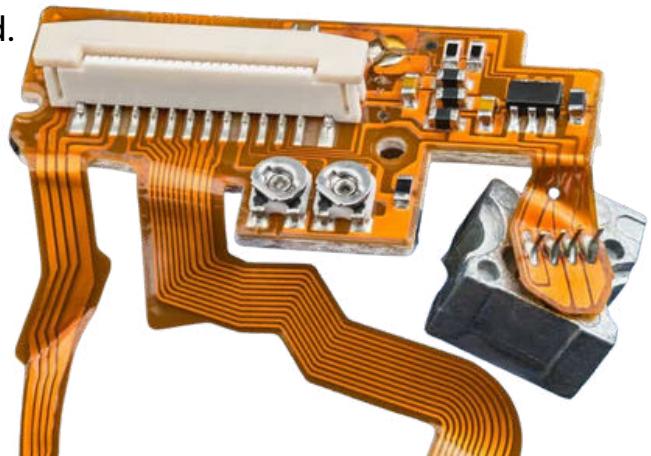
Recommended Materials

- Polyimide → Standard flexibility, widely used.
- LCP (Liquid Crystal Polymer) → Excellent for high-frequency and low-loss applications.

Thickness & Bend Radius

The thinner the flex, the tighter it can bend.

Layer Count	Thickness	Min. Bend Radius
1-Layer	0.05–0.1 mm	5 × thickness
2-Layer	0.1–0.2 mm	10 × thickness
4-Layer	0.2–0.4 mm	15 × thickness
6+ Layers	≥0.4 mm	20 × thickness



Design Considerations

- Use coverlay instead of solder mask for protection in flex areas.
- Keep traces perpendicular to the bend axis (avoid parallel traces across bends).
- Use curved traces and teardrop pads to reduce stress.
- Avoid vias and components in bend areas.

Applications

- Smartphones and wearables.
- Aerospace and medical devices.
- Automotive displays and sensors.
- Consumer electronics with compact enclosures.

FLEX & RIGID-FLEX LAYOUT STRATEGIES

Bend Radius Calculations

The bend radius is the minimum radius a flex PCB can bend without cracking, delaminating, or damaging copper traces.

It depends on board thickness and whether the bend is static (one-time) or dynamic (repeated).

Dynamic Flexing (Repeated Bends)

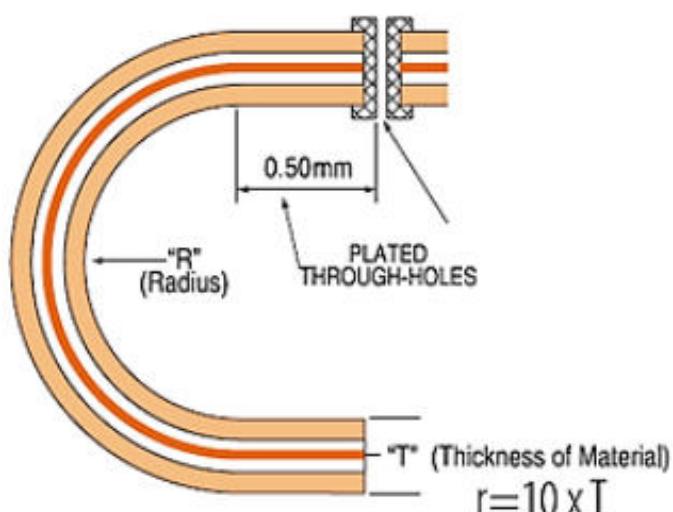
- Minimum Bend Radius: $6 \times$ total thickness
- Use stress-relief design (curved traces, teardrop pads).
- Route conductors perpendicular to the bend axis.
- Avoid vias in the bend region (they can crack).

Static Bending (One-Time Installation)

- Minimum Bend Radius: $3 \times$ total thickness
- Acceptable for cables that bend only during assembly or installation.
- Add stiffeners at bend edges for support.
- Balance copper layers to avoid warping.

General Tips

- Thinner flex = smaller bend radius possible.
- Always use overlay (not solder mask) in flex zones.
- Keep critical traces away from high-stress bend areas.
- For multilayer flex, increase bend radius ($15\times$ or $20\times$ thickness).



FLEX & RIGID-FLEX LAYOUT STRATEGIES

Rigid-Flex Transition Design

Rigid-Flex PCBs combine rigid FR-4 sections (for components) with flexible polyimide sections (for bending/folding).

The transition zone between rigid and flex areas is the most critical for mechanical strength and electrical reliability.

Stack-Up Considerations

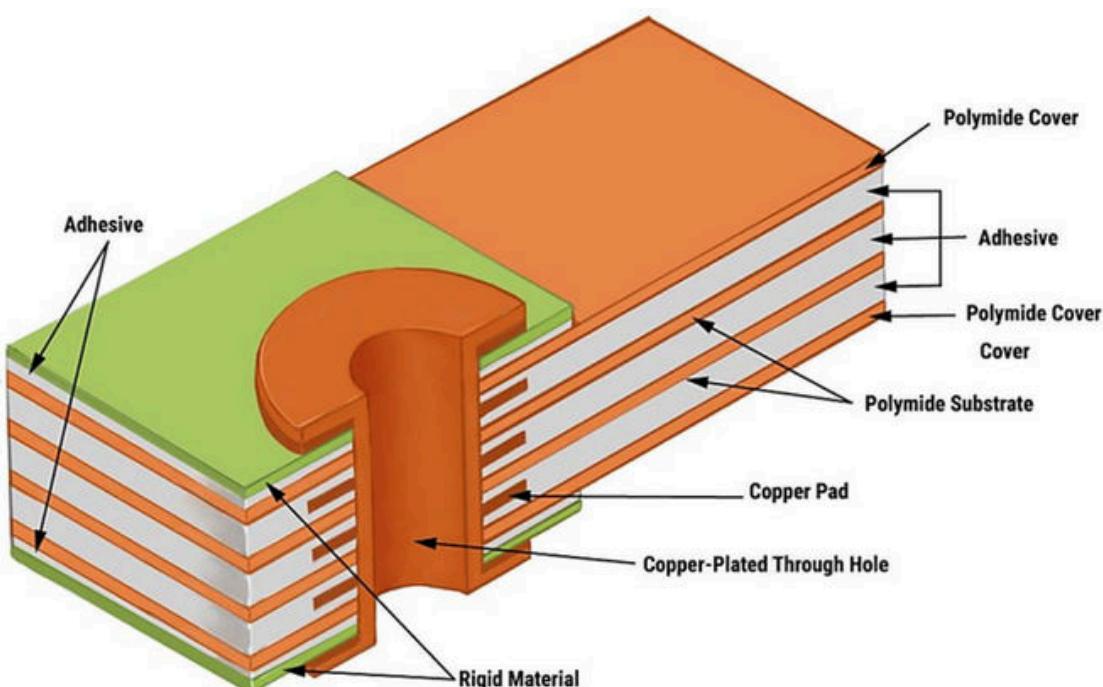
- Keep layer transitions only in rigid areas (not inside bends).
- Restrict via placement to rigid zones → avoid vias in flex regions.
- Maintain controlled impedance across transition zones.
- Use overlay adhesive instead of solder mask in flex areas.

Manufacturing Constraints

- Rigid section width: ≥ 6 mm minimum.
- Flex entry angle: $< 45^\circ$ (smooth entry into bend).
- Stiffener overlap: ≥ 1 mm to support connectors & parts.
- Use polyimide stiffeners under high-stress or connector regions.

Design Tips

- Place critical components only on rigid areas.
- Use teardrop pads and curved traces near transition boundaries.
- Avoid routing high-density or high-speed signals directly across the transition.
- Simulate mechanical stress if frequent bending is expected.



COMPONENT - LAYOUT STRATEGIES

BGA Escape Routing

BGA Escape Routing is the process of getting signals out from the ball grid array (BGA) pads to accessible traces for routing across the PCB.

As ball pitch shrinks, routing becomes more challenging and requires vias, microvias, and HDI techniques.

Techniques

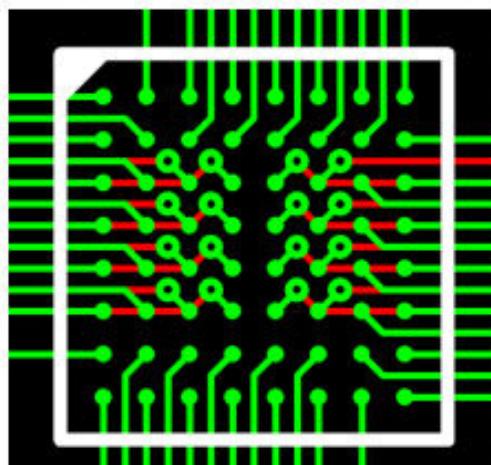
- Direct Escape (Dogbone): Simple fan-out using short traces and vias. Suitable for ≥ 1.0 mm pitch BGAs.
- Via-in-Pad: Vias drilled directly under the BGA pad, then filled and plated. Used for 0.8 mm pitch or smaller.
- Microvias / HDI: Laser-drilled vias (blind/buried) for fine-pitch BGAs (< 0.5 mm). Allows routing in higher-density designs.

Escape Routing Strategies

BGA Pitch	Via Size	Escape Method	Required Layers
1.0 mm	0.1 mm	Direct escape (dogbone)	2 layers
0.8 mm	0.1 mm	Via-in-pad	4 layers
0.5 mm	0.08 mm	Microvia only	6+ layers
0.4 mm	0.08 mm	HDI technology (stacked vias, via-in-pad)	8+ layers

Design Considerations

- Via Filling: Via-in-pad vias must be filled & plated for solderability.
- Pad Size Reduction: Helps increase escape channel space for tight pitch.
- Signal Integrity: Keep escape traces short and matched.
- Power/Ground Escape: Use multiple vias per ball for low impedance.
- Manufacturing: HDI adds cost; balance performance vs budget.



COMPONENT – LAYOUT STRATEGIES

Crystal Oscillator Layout

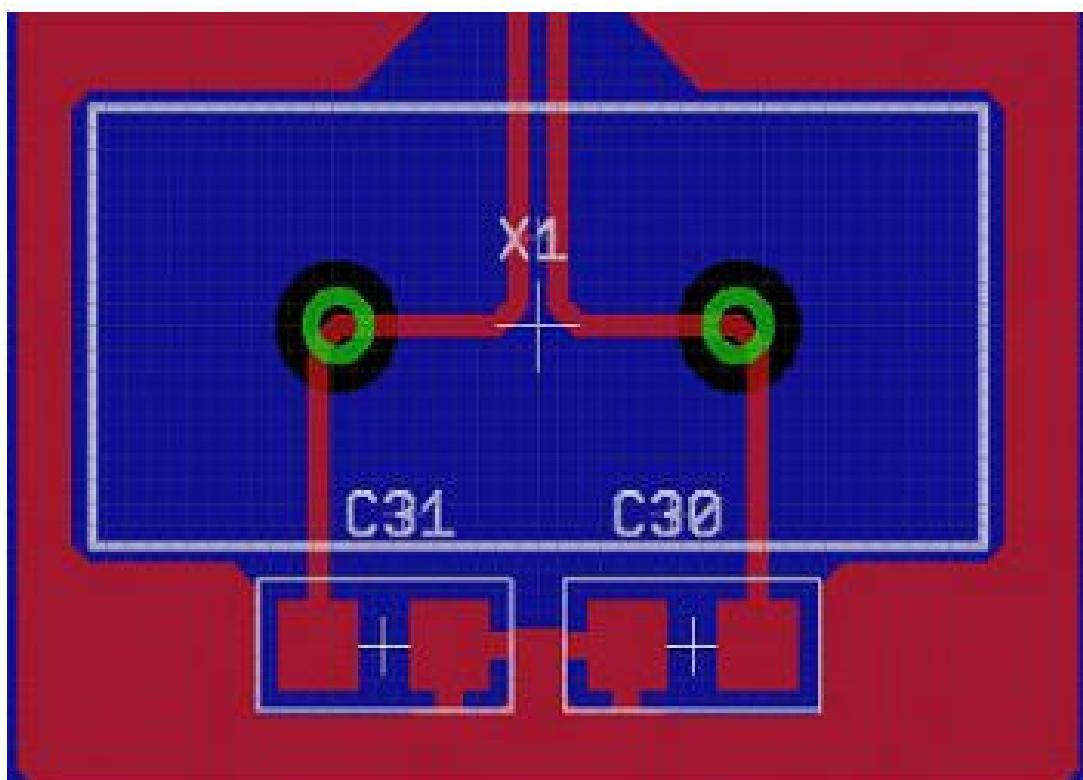
A crystal oscillator provides the clock signal for ICs (MCUs, processors, FPGAs). Since it controls timing, the layout must minimize noise, delay, and interference.

Critical Design Rules

- Ground Guard Ring: Place a continuous ground ring around the crystal to isolate noise.
- Short Traces: Keep connections between crystal and IC pins as short as possible.
- Load Capacitors: Place them within <5 mm of the crystal pads.
- Keep-Out Zones: Avoid routing switching signals or power traces near the oscillator.

Frequency-Specific Considerations

- Low Frequency (<10 MHz): Standard layout rules are sufficient.
- Medium Frequency (10–100 MHz): Guard rings around crystal and caps are essential.
- High Frequency (>100 MHz): Use a dedicated ground plane under the oscillator for stability.



COMPONENT - LAYOUT STRATEGIES

SMPS Layout

A switch-mode power supply (SMPS) efficiently converts power using inductors, capacitors, diodes, and switching ICs.

Because of high switching currents, the PCB layout strongly affects EMI, efficiency, and thermal performance.

Component Placement Priority

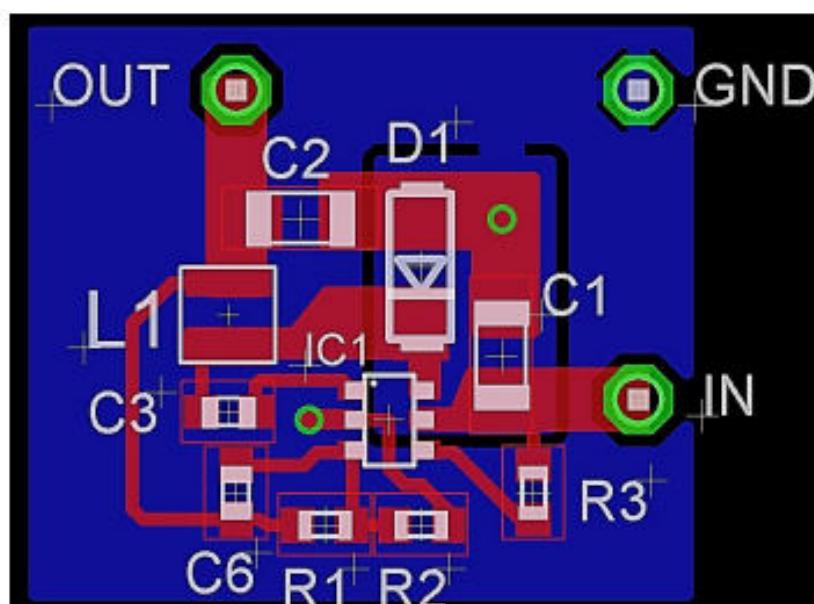
- Input/Output Capacitors → place closest to the IC (reduce loop area).
- Inductor → positioned to create the smallest loop with switch and output capacitor.
- Feedback Network → keep away from noisy switching nodes.
- Switching IC & Power Devices → ensure proper thermal management.

Critical Routing Guidelines

- Minimize Switching Loop Area: The smaller the loop, the lower the EMI.
- Grounding:
- Separate analog ground (feedback, control) from power ground (high current).
- Use a star connection point for grounding.
- Filtering Isolation: Keep input and output filtering paths isolated.
- Thermal Relief: Use copper pours and thermal vias for heat dissipation.

Example Rule of Thumb

- A buck converter requires a switching loop area $< 25 \text{ mm}^2$ for good EMI at 1 MHz switching frequency.



COMPONENT – LAYOUT STRATEGIES

Connector Design Integration

Connectors link the PCB to external signals, power, or other boards.

Their placement and routing affect signal integrity, mechanical strength, and reliability.

High-Speed Connector Requirements

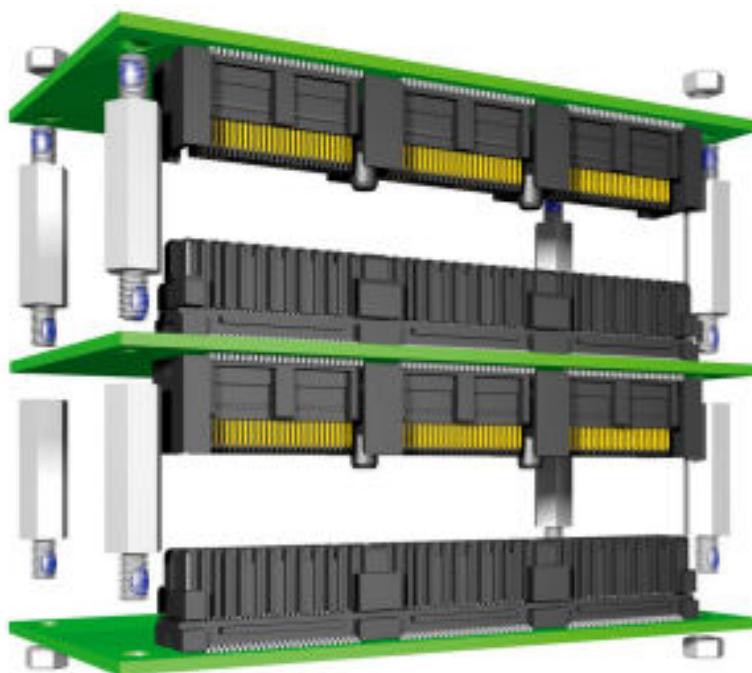
- Maintain controlled impedance through the connector.
- Plan via placement carefully for signal transitions.
- Ensure ground plane continuity under connector traces.
- Provide EMI shielding near high-speed connectors (e.g., PCIe, USB, Ethernet).

Power Connector Design

- Calculate current density per pin.
- Use multiple pin paralleling for high-current paths.
- Provide thermal management (copper pours, thermal vias).
- Minimize contact resistance for reliability.

Mechanical Considerations

- Add stress relief to prevent solder joint cracking.
- Reinforce board edges around connectors.
- Define keep-out zones for assembly tooling.
- Ensure connector locations are accessible for assembly & maintenance.



GROUND – CONCEPTS

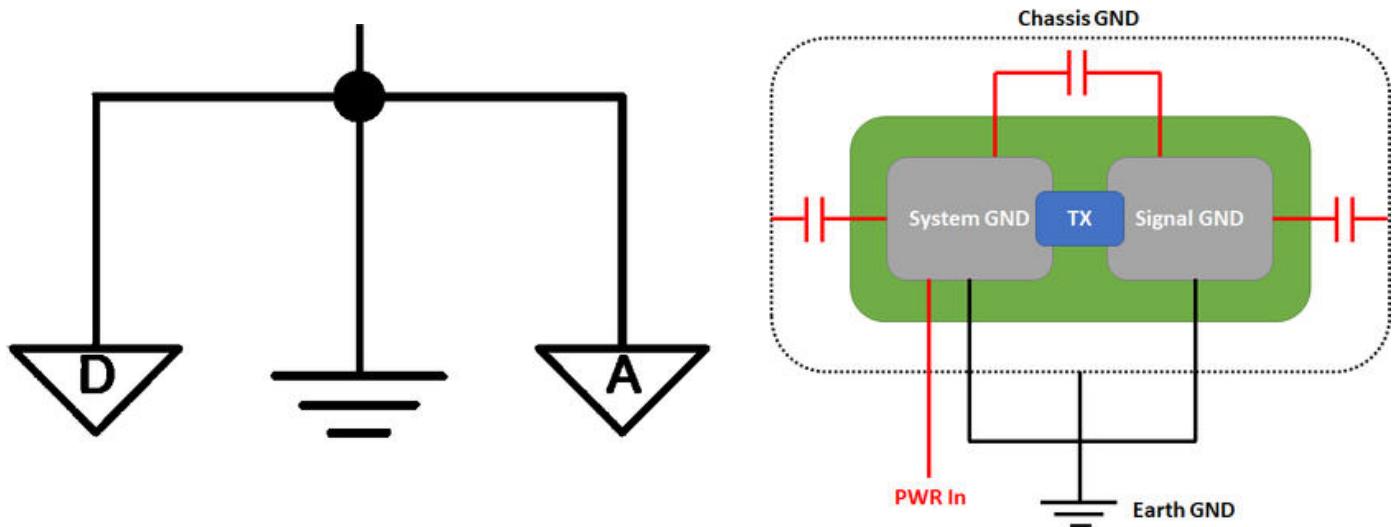
What is GND ?

Ground (GND) is the zero-voltage reference point in electrical circuits. It may serve different roles depending on design requirements: signal reference, safety, or EMI shielding.

1. Circuit Common (Signal Ground)

- **Reference point for all voltages** → All signals are measured relative to this point.
- **May not connect to earth** → Especially in floating or isolated systems.
- **Carries return currents** → Return paths are just as important as forward signal traces.
- **Voltage can fluctuate (ground bounce)** → Happens if high-current digital and sensitive analog circuits share the same ground path.

Tip: Use separate analog and digital ground planes where possible, then connect at a single star point.



2. Earth Ground (Protective Earth)

- **Physical connection to earth** → Via building ground or ground rod.
- **Safety protection** → Diverts dangerous fault currents away from the user.
- **Regulatory requirement** → All mains-powered equipment must connect earth properly.
- **Maintains reference** → Helps stabilize the overall system potential.

Tip: Always connect chassis/earth ground at the entry point of the system to minimize fault current paths.

GROUND – CONCEPTS

3. Chassis Ground

- **Connects enclosure to ground** → Links the case to the grounding system.
- **Provides EMI shielding** → The case acts like a Faraday cage.
- **Can be isolated with capacitor** → Blocks DC but passes high-frequency noise to ground.
- **Prevents static buildup** → Avoids ESD damage by safely discharging charges.

Tip: Place ground stitching vias around board edges and connector shields to tie them to chassis ground.

Ground Type Comparison

Ground Type	Function	Method	Resistance
Common	Voltage reference	Copper traces / planes	< 10 Ω
Earth	Safety protection	Ground rod / wiring	< 250 Ω
Chassis	EMI shielding & safety	Enclosure connection	< 0.1 Ω

Common Mistakes to Avoid

- ✗ **Mixing analog and digital grounds without control** → leads to noise coupling.
- ✗ **Creating ground loops (multiple return paths between grounds)** → causes hum and EMI issues.
- ✗ **Forgetting to tie connector shields to chassis ground** → increases susceptibility to EMI.
- ✗ **Using thin ground traces instead of planes** → increases resistance and voltage drops.

GROUND – CONCEPTS

The Physics of Ground

Ground is more than a simple “0V reference.” It also acts as a current-carrying conductor with measurable electrical properties that influence signal integrity, EMI, and overall circuit performance.

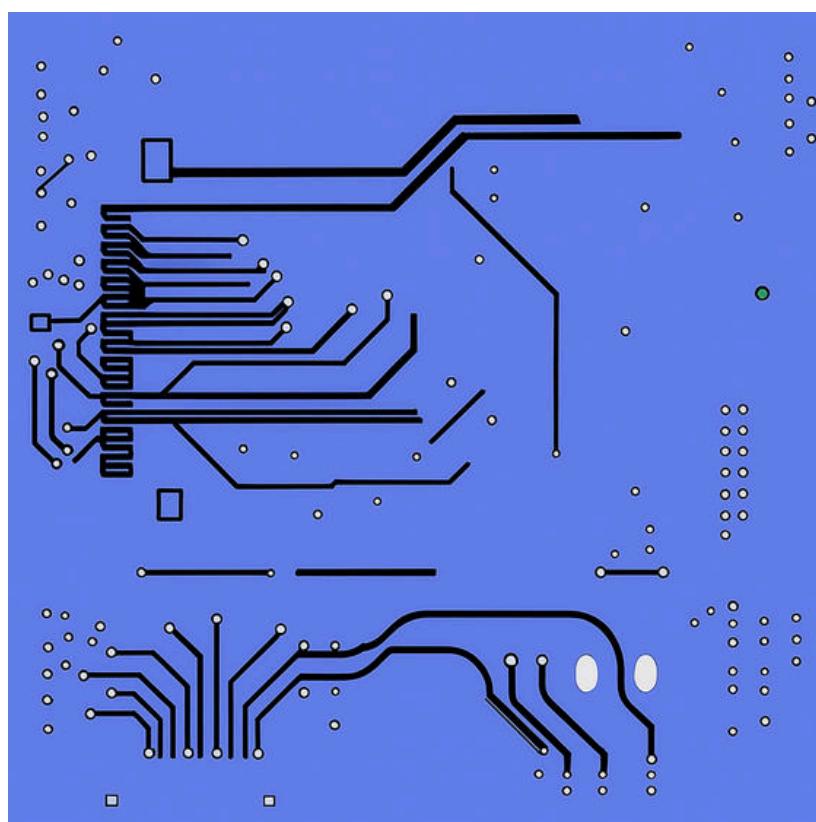
Ground as a Reference Plane

- Ground provides the zero-voltage reference for all circuit operation.
- All other voltages are measured relative to this point.
- In real PCBs, ground isn’t perfect – it has finite resistance and inductance.
- Ground bounce occurs when return currents flow through shared ground paths, causing unwanted voltage variations.

Tip: Always use a solid ground plane in multilayer PCBs to minimize impedance and provide low-noise return paths.

Impedance Characteristics of Ground

- Ground has both resistive and inductive behavior.
- At low frequencies (DC to kHz) → resistance dominates.
- At high frequencies (MHz to GHz) → inductance becomes the key factor.
- This means a “ground” path can behave like an inductor at high speed, leading to ringing, EMI, and crosstalk.



Tip: Use short, wide traces or planes for ground to minimize inductance. and Stitch ground planes with vias around high-speed signals to maintain return paths.

GROUND – CONCEPTS

Key Physical Properties of Ground

1. **Resistance (R):** Causes voltage drop proportional to current ($V = I \times R$).
→ High resistance ground traces = noise & ground bounce.
2. **Inductance (L):** Opposes changes in current. Above ~1 MHz, inductance dominates.
→ Longer, thinner traces = higher inductance = worse SI.
3. **Skin Effect:** At high frequencies, current flows only on the surface of conductors.
→ Effective resistance increases with frequency.
4. **Proximity Effect:** Current distribution is influenced by nearby conductors.
→ Can cause uneven current flow and localized heating.

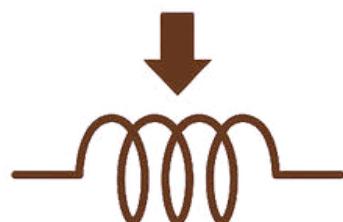
Tip:

- At high speeds, treat ground not as a wire but as a transmission line return path.
- Keep return paths directly under signal traces (microstrip/stripline) for consistent impedance.

$$V = I \times R$$

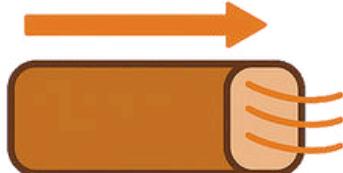


Resistance

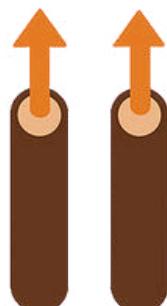


Inductance

High-frequency Current



Skin Effect



Proximity Effect

GROUND – CONCEPTS

The Return Path

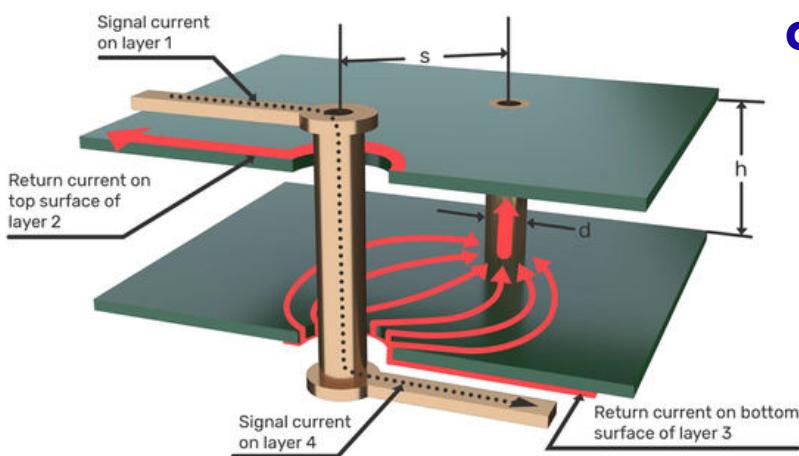
Current always flows in complete loops. The signal path is only half the story – the return path can be even more critical. Poorly controlled return currents lead to EMI, crosstalk, and signal integrity issues.

Return Current Behavior

- Current follows the path of lowest impedance back to its source.
- **At low frequencies (DC, kHz):** return current flows through the path of lowest resistance.
- **At high frequencies (MHz, GHz):** return current follows the path of lowest inductance, which is usually directly under the signal trace.

Return Path Characteristics

- **DC Currents:** Spread out across the ground plane, choosing the lowest resistance path.
- **AC Currents:** Flow directly beneath the signal trace to minimize loop area.
- **High-Frequency Currents:** Concentrate into a narrow band under the trace due to electromagnetic coupling.



Critical Design Implications

- Always provide a continuous ground plane under high-speed signals.
- Avoid routing signals across splits in ground/power planes.
- Use ground stitching vias when signals switch layers (to give return currents a nearby path).
- Minimize loop area → smaller loops = lower EMI.

Critical Design Implications

- **Signal Integrity depends on controlled return paths** → return loops must be predictable.
- **Uncontrolled return paths create EMI & crosstalk** → especially when crossing splits in ground planes.
- **Return path discontinuities cause reflections & noise** → if the ground plane is broken, current takes a detour, increasing inductance and emissions.

GROUND – LOOPS

Anatomy of a Ground Loop

A ground loop forms when there are multiple ground connections between two or more points in a system.

These parallel connections create unintended current paths, which can cause voltage differences, noise, and EMI problems.

How Ground Loops Form (Mechanism)

- A circuit connects to **system ground** at more than one point.
- Each path has **different impedance** (resistance + inductance).
- Currents flow through both paths. Because impedances differ, voltages at the “ground” nodes are not identical.
- This results in a **loop current** circulating in the system → producing noise, hum, and possible signal corruption.

Basic Ground Loop Components

- **Multiple Ground Connections:** At least 2 or more return paths to “ground.”
- **Impedance Differences:** Resistance and inductance vary in each path.
- **Current Flow:** Both AC and DC return currents travel through the loop.
- **Voltage Differences:** Small differences in ground potential (caused by $I \times Z$ drops).

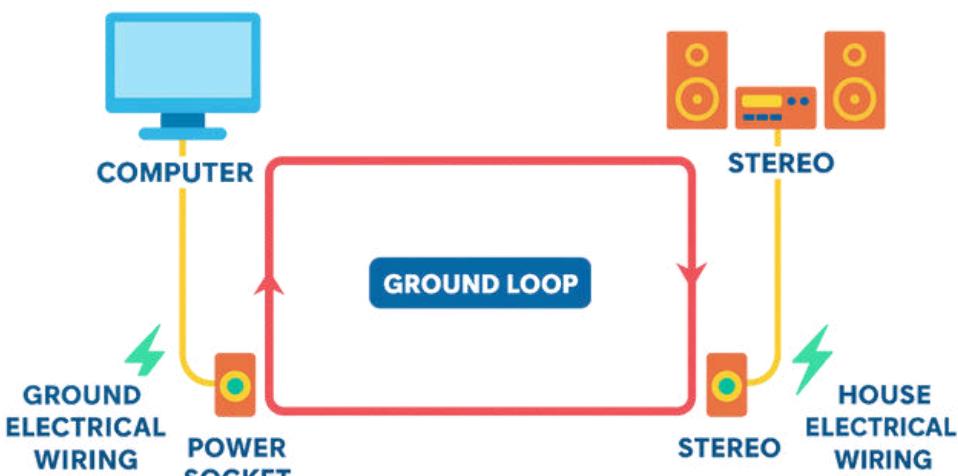
Mathematical Analysis

Ground loop voltage can be described as: $V_{loop} = I_1 Z_1 - I_2 Z_2$

Where:

- $I_1, I_2 \rightarrow$ Currents in the two parallel ground paths.
- $Z_1, Z_2 \rightarrow$ Impedances of each ground path.

Even millivolt differences in potential can be enough to **introduce audible hum in audio systems or cause timing errors in digital circuit**



GROUND – LOOPS

Consequences of Ground Loops

Noise Injection Mechanisms

- **Signal Corruption** → Voltage differences between grounds add error voltages into signals.
- **Increased Noise Floor** → Sensitive analog circuits (e.g., audio, instrumentation) pick up loop-induced hum and hiss.
- **EMI Generation** → Large ground loops act like antennas, radiating electromagnetic energy.
- **Oscillation Risk** → Feedback through ground impedances can cause amplifier or control system instability.

Frequency-Dependent Behavior

Ground loop effects change with frequency:

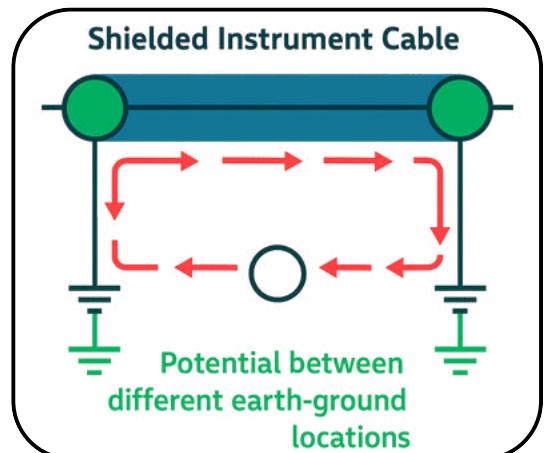
- **DC – 1 kHz** → Resistive effects dominate → noticeable hum (50/60 Hz).
- **1 kHz – 1 MHz** → Resistive + inductive mix → unpredictable ground noise.
- **>1 MHz** → Inductive effects dominate → high-frequency EMI and crosstalk.

Practical Consequences

- **Audio Systems** → 50/60 Hz hum in speakers due to ground potential differences across interconnected devices.
- **Measurement Equipment** → False readings in oscilloscopes and sensors caused by circulating loop currents.
- **Communication Systems** → Increased error rates and packet loss from EMI coupling into data lines.
- **Mixed-Signal Boards** → Digital switching noise couples into analog ground, degrading ADC/DAC performance.
- **Power Electronics** → Instability in SMPS or motor drives due to circulating high-frequency return currents.

Design Implications

- Ground loops often bypass isolation barriers, defeating shielding efforts.
- They can turn otherwise well-designed PCBs into EMI radiators.
- They are hard to detect because the issue often appears as random noise or interference during testing



GROUND – LOOPS

Ground Loop Scenarios

Ground loops can appear in different environments depending on how grounds are connected. Each scenario has unique risks and solutions.

1. Power System Ground Loops

What happens:

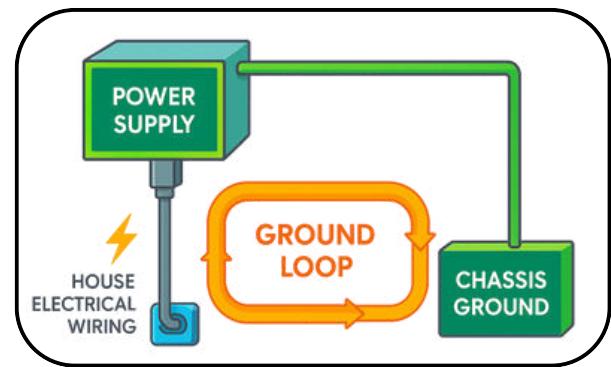
- Multiple connections between power supply grounds and chassis ground form current loops.
- Switch-mode power supplies (SMPS) are particularly problematic because they generate high-frequency noise that circulates through these loops.

Consequences:

- Power instability.
- Increased EMI emissions.
- Risk of equipment malfunction during load transients.

Example:

- A server rack where each PSU is earth-grounded separately, creating circulating noise currents



2. Audio Circuit Ground Loops

What happens:

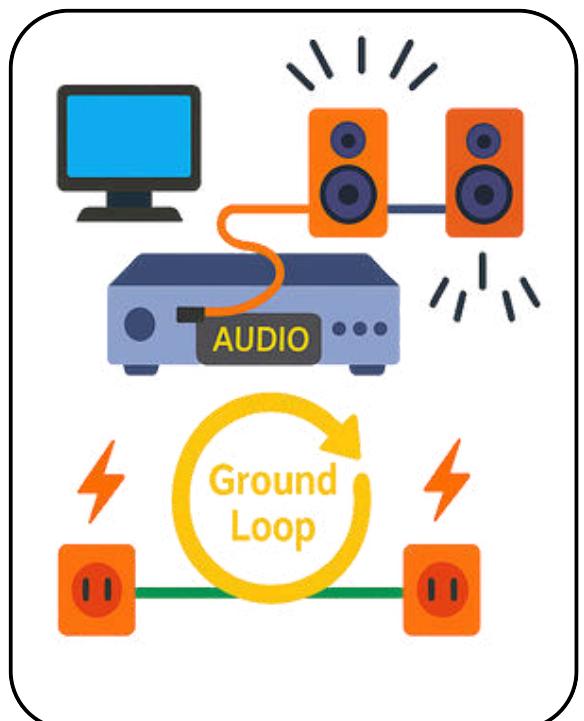
- Audio equipment (amplifiers, mixers, speakers) interconnected with shielded cables often ties shields to ground at both ends.
- This creates loops carrying 50/60 Hz mains frequency currents.

Consequences:

- Audible hum or buzz in speakers.
- Distortion and loss of dynamic range.

Example:

- A computer connected to powered speakers via an audio cable while both are plugged into separate wall sockets.



GROUND – LOOPS

3. Mixed-Signal Board Ground Loops

What happens:

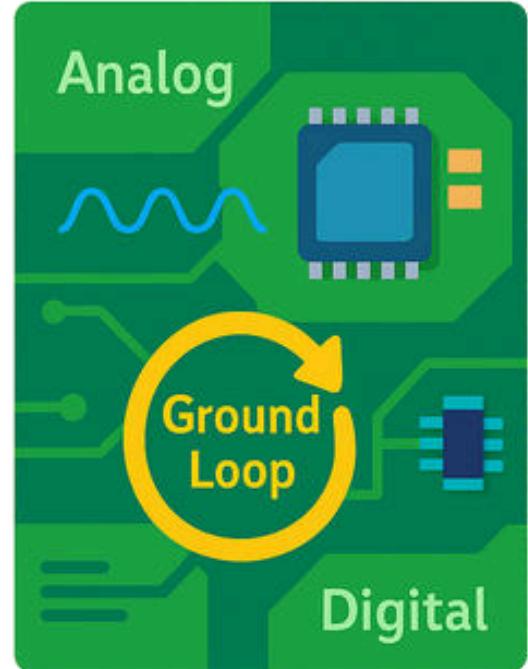
- Improper grounding between analog and digital sections of a PCB allows switching currents from the digital domain to couple into sensitive analog sections.

Consequences:

- Degraded ADC/DAC accuracy.
- Increased noise floor in sensor or RF circuits.
- Timing errors in precision measurement systems.

Example:

- A data acquisition board where high-speed digital logic shares the same ground return path as low-level analog sensor signals.



Prevention Strategies

- Single-Point Grounding** → Tie all grounds to a common point.
- Isolation Transformers** → Break loops in AC-powered systems.
- Differential Signaling** → Reject common-mode noise (e.g., Ethernet, RS-485, USB).
- Ground Lift Switches** → Temporarily disconnect ground in audio gear to break loops.
- PCB Partitioning** → Separate analog and digital grounds, join at a single star point.

GROUND – DESIGN

Ground Planes vs. Traces

Ground design is a critical foundation for PCB performance. Choosing between a solid ground plane and narrow ground traces directly affects signal integrity, EMI shielding, thermal performance, and current handling.

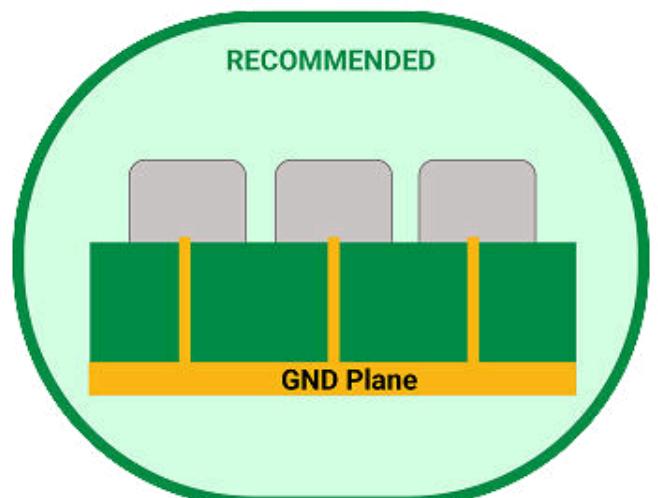
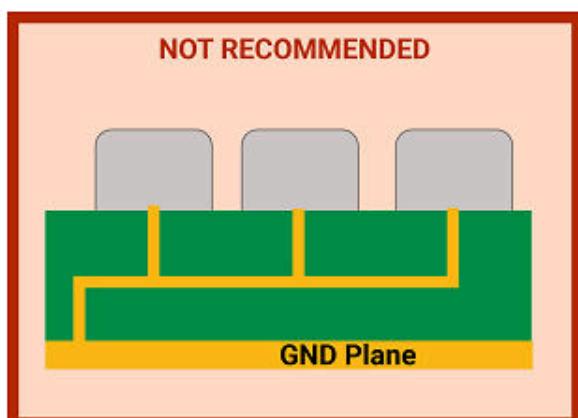
Why Ground Planes are Superior

Ground planes provide continuous, low-impedance reference surfaces that outperform simple traces in nearly every aspect.

Key Advantages:

- Ultra-Low Impedance: Large copper area lowers both resistance and inductance → stable reference for signals.
- Controlled Return Paths: Ensures high-speed signals flow directly under their traces (minimizing EMI).
- Impedance Control: Consistent plane geometry enables predictable impedance for high-speed designs.
- EMI Shielding: Solid copper planes act as shields, reducing radiation and susceptibility.
- Thermal Management: Distributes heat efficiently, lowering hot spots.
- High Current Handling: Supports wide current return paths for power supplies and motor drivers.
- Noise Isolation: Dedicated ground planes help separate analog, digital, and RF sections.

Note: Planes should have >50% copper coverage for effective shielding and return current flow.



GROUND – DESIGN

When Ground Traces Still Make Sense

Although inferior to planes, ground traces remain useful in some cases:

- **Low-Cost Single-Layer Boards:** Where adding a plane isn't possible.
- **Low-Frequency Circuits (<1 MHz):** Where inductance/EMI issues are minimal.
- **Simple Circuits:** Few interconnections, minimal current.
- **Prototyping/DIY Boards:** Cost and manufacturability take priority.

Limitations:

- High impedance → more noise and EMI.
- Poor current handling.
- Non-uniform return paths → signal reflections.
- Cannot provide effective shielding.

Best Design Practices

- **Use Planes for Anything >1 MHz:** Always dedicate at least one layer as a solid ground plane in multilayer PCBs.
- **Avoid Plane Cuts & Slots:** Signal return paths must remain continuous; splits force detours and create EMI.
- **Stitch Copper Pours:** If using copper pours instead of full planes, connect them with stitching vias for continuity.
- **Via Fencing for EMI Containment:** Place a row of ground vias along board edges to prevent emissions and improve shielding.
- **Chassis Ground Connections:** Tie PCB ground to chassis at mounting holes with low-inductance paths for EMI suppression.

Comparison

Aspect	Ground Plane	Ground Trace
Impedance ($R+L$)	Very low	High
EMI Shielding	Excellent	Poor
High-Speed Return Path	Controlled, predictable	Uncontrolled
Heat Dissipation	High efficiency	Minimal
Current Handling	Large currents supported	Limited
Noise Isolation	Strong (can separate domains)	Weak
Cost	Higher (multilayer)	Lower (single-layer)

GROUND – DESIGN

Star Grounding

Star grounding is a technique that connects all ground returns to a single central point, preventing circulating currents and minimizing ground loop issues.

Why Star Grounding?

- Prevents one circuit's return current from flowing into another circuit's ground path.
- Provides a clear, controlled reference point for all circuit sections.
- Reduces noise coupling between sensitive and noisy circuits.

Key Implementation Principles

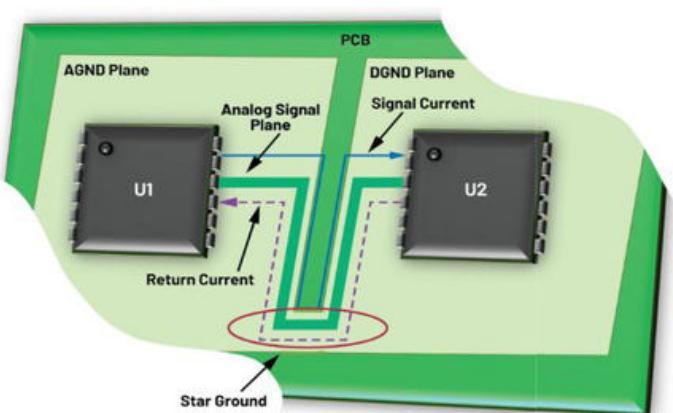
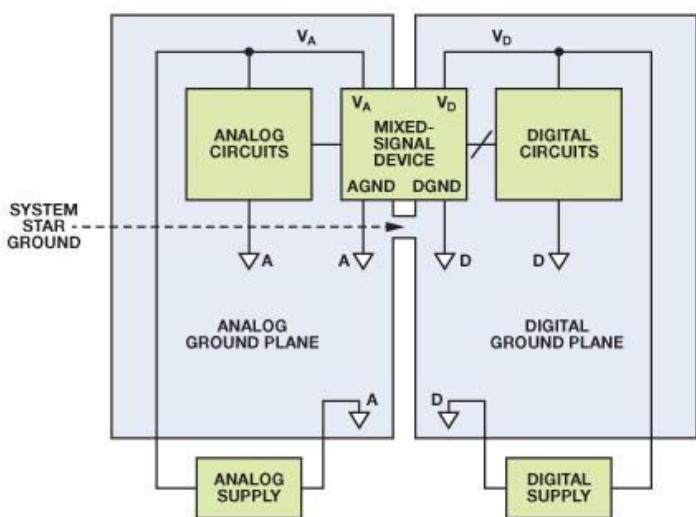
For effective star grounding, the PCB layout must ensure:

- **Central Ground Point:** A single, low-impedance node acts as the hub.
- **Isolated Groups:** Each circuit section (analog, digital, power) has its own path to the star point.
- **No Shared Returns:** Avoids cross-coupling between sections.
- **Short, Thick Returns:** Low inductance paths reduce voltage drops.

Prioritizing Circuit Sections (Most Sensitive First)

Grounding priority depends on sensitivity:

1. **Precision Analog Circuits** → Microvolt-level accuracy, most critical.
2. **Low-Noise Analog Circuits** → Audio amplifiers, sensor interfaces.
3. **Digital Control Circuits** → Microcontrollers, logic ICs.
4. **Power Switching Circuits** → Regulators, motor drivers.
5. **High-Current Loads** → Relays, solenoids, power outputs.



GROUND – DESIGN

Challenges

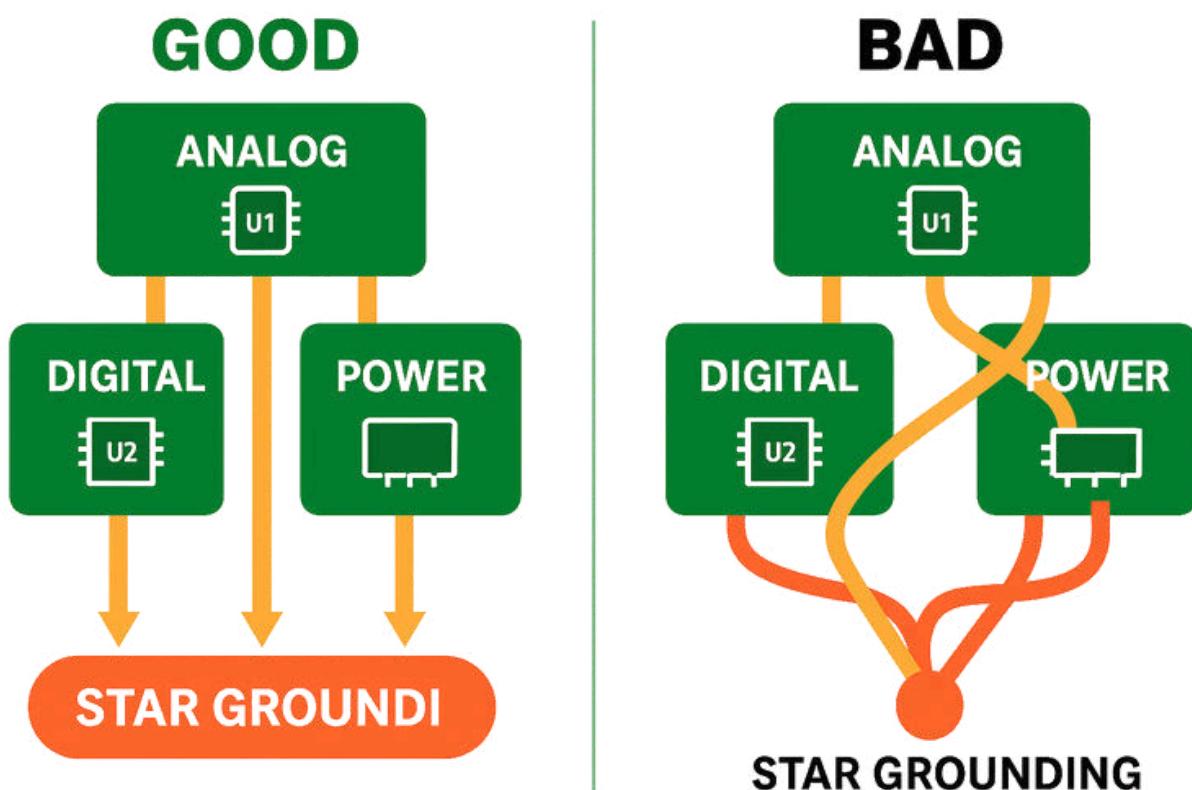
Star grounding requires careful balance → too long traces = inductance, too short connections = crowding.

Design Techniques

- Place star ground point at the geometric center of sensitive circuits.
- Use a dedicated ground layer with radial routing to the star point.
- Add thermal relief pads for manufacturability.
- Keep high-current grounds isolated until the star point.
- In mixed-signal PCBs, join analog and digital grounds only at the star point.

Star Grounding vs. Other Methods

- **Star Grounding** → Best for mixed-signal and sensitive analog circuits.
- **Single Solid Ground Plane** → Best for high-speed digital boards.
- **Hybrid Approach** → Sometimes combines planes and star grounding (e.g., analog star point connected to digital ground plane).



GROUND – DESIGN

Multi-Layer Board

Multi-layer PCBs provide the best environment for grounding strategies, enabling high performance in high-speed, high-current, and mixed-signal designs.

Why Multi-Layer Boards?

- Provide dedicated planes for ground and power.
- Reduce EMI by minimizing loop area.
- Allow controlled impedance for high-speed traces.
- Improve thermal management and current distribution.

Common Stack-Up Configurations

4-Layer Board (Basic High-Speed)

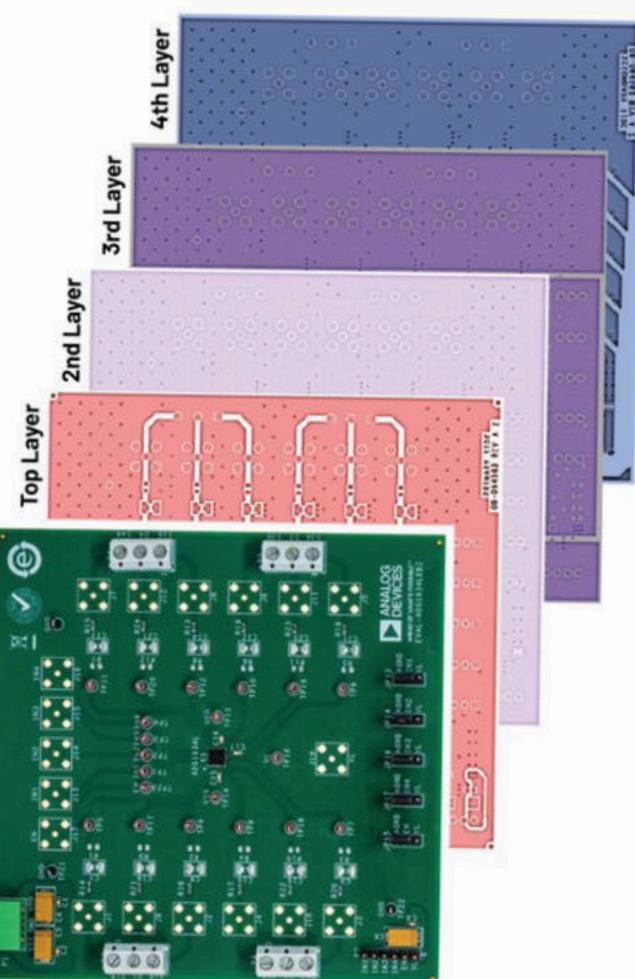
- L1: Component / Signal
- L2: Ground Plane (continuous)
- L3: Power Plane
- L4: Signal / Component

Good for mid-speed digital, basic RF, and mixed analog/digital circuits.

6-Layer Board (Improved Isolation)

- L1: Signal
- L2: Ground Plane
- L3: Signal (routed)
- L4: Signal (routed)
- L5: Power Plane
- L6: Signal

Best for high-speed digital, DDR, PCIe, USB 3.x, Ethernet, where return path control is critical.



Ground Plane Design Rules

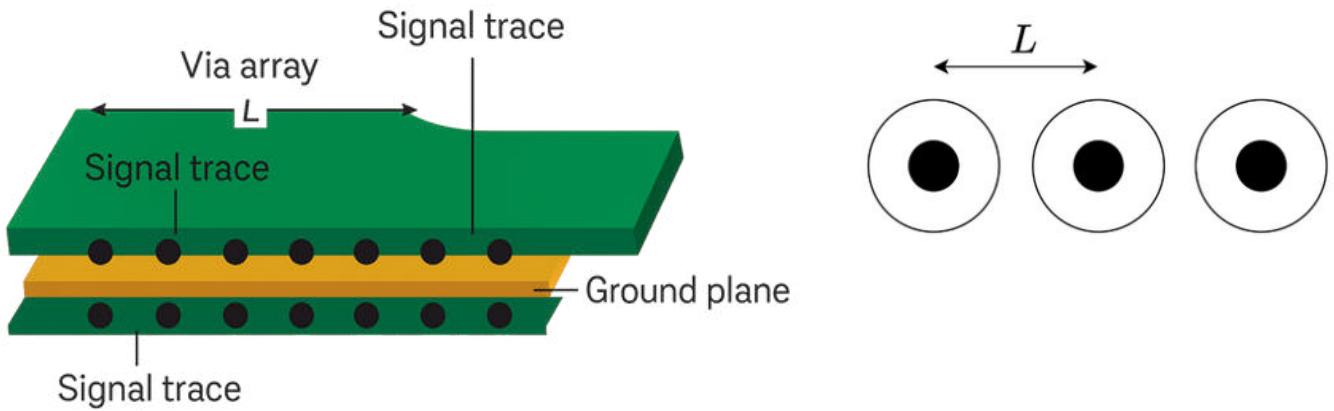
- Maintain $\geq 50\%$ copper coverage on all ground planes.
- Avoid slots or cuts under high-speed signals (breaks return path).
- Use multiple stitching vias to connect ground planes together.
- Isolate analog and digital grounds when required, join at a single star point.
- Place decoupling capacitors close to vias connecting planes.

GROUND – DESIGN

Via Stitching Strategy

Multiple vias connect ground planes across layers → reducing impedance & improving return current flow.

- **High-Speed Signals:** Place vias every 1–2 inches along trace length.
- **Power Connections:** Use via arrays with 0.5–1 inch spacing.
- **Layer Transitions:** Place stitching vias next to signal vias.
- **Board Edges:** Use via fences to contain EMI.



Best Practices

- Always put **ground planes adjacent** to signal layers → ensures controlled impedance.
- **Use symmetrical stack-ups** → minimizes warpage during manufacturing.
- Distribute **power and ground planes** evenly → improves return paths and reduces noise.
- For very high speed (>5 GHz), consider **embedded capacitance materials** between ground and power planes.

GROUND – DIVIDING

Mixed-signal designs require careful ground separation and bridging strategies to prevent noisy digital currents from contaminating sensitive analog circuits, while still maintaining reliable overall system operation.

Analog & Digital Ground Separation

Mixed-signal PCBs (those containing both analog and digital circuits) require careful ground separation to prevent noisy digital switching currents from degrading sensitive analog performance.

Why Separate Analog & Digital Grounds?

- Digital circuits generate sharp current spikes during switching (edges, clock transitions).
- These currents flow through ground, creating voltage fluctuations across shared impedance.
- If analog circuits share this return path, those fluctuations manifest as noise, distortion, or measurement errors.

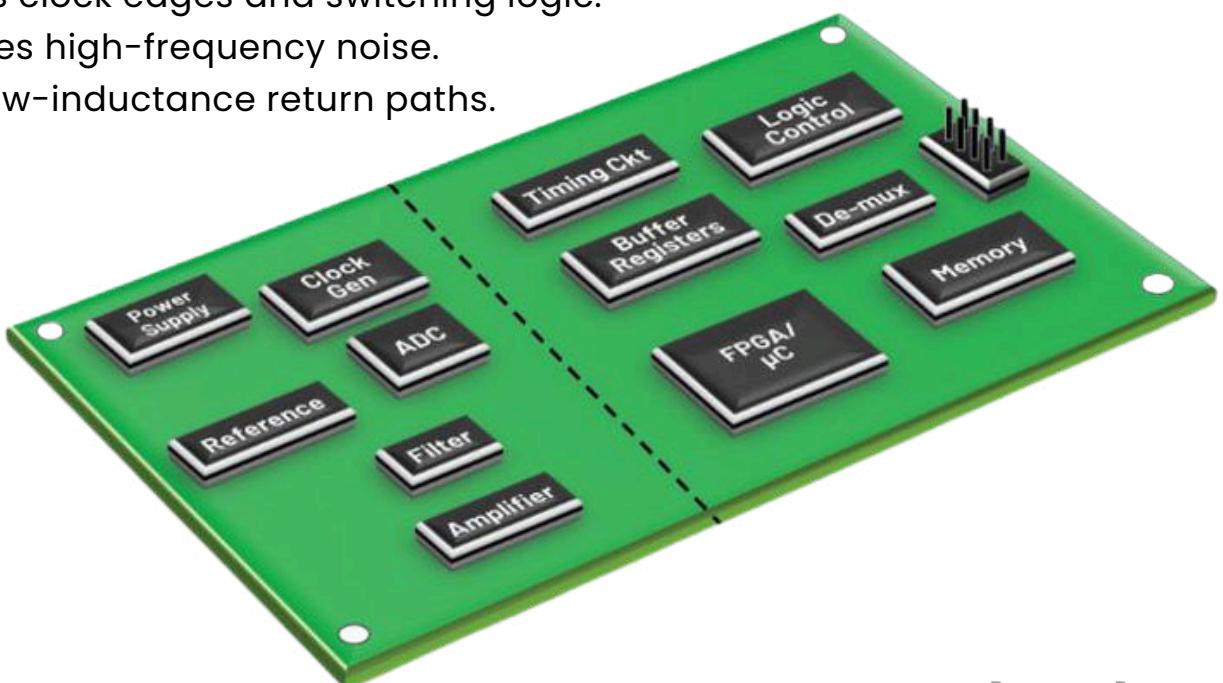
Ground Characteristics

Analog Ground (AGND):

- Carries small, continuous, or low-frequency currents.
- Needs stable, low-impedance reference (μV -level precision).
- Optimized for low-frequency and DC accuracy.

Digital Ground (DGND):

- Handles large, fast transient currents.
- Supports clock edges and switching logic.
- Generates high-frequency noise.
- Needs low-inductance return paths.



GROUND – DIVIDING

Separation Principles

- **Physical Isolation:** Use separate ground planes for analog (AGND) and digital (DGND).
- **Current Path Control:** Prevent digital return currents from flowing into analog ground.
- **Single Connection Point (Star Point):** Join AGND and DGND at one controlled location → usually near ADC/DAC or mixed-signal IC.
- **Placement Strategy:**
 - Place the join point close to the component where analog ↔ digital conversion happens.
 - Route analog traces only over the analog ground plane, and digital traces only over the digital ground plane.

Isolation Effectiveness

Frequency Range	Isolation Required	Typical Achievement
DC – 1 kHz	>60 dB	80–100 dB
1 kHz – 100 kHz	>40 dB	60–80 dB
100 kHz – 10 MHz	>20 dB	40–60 dB
>10 MHz	~0 dB	20–40 dB

Key Insight: Separation works well at low and medium frequencies. At very high frequencies (>10 MHz), parasitic coupling reduces effectiveness.

Best Practices

- Keep analog and digital sections physically separate on the PCB.
- Place mixed-signal ICs (ADC/DAC) on the boundary between AGND and DGND.
- Use short, wide traces or copper pours to connect AGND and DGND at a single star point.
- Avoid routing digital traces over analog planes and vice versa.
- Add ferrite beads or capacitors at the join point if extra filtering is needed.

GROUND – DIVIDING

Bridging Ground Planes

Even when analog and digital grounds are separated, they must be connected at a single controlled point to provide a common reference. This connection — or “bridge” — must be carefully designed to block unwanted noise while allowing proper return paths.

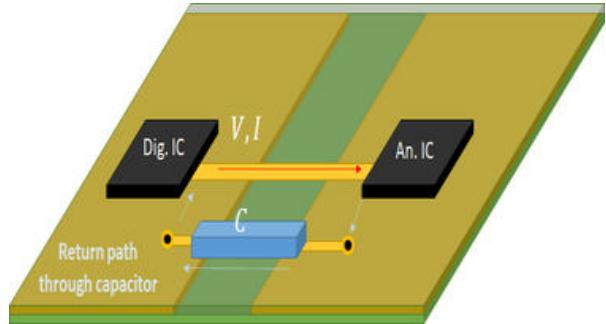
Single-Point Connection Principle

- **Why?** Ensures only one defined current return path between analog (AGND) and digital (DGND) domains.
- **Goal:** Prevent noisy digital return currents from leaking into sensitive analog circuits.
- **Location:** Place the bridge near ADC/DAC or mixed-signal ICs, where analog and digital domains interact.

Bridge Implementation Methods

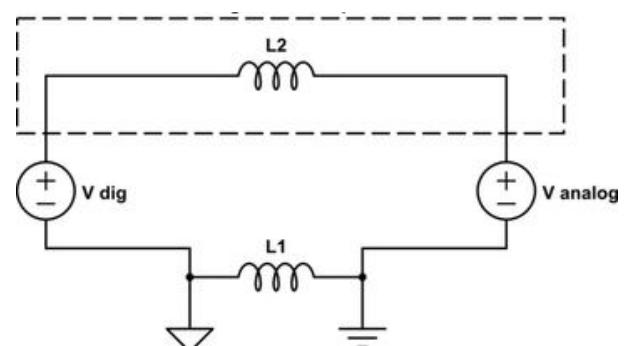
1. Capacitor Bridge

- Blocks DC, allows AC return.
- Acts like a high-pass filter.
- Typical value: 1000 pF – 0.1 µF.
- Use Case: When DC isolation is needed but high-frequency return coupling must be preserved.



2. Inductor Bridge

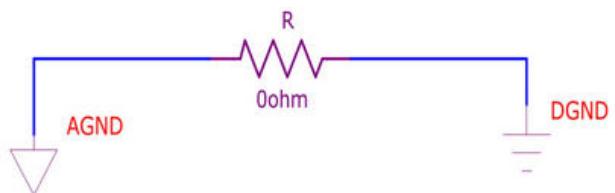
- Adds controlled inductance between grounds.
- Effective at blocking high-frequency noise.
- Requires careful selection to avoid resonance issues.
- Use Case: Specialized applications where selective frequency isolation is critical.



GROUND – DIVIDING

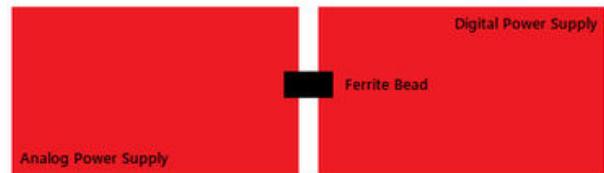
3. Zero-Ohm Resistor Bridge

- Provides a removable connection for testing and debugging.
- Adds small series resistance ($\approx 50 \text{ m}\Omega$).
- Limited high-frequency filtering ability.
- Use Case: Flexible option during prototyping and manufacturing.



4. Ferrite Bead Bridge (Most Common)

- Passes DC and low-frequency currents.
- Blocks high-frequency noise ($>1 \text{ MHz}$).
- Provides 20–40 dB attenuation.
- Effectiveness depends on ferrite's self-resonance frequency.
- Use Case: Standard choice for mixed-signal ICs to isolate digital switching noise.



Connection Placement Strategy

- Place bridge near boundary of analog and digital sections.
- Connect close to mixed-signal IC (ADC/DAC).
- Keep connection short and wide to reduce impedance.
- Avoid routing high-speed digital signals across the bridge.
- Consider thermal relief to avoid stress during soldering.

Best Practices

- Use ferrite beads as the default bridge unless a specific filter requirement exists.
- In critical designs, combine ferrite + capacitor for a broadband filter.
- For very high-speed ($>10 \text{ MHz}$) systems, sometimes no split ground (single solid ground plane) performs better.
- Always validate bridging strategy with EMI/Signal Integrity simulations.

GROUND – DIVIDING

High-Frequency Considerations (>10 MHz)

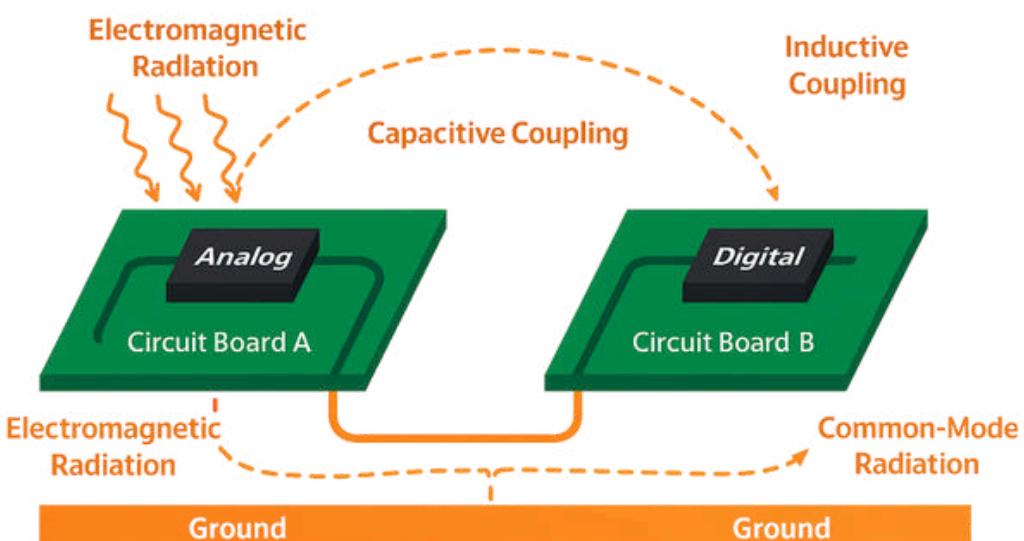
At high frequencies, ground separation becomes less effective due to parasitic effects and electromagnetic coupling. Even with isolated analog and digital grounds, unwanted noise can still couple through the board.

Why Separation Breaks Down Above 10 MHz?

- At low frequencies (<100 kHz): conductive coupling dominates → ground plane isolation works well.
- At medium frequencies (100 kHz–10 MHz): both conductive and electromagnetic effects exist → partial isolation.
- At high frequencies (>10 MHz): electromagnetic fields dominate → planes act like antennas → isolation is less effective.

Coupling Mechanisms at High Frequencies

- **Capacitive Coupling:**
 - Electric fields between planes/trace gaps.
 - Increases with reduced spacing and higher frequency.
- **Inductive Coupling:**
 - Magnetic fields linking current loops.
 - Bigger loop area → stronger inductive coupling.
- **Electromagnetic Radiation:**
 - Board dimensions comparable to wavelength → acts as an antenna.
 - Radiation couples noise across sections.
- **Common-Mode Radiation:**
 - Voltage differences between large ground planes generate antenna effects.



GROUND – DIVIDING

Frequency-Dependent Behavior

Low Frequency (<100 kHz):

- Conductive coupling dominates.
- Ground plane isolation very effective.
- Bridges (ferrite, capacitor) can filter well.

Medium Frequency (100 kHz–10 MHz):

- Mixed conductive + electromagnetic coupling.
- Ground isolation moderately effective.
- Resonances in ferrites/inductors matter.

High Frequency (>10 MHz):

- Electromagnetic coupling dominates.
- Ground isolation largely ineffective.
- Physical layout and shielding more important.

Mitigation Strategies for High-Frequency Designs

- **Minimize Ground Plane Gaps:** Avoid large slots or splits.
- **Multiple Bridge Components:** Use ferrite + capacitor combos to cover different frequency ranges.
- **Guard Traces:** Add grounded guard traces around sensitive analog circuits.
- **Local Shielding:** Use grounded shields or metal cans over critical analog sections.
- **Single Ground Plane Approach:** For very high-speed designs (RF, GHz digital), a solid ground plane often performs better than splitting.
- **Via Stitching / Fencing:** Create continuous low-inductance returns and contain EMI at board edges.

GROUND & POWER DELIVERY

Ground systems are just as important as power rails. They form return paths for supply currents, stabilize voltage references, and manage the impedance profile of the power distribution network (PDN).

Decoupling & Bypass Capacitors

Decoupling capacitors are the unsung heroes of PCB design. They ensure stable power delivery by supplying instantaneous current to ICs during fast switching events and by filtering noise from the PDN.

Why They're Critical

- **Switching Events:** Digital ICs draw sharp current spikes during clock edges and transitions.
- **Inductive Power Paths:** Traces and planes have inductance that delays current delivery.
- **Local Energy Storage:** Decoupling capacitors act like mini-reservoirs, discharging energy instantly to the IC.
- **Noise Suppression:** Bypass capacitors short high-frequency noise to ground, keeping supply rails clean.

Types of Current Demands They Address

- **Static Current (DC bias):** Constant draw for biasing.
- **Dynamic Current:** Varies depending on switching activity.
- **Switching Spikes:** Short, high-magnitude current bursts.
- **Broadband Frequency Content:** Extends from DC up to GHz in high-speed designs.

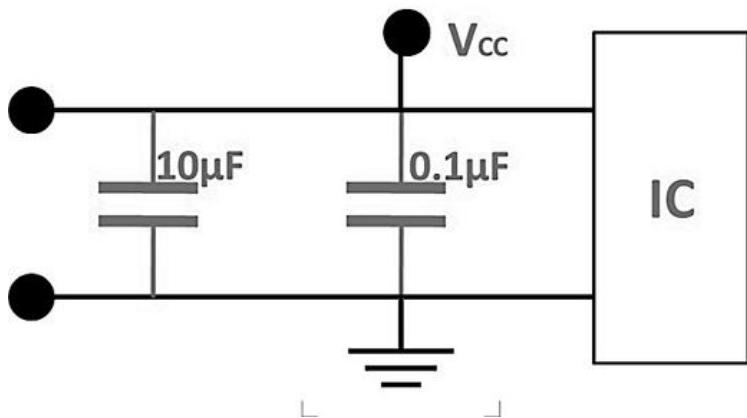
Capacitor Selection Criteria

- **Static Current (DC bias):** Constant draw for biasing.
- **Dynamic Current:** Varies depending on switching activity.
- **Switching Spikes:** Short, high-magnitude current bursts.
- **Broadband Frequency Content:** Extends from DC up to GHz in high-speed designs.

GROUND & POWER DELIVERY

Capacitor Selection Criteria

Capacitor Type	Value Range	Effective Frequency Range	ESR	ESL	Role in PDN
Electrolytic	10 μF – 1000 μF	DC – 1 kHz	0.1–1 Ω	5–20 nH	Bulk energy storage, low-frequency smoothing
Tantalum	1 μF – 100 μF	DC – 100 kHz	0.01–0.1 Ω	1–5 nH	Mid-frequency stability
Ceramic (X7R)	0.1 μF – 10 μF	1 kHz – 1 MHz	0.001–0.01 Ω	0.5–2 nH	High-speed decoupling, general
Ceramic (X5R/COG)	10 pF – 1 μF	100 kHz – 100 MHz+	<0.001 Ω	0.2–1 nH	Ultra-high-speed decoupling, GHz filtering



Best Practices

- Use a mix of capacitor values (bulk + mid + high-frequency) → covers wide frequency spectrum.
- Place smaller capacitors closest to IC pins (low ESL, handles high-speed spikes).
- Larger capacitors can be placed farther away for bulk energy.
- For critical ICs (FPGAs, CPUs, DDR), use multiple capacitors per supply pin.
- Always check PDN impedance targets (<10 mΩ typical for high-speed boards).

GROUND & POWER DELIVERY

Decoupling Placement

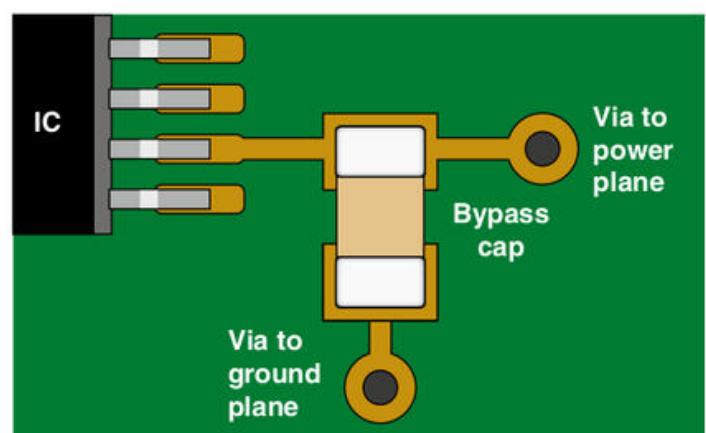
The effectiveness of a decoupling capacitor is not just about its value – placement on the PCB determines how well it works. Poorly placed capacitors act like useless ornaments; properly placed ones keep ICs stable and noise-free.

Why Placement Matters?

- Every trace and via has inductance. Even a few millimeters can reduce a capacitor's high-frequency effectiveness.
- If the capacitor is too far from the IC power pin, its response time is delayed.
- Direct, low-impedance connections ensure fast current delivery and effective noise suppression.

Optimal Placement Guidelines

- **Closest to Power Pins:**
 - Place small ceramics (0.01–0.1 μF) as close as possible to IC VCC pins.
 - Use via-in-pad or short traces directly to planes.
- **Shortest Current Loop:**
 - The loop formed by the capacitor \rightarrow IC \rightarrow ground must be small and tight.
 - Shorter loops = lower inductance = better high-frequency performance.
- **Direct Plane Connections:**
 - Connect capacitors to power and ground planes via multiple vias.
 - Avoid long thin traces – they add resistance and inductance.
- **Use Multiple Capacitors:**
 - Place a small, mid, and large capacitor per IC or per supply rail.
 - Small caps near the pins, larger ones slightly farther.
- **Progressive Placement:**
 - Bulk capacitors (10–100 μF) can be placed farther away (edge of board or near regulators).
 - Mid-value capacitors (1 μF , 10 μF) should be distributed across the PCB near clusters of ICs.



GROUND & POWER DELIVERY

Power Distribution Network (PDN) Design

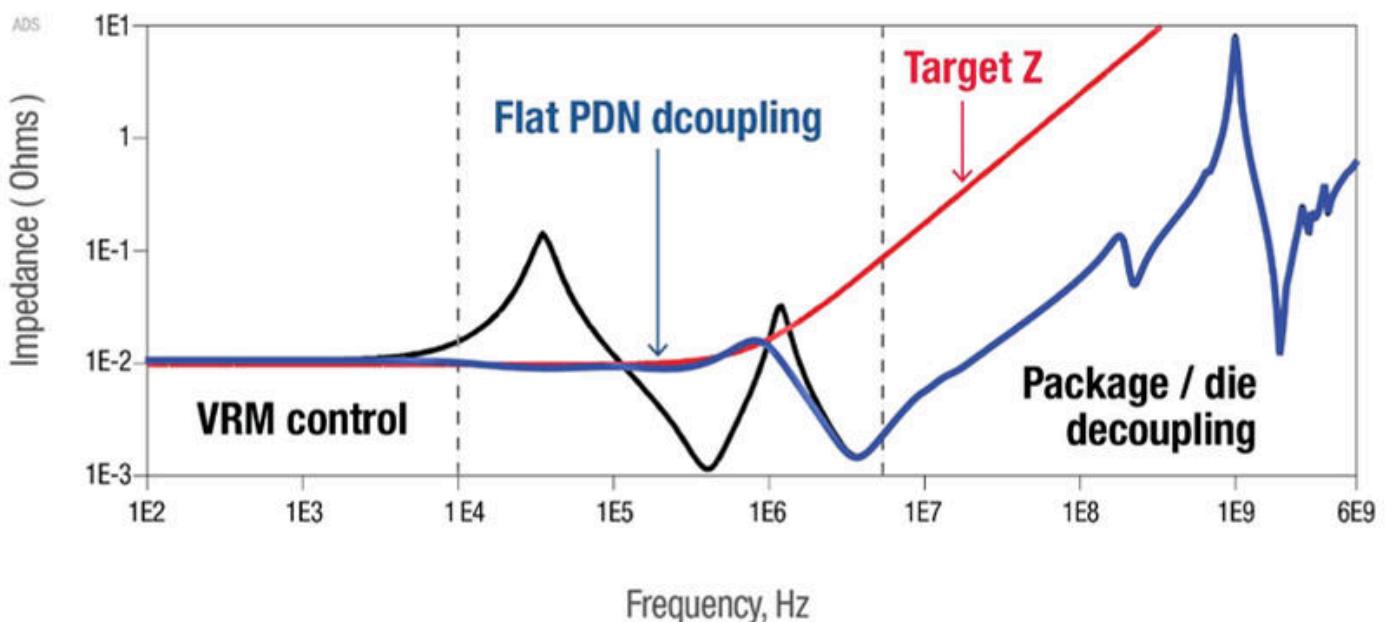
A well-designed PDN ensures the supply impedance remains flat and below target across frequency.

PDN Impedance Targets:

- DC–1 kHz → $<10\text{ m}\Omega$ (bulk capacitors dominate).
- 1 kHz–1 MHz → $<1\text{ m}\Omega$ (tantalum/ceramics support).
- 1 MHz–100 MHz → $<0.1\text{ m}\Omega$ (small ceramics handle spikes).
- 100 MHz → $<0.01\text{ m}\Omega$ (on-die/package capacitance of IC).

Key Principle: A wideband mix of capacitor values + proper placement = stable PDN.

PDN Impedance vs Frequency



Best Practices

- Always put smallest capacitors directly at the IC pins.
- Group capacitors logically per supply rail.
- Use multiple vias to reduce loop inductance.
- Distribute decoupling capacitors evenly across large ICs (e.g., FPGAs, CPUs).
- Validate placement with Power Integrity (PI) simulations when possible.

GROUND & POWER DELIVERY

Power Supply Return Paths

Power delivery is not just about supplying current – every amp that goes out must return. The ground path is the hidden highway that completes the circuit. Its impedance directly affects voltage regulation, noise, and system stability.

Return Current Path Analysis

- A supply current flows: **Power Source → Load → Ground Return → Source.**

The return path quality is critical:

- Low-frequency/DC currents:** Take the lowest resistance path.
- High-frequency currents:** Take the lowest inductance path – usually directly under the signal or supply trace.
- Discontinuities:** Force current to detour → causes voltage drops, EMI, and crosstalk.

Return Path Components:

- Ground Plane Resistance** → DC voltage drop across copper.
- Ground Plane Inductance** → Causes high-frequency impedance.
- Via Resistance/Inductance** → Adds extra impedance when transitioning layers.
- Connector Resistance** → Critical in modular/board-to-board systems.

Voltage Drop Calculations

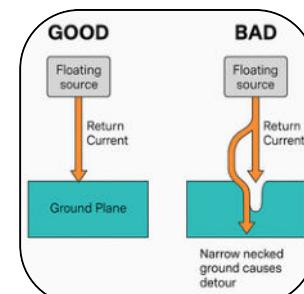
For DC conditions:

$$V_{drop} = I \times R_{ground} = I \times \frac{\rho \times L}{W \times T}$$

Where:

- I = return current
- ρ = copper resistivity
- L = current path length
- W = ground plane width
- T = copper thickness

Key Insight: Wider, thicker planes = lower resistance.



GROUND & POWER DELIVERY

AC Impedance Considerations

At high frequencies, inductance dominates:

$$Z_{\text{ground}} = \sqrt{R^2 + (2\pi fL)^2}$$

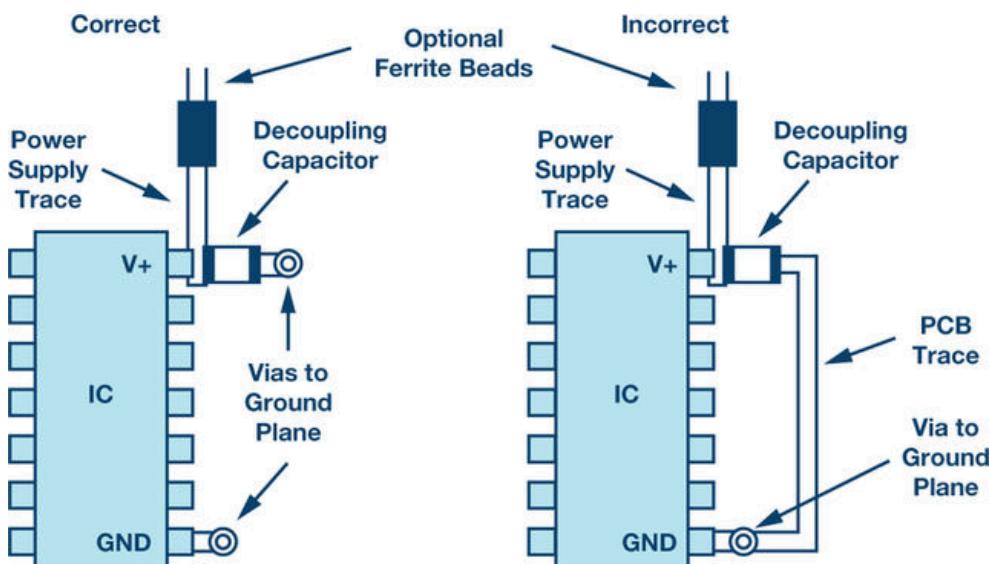
- Higher frequency → higher impedance.
- Ground plane discontinuities (splits, slots) = huge spikes in impedance.
- Leads to voltage bounce, jitter, and EMI.

Current Distribution Optimization

- **Maximize Ground Plane Area:** Wide copper spreads current evenly.
- **Multiple Vias:** Use via arrays to reduce transition impedance.
- **Place Power Connections Near Loads:** Shorter paths minimize drops.
- **Avoid Narrow Necks:** Don't funnel large return currents through thin copper.
- **Thicker Copper for High Current:** Upgrade to 2 oz or 3 oz copper when current is >3–5 A.
- **Separate High-Current Returns:** Keep noisy power returns (e.g., motor drivers) away from sensitive analog/RF returns.

Best Practices

- Always provide continuous return planes beneath high-speed traces.
- Tie ground planes with stitching vias near signal vias to preserve return path continuity.
- Simulate current density in high-power boards to prevent hot spots.
- Validate voltage drops against design margins (e.g., $\leq 5\%$ supply tolerance).



GROUND & POWER DELIVERY

Ground & Power Islands

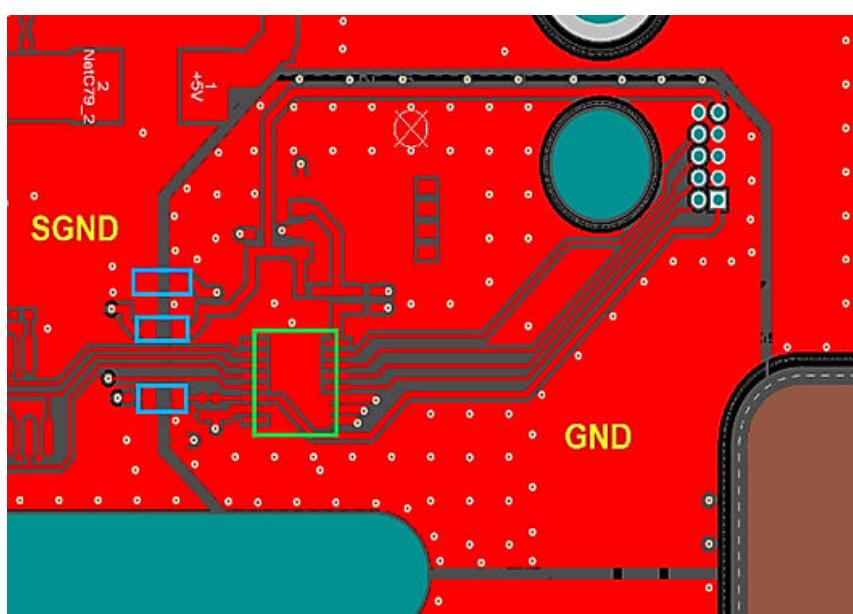
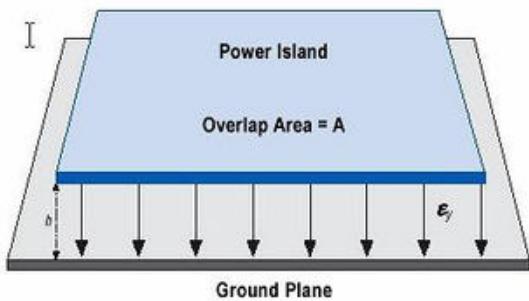
Power islands are isolated power and ground regions on a PCB that supply specific circuit sections. They are crucial when different subsystems require clean, stable, or independent voltage domains.

Why Use Power Islands?

- **Noise Isolation:** Prevents switching noise from digital/RF circuits contaminating analog or precision blocks.
- **Multiple Voltage Domains:** Supports mixed IC requirements (e.g., 1.2 V core, 3.3 V I/O, 5 V analog).
- **High-Current Management:** Separates heavy loads (motors, drivers) from sensitive logic circuits.
- **Improved Stability:** Enables local regulation and optimized decoupling.

Island Design Requirements

- **Electrical Isolation:** No direct copper tie to the main ground or power plane.
- **Controlled Connection:** Use single-point links (ferrite bead, inductor, resistor).
- **Local Regulation:** Place LDOs or DC-DC converters within the island.
- **Sizing & Copper Area:** Ensure adequate copper pour for the island's current demand.
- **Thermal Management:** Add vias under high-current islands for heat spreading.



GROUND & POWER DELIVERY

Common Applications

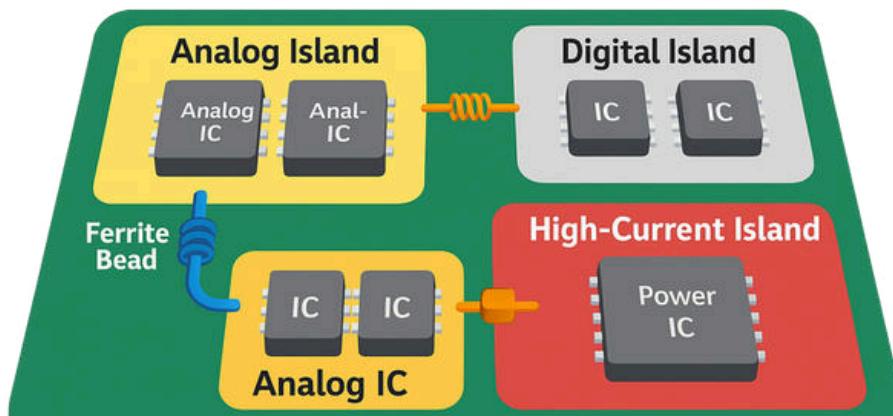
- **Analog Islands:** Clean supply for ADC/DAC, precision op-amps.
- **RF Islands:** Low-noise ground/power for high-frequency front-ends.
- **Multi-Voltage Systems:** 1.2 V, 1.8 V, 3.3 V rails on the same PCB.
- **High-Current Islands:** Isolated supplies for motor drivers, power amplifiers, FPGAs.

Isolation Techniques

- **Inductor Isolation**
 - Passes DC, blocks high-frequency noise.
 - Typical: $1 \mu\text{H} - 100 \mu\text{H}$ (depends on frequency).
 - Must handle full load current without saturation.
- **Ferrite Bead Isolation (Most Common)**
 - Blocks high-frequency noise ($>1 \text{ MHz}$), passes DC.
 - Provides 20–40 dB attenuation.
 - Cheaper and smaller than inductors.
- **Resistor Isolation**
 - Simple, low-cost method.
 - Creates small voltage drop proportional to load current.
 - Limited to low-current analog islands.

Island Layout Considerations

- Maintain minimum spacing to prevent copper bridging.
- Use guard traces or copper barriers for additional isolation.
- Place decoupling capacitors inside the island (close to IC pins).
- Use thermal vias to spread heat from high-current islands.
- Avoid routing high-speed signals across island boundaries.



GROUND

GROUND MIRROR

Ground Mirror – The Role of Planes in Signal Integrity

Ground planes act as electromagnetic mirrors for signals, controlling impedance and field distribution around conductors. They provide stable return paths, suppress EMI, and reduce crosstalk.

Ground Mirror Physics – Electromagnetic Reflection

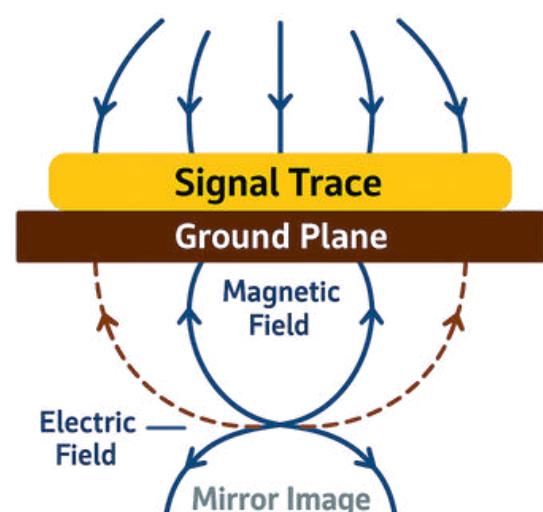
Ground planes act like electromagnetic mirrors for signals. When a current flows in a trace above a ground plane, electromagnetic fields are formed between the conductor and the plane. The plane provides a stable return path and controls the impedance of the signal line.

Electromagnetic Field Behavior

- **Electric Field Lines**
 - Terminate perpendicularly on the ground plane surface.
 - Confined fields reduce crosstalk to nearby traces.
- **Magnetic Field Lines**
 - Run parallel along the ground plane.
 - The plane supports low-inductance return paths.
- **Current Distribution**
 - Return current flows directly under the signal conductor at high frequencies.
 - At lower frequencies, current spreads more broadly across the plane.
- **Impedance Control**
 - Trace-to-plane spacing determines the characteristic impedance.
 - Wider traces = lower impedance, higher spacing = higher impedance.

Mirror Image Theory – Why Mirror?

- The ground plane behaves like a mirror that duplicates the signal trace beneath the surface.
- This virtual image allows mathematical calculation of impedance and field behavior.
- Used in microstrip impedance formulas for PCB design.



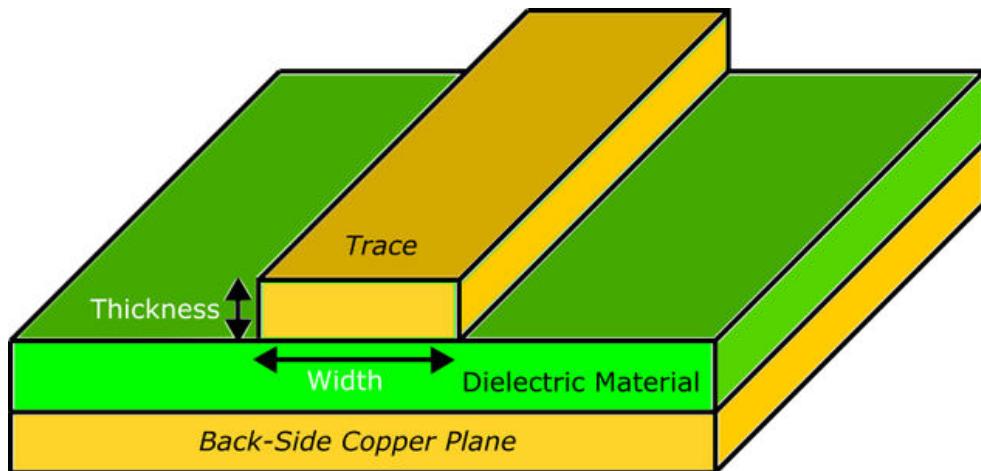
GROUND MIRROR

- **Characteristic Impedance (Microstrip):**

$$Z_0 = \frac{377}{\sqrt{\epsilon_r}} \times \frac{1}{\left(\frac{W}{H} + 1.393 + 0.667 \ln\left(\frac{W}{H} + 1.444\right)\right)}$$

Where:

- W = trace width
- H = distance to ground plane
- T = trace thickness
- ϵ_r = dielectric constant of substrate



Benefits of a Ground Mirror

- **Field Containment:** Confines electric/magnetic fields, preventing excessive EMI.
- **Crosstalk Reduction:** Electric fields terminate on the plane instead of adjacent traces.
- **Stable Impedance:** Maintains consistent signal integrity for high-speed signals.
- **Return Path Control:** Ensures lowest-inductance current return path.
- **EMI Suppression:** Prevents radiation into free space by containing fields near the conductor.

GROUND MIRROR

Crosstalk – When Fields Talk to Each Other

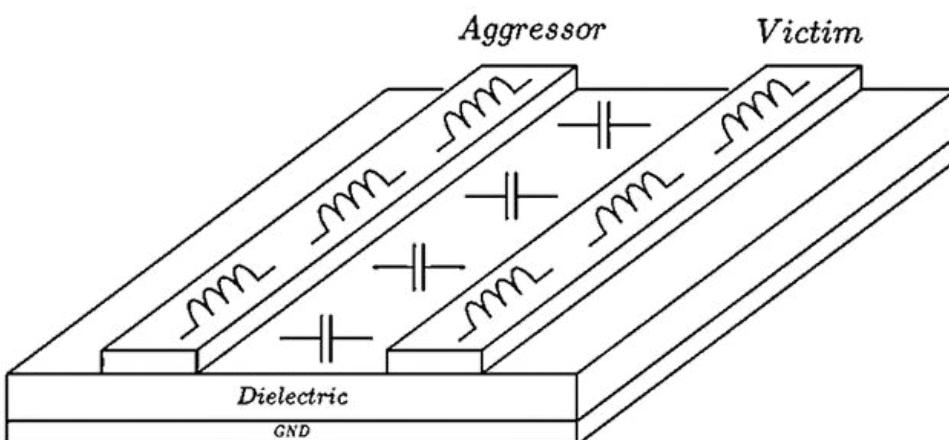
Crosstalk occurs when electromagnetic fields from one signal trace couple into another, causing unwanted noise, jitter, and signal distortion. At high frequencies, crosstalk becomes one of the most critical challenges in PCB design.

Crosstalk Coupling Mechanisms

- **Capacitive Coupling (Electric Field)**
 - Voltage changes on an aggressor trace induce displacement currents in nearby victim traces.
 - Dominant at high edge rates and close spacing.
- **Inductive Coupling (Magnetic Field)**
 - Current changes in one trace induce noise voltage in adjacent loops.
 - Stronger when return paths are not well controlled.
- **Electromagnetic Coupling**
 - Combination of capacitive + inductive effects.
 - More pronounced at high frequencies where fields extend further.
- **Common Impedance Coupling**
 - Shared return paths create multiple signals riding on the same impedance → mutual interference.

How Ground Planes Reduce Crosstalk

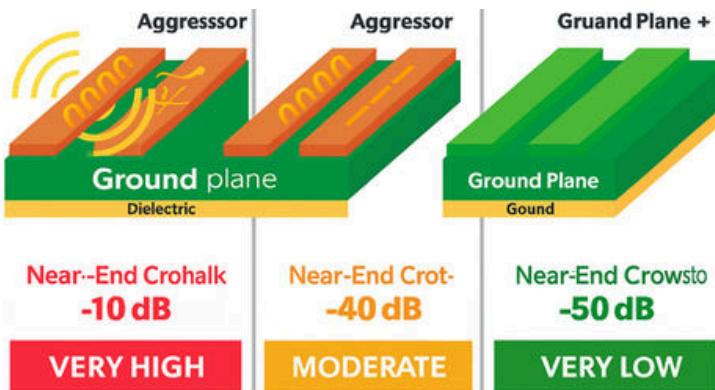
- **Field Termination:** Electric fields terminate into the plane instead of nearby traces.
- **Current Localization:** Return currents flow directly under each signal, minimizing loop area.
- **Impedance Control:** Consistent trace-to-plane spacing ensures predictable behavior.
- **Shielding Effect:** A solid plane absorbs and blocks radiation between aggressor and victim traces.



GROUND MIRROR

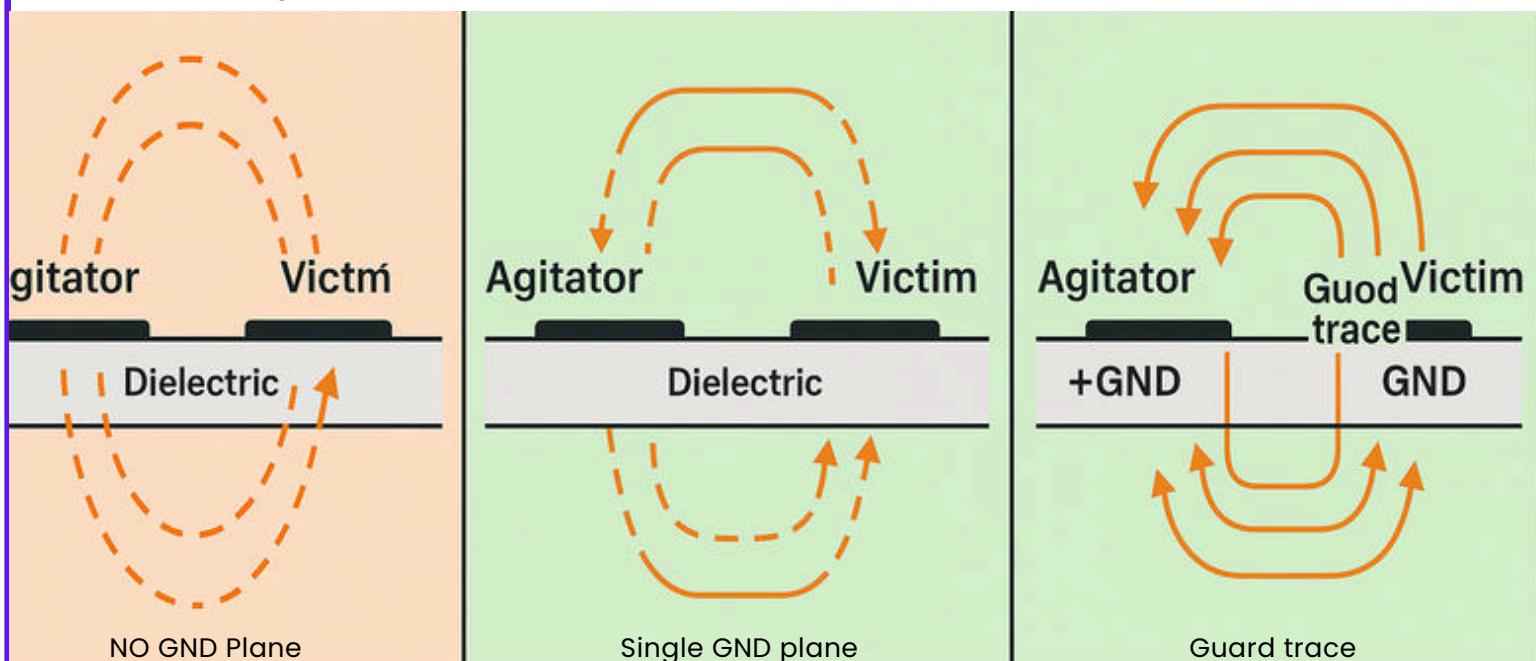
Crosstalk Reduction Effectiveness

Configuration	Near-End Crosstalk	Far-End Crosstalk
No ground plane	-10 dB to -20 dB	-10 dB to -20 dB
Single ground plane	-30 dB to -40 dB	-25 dB to -35 dB
Dual ground planes	-40 dB to -50 dB	-35 dB to -45 dB
Ground plane + guard trace	-50 dB to -60 dB	-45 dB to -55 dB



Design Guidelines for Crosstalk Control

- Maintain a **continuous ground plane** under high-speed signals.
- Use the **3W spacing rule** ($\text{space} \geq 3 \times \text{trace width}$) for critical nets.
- Add **guard traces** tied to ground between aggressor and victim signals.
- Keep **parallel trace length** as short as possible.
- Route **aggressor and victim signals on different layers** with orthogonal routing when possible.



GROUND MIRROR

Disrupted Ground Mirrors – When Planes Are Cut

Ground planes act as electromagnetic mirrors, confining fields and stabilizing impedance. But when these planes are **cut, slotted, or gapped**, the mirror effect breaks down. This forces return currents to detour, increases loop areas, and causes major **signal integrity (SI) and EMI problems**.

Ground Plane Discontinuity Effects

- **Impedance Discontinuity:**
 - Trace crossing a gap suddenly sees a change in characteristic impedance.
 - Results in signal reflections and degraded eye diagrams.
- **Return Path Lengthening:**
 - Current detours around the gap instead of flowing directly under the trace.
 - Creates a **larger loop area → higher inductance → more EMI**.
- **Increased Crosstalk:**
 - Uncontrolled fields spread to adjacent traces.
- **Signal Quality Degradation:**
 - Reflections, overshoot/undershoot, jitter, and ringing.

Ground Plane Discontinuity Effects

- **Low Frequency (<1 MHz):** Return currents spread widely → little impact.
- **Mid Frequency (1–100 MHz):** Currents concentrate below trace, but at gaps, detour paths create delay and EMI.
- **High Frequency (>100 MHz):** Currents tightly hug the trace → discontinuities cause severe disruption and radiation.

Measured Effects

- **Rise Time Degradation:** 10–50% slower edge transitions.
- **Overshoot/Undershoot:** 5–20% voltage excursions beyond supply rails.
- **Ringing:** Oscillations lasting several nanoseconds.
- **EMI Increase:** 10–20 dB higher radiation emissions.

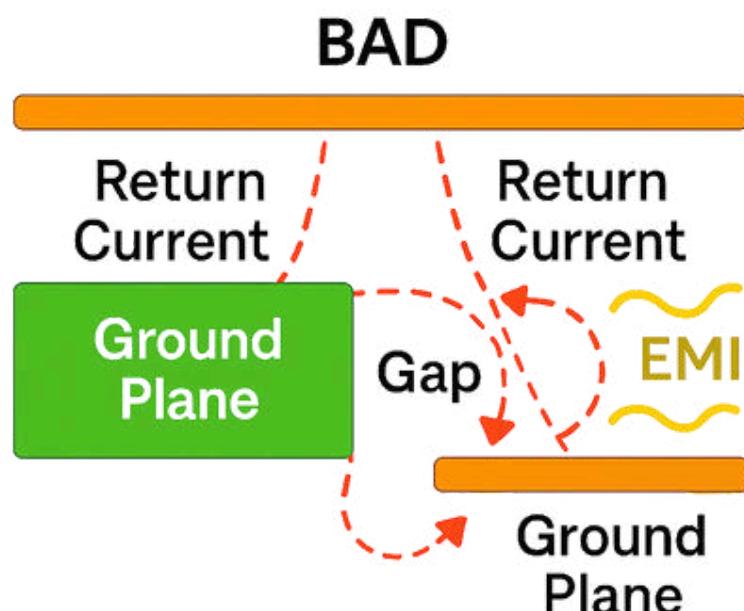
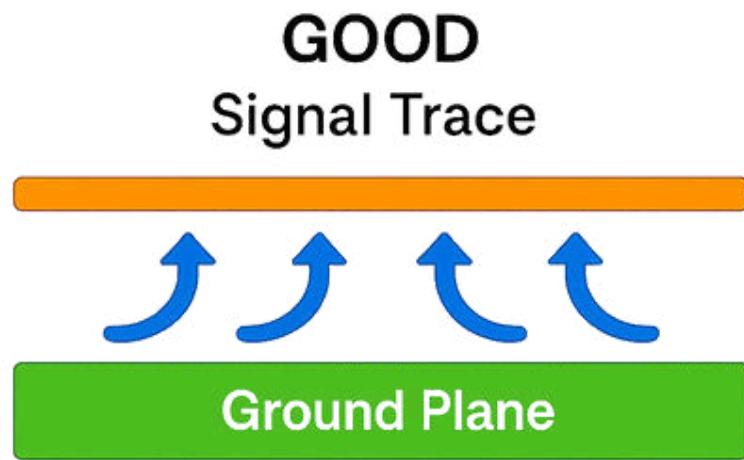
GROUND MIRROR

Mitigation Strategies for Plane Gaps

- **Stitching Capacitors:** Place across gaps to provide AC return continuity.
- **Via Stitching:** Connect adjacent ground planes with multiple vias around gap edges.
- **Overlapping Planes:** On multi-layer PCBs, ensure alternate planes cover gaps.
- **Signal Rerouting:** Avoid critical high-speed traces crossing plane splits.
- **Guard Traces:** Add grounded traces near gaps for additional shielding.

Gap Size Guidelines

- Gaps $< \lambda/20$ → minimal impact on SI.
- Gaps $\lambda/20 - \lambda/4$ → mitigation required (stitching, rerouting).
- Gaps $> \lambda/4$ → unacceptable for high-speed signals.
- Example: At 1 GHz in FR-4, $\lambda/20 \approx 15$ mm.



HIGH SPEED GROUND

High-frequency circuits require specialized grounding techniques to effectively manage current flow, minimize impedance, and control electromagnetic interference (EMI). Above 1 MHz, current behavior departs significantly from DC rules due to skin effect and proximity effect, both of which concentrate currents in limited regions of a conductor rather than uniformly.

High-Frequency Current Flow – The Role of Skin Effect

Skin Effect Fundamentals

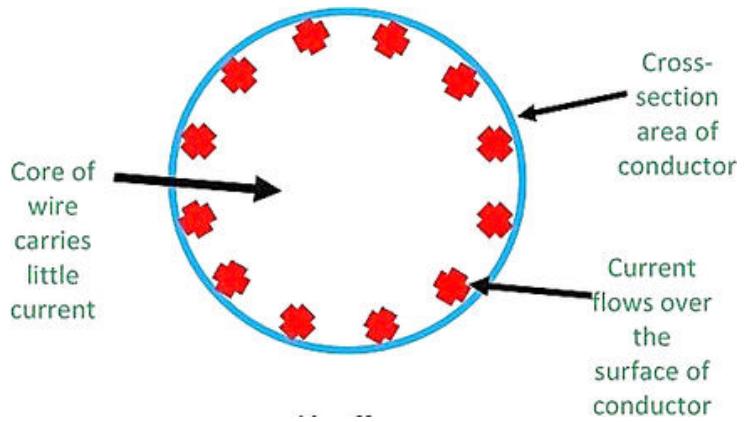
At higher frequencies, alternating current (AC) tends to flow near the outer surface of a conductor instead of uniformly through the cross-section. This phenomenon, known as the skin effect, reduces the effective conducting area, thereby increasing AC resistance compared to DC.

Skin Depth Formula:

$$\delta = \sqrt{\frac{2}{\omega\mu}} = \frac{\sqrt{\rho}}{\pi f \mu}$$

Where:

- δ = skin depth (m)
- $\omega=2\pi f$ = angular frequency (rad/s)
- μ = magnetic permeability (H/m)
- σ = conductivity (S/m)
- ρ = resistivity ($\Omega \cdot m$)
- f = frequency (Hz)



When conductor thickness $> \sim 3 \times \delta$, the current is almost entirely confined to the surface layer.

Skin Effect Fundamentals

Frequency	Skin Depth (δ)	Current Distribution
1 kHz	2.1 mm	Uniform across conductor
100 kHz	0.21 mm	Slight surface concentration
1 MHz	66 μ m	Moderate surface concentration
10 MHz	21 μ m	Strong surface concentration
100 MHz	6.6 μ m	Extreme surface concentration
1 GHz	2.1 μ m	Current confined to thin surface layer

HIGH SPEED GROUND

Design Implications:

- Thin conductors waste material at high frequency because the core carries little current.
- Plating (e.g., silver, tin) can improve surface conductivity.
- Wide conductors are preferred to reduce resistance, but thickness alone does not help beyond a few δ .

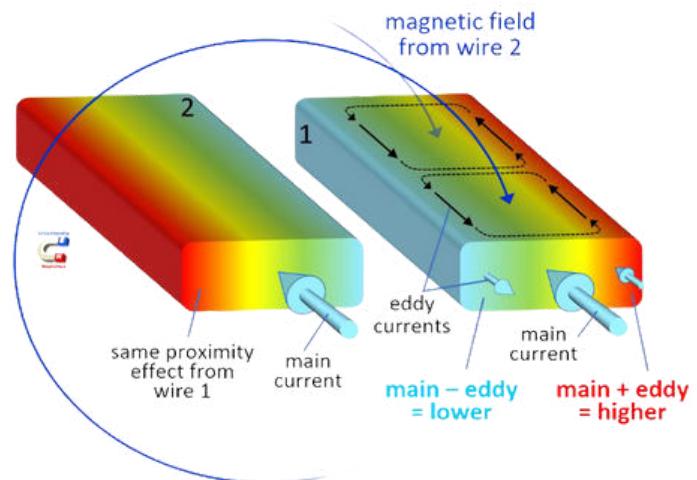
Proximity Effect in Ground & Signal Planes

Proximity Effect Basics

When conductors carrying AC are close to each other, the magnetic field of one conductor redistributes the current density in the other. In PCB planes, this causes return currents to flow directly under their associated signal traces rather than spreading uniformly.

Return Current Concentration Characteristics:

- Return current width \approx signal trace width
- Current density decreases exponentially with distance from the signal path
- ~90% of return current flows within $3 \times$ trace width of signal centerline
- Current concentration increases with frequency



Impedance & Ground Plane Inductance

At high frequency, impedance is dominated by inductance rather than resistance, because skin effect limits conductor depth.

Factors Affecting Ground Plane Inductance

- Path Length: Inductance \propto loop length; longer return paths increase impedance.
- Current Distribution: Concentrated currents (due to proximity) increase effective inductance.
- Ground Plane Thickness: Thicker planes spread current better, lowering inductance.
- Via Inductance: Vias add significant inductance; multiple vias in parallel reduce it.

HIGH SPEED GROUND

PCB Design Recommendations:

- Minimize loop area between signal and its return.
- Place return vias close to signal vias to maintain low inductance return paths.
- Avoid splitting ground planes under high-speed traces, as it forces return currents into detours → higher EMI.
- Use solid reference planes to control impedance and improve signal integrity.

Losses and Mitigation Techniques

Skin & Proximity Effect Losses:

- Increased AC resistance → higher I^2R losses
- Non-uniform current density → local hot spots and reliability issues
- Distorted return currents → crosstalk & EMI radiation

Mitigation Strategies:

- Use wide, thin traces or planes instead of thick conductors.
- Employ litz wire (for cables) to reduce AC losses.
- Maintain tight coupling between signals and return planes.
- Optimize via placement for shortest return paths.
- For very high frequencies (GHz), consider surface finishes (e.g., silver, ENIG) to improve conductivity at the skin layer.

HIGH SPEED GROUND

Via Stitching – Controlling Inductance

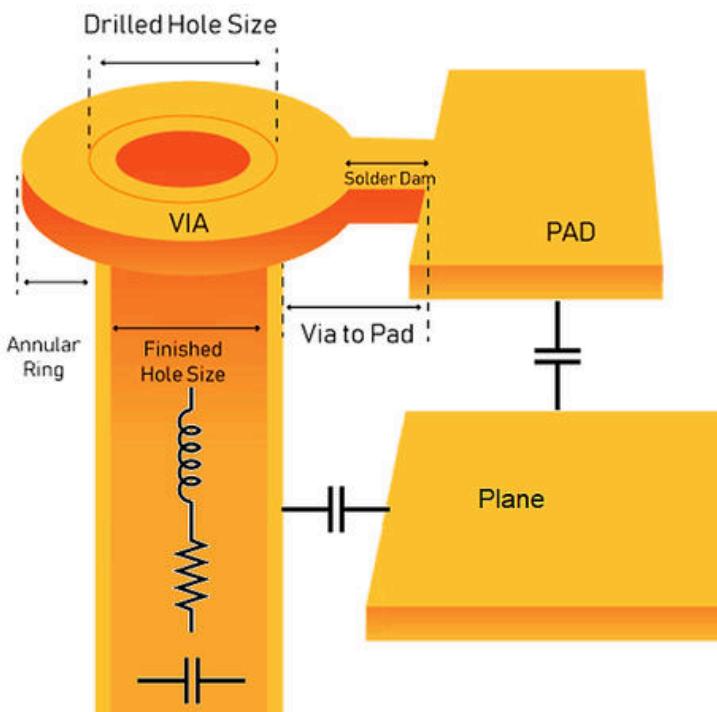
Purpose of Via Stitching

Via stitching is the practice of connecting ground or power planes using multiple vias distributed across the PCB. At high frequencies, vias act as inductive elements, and a single via can significantly increase return path impedance. By using multiple vias in parallel, designers:

- Reduce **connection inductance** and impedance
- Provide **redundant current return paths** (improves reliability)
- Enhance **EMI/EMC performance** by containing electromagnetic fields
- Improve **thermal conductivity** by spreading heat across layers
- Ensure **uniform ground potential** across multilayer boards

Individual Via Characteristics

- **Via Inductance:** Typically 0.5–2 nH, depending on via length, diameter, and surrounding planes.
- **Via Resistance:** Generally $< 1 \text{ m}\Omega$ for standard geometries, negligible at low frequency but relevant in high-density arrays.
- **Current Capacity:** ~1–3 A per via (limited by copper plating thickness and thermal dissipation).
- Frequency Response:
 - Below ~1 MHz: resistive effects dominate.
 - Above ~1 MHz: inductance dominates, making vias a major source of high-frequency impedance.
- **Parasitics:** A via is not just an interconnect—it introduces:
 - Inductance (series element)
 - Capacitance (to planes and pads)
 - Stub resonance (unconnected via barrels can resonate, causing signal degradation).



HIGH SPEED GROUND

Optimal Via Spacing

Choosing via spacing determines how well currents return and how effectively EMI is controlled.

- **Tight Spacing (<0.5 mm):**

- Strong mutual inductive coupling.
- Diminishing returns; vias act almost like a single conductor.
- Increases drill density (manufacturing cost).

- **Moderate Spacing (0.5–2 mm):**

- Ideal for most high-speed and RF designs.
- Balances inductance reduction with minimal coupling.

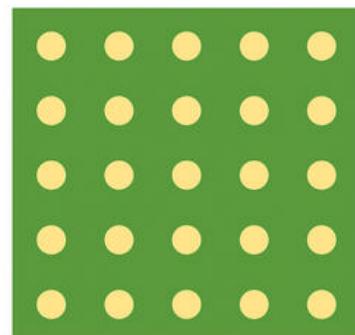
- **Wide Spacing (>5 mm):**

- Each via functions independently.
- May leave gaps in return path, leading to higher EMI radiation.

Common Stitching Patterns

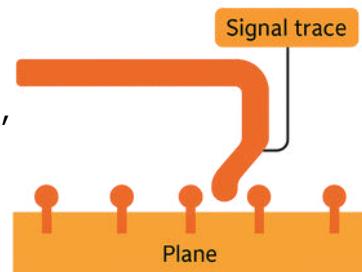
a. Grid Pattern – Uniform Ground Reference

- Vias placed evenly across a ground plane.
- Provides consistent impedance characteristics.
- Spacing guideline: 1–2 mm for high-speed layers.
- Best for general-purpose grounding in multilayer PCBs.



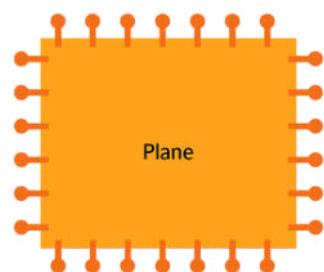
b. Signal-Following Pattern – Return Path Control

- Vias placed directly alongside critical signal traces.
- Keeps return current tightly coupled to its signal, minimizing loop area.
- Rule of thumb: Place vias every 1–2 trace widths.
- Essential for differential pairs and transmission lines.



c. Perimeter Stitching – EMI Shielding Fence

- Vias placed around PCB edges, slots, and cutouts.
- Creates a Faraday cage effect, blocking EMI leakage.
- Spacing guideline: No greater than $\lambda/10$ at the highest frequency of concern (often $\lambda/20$ for stricter EMC).
- Critical for RF designs, mixed-signal boards, and compliance testing.



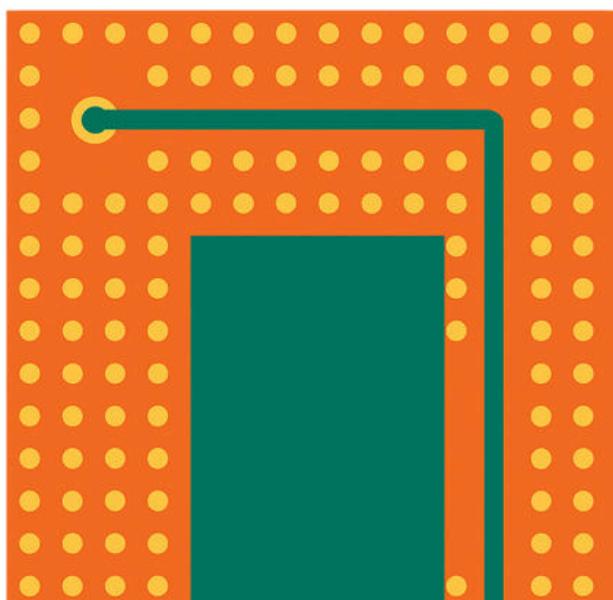
HIGH SPEED GROUND

Via Stitching Design Guidelines

- **Standard Sizes:** Use finished hole diameters of 0.2–0.3 mm for high-speed designs; smaller microvias possible in HDI.
- **Annular Ring:** Maintain minimum IPC-compliant ring for mechanical reliability.
- **Via-in-Pad:** Recommended for dense BGA packages; fill and cap to avoid solder wicking.
- **Thermal Role:** Place stitching vias under power components and heatsinks for thermal spreading.
- **Stub Management:** Use back-drilling or blind/buried vias to remove stubs and eliminate resonance.
- **Redundancy:** Always provide multiple vias for current sharing; one via is a single point of failure.
- **Balance:** More vias reduce inductance but increase drill count and cost—strike the right balance for manufacturability.

Practical Considerations

- **High-Frequency Behavior:** At GHz frequencies, via inductance can dominate, so denser stitching becomes essential.
- **Mechanical Reliability:** More vias improve robustness against PCB flexing and delamination.
- **Thermal Management:** Arrays of vias act as heat pipes, critical in power electronics.
- **Manufacturing Cost:** Dense stitching increases drill count and plating time; must be justified against EMC/thermal requirements.



HIGH SPEED GROUND

Return Path Discontinuities – Silent Signal Killers

Return path discontinuities are among the most critical challenges in high-frequency PCB design. They break the continuity of return currents, leading to signal integrity degradation, EMI radiation, and impedance mismatch.

Causes of Return Path Discontinuities

Several PCB features can disrupt return paths:

- **Layer Changes:** Signal transitions through vias force return currents to switch planes.
- **Ground Plane Gaps:** Slots, cutouts, or splits in planes block continuous return.
- **Via Transitions:** Moving between different ground planes without stitching vias.
- **Component Keepouts:** Removed copper under sensitive components.
- **Connector Transitions:** Interface points where PCB return planes may not align with external connectors.

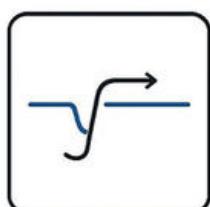
Return Current Behavior & Layer Transitions

When signals change layers through vias, return currents must also transition. If no clear path is provided, currents detour, creating long loops and higher EMI.

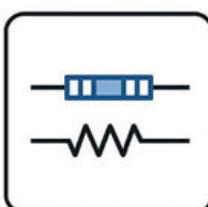
- Current follows the signal path as closely as possible (smallest loop area principle).
- At via transitions, return must jump to an adjacent ground plane.
- Without stitching vias, return current travels around the gap, forming large loops.
- Larger loops = higher inductance → stronger EMI radiation.

Return Current Behavior & Layer Transitions

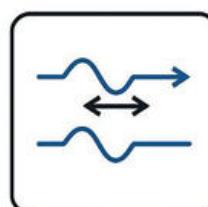
- Place stitching vias within 0.5 mm of the signal via.
- Use multiple stitching vias for critical high-speed or differential signals.
- Ensure ground plane overlap at transition zones.
- For ultra-high frequencies, consider coaxial via structures or via fences.



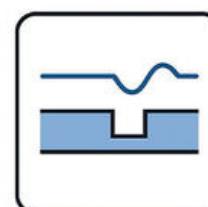
Reflections



Impedance Mismatch



Crosstalk



Return Path Discontinuities

HIGH SPEED GROUND

Ground Plane Gaps – How Bad Are They?

Return currents hate detours. When gaps exist, impedance spikes occur.

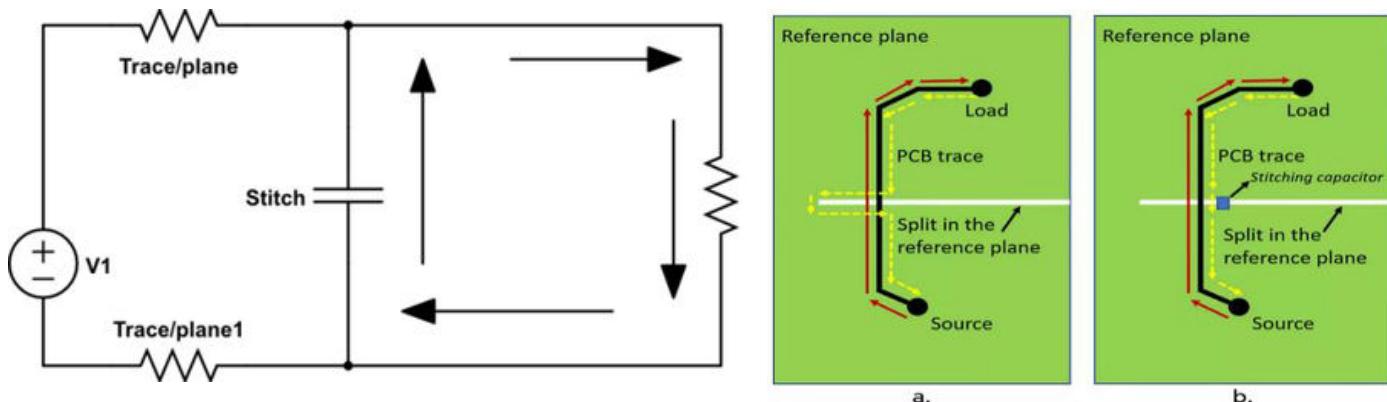
Gap Severity (relative to wavelength λ):

- **Small gaps ($< \lambda/20$)**: Minimal effect, often tolerable.
- **Medium gaps ($\lambda/20$ to $\lambda/4$)**: Noticeable signal degradation → requires mitigation.
- **Large gaps ($> \lambda/4$)**: Severe problems; redesign recommended.

Fixing Discontinuities – Mitigation Techniques

a. Stitching Capacitors

- Bridge ground plane gaps using capacitors.
- Typical values: 100 pF – 1 nF (optimized per frequency band).
- Provide AC continuity while blocking DC.
- Use multiple capacitors in parallel for wide gaps and broad frequency coverage.
- **Placement:** as close as possible to the signal crossing point.



b. Ground Guard Traces

- Run grounded traces parallel to high-speed signals crossing gaps.
- Provide controlled return paths and shield aggressors from victims.
- Maintain impedance consistency by matching trace geometry.
- Must be tied to ground planes at both ends (stitching vias required).

c. Alternative Routing Strategies

- Avoid crossing gaps when possible → choose layers with continuous planes.
- If unavoidable, minimize trace length over gap.
- Use orthogonal routing to reduce coupling and crosstalk.
- Balance signal integrity vs routing convenience carefully.

HIGH SPEED GROUND

EMI Consequences of Return Path Discontinuities

Radiating Antennas

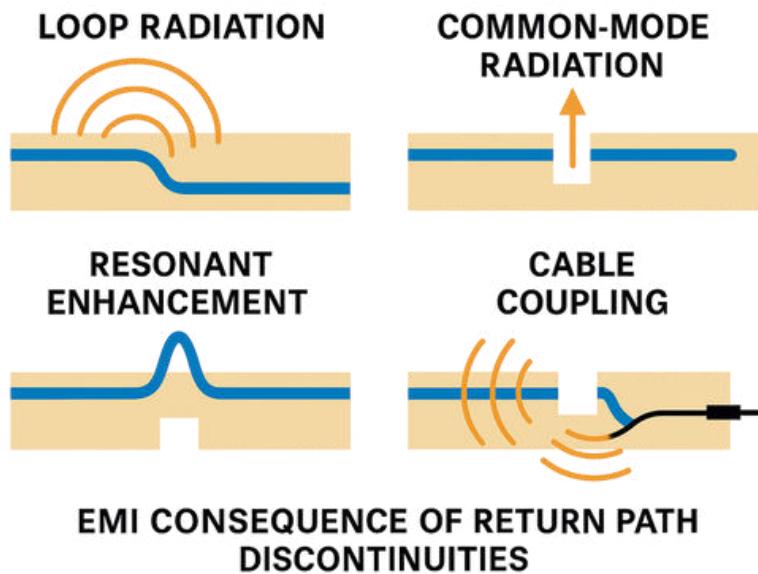
Discontinuities act as radiating antennas at high frequency.

- **Loop Radiation:** Proportional to loop area \times frequency².
- **Common-Mode Radiation:** Voltage imbalance between ground references.
- **Resonant Enhancement:** Gap length approaching $\lambda/2$ creates strong resonances.
- **Cable Coupling:** Discontinuities couple noise into external cables/connectors.

Measurement & Verification Tools

Validating return path continuity requires both simulation and measurement.

- **TDR (Time Domain Reflectometry):** Identifies impedance discontinuities.
- **Vector Network Analyzer (VNA):** Measures S-parameters for insertion/reflection loss.
- **Near-Field Probing:** Maps local EM field around gaps.
- **EMC Pre-Compliance Testing:** Ensures emission limits before certification.
- **Field Solvers & SI/PI Tools:** Predict discontinuity impact during PCB design stage.



Key Takeaways

- Return paths must always remain continuous, short, and tightly coupled to signals.
- Gaps or poor via transitions create long loops, reflections, and EMI hotspots.
- Mitigation tools: stitching vias, stitching capacitors, ground guard traces.
- Always verify with simulation + measurement before fabrication.
- Remember: A broken return path = a broken high-speed design.

EARTH GROUND

Earth Ground – The Foundation of Electrical Safety

Earth grounding provides safety protection, reference potential, and surge dissipation. It is a fundamental requirement for all electrical and electronic systems.

Purpose of Earth Ground

Beyond providing a simple zero-voltage reference, earth ground ensures:

- **Safety:** Directs fault currents safely into the earth.
- **Voltage Stabilization:** Prevents floating voltages on enclosures and chassis.
- **Equipment Protection:** Works with protective devices (fuses, circuit breakers, GFCIs) to interrupt fault conditions.
- **Lightning Protection:** Safely dissipates surge currents from strikes or switching events.
- **EMI/Noise Control:** Provides a reference plane for shielding and sensitive circuits.

Safety Protection Mechanisms

Primary Functions of Earth Grounding:

1. Fault Current Path:

- Provides a low-impedance path for fault currents.
- Ensures overcurrent devices trip quickly.

2. Voltage Limiting:

- Keeps exposed metal chassis from rising to dangerous potentials.
- Protects personnel from electric shock.

3. Circuit Protection:

- Ensures reliable operation of fuses, breakers, surge protectors, GFCIs.

4. Lightning & Surge Dissipation:

- Diverts high-energy surges (lightning, switching) to earth.
- Prevents equipment damage.

Earth Ground Resistance Requirements

The effectiveness of grounding is measured by resistance to earth (R_e).

- **NEC (National Electrical Code):** $\leq 25 \Omega$ maximum.
- **IEEE 142 (Green Book):** $\leq 5 \Omega$ recommended for sensitive electronics.
- **IEC 61000-5-2:** $\leq 1 \Omega$ for lightning protection systems.
- **Local Codes:** May impose stricter requirements.

⚡ **Rule of Thumb:** Lower resistance = safer and more reliable ground.

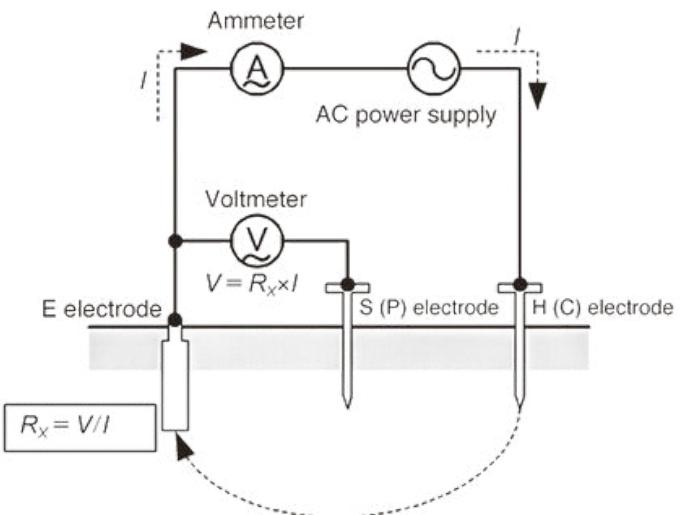
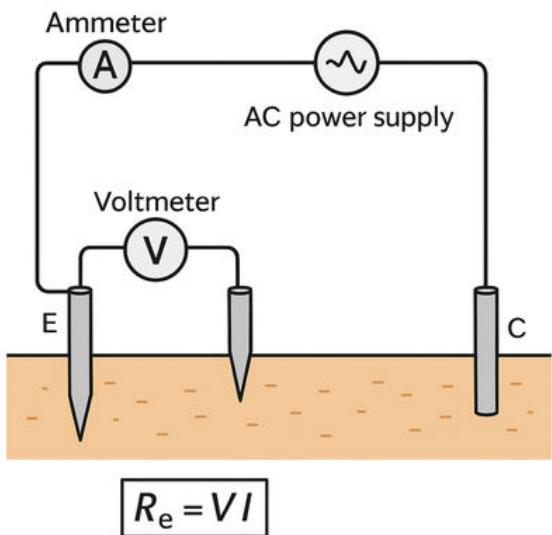
EARTH GROUND

Grounding System Design Factors

- Soil Resistivity: Varies with moisture, temperature, and composition. Sandy/dry soil has high resistivity; clay/wet soil has lower resistivity.
- Electrode Material & Size: Copper or galvanized steel rods improve conduction. Longer rods reduce resistance.
- Depth & Spacing: Multiple deep rods, properly spaced, lower resistance.
- Moisture & Treatment: Salts or bentonite can reduce soil resistivity in poor conditions.

Measuring Earth Ground Resistance

- The standard test method is the Fall-of-Potential Method (3-point).
- **Equipment:** Earth tester, ammeter, voltmeter, auxiliary electrodes.
- Setup:
 - Drive test electrode (E) into ground.
 - Place auxiliary current electrode (C) far away.
 - Insert potential electrode (P) between them.
- **Measurement Formula:** $R_e = V/I$
- Repeat at different P positions to confirm stable readings.



Types of Earth Grounding Methods

- **Rod Grounding:** Vertical rods driven into soil (most common).
- **Plate Grounding:** Buried copper/steel plates, used in rocky soil.
- **Mesh/Grid Grounding:** Large-area grids for substations and power plants.
- **Chemical Grounding:** Treated electrodes with conductive compounds for high-resistivity soil.

EARTH GROUND

Chassis Grounding – Shielding, Safety, and Signal Integrity

Chassis grounding ensures that metal enclosures, connectors, and shields are properly tied into the ground system. This serves safety, EMI shielding, and functional stability roles in both low-frequency and high-frequency designs.

Why Chassis Grounding Matters

Safety Functions

- **Shock Protection:** Prevents chassis from becoming energized under fault conditions.
- **Fault Clearing:** Provides a low-impedance path for protective devices to trip.
- **Voltage Equalization:** Maintains chassis at earth potential to avoid dangerous touch voltages.
- **Code Compliance:** Meets NEC, IEC, and UL standards for equipment safety.

EMI Shielding Benefits

- **Faraday Cage Effect:** Conductive chassis blocks external electromagnetic fields.
- **Common-Mode Rejection:** Provides a stable reference for differential signaling.
- **Cable Shield Termination:** Correct ground reference for shielded cables.
- **Emission Reduction:** Prevents internal circuits from radiating noise outward.

Chassis Grounding Implementation Methods

A. Direct Connection (DC Bonding)

- **How:** Solid conductor from chassis to ground system.
- **Pros:**
 - Lowest impedance path.
 - Best for low-frequency and DC safety grounding.
- **Applications:**
 - When chassis and circuit grounds can be common.
 - Benchtop equipment, power supplies, simple instruments.

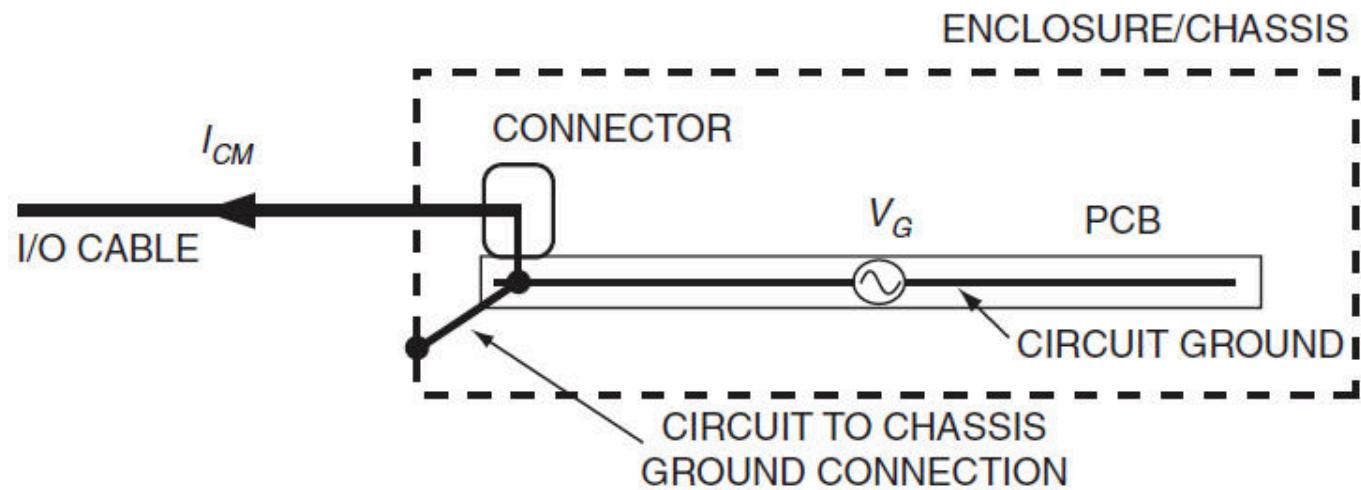
EARTH GROUND

B. Capacitive Coupling (AC Bonding)

- **How:** Connect chassis to ground through a capacitor (typically 1000 pF – 0.01 µF).
- **Pros:**
 - Provides AC grounding for EMI shielding.
 - Maintains DC isolation, preventing ground loops.
- **Applications:**
 - Sensitive analog, RF, and measurement systems.
 - Audio equipment to prevent hum from ground loops.

C. Safety Ground with Circuit Isolation

- **How:** Chassis connected to safety earth, while circuit ground is isolated via transformer or opto-coupler.
- **Pros:**
 - Ensures patient/operator safety in critical applications.
 - Prevents leakage currents from affecting sensitive circuits.
- **Applications:**
 - Medical devices (IEC 60601 compliance).
 - Hazardous or intrinsically safe equipment.



EARTH GROUND

High-Frequency Considerations

At high frequencies (RF, EMC compliance ranges), grounding behavior changes:

- **Bonding Method Matters:** DC-only bonding may be ineffective at RF due to skin/proximity effects.
- **Multiple Bonding Points:** Helps reduce ground impedance at GHz frequencies.
- **Shield Terminations:** Cable shields should be bonded 360° around the connector to chassis (not just a pigtail).
- **Stray Inductance:** Even short leads add significant impedance at RF → minimize length and maximize surface contact.

Best Practices for Chassis Grounding

- Use **short, wide conductors** (low inductance) for chassis bonds.
- For mixed-signal systems:
 - **Single-point ground** for low-frequency analog.
 - **Multi-point bonding** for RF/digital shielding.
- Terminate cable shields **directly to chassis** at entry point.
- Ensure **paint, anodization, or coatings** are removed at bonding surfaces.
- Use **star grounding** in safety-critical equipment to control leakage paths.
- Always validate with **EMI pre-compliance testing**.

Key Takeaways

- Chassis grounding is **multifunctional**: safety, EMI shielding, and stable reference.
- Choice of **direct, capacitive, or isolated connection** depends on safety vs EMI trade-offs.
- High-frequency applications require **multiple low-inductance bonds** and proper shield termination.
- Proper implementation **reduces shock hazards, emissions, and susceptibility**.

ADVANCED GROUND

Guard Traces – Localized Shielding for Signal Integrity

Guard traces are grounded conductors placed alongside sensitive signal traces to intercept electromagnetic fields, reduce crosstalk, and provide controlled return paths. They are widely used in precision analog, high-speed digital, and RF circuits.

Guard Trace Functions

- **Electrostatic Shielding:** Absorbs electric field coupling from nearby aggressor traces.
- **Crosstalk Reduction:** Provides an alternate low-impedance path to ground, reducing noise coupling into victim traces.
- **Impedance Control:** Helps maintain consistent impedance in differential and single-ended lines.
- **Return Path Control:** Offers a clearly defined ground reference, improving current return behavior.

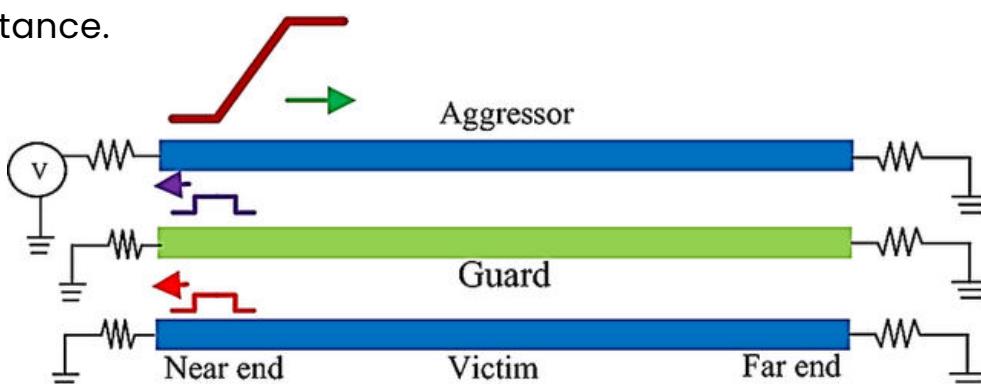
Implementation Strategies

A. Coplanar Guards

- Placed on the same layer as the signal trace.
- Typically run along both sides of the sensitive trace.
- Spacing Rule: 1–3 trace widths away from the signal.
- Connected to ground using stitching vias every $\lambda/20$ or $\sim 5\text{--}10$ mm (whichever is smaller).
- Best for critical analog and high-speed nets that run in parallel with aggressors.

B. Interlayer Guards

- Placed on adjacent layers above or below the signal.
- Provides 3D shielding around the conductor.
- Effective for RF, microwave, or differential pairs in multilayer PCBs.
- Requires careful via stitching between guard layers to ensure low inductance.



ADVANCED GROUND

Design Considerations & Best Practices

- **Termination to Ground:**
 - Guard traces must be tied to ground frequently with vias.
 - Long floating guard traces can act as antennas and worsen EMI.
- **Frequency Dependence:**
 - Most effective at low-to-mid frequencies (<1 GHz).
 - At higher frequencies, guard traces lose efficiency unless via stitching density is increased.
- **Width & Spacing:**
 - Wider guard traces provide better shielding but consume routing area.
 - Maintain clearance to satisfy design rules and impedance targets.
- **Trade-offs:**
 - Guards improve signal integrity but increase routing congestion and PCB area.
 - In very dense designs, differential pair routing or stripline geometries may be preferable.
- **Applications:**
 - Sensitive analog traces (e.g., ADC inputs, sensor lines).
 - High-speed clocks and SERDES lanes running near aggressors.
 - Medical, audio, and RF systems requiring ultra-low noise.

Key Takeaways

- Guard traces provide localized shielding to protect critical signals.
- Must be well-grounded with frequent vias—floating guards harm more than help.
- Coplanar guards are simple and effective for most high-speed designs.
- Interlayer guards add 3D protection in multilayer RF/analog boards.
- Use guards selectively—not every trace needs them; apply where crosstalk or coupling risk is highest.

ADVANCED GROUND

Virtual Ground – Creating Stable Midpoint References

Virtual grounds are artificial reference nodes that provide a stable midpoint voltage in systems without a direct ground connection. They are especially useful in single-supply circuits that require a pseudo-bipolar supply.

Virtual Ground Concept and Applications

Instead of connecting directly to earth or chassis ground, a virtual ground is generated using active or passive circuits.

Key Applications:

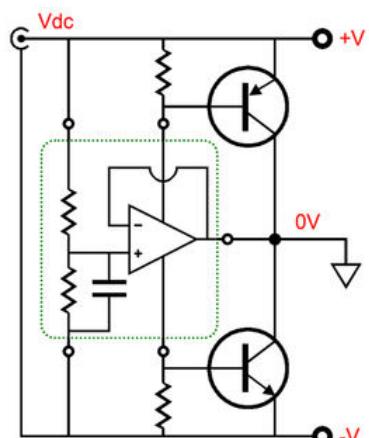
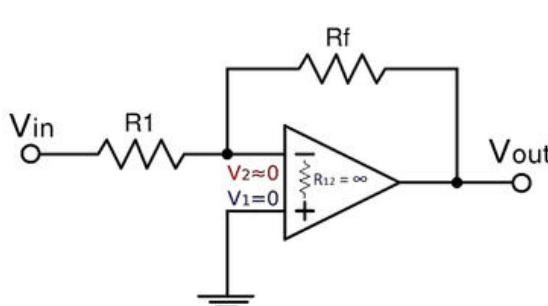
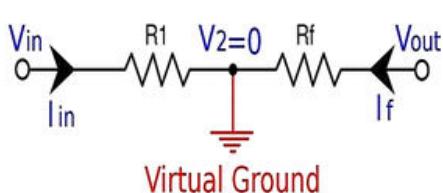
- **Single-Supply Operation:** Create $\pm V$ rails from a single positive supply.
- **Level Shifting:** Provide midpoint reference for signal translation and interface compatibility.
- **Isolation:** Act as a ground reference without tying into system or chassis ground.
- **Noise Reduction:** Generate a clean reference point independent of system ground noise.
- **Analog/Digital Separation:** Prevent interaction between analog and digital return currents.

Op-Amp Virtual Ground Implementation

An operational amplifier configured as a buffer (voltage follower) can generate a stable, low-impedance virtual ground reference.

Basic Virtual Ground Circuit

- **Voltage Divider:** Resistors split supply voltage to create midpoint ($V_{cc}/2$).
- **Buffer Amplifier:** Op-amp follower provides low output impedance, stabilizing the divider.
- **Bypass Capacitors:** Filter supply noise and stabilize reference voltage.
- **Load Capability:** Buffer sources/sinks current to maintain virtual ground at required operating point.



ADVANCED GROUND

Design Parameters & Considerations

- **Reference Accuracy:** Depends on resistor divider tolerance.
 - Precision resistors or reference ICs recommended for accurate midpoint voltage.
- **Output Impedance:** The op-amp buffer reduces divider impedance.
 - Output impedance determines ability to hold stable voltage under varying loads.
- **Frequency Response:** Limited by op-amp bandwidth and slew rate.
 - For high-frequency or dynamic loads, ensure op-amp has sufficient GBW (gain-bandwidth product).
- **Current Capacity:** Virtual ground can only sink/source as much current as the buffer can handle.
 - For higher loads, consider power op-amps or complementary transistor buffers.

Virtual Ground Circuit Variants

- **Passive Divider Only:** Simple, low-cost, but high impedance → not suitable for dynamic loads.
- **Op-Amp Buffer Divider (Most Common):** Stable low-impedance reference for audio, sensor, and signal conditioning circuits.
- **Active Split-Rail Generator ICs:** Dedicated ICs (e.g., TLE2426 “rail splitter”) provide precision, higher current handling, and improved noise performance.
- **Discrete Buffer (Op-Amp + Transistors):** Op-amp controls complementary transistors to extend current drive capability. and Used in audio amplifiers and mixed-signal designs.

Limitations and Stability Issues

- **Asymmetrical Loading:** If load current demand is unbalanced, virtual ground voltage may shift.
- **Thermal Drift:** Reference can vary with temperature unless precision resistors/ICs are used.
- **Stability:** Poorly decoupled virtual grounds can oscillate; always use bypass capacitors near the op-amp.
- **Isolation Limitation:** Virtual ground is not a substitute for true galvanic isolation (use transformers or isolation amplifiers when required).

PANELIZATION STRATEGIES

Panelization Fundamentals

Panelization is the process of arranging multiple PCBs onto a single manufacturing panel.

This allows many boards to be fabricated and assembled at the same time, reducing cost and improving efficiency.

Why It's Done (Benefits)

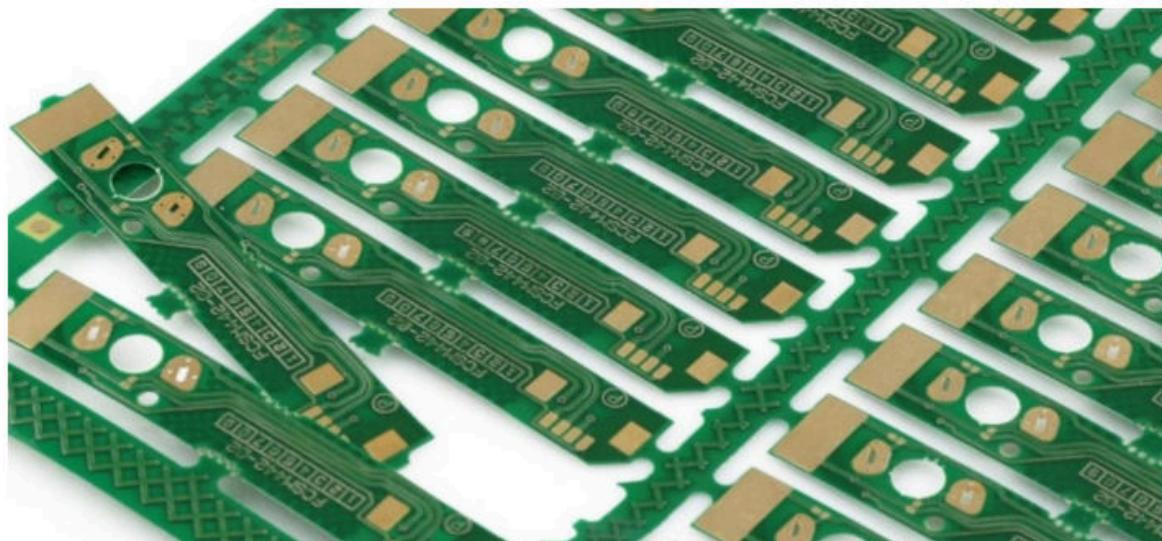
- Cost Reduction → Share setup costs across multiple PCBs.
- Manufacturing Efficiency → Batch processing for high-volume builds.
- Handling Improvement → Larger panels are easier for automated machines.
- Yield Optimization → Better use of material, less waste.

Standard Panel Sizes

Panel Size	Dimensions	Application
Small	50 × 80 mm	Prototype runs
Medium	100 × 80 mm	Production batches
Standard	100 × 160 mm	High-volume manufacturing
Large	160 × 100 mm	Industrial applications

Key Considerations

- Panel size depends on fabrication limits and assembly line capacity.
- Spacing between boards must allow for separation methods (V-scoring, tab routing, mouse bites).
- Panelization should balance material utilization with ease of depanelization



PANELIZATION STRATEGIES

Panel Layout Strategies

Panel layout is how multiple PCBs are arranged inside a single manufacturing panel to maximize efficiency, reduce waste, and make assembly easier.

Array Configurations (Single Design Panels)

- 1×2 arrangement → Simple doubling for small boards.
- 2×2 configuration → Standard four-up panelization.
- 3×3 layout → Nine-up for very small designs.
- Custom arrays → Optimized to fit unusual board shapes or maximize panel space.

Mixed Design Panels

- Product Family Grouping → Place related designs together.
- Complementary Sizing → Fit boards of different sizes to fill unused panel areas.
- Test Boards Included → Add test coupons or quality control samples.

Spacing Requirements (Between Boards)

- Minimum Separation: ≥ 2.0 mm between board edges.
- Routing Channels: ~ 3.0 mm for mechanical separation.
- V-Groove Spacing: ~ 0.5 mm depending on scoring depth.
- Tab Connections: 1.5–3.0 mm wide (depends on thickness & depaneling method).
- Panel layout strategies aim to maximize material usage while making depaneling easy.
 - Use 1×2 , 2×2 , or custom arrays for single designs.
 - Use mixed design panels to combine different products.
 - Follow spacing rules to avoid damage during separation.

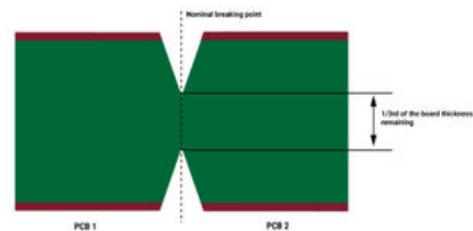
PANELIZATION STRATEGIES

Separation Methods

When multiple PCBs are panelized, they must be separated (depanelized) after manufacturing. Separation method choice affects cost, board strength, and ease of assembly.

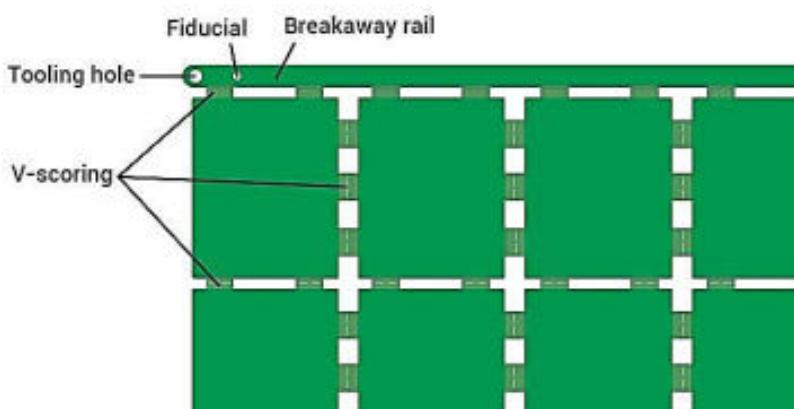
1. V-Scoring (V-Groove)

- **How it works:** Shallow "V" grooves are cut on both sides of the panel, leaving a thin web of material. Boards are snapped apart after assembly.
- **Design Rules:**
 - Straight-line separation only.
 - Board thickness: 0.8–3.2 mm.
 - Score depth: $\sim\frac{1}{3}$ of board thickness.
 - Keep ≥ 0.5 mm clearance from components.
- **Pros:** Low cost, clean edges, fast.
- **Cons:** Stress along straight lines; not suitable for irregular shapes.



2. Tab Routing

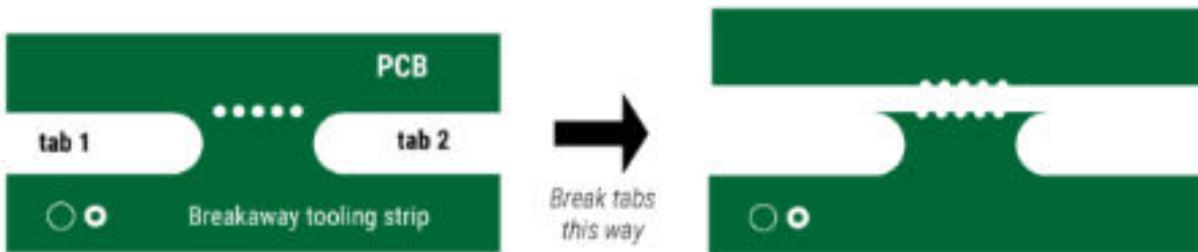
- **How it works:** Boards are held in the panel by small "tabs" of material, often with perforations. Tabs are broken or cut after assembly.
- **Tab Design:**
 - Width: 1.5–3.0 mm typical.
 - Thickness: Full board thickness maintained.
 - Tabs per board: 3–6 along the perimeter.
- **Tab Placement Guidelines:**
 - Corners for structural support.
 - Evenly spaced along edges.
 - Avoid near critical components.
 - Use rounded pads for stress relief.
- **Pros:** Works for irregular shapes.
- **Cons:** Leaves small "nubs" after breaking; may require sanding.



PANELIZATION STRATEGIES

3. Mouse Bites (Perforated Tabs)

- **How it works:** Tabs include a row of small drilled holes, making them easy to snap apart.
- **Design Rules:**
 - Hole diameter: ~0.5 mm.
 - Hole spacing: 0.5–1.0 mm centers.
 - Perforation length: 2–4 mm typical.
- **Pros:** Easy to break by hand or depaneling tool.
- **Cons:** Edges may be rough; needs post-processing for clean finish.



4. Choosing the Right Method

- V-Scoring: Best for straight-edged, rectangular boards in mass production.
- Tab Routing: Best for irregularly shaped boards that require strong panel support.
- Mouse Bites: Useful when easy manual depaneling is required.

PANELIZATION STRATEGIES

Flex-Rigid Panel Design

Flex-rigid PCBs combine rigid FR-4 areas (for components) with flexible polyimide sections (for bending).

Panelization of flex-rigid boards needs special design considerations to protect the flex areas during fabrication and assembly.

Key Considerations

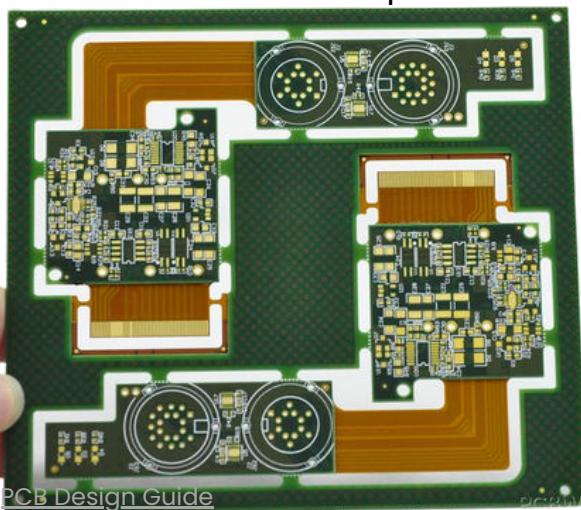
- **Stiffener Coordination**
 - Add stiffeners to support thin flex sections during handling and assembly.
- **Bend Relief Integration**
 - Provide bend relief zones to reduce mechanical stress in flex areas.
- **Separation Planning**
 - Avoid V-scoring or rough separation methods near flex sections.
 - Use laser cutting or routing for clean edges.
- **Handling Fixtures**
 - Panels may require custom tooling or support carriers to prevent flex damage during soldering and assembly.

Manufacturing Guidelines

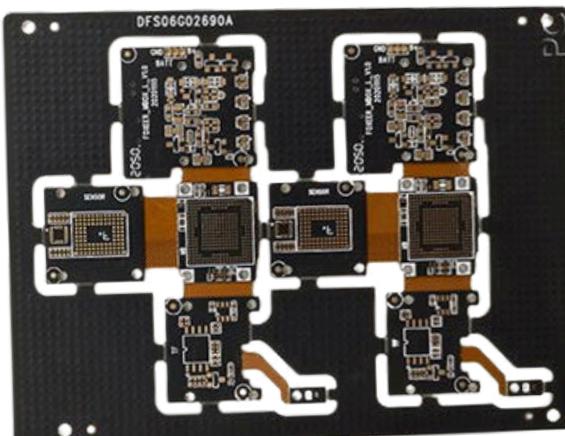
- Keep flex sections small relative to rigid areas for stability.
- Always apply overlay film instead of solder mask in flex zones.
- Avoid vias or components in flex regions near panel edges.
- Verify panelization method with manufacturer (may need laser depaneling).

Pros & Cons

- **Pros:** Saves space, allows 3D packaging, improves reliability in compact products.
- **Cons:** More complex manufacturing, requires custom fixtures, higher cost.



PCB Design Guide



- Bargunan Ponnusamy

PANELIZATION STRATEGIES

HDI Panelization

HDI (High-Density Interconnect) panelization is the process of arranging multiple HDI PCBs (with microvias, blind/buried vias, and fine features) on a single manufacturing panel.

It requires special planning because of tight tolerances and advanced fabrication steps.

Key Considerations

- **Microvia Alignment**
 - Ensure precise alignment across all panelized boards.
 - Misalignment can cause open circuits in stacked or staggered microvias.
- **Sequential Lamination**
 - HDI boards often need multiple lamination cycles.
 - Panelization must account for shrink/expansion during lamination.
- **Defect Isolation**
 - Panel design should allow defective boards to be isolated without scrapping the whole panel.
- **Test Accessibility**
 - Provide space for test coupons and electrical test pads within the panel.
 - Critical for verifying impedance, plating, and via reliability.

Design Guidelines

- Use balanced panel arrays to avoid warpage.
- Maintain consistent copper distribution across the panel.
- Add process control coupons at panel edges for quality checks.
- Increase board-to-board spacing slightly (compared to standard PCBs) to allow for laser drilling and fine routing.
- Plan depaneling methods (prefer routing/laser depaneling instead of V-score).

Pros & Cons

- **Pros:**
 - Efficient mass production of HDI boards.
 - Cost savings at volume. & Allows advanced testing and yield tracking.
- **Cons**
 - More complex panel design. & Higher risk if not aligned properly.
 - Specialized fabrication needed (higher cost per panel).

PANELIZATION STRATEGIES

Mixed Technology Panels

Mixed technology panels combine different PCB designs (or technologies) into one manufacturing panel.

Example: A panel may include standard FR-4 boards, HDI boards, and flex-rigid boards together.

Why It's Used

- **Cost Optimization** → share tooling and setup costs across multiple designs.
- **Material Utilization** → fill unused panel space with smaller PCBs.
- **Prototyping Efficiency** → test multiple related designs in one run.
- **Product Families** → panelize variations of the same design together.

Key Considerations

- **Thickness Matching**
 - Boards in the same panel should have similar thickness for uniform assembly.
- **Material Compatibility**
 - Avoid mixing boards with very different materials (e.g., FR-4 vs ceramic) unless the fab supports it.
- **Process Optimization**
 - Group designs that use the same surface finish, solder mask, and copper weight.
- **Quality Segregation**
 - If boards require different test criteria (e.g., RF vs power), keep test access organized.
- **Depaneling Method**
 - Choose a separation method (V-score, tab routing, laser) that works for all designs in the panel.

Pros & Cons

- **Pros**
 - Lower fabrication costs.
 - Better material utilization.
 - Faster prototyping and parallel development.
- **Cons**
 - More complex panel planning.
 - Risk of yield loss if one design fails quality checks.
 - Limited flexibility if boards need very different processes.

PCB OUTPUT PREPARATION

Preparing manufacturing (MFG) output is the final step before PCB production, where all design data is translated into industry-accepted formats for fabrication, assembly, and testing. A well-prepared output package ensures accurate builds, reduced errors, faster turnaround, and compliance with customer requirements.

Typical Deliverables in MFG Output Package

A. Fabrication Outputs (PCB Bare Board)

1. Gerber/ODB++ Files

- Layer artwork for copper, silkscreen, solder mask, paste, mechanical outlines.
- Must comply with RS-274X Gerber standard or ODB++ unified database.

2. Drill Files (NC Drill/Excellon)

- Plated and non-plated hole definitions.
- Tool sizes, drill maps, and tolerance notes.

3. Board Stack-Up & Materials

- Layer sequence, dielectric thickness, copper weights.
- Controlled impedance requirements with target values.

4. Fabrication Drawing

- Board outline, dimensions, tolerances, hole table, reference designators.
- Special notes: impedance control, controlled depth, back-drilling, etc.

5. Netlist File (IPC-D-356):

Electrical connectivity for netlist verification during bare board testing.

6. Panelization Files (if required):

Breakaway tabs, V-scoring, fiducials, tooling holes.

Sample FAB Notes

NOTES:

1. FABRICATE PER IPC-6012A TYPE 2 CLASS 2
2. MATERIAL:
DIELECTRIC: FR4 PER IPC-4101 MINIMUM Tg 130C
COPPER: AS PER LAYER STACKUP DETAILS
UL RATING: 94V-0 MINIMUM
3. PRINTED WIRING BOARD SHALL COMPLY WITH REQUIREMENTS OF ANSI/J-STD-003.
TEST A SECTION 4.2.1 WITH NO EVIDENCE OF MEASLING OR DELAMINATION.
4. SURFACE FINISH: ELECTROLESS NI/IMMERSION Au
5. SOLDER MASK MATERIAL SHALL MEET ALL THE REQUIREMENTS OF
IPC-SM-840C. SHALL BE GREEN IN COLOR AND APPLIED OVER BARE COPPER
(S.M.O.B.C.). MAXIMUM THICKNESS TO BE 0.004 FOR THRU-HOLE
TECHNOLOGY AND 0.002 FOR SURFACE MOUNT OR MIXED TECHNOLOGY. ALL
EXPOSED AREAS TO BE THE SELECTED SURFACE FINISH PER NOTE 4 AND
MEET THE SOLDERABILITY ACCEPTANCE OF J-STD-003 CATALOGY 2.
6. SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING WHITE
NON-CONDUCTIVE EPOXY INK.
7. 100% CONTINUITY TESTING USING DATABASE NETLIST SHALL BE PERFORMED
VENDOR TO IDENTIFY TEST PASSED (primary/secondary) SIDE.
8. VENDOR TO MARK DATE CODE AND LOGO IN ETCH OR IN LEGEND
9. THIS PRINTED WIRING BOARD IS DESIGNED WITH A MINIMUM CONDUCTOR
WIDTH AND SPACING OF 0.004 and 0.004 (0.101 mm & 0.101 mm). THE MINIMUM
FINISHED CONDUCTOR WIDTH SHALL BE 0.004(0.101 mm) +/-10%.
10. BOW AND TWIST SHALL NOT EXCEED 0.180mm (0.007in) PER INCH, AS MEASURED
PER IPC-TM-650

PCB OUTPUT PREPARATION

B. Assembly Outputs (PCB Assembly – PCBA)

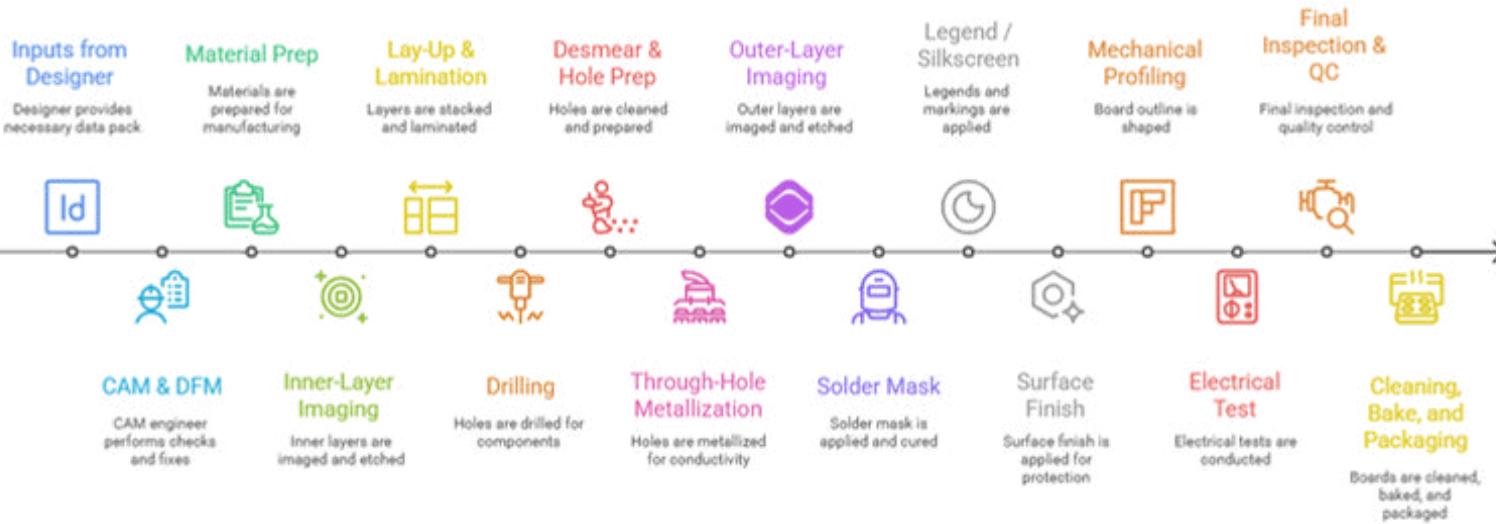
1. **Bill of Materials (BOM):** Component reference, MFG part number, quantity, package type, and Alternate sourcing options, lifecycle status, and RoHS compliance.
2. **Pick and Place (XY Data / CPL File):** Exact component centroid coordinates, rotation, and placement side.
3. **Assembly Drawing:** Mechanical outline, polarity markings, special instructions, and Labels for hand-soldered or non-standard placements.
4. **Solder Paste Stencil Files:** Gerber data for stencil cutting (aperture reduction/expansion included).
5. **Assembly Notes:** Solder type (SnPb/RoHS), reflow profile, conformal coating, cleaning, etc.

C. Testing & Quality Outputs

1. Test Point Report
 - a. Defined access for ICT (In-Circuit Test) or flying probe.
 - b. Coverage summary and testability notes.
2. DFT/DFM Reports
 - a. Verification logs from design rule checks for fabrication & assembly readiness.
3. X-Ray/Optical Inspection Guides (optional)
 - a. For BGAs and hidden-joint packages.
4. Programming & Test Files (if applicable)
 - a. Firmware load, boundary scan (JTAG), and test scripts.

DFM

PCB Fabrication Process



01. Inputs from Designer (Data Pack)

- Gerbers / ODB++, NC drill (PTH/NPTH), netlist (IPC-356)
- Fab drawing (board outline, stackup, tolerances, finishes)
- Impedance targets & coupon specs, panelization/quantity, accepted DRC limits

02. CAM & DFM

- CAM engineer runs DFM checks, fixes apertures, merges layers, adds tooling holes, fiducials, coupons, and final panel layout.
- Confirms stackup (prepreg/core thickness, copper weight) to hit impedance.

03. Material Prep

- Pull laminates (cores), preps, copper foil per stackup.
- Cleaning/Brushing of copper to ensure photoresist adhesion.

04. Inner-Layer Imaging (Multilayer boards)

- Photoresist coat → Expose (film or LDI) → Develop inner layers.
- Etch away unwanted copper → Strip resist.
- AOI (Automated Optical Inspection) for shorts/opens.
- Oxide/oxide-alternative treatment to promote lamination bond.

05. Lay-Up & Lamination (Build the multilayer)

- Stack inner layers with prepreg and copper foils top/bottom.
- Vacuum press cures resin → forms a single laminated panel.
- Controls: registration pins, pressure/temperature/time profile.

HDI note: HDI uses sequential lamination cycles (laminate → laser drill → copper fill → re-laminate) to build stacked microvias.

DFM

06. Drilling

- Mechanical drilling for PTH and tooling holes.
- Laser drilling for microvias (HDI) and fine features.
- Depth/controlled depth where needed.

07. Desmear & Hole Prep

- Plasma/permanganate desmear to remove resin smear from hole walls.
- Micro-etch for better copper adhesion.

08. Through-Hole Metallization

- Electroless copper (seed layer) coats hole walls.
- Electrolytic copper plating increases copper thickness in holes and on outer surfaces.

09. Outer-Layer Imaging

Two common flows:

- **Pattern-plate flow:** Resist → Image **tracks & pads** → Plate copper (and tin) in exposed areas → **Strip resist** → Etch base copper using tin as etch resist → **Strip tin**.
- **Panel-plate + etch flow:** Panel plate to target copper, then image and etch.

AOI (outer layers) after etch to catch shorts/opens.

10. Solder Mask

- **Clean & tack-dry, apply LPI solder mask, expose** (open pads), develop, final cure.
- Check **mask dams** and **registration**.

Rigid-flex note: Flex areas use overlay films instead of solder mask; overlay is laminated and laser-opened.

11. Legend / Silkscreen

Apply **component reference text, polarity marks, logos** (ink or LDI legend). Cure.

12. Surface Finish (Protect pads & aid soldering)

- **HASL/HASL-LF, ENIG, Immersion Silver/Tin, OSP, Hard Gold** (edge connectors).
- Thickness measured; verify solderability.

DFM

13. Mechanical Profiling (Board Outline)

- Routing (CNC), V-scoring, tab-route / mouse-bites, or laser (for flex/HDI).
- Deburr, edge cleanup.

14. Electrical Test

- Flying-probe (proto) or bed-of-nails (volume) for continuity & isolation vs netlist.
- Record yield & failures.

15. Final Inspection & QC

- Dimensional checks, hole sizes, finish thickness, solder mask registration.
- Microsection cross-sections for plating & laminate quality.
- X-ray for via-fill (HDI) when applicable.
- Cleanliness/Ionic contamination test; visual to IPC-A-600 class.

16. Cleaning, Bake, and Packaging

- Final wash (if required), bake to reduce moisture.
- Vacuum/ESD bags, desiccant, humidity card, COC & test reports.
- Ship panels or depopulated boards per PO.

Variant Notes (Quick)

- **HDI:** Sequential lam, laser microvias, via-fill & planarization, stricter registration.
- **Rigid-Flex:** Overlay, stiffeners, laser cutting, custom carriers for assembly.
- **Metal-Core (MCPCB):** Special drilling/routing; thermal dielectric controls.
- **Impedance-Controlled:** Build includes coupons; TDR verification.

PCB Design Guide

THANK
YOU

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