SEMESTER-1

AY 2021-22

PREFACE

Placements, for some, it's the one single thing that matters, for others it's just another piece of the college puzzle that shapes our future. Without a doubt, it is a life-changing event or process in a student's college life. Undoubtedly, one of the key factors that contribute to it is guidance from seniors. We have decided to streamline the process a little, so you can focus more on the actual preparation. We hope that you find the PU Chronicles helpful in the same.

Some general tips for placements:

- Think and plan well in advance about the career path you want to pursue.
- Have a clear understanding of what is being expected in the interviews by the sector and then also get an idea about the previous years company-specific details using this book.
- Ensure you understand the rules and choose the companies you appear for wisely.
- Keep your motivation levels and energy high through all the ups and downs. Your enthusiasm plays a key role in the interviews
- Get in touch with alumni and seniors for advice and mentorship, these are people who have been in the same situation before and can give you great advice and support.
- Stay in touch and cooperate with the PU Team, they are there to help you throughout the placement season

A word of caution. Placements is an extremely volatile area and changes based on a number of factors such as market conditions, recruiter relationships and business constraints. Please read through the document with the awareness that the trend for a certain year may not be the trend for the next year. For instance, a stream that did not do well in a particular year may well be the best placed in the following year. The rounds and processes conducted by a company in the previous semester may very well differ this semester.

Hence, be the best you, rest will follow!
And rest assured that the Placement Unit is always there for you!

All the Best,
The PU Team

DISCLAIMER

All the feedback is provided by the students who have secured jobs in various organizations. We have tried our best to ensure that every detail in the PU Chronicles (the "Service") is correct.

The Placement Unit assumes no responsibility for errors or omissions in the contents of the Service.

The Placement Unit reserves the right to make additions, deletions, or modifications to the contents of the Service at any time without prior notice.

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Aditya Birla Science and Technology

Mumbai

Chemical

Research and development

Compensation Offered (CTC) : 5.50 LPA

CGPA: 9.05

Recruitment Procedure

Round 1: Technical presentation:
Speak about your background and your qualifications;
A brief overview about internships and thesis/dissertation topics and counter questions regarding the same;

Round 2: HR interview: Questions about soft skills and future plans; Why choose the company and why they should hire you;

Important Topics and Subtopics to Remember

Your thesis/dissertation topics, should know about it in depth and also topics related to it and about your practice schools.

Sources of Preparation

I referred to my thesis topics literature

Additional comments

Should be confident and brave enough to say I don't know rather than move around the question

Aequs

Belgaum

Mechanical/Design

Compensation Offered (CTC) : 6.50 LPA

Postgraduate engineering trainee

CGPA: 9.13

Recruitment Procedure

Round 1: Test
In this round they conduct a test which includes aptitude and technical questions. Test is not that difficult. Test duration is 60min
Round 2: Technical and HR interview
In my second round, a total of 3 members were in the panel. Two of them are from the technical side and one from the HR side. HR said that they are hiring for a new product development role. So my first question is how you Mechanically design a pressure cooker. I explained it by using the pressure vessel concept. They said how we calculate the thickness, diameter etc. Other questions are related to product design like product development stages. Design for manufacturing and design for assembly etc they asked. HR question is like is it ok to relocate like that...

Important Topics and Subtopics to Remember

Strength of materials, product design and development

Sources of Preparation

Gate notes for SOM, Class notes for product design and development

Aerospace Processing India Pvt Ltd

Belagavi

Chemical

Compensation Offered (CTC) : 6.5 LPA

PGET

CGPA: 8.5

Recruitment Procedure

Round 1: Aptitude and Core MCQ questions

Round 2: Technical Interview
The interview began with the interviewer asking me to introduce myself. A few questions were asked on my thesis and the projects and internships that I had done previously. Few questions on surface treatment were asked. They even asked me to explain any one of the surface treatment processes that I know. Few basic questions on Reaction Engineering and Thermodynamics like first law, second law and zeroth law. By the end of the interview, they asked me if I wanted to work in R&D or Manufacturing.

Round 3: HR Interview
Asked me to introduce myself and asked me if I'm willing to relocate to Belagavi. Basic HR questions like strengths and weaknesses were asked. They asked me about the lowest point of my life and asked me how I overcame it.

Important Topics and Subtopics to Remember

Thermodynamics
Reaction Engineering
Mass and Heat Transfer

Sources of Preparation

IndiaBix for Aptitude
GATE tutor for Core

Additional comments

The art of staying calm. Eventually we will all end up at the place that is destined to be ours. If something doesn't click, then remember that there's something bigger waiting.

Addverb Technologies Pvt Ltd

Noida

IT

Compensation Offered (CTC) : 14 LPA

Graduate Engineer Trainee (Software)

CGPA: 9.14

Recruitment Procedure

There were 4 rounds. All interviewers gave some time at the end to ask about them/their work/the company.

Round 1: Technical Interview
Very basic DSA questions were asked, things like "how to reverse a string?, explain at least 2 ways to do it, then compare the methods".

Round 2: Technical Interview
Questions mostly based on the resume. Explaining what projects/internships I had worked on.

Round 3: Technical Interview
Questions mostly based on the resume. Explaining what projects/internships I had worked on. Some hypothetical questions related to some projects that I had done.

Round 4: HR + some technical
Interviewer started off by asking things like "Why Addverb?", "Why not start your own, given that your college has many startups?". Then he asked me to tell the subjects that I liked the most and disliked the most from college and why. Then he asked to tell one subject that I studied with the greatest interest and asked some questions based on that. Then finally he asked me to pick out one of the courses that I had mentioned on my resume and asked some questions based on that as well.

Important Topics and Subtopics to Remember

DSA, Computer Networks, OS, DBMS

Sources of Preparation

DSA: Practice questions on InterviewBit, Leetcode etc
College notes suffice for other subjects.

Additional comments

Be sure you really know the projects and courses that you put up on your resume

Amazon

Bangalore, Hyderabad, Chennai, Delhi, Pune, Mumbai

IT

Compensation Offered (CTC) : 18.60 LPA

SDE

CGPA: 8.56

Recruitment Procedure

Round 1: Coding round
This round consisted of 4 sections: Debugging, coding, values and aptitude

1. Debugging: This round was very straightforward. A problem statement was given explaining what the program was expected to do along with a sample input and output and the erroneous output. It was expected to make a small change in the code to match the expected output (for example, the code for bubble sort was given and the code printed out the numbers in decreasing order. It was expected to print out the numbers in increasing order. Simply changing the comparison operator from < to > or vice versa would fix the problem). All the problems in this section required very small changes to the code to fix it and no complex debugging was required.
2. Coding round: This round was 70 mins. It had 2 coding questions, both of which were easy.
a. https://leetcode.com/problems/maximum-units-on-a-truck/
b. https://www.geeksforgeeks.org/sliding-window-maximum-maximum-of-all-subarrays-of-size-k/
3. Values round: This round is primarily based on Amazon's leadership principles. Do not skip this round or take it lightly (those who did really well in all the other rounds but didn't take this seriously were not shortlisted)
https://www.amazon.jobs/en/principles
Some of the questions here were rather confusing. Often, when a choice was presented between A and B, both seemed applicable as they weren't mutually exclusive. Answering honestly (the first answer that strikes you when you see the question is a good rule of thumb) in adherence with the leadership principles is the best course of action.
4. Aptitude round: This was a simple aptitude round. Nothing particularly complicated and no special preparation required

Round 2: Technical interview 1
The interviewer just asked me my name and directly jumped into the questions. This round consisted of 2 questions. (All interviews are about an hour long)

1. You are given a number n. There are nodes numbered 0 to n-1 in the graph. You are given an array of left child and right child each of size n. The value at each index represents the corresponding node which is the left or right child. For example, for the following graph
0
/ \
1 2
leftChild=[1,-1,-1], rightChild=[2,-1,-1]. Check if the given graph forms a tree.

Solution: First find the root. For this, check which number from 0 to n-1 never occurs in the left and right child and this will be the root. Run cycle detection and connected components on the graph.

2. Given a linked list, check if it is a palindrome (O(1) space)

Solution: Use slow and fast pointers to find the midpoint of the list. Then reverse the right half of the list from the midpoint. Then traverse the reversed right half and the left half of the list and check if they have the same elements.

Round 3: Technical interview 2
The interviewer asked me for my introduction and he introduced himself, then proceeded with the technical questions. This round also consisted of 2 questions.

1. Given a running array where elements keep coming in, find the max product of 3 elements in the array. For example, if the array is [1, 2, 3, 4, -5, -6], expected output: [6(2*3*1), 24(4*3*2), 24(4*3*2), 120 (4*-5*-6)]

Solution: Keep track of the largest 3 elements and smallest 2 elements in the array(for negative numbers). Check at every element if any of these change and change accordingly and find max product.

2. Given a tree, return all root to leaf paths
(https://www.geeksforgeeks.org/given-a-binary-tree-print-all-root-to-leaf-paths/)

Solution: Simple dfs.

After these questions were over, we had quite a lot of time, so we discussed my internship project for about 20 minutes.

Round 4: Technical interview 3
The interviewer asked me for my name and introduction and then he introduced himself as well. Then he asked me to pick a project of my choice from my resume. We then had a detailed 30 minute discussion about the project I had worked on at my summer internship including multiple use cases, how the application was made scalable etc. So it is important to be very familiar with the projects on your resume and have a deep understanding of why certain decisions were made and so on. He was also able to ask me certain HR oriented questions such as when I took some initiative or when I had to take a risk and what the result was. Amazon recommends the STAR methodology to answer these questions (situation you were in, task you were expected to perform, action you took and the result). I answered following this guideline. Then we jumped into the technical questions. He asked me to explain the difference between an array and a linkedlist and then asked a DSA problem on each of them.

1. Given 2 arrays check if they have the same elements in any order

Solution: Use a hashmap to keep count of the frequency and check (or sort and go elementwise)

2. Given a linked list, move all prime numbers to the head of the list. This should be done in place and assume the function isPrime(int x) is implemented for you.

Solution: Simply keep track of the first composite and the last prime number. If the number encountered is a prime, change the links accordingly.

He then asked me how the code would change if even numbers had to move to the front of the list and I explained how this code can work for moving any number(s) satisfying a particular condition to the head of the list. He then told me that this function was going to be exposed as an API and multiple customers would use it and new functions would have to be added as and when we need and asked how the application would be made scalable for this. I told him that we can have some form of database (or a hashmap) which maps a choice index of the function we want to call (prime or even or any function that returns T/F) to the actual function call (or API call) of that condition. And we can use a microservice to add entries into the database (or Hashmap) dynamically without taking down the system from production or changing any existing code.
He then asked if I had any questions for him and I asked him about the ML opportunities available at amazon. He told me about it and the interviews were over.

Important Topics and Subtopics to Remember

Primary topics: DSA (Most important), OOP
Secondary topics: DBMS, OS, CN
Tertiary topics: System design

Sources of Preparation

GeeksForGeeks, LeetCode, InterviewBit, Gaurav Sen system design (youtube), Placement Unit Prep material
All the other courses I had done as CDCs on campus.

Amazon archive leetcode: https://leetcode.com/list/5pg5vqgc/
Amazon interview experiences GFG: https://www.geeksforgeeks.org/tag/amazon/

Additional comments

Amazon's questions were focused less on memorization and more on application. There was not a single point in the interview where I had to actively remember something, be it an algorithm or some theoretical point from any CDC. For this reason, it is more important to focus more on DSA.
Be very confident of all the skills and projects you mention in your resume; if you are not confident about explaining something, don't include it as it is fair game to be questioned extensively on anything

mentioned there. But make sure you have at least one really good project (SOP, internship, personal, etc) on you resume that you can talk at length about (at least 30 minutes of discussion)
Do give mock interviews with peers or seniors if possible before (but not too close to) the final interview. This will give you a good idea of what you should work on and where you struggle the most. You should also practice writing code by hand as interviews might not be virtual
Practice explaining your solution as you go along (with a peer if necessary). It is difficult for the interviewer to evaluate you if they don't understand your thought process. If you get stuck on a problem and don't know how to solve it, don't panic. Try to talk to the interviewer and think through it. Most often, they will give you hints if you are stuck as well. For other general tips on coding interviews, watch this channel on youtube - clément mihailescu
Amazon really values their leadership principles. Any answers that you provide around this or quoting their leadership principles are certain to fetch brownie points. Prepare certain questions in advance such as "give an instance where you did well", "give an instance where you failed or had to take a risk and it didn't work", "give an instance where you had a difference of opinion", etc.
Spend time working on your intro highlighting your strengths (from the job description), past work experience, personal connect with the company and a desire to work there(optional but good - I told them I use alexa, prime video, aws, etc) and finally, what you can bring to the table and why you would be a good fit there. Your introduction can have a massively positive impact on the interviewer if you do it right, so do not take this point lightly.
Present yourself well and be confident. The questions asked aren't as difficult as a lot of other companies and if you have practiced enough, you can certainly do great. All the best!

Amazon

Hyderabad/Bangalore

IT

Compensation Offered (CTC) : 31.50 LPA

SDE

CGPA: 8.5

Recruitment Procedure

Round 0: Coding round
There are 4 sections for Amazon's coding round:
a. Debugging
b. Problem Solving
c. HR questions
d. Logical reasoning

In sections a. and b. you could choose your preferred programming language. The debugging section is essentially basic code snippets, similar to CP course labs. To save time, you can just read the question and code it yourself instead of debugging the code given. There's more than sufficient time for this section.

Section b. has 70 minutes, has standard LeetCode questions, I finished this section in under 20 minutes, just to give you an idea of how simple it was.
The questions were as follows:
1. Minimum sliding window.
Solution: Employ the same logic as of maximum sliding window, just change the comparator.
2. A simple sorting based question.

Section c. has generic HR based questions, its fairly obvious what they are looking for as answers.
The questions give a statement and ask for your scale of agreement or disagreement.
For instance:
In difficult situations I do not give up hope.
From 0 to 5 rate your agreement or disagreement to this statement. 0 being completely disagree, 5 being completely agree.
Very clearly they are looking for 5 as the answer, even if you think you hover around 3 or 4, put 5.

Tip to solve this section: Try to pick either of the extremes or at most 1 or 4, avoid 2 and 3 completely, this shows that you are decisive, imo. This is the section which I think is sorta the filter, cause the other three sections are fairly easy for everyone.

Section d. has easy logical reasoning problems, more than sufficient time, so do not hurry, you have to follow the ordering of questions.

Round 1:
Interview (technical)
2 DSA questions

a. Edit Distance
b. Minimum cost with a curved edge.

I was able to answer both the questions in the timeframe given.
Amazon has HR type questions in technical interviews as well. So answer those very clearly too. Converse with the interviewer about the work they are doing in the company, if they find it interesting, why did they shift to that particular company, if they have, then why. There are multiple questions you can think of, I don't know if this shows anything to the interviewer or not, but I would like to know their reasons behind joining the company I am planning to

Round 2:
A half-an-hour discussion on my projects and my internship at Walmart.
2 DSA questions
(All the interviews are always strictly one hour for Amazon, no more time is allotted to you, so keep that in mind)
1. A basic stack question, finished in 10-15 minutes.
2. Merge k sorted arrays of size n each, we discussed 4 approaches, calculating time and space complexity as we went along. Coded the merge-ing approach.

Asked my questions about the interviewer's work at Amazon.

Round 3:
This was an HR round, sorta, we talked a lot about my and the interviewer's industry experiences. He was a BITSian, so there were a lot of things to discuss. This was the last part of the interview, which took about 30 minutes.
Initial part was a simple DSA question and questions pertaining to my projects.
DSA q: find number of ways from (0,0)to (n,n).

Important Topics and Subtopics to Remember

DSA
A lot of people include OOP, OS etc.
I don't agree.
These subjects are rarely asked, the source to prepare them is GFG last-minute-notes and Most-Frequently-Asked questions.
The above thing for OOP, OS ,DBS,CN takes less than 5 days.
Using the course-work we have is a complete overkill for any interview for these subjects, please don't spend time doing that.

Sources of Preparation

OOP, OS, DBMS, CN -: GFG Last minute Notes, Most Frequently Asked questions, InterviewBit also has articles for all of them, good source.

DSA-: InterviewBit and LeetCode, InterviewBit is far better when you are starting, since it has a timer for each question and hence in at least some way ensures you are not wasting time on one question too much. Though I did both, please do both.

Additional comments

If you have a summer internship, start preparing as soon as you can. I started fiddling from January, starting properly in March. I had a lot of things to do along with my internship, I worked under a college prof as well so I had practically no time left for DSA then.
Regardless of you getting a PPO or not, just start asap. You will be at a huge disadvantage if you have a summer internship and are not a big fan of competitive coding and then you do not get a PPO or refuse to take it.

People who do not have a summer internship, do not worry, prep DSA and you are good to go.

You can contact me for any help you need.

PS: The interview process is luck based to a considerable extent for all the companies. Please try not to take any rejection to your heart, this will affect your performance negatively in upcoming interviews/coding rounds. I know this is easier said than done, but I think it's better if someone puts it out there in writing.

AMD-Xilinx

Hyderabad

Electronics

Compensation Offered (CTC) : 21 LPA

Silicon Design Engineer 1

CGPA: 8.27

Recruitment Procedure

Round 0: Online test followed by Resume Shortlisting
Test consisted of three parts: Aptitude, Digital and Analog. Aptitude was based on mental ability questions, some class 10 Maths problems (like finding the area of a part and AP GP questions), basic simple interest, Work time people problem, bar graph and finding the logic using information in square boxes. Analog section had questions on finding the gain of the circuit, RC Circuit, Vo at some random point in a single ended differential amplifier, OpAmp based negative feedback Passive component questions, a question on diodes attached along with RC circuit and finding how the output graph will be, a question on rectifier with RC filter was asked, output impedance of current mirror. In Digital, questions were asked on Static Timing Analysis (like max frequency calculation), a Verilog code was given and asked what the Digital Component being designed is, a question on Race Around Question (this is an important one as it was asked in many companies' Online test process), CompArch based questions on Hit rates, Basic NAND Gates based DD logic question, a common question from GATE on Modulo N circuit.

36 people from all 3 campuses were shortlisted for the next round of HW interviews.

Round 1: Technical Interview
Interview had a pleasant start, the interviewer was happy with my resume and started asking questions on my resume. He asked me to introduce myself and then we had a general chat on COVID situations, college Life and about what Xilinx works on. He then proceeded on to industry level questions if I knew about LVT test in Synthesis of Circuits, to which I assumed it to be Low Voltage Threshold test required in Digital Design and explained to him why LVT test is important based on my understanding, which he agreed to. The interviewer asked me question on difference between latch and flip flop, to explain how an SR Latch functions, he asked me very basic questions on Verilog like what is blocking and non-blocking assignment, asked me if I knew about dynamic power consumption and techniques to reduce it, asked me to explain setup time and hold time and asked me a question based on it. The 1st round ended with us discussing opportunities in Xilinx.

18 people out of 36 were then shortlisted to the 2nd round.

Round 2: HR + Technical Interview

The panel of interviewers comprised 3 people, one from Analog background, one from Digital and one from HR. Interviewer started by asking me what were your past experiences in electronics and do you hold any PoRs like TAships and I described the same based on my resume. The interviewer asked me questions on Cadence Virtuoso Operations like plotting output gain and regions of operation, then he asked me to describe the difference between differential input single ended vs differential output

amplifier, he asked me what are the parameters on which Slew rate of a D2S amplifier is dependent and then follow-up questions on it by asking me if I increase Load capacitance and keep the slew rate same, then how will the whole circuit get affected, one is if slew rate is kept constant, then as Slew Rate is Iss/CL, so we will have to increase current and if we increase current then, we will have to increase overdrive voltage, which reduces the Output Voltage Swing. The Analog interviewer also asked me if I knew the internal structure of SRAM Memory and ended the Analog part of the 2nd interview round. In digital, the interviewer asked me the difference between Mealy and Moore circuits, I explained the basic difference but the interviewer wanted me to explain it based on industry design, so I responded that output changes after one clock cycle in Moore circuit while Mealy circuits respond in the same clock cycle and they don't need to wait for the clock. The interviewer was satisfied with this answer, he then proceeded with how would you design an f/2 circuit and 2*f circuit (both of them using digital components). The first one is simple, by using D flip flop, the 2*The circuit was basic but a bit new to me. A 2*f circuit is designed by giving the input A to XOR gate and input B is of the XOR is Vin passed through an inverter (which has a delay of 1/4th of clock period) and the XORed output is 2*f circuit. After these questions, the HR part of the interview occurred in which she asked me to tell me about my background (family and resume based) and she ended the interview with a witty question - "Describe yourself in one word".

5 people were finally shortlisted for the Full time role.

PS: If you guys have time, try to do a project in Digital Electronics which is based on Verilog HDL as most of the interviewers check for a digital project.

All the best !!

Important Topics and Subtopics to Remember

Computer Architecture (Pipelining, Pipelining Hazards, Cache Mapping, Hit Miss, SRAM, DRAM), Verilog (Pattern detector and all other digital components), Static Timing Analysis, ADVD (Designing Different Gates using CMOS circuits), Analog Electronics (Opamp Positive and negative feedback), Microelectronics (Feedback, stability, Frequency Response and basic gain finding).

Sources of Preparation

https://www.youtube.com/playlist?list=PL5Q2soXY2Zi_FRrloMa2fUYWPGiZUBQo2 (Onur Mutlu Lectures on CompArch)

http://www.asic.co.in/DesignGuidlinesRTLcoding.htm (Verilog RTL Design guidelines)

http://www.asic.co.in/Index_files/verilogexamples.htm#link14 (basic Verilog Codes)

https://www.chipverify.com/verilog/verilog-pattern-detector (Verilog Pattern Detector)

http://www.vlsi-expert.com/2011/04/static-timing-analysis-sta-basic-part3a.html (Static Timing Analysis)

https://www.youtube.com/watch?v=amu-wEGgE8s (Dynamic Power Consumption)

https://www.youtube.com/watch?v=Ee_OHwVJ344 (CMOS Buffer)

https://www.youtube.com/watch?v=ULDFB4J04fc (FIFO Depth calculation)

https://www.youtube.com/watch?v=2V41i4xVTZ8 (Metastability)

https://www.youtube.com/watch?v=yVNrBDF20uY&list=PL6qRG5-NfbLvagdQOwShX9FMrzb5hSvrq (Chembiyan Sir's Video lectures on Passive components, do this only if you are done with DD and CompArch)

Additional comments

Guys, if you are aiming for a core job, do note that only one company comes for Analog role (which is Texas Instruments) and other companies hire for digital roles. Noting this point, do put maximum effort in Digital compared to Analog.

ANAND Group

Pune

Mechanical/Design

Compensation Offered (CTC) : 6.5 LPA

GET-1

CGPA: 6.05

Recruitment Procedure

Round 1: Written test : It was a MCQ test and it was easy comparatively
Round 2: GD : Were told to talk about Apple vs Samsung
Round 3: Technical and HR interview : Both Technical and HR interview were conducted at the same time. The interview for me was mainly based on supply chain as I had put a lot of emphasis on the topic in my resume. I was able to steer the interview towards that direction and was successful in it. The overall experience was good

Important Topics and Subtopics to Remember

Topics mainly related to the projects which you have put a lot of emphasis on your resume

Sources of Preparation

Course materials for supply chain management which is a DEL and also from Coursera website

Additional comments

From BITS as a whole, 3 from BE were selected and 6 from ME. In BE only I was from Goa, and 2 were from Hyderabad

BIOCON Biologics

Chemical

Senior Executive (Production)

Bengaluru

Compensation Offered (CTC) : 7 LPA

CGPA: 9.2

Recruitment Procedure

Round 1: Resume Shortlisting
There were only two rounds and the first one was Resume shortlisting which was based on the projects that I have worked on and the right skills which seemed to fit the role offered.

Round 2: Technical and HR
The interviewers introduced themselves and they asked me to introduce myself.Once that was done they asked me about the projects that I had worked on.As my work majorly focused on fluid operations and reaction engineering the questions were based on that.

Technical Questions

Question 1 : How would you define Reynolds number and what type of flow do you come across in a micro channel?

Answer: Reynolds number is usually very less in case of micro channels as diameter is very small.

Question 2 : When would you use a CSTR and in which cases do u go for a PFR

Answer: CSTR are used in liquid phase reactions and PFR are used for gas phase reactions

Question 3 : Explain the reason for the same

Answer : Gas phase reactions do not require mixing as reactions are instantaneous.

Question 4 : What do you know about cavitation in pumps and Net Positive Suction Head?

Answer: Cavitation occurs when the pressure at the suction top is equal to the vapor pressure
NPSH is used in designing pipe systems to avoid cavitation which is given by their difference where different losses are taken into consideration.

HR Questions
1. A brief introduction about myself
2. As I had mentioned about working out we started having a discussion about it.
3.He asked me what are your interests and a few qualities that people have observed from me
4. Then he asked me if I would be fine with working with shifts and manufacturing as I was working on my thesis.

That was it. Overall the interview was very smooth and it lasted around 30-40 min

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Important Topics and Subtopics to Remember

As all my questions were based on how my introduction was, it's best if you tell them things and subjects that you feel confident about .

Topics are usually Heat, Mass ,Fluid and Design
Additionally if you have mentioned MATLAB ASPEN or COMSOL on your resume you must be ready to face some tough questions.

Sources of Preparation

CRE by Octave levenspiel is something that I went through the day before the interview as I was expecting my questions from reaction engineering.

Cisco Systems India Private Limited Bangalore

IT

Compensation Offered (CTC): 21 LPA

SDE

CGPA: 8.3

Recruitment Procedure

Good overall experience. 4 rounds of interviews

Round 1:
Technical round
Discussion on the projects completed in my internships and college
DSA, OOP, Databases, Networks, and other CS topics-related questions

Round 2
Technical + Behavioral
Discussion on the projects completed in my internships and college
DSA, OOP, Databases, Networks, and other CS topics-related questions
Behavioral aspects - what would you do in such a scenario, examples of your decision making, etc

Round 3:
Technical + Behavioral
Discussion on the projects completed in my internships and college
DSA, OOP, Databases, Networks, and other CS topics-related questions
Storage of shared info - repository vs a simple HTML page, etc

Round 4:
HR
Generic HR questions, location preference

Important Topics and Subtopics to Remember

DSA, OOP, Databases, Networks, OS

Sources of Preparation

Multiple - geeks for geeks, college material, online courses, etc

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Additional comments

Be confident; think and answer to the best of your knowledge

CISCO Systems India Pvt. Ltd

Bangalore

IT

Compensation Offered (CTC) : 23 LPA

Software Engineer

CGPA: 8.38

Recruitment Procedure

Round 1: Technical Interview
Interviewer asked several questions related to Computer Networks, DSA, OS and DBMS. Few are listed below.

- Explain the different OSI layers.
- TCP vs UDP
- Cryptography and its types.
- Deadlocks
- Mutex
- Two basic binary tree questions
- Some SQL queries

Round 2: Technical + Managerial Interview
The interviewer asked about my previous internship, the project I worked on, and the tools used. She also asked how this project would affect the organization and whether I would take a PPO from the organization. Then she asked in detail about different projects that I had worked on. This round also included several managerial questions.

Round 3: Technical + Managerial interview
In this round, the interviewer focused on conceptual OSI layer questions and how to implement a particular model/protocol. He also asked a few questions regarding C program workings and DBMS. Asked me to explain one of my projects in detail. He asked about my likes/hobbies and future goals.

Round 4: HR Round
This round included an introduction, place preferences, and a few questions like why cisco, etc.

Important Topics and Subtopics to Remember

Computer Networks, OS, DSA, DBMS

Sources of Preparation

Geeksforgeeks, InterviewBit, Leetcode, Lecture Slides

CISCO Systems India Pvt Ltd.

Bengaluru

IT

Compensation Offered (CTC) : 24 LPA

SDE

CGPA: 7.39

Recruitment Procedure

Round 0: Online Test
It had 2 coding questions and about 30 objective questions from other topics in CS (Networks, DBMS etc.)

Round 1: Data Structures/Networks:
I was asked what data structures I would use in different scenarios of data storage (data about the customer usage of say Cisco Webex) (Basically hashmaps and hash queues). I was asked based on what property of data I would hash the data points for the easiest and quickest access. They asked me how scalable it would be to use this design for a larger database (100k+ users).

I was also asked questions on Network layers; what are the basic layers in the OSI model. I was also asked if I had to make sure certain websites are more/less easily accessible, what layer would I implement the filter on.

Round 2: Coding/problem solving:
Was again asked what data structure would best store a large amount of data such that it is quickly searchable (hashing).

They asked me for an algo to sort unsorted data and its complexity. I told quick sort, and was asked to write the pseudo code and later the c code for it.

They asked me very briefly about the subjects I had studied.

Round 3: Problem solving/projects:
They asked some basic questions about searching in trees and graphs.

This round was more focused on my projects. I was asked about 2 of my projects (basic outline) and how I contributed (one was a group project). I was asked to explain some of the things in depth, mostly to ask

if I had understood the project myself. You'll do good to revise your previous projects.

Round 4: HR Round
I was asked basic HR round questions like conflict management etc. They asked me if I had any questions with the role, and about my interviewing experience.

Important Topics and Subtopics to Remember

DSA: maps, trees and graphs were asked more than other sub topics
Networks: Cisco is a networking company predominantly so this matters to them
OOP, DBMS, OS: Wasn't asked explicitly, but was part of questions here and there

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Sources of Preparation

InterviewBit: Finished all topics. It's not a very large question bank. Probably the ideal place to start.
LeetCode: Easily the most comprehensive set of questions there is. Started doing these after IB.
GFG: Didn't code here. This was just to clear doubts.
Stack Overflow: Helps in clearing all doubts of all difficulty levels.

Dell Technologies

Bangalore

IT

Compensation Offered (CTC) : 14 LPA

Software Engineer - 2

CGPA: 9.21

Recruitment Procedure

Round 0 - Resume screening
Round 1 - Online test - MCQs - 75 mins
Aptitude and technical questions, no coding questions were asked
Round 2 - Technical Interview
I think I was asked 2 coding questions and other questions on CS fundamentals.
Coding question 1: Print the longest consecutive sequence.
Don't remember the second one.
Round 3 - Managerial Interview
General discussion about the team I was being hired for, the work being done, work location etc.
Received positive feedback.
Round 4 - HR round
Was informed that I was selected and had a general discussion.

Important Topics and Subtopics to Remember

DSA, OOPS, OS, CN

Sources of Preparation

Leetcode, Interviewbit, Gfg

eightfold.ai

Noida/Bangalore

IT

Compensation Offered (CTC) : 23 LPA

Member of Technical Staff

CGPA: 8.08

Recruitment Procedure

Round 1 (Technical Interview-DSA)

1. I was asked the print all parenthesis question (https://www.geeksforgeeks.org/print-all-combinations-of-balanced-parentheses/). I had to explain my approach, write and run the code and explain the time and space complexity. The interviewer asked follow up questions like what is dynamic programming and could we benefit by using dynamic programming in this particular problem
2. The interviewer asked me about my favorite data structure, why it was my favorite and how it was implemented.

This interview lasted for about 45 minutes

Round 2 (Technical Interview-System Design + DSA)

1. Merge two sorted arrays (Write pseudo code)
2. Sort an array such that the entire array does not fit in memory (I was asked to assume that the array was present in a file)
3. Design a Chess game (No code just explain approach) - I explained all the classes i would require and explained a brute force approach to get all valid moves for the pieces. (There was no time to explain optimal approach)

This interview lasted for 45-50 minutes

Round 3 (Managerial Round)

1. This interview was with the Head of Engineering in India. He grilled me about one of my projects.
2. Asked general questions like why you want to join this company etc

This round lasted for about 30 min.

Important Topics and Subtopics to Remember

Data Structures and Algorithms
Object Oriented Programming
System Design

Sources of Preparation

DSA (Leetcode , GFG, Interviewbit)
Object Oriented Design + System Design (Cracking the Coding Interview)

Espressif Systems

Pune

Electronics

Compensation Offered (CTC) : 22.50 LPA

Digital Design/Verification Engineer

CGPA: 8.42

Recruitment Procedure

First Round: Written
There were approximately 60 questions, mostly about Digital Design, STA, Computer Architecture, and basic programming. Four students were shortlisted.

Second Round: Technical Round
This round consisted of two back-to-back interviews lasting around 45-60 minutes each. The interviewer first asked me about my interests, projects, and internships. Then he asked me a few questions about digital design, such as FSM, building circuits using only NAND gates, and clock divider circuits. Additionally, he asked basic questions about memory organization, such as calculating the average memory access time of the Cache, and calculating the size of FIFO.
In the next interview, he asked me to code in C or Python and asked me questions related to my code. For example, what are the drawbacks of loops? How can you make it more efficient? Which process is going to be the most CPU intensive?

Third Round: Technical Round
This was a short interview that lasted around 20 minutes, conducted by the Director of ASIC Engineering. We first talked about my background, then he asked me a few technical questions regarding digital design, STA, and clock divider circuits.

Fourth Round: HR Round
The HR asked me a few questions about my family background, personal strengths, my future plans, and then we had a short general conversation. This took around 30-35 minutes.

All the interviewers were very friendly and they helped me whenever I got stuck.

Important Topics and Subtopics to Remember

Computer Architecture
Basics of VLSI
Digital Design (Imp: Clock divider circuits, FSM, details of FF and Latches)
STA
Verilog

Sources of Preparation

STA : http://www.vlsi-expert.com/p/vlsi-basic.html , Technical Bytes Youtube channel
Verilog : https://hdlbits.01xz.net/wiki/Main_Page , Samir Palnitkar's book
Digital Design : Morris Mano, Technical Bytes Youtube channel
Computer Architecture: Hennessy and Patterson
Digital Electronics Gate Questions

ExxonMobil

Bangalore

Chemical Engineer

Compensation Offered (CTC) : 11.50 LPA

CGPA: 9.01

Recruitment Procedure

Round 1: Online test - It was a proctored online 90 minutes test, and consisted of 2 parts. First was aptitude test which had 60 questions that you have to solve 60 Mins (3 sections: English – 15 Q, Analytical – 25 Q, Quantitative Aptitude – 20 Q) and second was the technical Test in which 30 questions were to be solved in 30 Mins. Most of the questions in the aptitude were easy, just the time management was important as the test is very lengthy as compared to the time provided. For technical test, time given was sufficient as mostly theory questions were asked or short numerical ones. Do focus on thermodynamics, KRD and fluid mechanics for this part. Mostly everyone who gave this test cleared this round.

Round 2: Group discussion - We got divided into groups of 8, and the topic given to our group was - "Electronic voting machine versus paper ballots: which is better to use". We had been given 2 minutes to prepare, and 14 minutes to speak, after which 1.5 - 2 minutes were given for preparation of conclusion and then each speaker was given a minute to conclude the entire discussion. They test your listening skills and how clearly you put through your points. I got to speak quite less in the discussion, but I tried covering all the points discussed by each speaker and referred to them in my conclusion.

Round 3: Interview - The interviewers are quite chill, and it feels like having a normal conversation with them. They try their best to comfort you and do not unnecessary intimidate you with tough questions. In my interview, they first started with the introduction and asked me about the most important point in my resume. I explained about one of my projects in depth and what all were my contributions in it. I would say go through each and every line mentioned in your resume and be prepared to be asked questions based on that, they may even counter question your projects' explanation (although not in my case), so read about the concepts associated with the projects listed by you. Then they started with my technical round, and asked that they can see Process Control and Dynamics in my course list, so if it's fine if they ask questions based on that or I want them to ask questions from my favorite subject. I got a bit lucky here as PDC was amongst the two of my favorite subjects that I prepared for. I replied that I am fine if you asked from PDC or else you may ask from Fluid Mechanics. They asked basic questions like what are the types of controllers, final control element, valves, and similarly for Fluid Mechanics, few basic questions and applications. After this, behavioral round started - they asked me questions based on my Position of Responsibility, like how did I manage conflicts if any and showcased team leadership and other situation specific questions. For such questions I would suggest you to use STAR method (situation, task, action, result). I narrated anecdotes for each HR question and to support each of my skill. They ended the

interview by asking "Why Exxon" and if I have any questions for them. Make sure you have at least one question in mind to ask them. Also, ensure that you are punctual for the interview, they take note of that.

Important Topics and Subtopics to Remember

For online test, I would recommend to go through all the thermodynamic cycles thoroughly, KRD and Fluid Mechanics. For the technical round, prepare for at least 2 favorite subjects, and apart from that have some basic knowledge in all of your core subjects (mainly Fluid Mechanics, PDC, Heat Transfer, Process design, Mass Transfer, KRD).

Sources of Preparation

Interview questions might be similar to your CEL vivas, so if you are short of time you may go through the lab manuals/reports. But for thorough preparation, 2 months are fair enough, your notes, slides and textbooks are the excellent sources for the core chemical subjects.

Additional comments

I would recommend that you sit and prepare for certain HR questions beforehand, think about instances in your life, or make some anecdotes in your mind so that you don't get blank during the interview. They judge your communication skills, your clarity of the subjects and the way you present your points in front of them. Be calm in answering, and listen to every question/discussion carefully and patiently. Also, make sure that your resume is clear and you are thorough with the basics of each and every point listed there.

Flipkart

Bangalore

IT

Compensation Offered (CTC) : 26.60 LPA

SDE

CGPA: 7.71

Recruitment Procedure

Round 1: Online Test

3 coding questions - 90 mins

Q1 - Given 3 integers a, b and c, return (((a^b)%10)^c)%1000000007.

Q2 - Two integer arrays of 0s and 1s are given depicting a queue of students with their choice of scholarship and a queue of scholarships we can provide (we can only provide the scholarship at the front at any moment). If the student at the front wants the same scholarship that is at the front, we give it to the student, otherwise the student rotates back to the end of the queue. Return the number of students who will end up without a scholarship.

Q3 - Graph based question on shortest path.

Round 2: Technical Interview

Q1 - Given an array of characters 'M' and 'C' depicting mouse and cat respectively, and an integer K, a cat can move a maximum of k steps in search for a mouse. Return the maximum number of cats that can be fed.

Q2 - Given an array of integers showing the price of a stock on a particular day, return the maximum profit. Unlimited transactions allowed. You cannot buy and sell the stock on the same day.

Q3 - Same as Q2 but with limited transactions allowed.

Round 3: Hiring Manager round

In depth discussion of any project in resume (~50 mins). Motive behind the project, what you did and why you did it, reason for choosing any particular technology for a problem. If possible, how would you scale up your project for a large number of users. What factors to consider improving (scalability, performance). Questions like what's your strength, weakness etc, why Flipkart, situation based questions.

The overall experience of both the interviews were good. They started with introductions as an ice breaker, also made it clear to share any approach or thought process while solving the problems.

Important Topics and Subtopics to Remember

Arrays, Trees, Two Pointers, Dynamic Programming, Graphs

Sources of Preparation

Interviewbit, GeeksForGeeks

Additional comments

Make sure to share your thought process while solving the problem. If unable to solve, try to share the brute force solution at least. In the case of an online interview, try to use the editor provided to explain any custom example or test case.

Galytix Analytics Pvt Ltd

Gurugram

IT

Compensation Offered (CTC) :13 LPA

SE

CGPA: 7.62

Recruitment Procedure

Round 0: 50 MCQs from aptitude, logical reasoning, english and core CS subjects. Round 1: Technical Interview: Started with my Introduction and how I landed in choosing the IT sector despite being from an Electronics background. Then there were questions regarding my work experience and projects mentioned in my Reśume. After that they asked me a DSA question. At last, the questions were regarding core CS subjects and in general questions related to my development tech stack.
Round 2: They gave me a project. I had to develop a website right from scratch using Angular.js.

Important Topics and Subtopics to Remember

DSA, OOPS, DBMS, OS, CN, System Design and Development.

Sources of Preparation

GFG, Leetcode, Github and Developer's society.

GE Healthcare

Bangalore

IT

Compensation Offered (CTC) : 16.40 LPA

EEDP-Edison Engineering Development Programme

CGPA: 8.18

Recruitment Procedure

Round 1(Online Test):
1. Coding(2 questions)
One was on Tree and the other was related to DP.
2. Technical MCQs
Questions on data structures, C and C++, OS, DBMS, Computer Networks etc.
3. Aptitude(quantitative, logical reasoning and English)

Round 2(Pymetrics Assessment):
It's like a game based test to analyze your cognitive, social and behavioral traits.
link- https://youtu.be/GpLYe662PfY

Round 3(Technical Interview):
The interviewer was very nice. He requested an introduction from me. I explained about myself and also shared insights on some of my projects that I did. In addition, I told him about the project I enjoyed working on the most.
He picked a project from my resume on which I had a research paper published. He requested that I describe the project and how it differs from others. He got interested in my project as it was around his domain and went deep into it. He noticed every term beneath the project in the resume and asked for an explanation. He was also incredibly helpful; whenever I struggled with a concept, he would help.
He asked about the uniqueness of the project.
He then asked about other projects that were mentioned in my resume.

After this he moved into coding. He gave me two coding questions.
There was an array question. I began by applying a brute force strategy. He instructed me to code it, which I was able to do. Then he inquired as to the code's time complexity and was instructed to optimize it. Also asked about the optimized code's time complexity. He then moved on to a different code question. He concentrated just on the approach because there wasn't much time left.
At the end he asked if I had any questions for him. I enquired as to the nature of their work. What technologies do they work with?

Round 3(Managerial Round):
Again we started with my introduction. After that she asked about my experience with the previous round. I shared my experience. Next she asked me why Healthcare? To which I gave an example and explained

its importance. She then began asking questions about companies like Do you know about GE Healthcare etc.
I already had explored their company site so was perfectly able to answer those.
She then asked why do you want to join this company? What are your expectations from it?
Some questions were around the strengths and weaknesses and context about it.
What are you gonna do in the next 5 years?
To which I answered by breaking it in 2+3 yrs like for the first 2 years and then stuff to do in the next 3 yrs.
She asked about teamwork.
Challenges faced in life and also while doing projects and how you overcome that.
Then she explained about the profile , the work they do and its importance. She also gave a glance about the new technologies used and the new things they launched.About the company's ethics,values and what they expect.

Round 4(HR round):
Started with introductions and discussion that were done on the previous round. Questions on strengths and weaknesses? And some common HR questions. Asked me about my interests. Also on whether you want to pursue a PHd? To which I focused on gaining experience first then later thinking about it. What makes you different? What are your qualities? Some situation based questions.
HR round focuses more on having straight forward answers.Be practical and express clearly.
And yeah that's it! It went well for me and I got selected.

Important Topics and Subtopics to Remember

Prepare DSA well.Be clear about what you mention in your resume.Also should have a background information about the company you are going for.

Sources of Preparation

Geeks for geeks
Leetcode
Interview Bit
Book- Cracking the coding interview
Project resources. Research Paper.

Additional comments

Apart from all these you can also highlight some of your achievements and can relate that as context to some questions. Be straightforward. Don't try to fool anyone. Know about companies goals, visions.
Practice mock interviews. Write down points and prepare.

Google

Hyderabad

IT

SWE

Compensation Offered (CTC) : 48 LPA

CGPA: 8.52

Recruitment Procedure

Always remember to break down problems into smaller subproblems, think of recursive solutions.

Coding Assignment- There were two problems, one based on DP and other on Tree+DP. The problems were very logical and challenging. I was able to solve only the first problem. In the second problem, I printed the correct answer in the wrong format(This is a very common mistake, don't do this juniors!). I scored 100/200, but was called for the interview which is proof that they actually read my code. Remember to follow good practices in your code, it helps eventually.

Interview 1 - This interview started with a simple string problem, and then the interviewer put larger constraints which required the KMS algorithm. Then in the followup difficult problem he introduced another constraint that required Dynamic Programming. Towards the end there was a simple googliness 10 min session(consider this as a 10 min HR round)

Interview 2 - This interview required some mathematical observation. The interviewer introduced more constraints and the problem turned into a binary search problem. And at the end a converted the 1D array into 2D array, resulting in dfs on grid problem. Again, towards the end googliness 10 min session.

Interview 3 - The interviewer started with a simple array problem. Some constraints followed, that required the knowledge of stacks(next greater/next smaller index in an array generally known as stock span problem). Then he introduced another dimension to the problem which required DP. Googliness followed

You must have figured out that the nature of interviews is based on followup questions. There generally is one question which is bent and twisted to make it more challenging throughout the interview span. Nothing outside DSA!!

Important Topics and Subtopics to Remember

Dynamic Programming, Stacks(Next Greatest; Next Smaller in arrays), Mathematics, Some graphs too, Binary Search, Basic string algorithms

Sources of Preparation

Leetcode, Google Kickstart, Codeforces

Additional comments

Towards the end of each interview, the interviewer will ask you googliness questions. Make sure to reflect the following in your answers:-
- You are an inclusive person (you believe in equality of genders, race, etc.)
- You can switch context quickly (can work on multiple projects in parallel)
- You are passionate about technology and bringing a positive change in the world

Honeywell UOP

Gurgaon

Chemical

Compensation Offered (CTC) : 7 LPA

Field Advisor

CGPA : 8.28

Recruitment Procedure

Round 1- Resume Shortlisting

Round 2- Technical Interview: Basic questions on the workings of a distillation column, slurry flow in pipe bends. Questions were technical and gauged your practical understanding rather than the theoretical. Q1. Will increasing the reflux ratio inc/dec the pressure in the column?

Q2. What should you need to know if you're pumping a slurry-like fluid through pipes?

Ans
Properties of fluid - heat capacity, density, pour point etc
Conditions - Temperature, Pressure etc
Ensuring that there is no choking

Round 3 - HR: Basic HR questions on introduction, why you want the job and what you know about the company. Speaking with confidence suffices.

Important Topics and Subtopics to Remember

1. Mass Transfer - McCabe Thiele is very important
2. Fluid Mechanics - Friction Losses, Darcy Weisbach Equation
3. Heat Transfer - Heat Exchangers
4. Petroleum Refining Technology - Should know a few licensor technologies by UOP

   Knowledge of thermodynamics, unit operations and reaction engineering are always a

   plus.

Sources of Preparation

ChemEng - Notes, TBs
Aptitude - Indiabix, GRE Math and Verbal is more than enough

Additional comments

Do research on the company before going to the interview.
Ask questions related to the same to the panel.
This shows that you are interested.
And stay confident. It's ok to not know all the answers but what you know you should say it well.

IFB

Verna Goa

Management Trainee

Compensation Offered (CTC) : 5.50 LPA

GET

CGPA: 6.09

Recruitment Procedure

Pre Placement Talk
Resume Shortlisting
Technical Interview : A panel of interviewers first asked me to introduce myself, talk about interests, proficiencies, interests, and projects that I have done.
After which they asked me the most well versed in subject. I told them Product Design, the last DEL in my requirement sheet. Then I talked about the project I proposed. There were some inquiries from their side and then they asked me if I wanted to ask anything of them.

Important Topics and Subtopics to Remember

Just keep in mind what has been done so far. keep one project that has been done be it a SOP, DOP, LOP or a project in a 5 unit course.

Sources of Preparation

Coursebooks
https://mechanicalenotes.com/ for quick lookup

Indeed.com

Hyderabad

IT

Compensation Offered (CTC) : 18 LPA

SDE

CGPA: 7.92

Recruitment Procedure

Round 1: Coding test:
The test was conducted on hackerrank and included 2 questions.
1) The 1st question was related to DSU, where for each query we had to return the size of the unit formed after Union operations.
2) Given a matrix and integer K, find the maximum size S such that every square of size S that can be formed within the matrix has a sum less than K.
(15 students were selected for next rounds)

Round 2: Technical Interviews 1:
The interviewer asked me to introduce myself and told me that the round is going to be a coding round. The question asked was related to binary trees. He started by discussing the structure of a Node and how a lot of memory is wasted to store pointers to left/right nodes in this representation. He then asked me to implement a binary tree which solved this problem and doesn't waste memory.
At first I implemented the tree using arrays, where in a 1-index based array, for with index, 2*i is left child and 2*i+1 is the right child.
Since this representation would waste a lot of memory for storing null values in a sparse tree, later I decided to use maps. At last he asked me to combine both the representations, where an array is used for storing nodes up to certain height and for greater heights map is to be used.

Round3: Technical Interviews 2:
The format of the interview was the same as round 1. The question was to find the closest leaf node to the root node in a tree which is given in the form of a directed graph. Structures for edge and nodes were already provided. This can be easily solved using BFS or DFS.
After this the tree was changed to Directed Acyclic Graph and the question was the same, to find the leaf closest to root. At first I used DFS and we discussed the time complexity of the algorithm which came out to be exponential. Finally I used Dijkstra's Algorithm using priority queue to optimize the solution. The trick was to stop the algorithm as soon as any leaf node popped from the queue, this leaf is the answer.

Round4: Technical Interviews 3:
The format of the interview was the same as previous rounds. The question was related to strings and maps. We are given RawTitle(string: a sentence consisting of many words) and CleanTitles(a list of strings where each string is a sentence consisting of many words)
The question was to find the clean title which has the most number of common words with the raw title. Repetition of words was allowed in raw title and in clean title.
(3 students were selected for Manager Round)

Round 3: Manager Round

This was a purely HR round. The interviewer asked about my interests and discussed my internship company, what I liked and what I disliked about it. He asked about my dream company and the reason for the same. In the end we discussed a bit about Indeed and its work culture.
(All 3 students received the final offer)

Important Topics and Subtopics to Remember

DSA (Very Important). Primarily Graphs, Trees and maps.
Otherwise all topics that you have included in your projects and internships are a must but this will be asked only in the manager round.

Sources of Preparation

DSA: Leetcode, GFG, interviewBit, PU List of Questions. While solving questions you will come across tricks like Union Find. Be sure to master them.
OOP, DBMS, CN: Google "Last minute prep notes for xxxx topic"
OS: http://www2.cs.uic.edu/~jbell/CourseNotes/OperatingSystems/

Indeed

Hyderabad

IT

Compensation Offered (CTC) : 38.85 LPA

SDE

CGPA: 8.91

Recruitment Procedure

Round 1: Coding test:
The test was conducted on hackerrank and included 2 questions.
1) The 1st question was related to DSU, where for each query we had to return the size of the unit formed after Union operations.
2) Given a matrix and integer K, find the maximum size S such that every square of size S that can be formed within the matrix has a sum less than K.
(15 students were selected for next rounds)

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After this the tree was changed to Directed Acyclic Graph and the question was the same, to find the leaf closest to root. At first I used DFS and we discussed the time complexity of the algorithm which came out to be exponential. Finally I used Dijkstra's Algorithm using priority queue to optimize the solution. The trick was to stop the algorithm as soon as any leaf node popped from the queue, this leaf is the answer.

Round4: Technical Interviews 3:
The format of the interview was the same as previous rounds. The question was related to strings and maps. We are given RawTitle(string: a sentence consisting of many words) and CleanTitles(a list of strings where each string is a sentence consisting of many words)
The question was to find the clean title which has the most number of common words with the raw title. Repetition of words was allowed in raw title and in clean title.
(3 students were selected for Manager Round)

Round 3: Manager Round

This was a purely HR round. The interviewer asked about my interests and discussed my internship company, what I liked and what I disliked about it. He asked about my dream company and the reason for the same. In the end we discussed a bit about Indeed and its work culture.
(All 3 students received the final offer)

Important Topics and Subtopics to Remember

Data Structures and Algorithms

Sources of Preparation

GeeksforGeeks and Leetcode

Additional comments

Each technical interview was focused mainly on a single topic or a basic idea, the difficulty and complexity of the question was progressively increased as you answered the previous one. Fundamentals of data structures and algorithms must be strong. The interviewers were very helpful and would guide you if you got stuck somewhere.

Infineon Technologies

Bengaluru

Embedded Design Engineer

Compensation Offered (CTC) : 19 LPA

CGPA: 8.61

Recruitment Procedure

Round 1: Written Test:'
It is the toughest part in the entire recruitment process. It has 8 sections; each section has sectional cut-off. Sections include aptitude, scripting, microcontrollers, Digital electronics, Analog electronics, Embedded C, Verilog HDL, Power electronics. (Concentrate more on digital electronics, analog electronics and aptitude. Mostly questions are from the gate). After clearing the written test, there are four technical interviews (each interview went for 1hr) followed by a HR round.
'Round 2: Technical interview:'
Interviewer asked me subjects and areas of my interest (I told him VLSI architecture, VLSI design and Physical design) and my whole interview went in that particular domain. He asked me to explain RTL to GDSII flow in detail, tools used in each step and outputs of each step. If STA is conducted in each step? Basic definitions of setup and hold time, origin of setup and hold time? How are they calculated (I explained him taking an example).Does negative setup and hold time exist? What can be done if there is any setup and hold time violation? Are they related? Then he asked questions related to mosfets. To be particular he went very deep into mosfets. He started with operation of mosfets, different capacitances in mosfets, mosfet short channel effects, What happens to capacitance if thickness of oxide layer is increased/decreased, Variation in current if you vary length and width of mosfet. Transfer characteristics of mosfet etc.
'Round 3: Technical interview:'
There were 2 panel members and this round completely went on design questions. They gave me around 7-8 design questions and I was able to solve only 3 of them rest I told them the approach. It seems they were much interested in the approach that I follow rather than the solution (they were giving hints in between). Questions were like designing a circuit that detects alternate edges of input? An infinite bit stream is coming (containing ones and zeros into a register), at any point how do you detect if the number is divisible by 3 or not? Draw circuit of D flip-flop and latch with synchronous reset and asynchronous reset Verilog code for the same? Design a 4-bit adder using full adders and if 16 such 4-bit adders are used, what will be the length of the output? Memory module Verilog code. Two basic aptitude questions were asked one based on time speed distance and other based on reasoning.
'Round 4: Technical interview:'

There were two panel members in this round, this round completely went on CMOS circuits (VLSI design) and physical design. In VLSI design questions were related to transfer characteristics of CMOS inverter, on what factors does transfer characteristics depend upon? What happens if we change the gain of the inverter? , relation between transfer characteristics and channel length modulation? , will you prefer a large inverter to drive a large capacitive load? If not, what would be the alternate method? , What happens if you
interchange PMOS and NMOS in a CMOS inverter, what does the circuit act like, draw waveforms? What are the sources of power dissipation in CMOS inverters? On what factors does power dissipation depend on? What are the techniques used to reduce power in CMOS circuits? What is clock gating, power gating etc. Coming to physical design, very basic questions were asked like what is cross talk, reasons for it, methods to reduce it? Static Timing Analysis (in detail), given material of length L, cross section area A, comment on resistance of the material.

'Round 5: Technical interview:'
There were three panel members in this round and this round went for 1.5hr. Questions were related to the projects and Verilog HDL. He asked me to explain the implementation of MIPS processor (project), Verilog code for memory module and instruction fetch module. What are the advantages of pipelining, hazards of
pipelining, different types of hazards in a processor? They asked me to write a Verilog code for a traffic light signal? A design question based on memory is given and asked me to write a Verilog code for it, Is case statement in Verilog synthesizable?, Verilog code for 6*1 mux, What are inferred latches, why do they come into picture, what are the methods to eliminate them? Difference between 'x' and 'z' in Verilog, Design integrated clock gating cell and Verilog code for the same. A chunk of memory is to be transferred from one part of memory to another part of memory. Write a Verilog code for it, bottlenecks that are to be considered in this design. Importance of 'default case' in case statement and multiple basic questions in Verilog were asked.
'Round 6: HR round:'
Went for 40 mins. Pretty simple and basic questions like how many companies have you lost and why? Family background, future studies, why BITS goa why not BITS Hyderabad? He asked me why there's a drop in my UG percentage. Are you satisfied with the compensation structure? Any suggestions in the recruitment process?

Important Topics and Subtopics to Remember

Embedded profile :
Be strong in your C basics especially pointers, bitwise operators, bus protocols,OS fundamentals digital profile :

STA ,Verilog, RTL to GDS flow, Design questions

Sources of Preparation

It depends on the profile you are preparing for
I followed these for embedded profile:
C - Neso academy
Embedded C - Udemy ()
Operating systems - Neso academy
Data structures - Udemy(Abdul Bari)
C++ - Udemy (Abdul Bari)
Embedded system Design - Anupama ma'am and Vipin sir notes
For digital profile :
VLSI architecture - Gurunarayan sir lectures Pilani.
VLSI Design - Rabaey, kang.
Physical design - Udemy (Krunal Ghosh)
Digital design - Morris Mano
STA - VLSI expert, Mane sir notes

Additional comments

Don't stick to one profile. you'll never know which company will come for which profile. It is completely dynamic

Infineon Technologies

Bangalore

Electronics

Compensation Offered (CTC) : 19.30 LPA

Analog Design

CGPA: 7.65

Recruitment Procedure

Round 0 - Written Test: The syllabus of this test was Embedded C, Scripting, HDL, Analog & Digital Electronics, Power Electronics and Aptitude. The questions were mid-level and did not have negative marks. Being an ECE student, I did not do any Power Electronics courses, but that didn't set me back by a lot because each of these topics was split into a different (but tiny) section in the test. A word of advice for written tests in general – play to your strengths and try maximizing your score in the sections or topics you are comfortable with. Having deep rooted knowledge in a few topics might help you extend that to something you haven't done, or will push you to derive something you forgot.

Round 1 – Technical Interview 1: My interviewer was a very sweet and friendly gentleman. He asked me to introduce myself in two lines, and then asked me the 'Job v/s Masters' question. Then, he jumped into the technical questions.
Q1. Drew a simple RC low pass filter and fed a Pulse voltage to it. He asked me to explain the output in time domain. He also asked me why I would get an exponential curve and not anything else. Q2. Repeated the previous question with a high pass filter this time
Q3. Asked me the definitions of Pole, Zero, Gain Margin, Phase Margin and Stability. Q4. Drew an OpAmp with purely resistive components. First in positive feedback and then in negative feedback. I was asked to identify the voltage at the feedback node and output node. I answered all but Q3 satisfactorily, because I blanked at Gain and Phase Margin. The importance of Control Systems for Analog is underrated, and I'd definitely recommend brushing it up a couple of times. My interviewer didn't hold this against me though, he helped me arrive at the definition once he'd established that I knew the Stability part (Barkhausen Criterion).

Round 2 – Technical Interview 2: My second interviewer started off by asking me to introduce myself. He then asked me what I preferred among Analog & Digital and asked me to explain why. He then asked me to write the equation for current flowing through an NMOS transistor when operated in saturation region and show it to him. He then asked me what each of the terms I wrote meant. Then, he asked me to explain the dependence of each term on temperature.
Q1. Once I had established all of the above information, he asked to explain why it is preferred to have circuit operation at cooler temperatures (the question was actually a little more abstract than my current framing, and the question was not about keeping the circuit cool, but rather why is a low temperature attributed to improved performance). It took me a couple of attempts to evaluate and reiterate my reasoning (my arguments were on the lines of ED stuff like threshold

voltage/characteristics and
bandgap), but I didn't get too far with that. After some back and forth, he moved on to the next question after affirming all other aspects of the question.
Q2. He asked me to draw the characteristics of a CMOS inverter, and asked me to define noise margins.
Q3. He drew an RC Circuit with two voltage inputs at different locations, one DC and one Pulse. He asked me to draw the output voltage.
Q4. He proceeded to ask me about the projects I had done, and why I did them.
This round made me realize that communicating with the interviewer is very important. Speaking my mind openly helped my interviewer get an idea about where my ideas where headed, even though I didn't eventually make it to a concrete final answer.

Round 3 – HR Interview: The HR person was very kind and engaging. He was very attentive and thoroughly examined and tested anything I had to say.
Q1. 'Masters v/s Job' question
Q2. What are some hurdles you have faced so far?
Q3. You mentioned an academically loaded degree. How did you prioritise/multi-task? Q4. How would your professors describe you?
Q5. How would your friends describe you?
He also asked me about my family background etc.

Important Topics and Subtopics to Remember

Here's a classified list of stuff that would be of use. This list is for Analog alone.
Need-To-Know Topics - It is an absolute must to be very comfortable with these: 1. ES: RC, RL and RLC circuits – This is the bread and butter of Analog interviews. You need to be very comfortable and completely intuitive with this. That means no big equations, no complicated and lengthy steps, just looking at the circuit presented and verbalizing what's actually happening there. RLC Circuits are a little rarer, but it is important to know Quality Factor, the nature of Damping, being able to calculate the resonant frequency, etc.
Dependent and Independent Current/Voltage Sources - Helpful in handy circuit solving problems if you know this well, it will help you cut down steps and speed up.
2. MuE – Although I haven't encountered/heard about complicated transistor questions in Placements, it is very important to know and identify the three basic MOS Transistor configurations. A standard question is 'What is the resistance/gain I will see if I look from one MOS terminal to another?'. It is also useful to know handy MOS-to-BJT comparisons and analogies. Miller's theorem, its application and identification, is also very important.
3. Control Systems: Barkhausen criterion for stability is very important. Poles, zeroes and transfer function arithmetic can be very handy in solving a variety of problems. It is also important to study the technique of evaluating the nature of feedback in a system by breaking the feedback loop. 4. Analog Electronics: OpAmp basics, how it behaves in positive and negative feedback. It is very important to

grasp the difference in the usage of opamps with different kinds of feedback. 5. ADVD: MOS Inverter Characteristics are very important. This is mostly theoretical and questions cannot be convoluted beyond a point under this topic

6. Electronic Devices: It is important and very useful to have a clear idea as to how transistors (MOS and BJTs) work. Though ED is equation-heavy, it is important to know some basic equations and the physics associated with it (effect of temperatures, voltages, charge injections, etc.) if you are unable to study or retail topics in detail.

7. Diodes in ES and AnalogE: This is a recurring favourite for recruiters to insert a diode into an existing circuit to test your understanding. Use of diodes in Rectifiers, Clippers, Clampers and Peak Detectors are very important. As an extension, superdiodes (OpAmps+Diodes) are also widely asked. Precision Circuits using OpAmps and diodes can be easily disguised into more complicated looking circuits.

Nice-To-Know Topics – They might help solving some off-the-bat questions:

1. Basic Communication Theory: Most important under this would be the differences between different kinds of transforms (Fourier, Laplace, Z, others from SAS/DSP/CommSys), particularly, the overlap of Fourier and Laplace transforms and how to calculate time domain to any transform domain quickly for some standard inputs like impulse, step and ramp functions.

2. Control Systems: Gain and Phase Margins, some advanced topics from Control Systems. While it is rare to find questions that delve deeply and exclusively to ConSys, having a strong command over basic definitions, problem solving techniques, is useful.

3. Advanced ED: Although it is rare, the working principles behind other semiconductor devices (JFETs, etc.) might be helpful.

Some miscellaneous advice for someone who is looking to sit for core placements would be to not restrict or confine yourself to Analog related topics alone. A good grasp on DD, Static Timing Analysis (and the Delay and Timing related topics at the end of ADVD) and maybe even Basics of Embedded Systems/Computer Architecture/Microprocessors are all quite useful skills to have and hone if your preparation makes room.

Sources of Preparation

Here are the sources that I relied on:

For the most part of my prep, I used YouTube videos to help me clear out concepts and revise stuff. I relied on Chembiyan sir's YouTube channel almost exclusively. His explanations are exceptionally clear, and he engages you with problems which, in all probability, you will face during your placement process.

For ES: I studied from the playlist titled 'Introduction to Electrical Sciences'. When you hear from someone that they want an intuitive answer for a question, an answer that sounds sir's explanations are precisely what they're looking for. Sir takes up different arrangements and permutations of RLC circuits with a variety of inputs in both time and frequency domain, which makes it a good source to practice from as well.

(https://www.youtube.com/watch?v=yVNrBDF20uY&list=PL6qRG5-NfbLvagdQOwShX9FMrzb5hSvrq)

For MuE: The playlist on Chembiyan sir's channel titled 'Introduction to Analog Integrated Circuits' is very useful. The videos are very deep and engaging, which might become cumbersome if you're pressed for time. The first 25 lectures are mostly sufficient. These discuss gains and resistances from one node to another (https://www.youtube.com/watch?v=JmR0-gzPjwY&list=PL6qRG5-NfbLvCFCeCDwLWrIoeOrQxP9ZE). A similar lecture series has been presented by Professors Shanthi Pavan and Nagendra Krishnapura at IIT Madras. Alternatively, you could pick either Razavi/Sedra Smith (whichever you have been taught from in MuE).
For Analog Electronics: I watched the playlist titled 'Analysis of OpAmp Circuits' and 'Introduction to CMOS OpAmp Circuits'. These playlists are brief, and you may have to use Sergio Franco/LK Maheshwari (Analog Electronics textbooks) to bolster your prep if required.
For Control Systems: I read the articles on Tutorialspoint and the like to brush up concepts. Standard analog electronics books discuss control systems more from a circuit perspective, which would be helpful as well.
In addition to the playlists mentioned above, Chembiyan sir has consolidated a playlist titled 'Intuitive and Non-Conventional Analysis'. This is a useful quick-revision guide before a test or an interview. For topics like diodes in circuits, I watched the YouTube videos from Electronics4u. There is a large table in Oppenheim and Schafer (SAS textbook) on Fourier Transform/Laplace Transform properties. Memorizing some key transforms from there would be helpful. Additionally, the relationship between transforms (like when are fourier and laplace transforms identical/interconvertible using s = jw, etc) are good to keep in mind. In a couple of other tests (not Infineon's) I remember there being some questions from DSP (FFTs etc), so if time permits, it may help to breeze through them.
The problems we solve in class are different in the nature of their evaluation of your skills as compared to Placement tests. Hence, trying to solve textbook sums without pen/paper or solving them by figuring what exactly is happening in that circuit rather than whipping out the arithmetic would be very good for your prep. GATE Papers also have some degree of similarity of placement tests, if one is looking for additional sources for practice.

Additional comments

0. Cultivate your intuition. When you look at/solve a question, try answering to yourself 'What is happening in this circuit?', and answer in terms of how a charge is getting accumulated, what direction the current is flowing, what voltage is appearing across a component
1. Plan your prep. Sit down a couple of months before the season starts, assess your skills and confidence thoroughly and then tailor your preparation to it. Set goals and track your progress. Reach out to seniors or PU for any prep materials/questions and give mock tests or interviews, even if you are not very well prepared.
1a. No matter how much/little you study, do it very thoroughly. Depth is always better then breadth. 1b. A lot of us engage in different activities and projects throughout college, and so we might forget some details about a project/activity on our Resume. Know your resume very thoroughly and spend time

thinking about how you would explain your projects to someone if they asked you to elaborate upon it. 2. Ensure to speak your mind completely and thoroughly during your interview. It helps your interviewer understand how you solve a problem and trace your thoughts. It is almost always about the approach rather than the answer. Also, what you might perceive to be a setback in an interview (for eg: not being able to answer a question) may not necessarily be one, so maintain your confidence throughout. 3. Dress well, and be pleasant during the interview. Engage with the interviewer beyond the scope of the technical questions you're asked. Don't say 'No' to 'Do you have any questions for me?'. Be truthful and honest.
4. Don't stress too much, you will find a way to make it work out in the end :D

Jivox

Bengaluru

IT

Compensation Offered (CTC) : 26 LPA

SDE Frontend

CGPA: 8.5

Recruitment Procedure

Round 1: Technical Interview

Focus on DSA problems, leetcode easy and medium, related to strings

Round 2: Technical Interview

Short question about dbms, oop
had to write sql queries such as join
1 dsa question

Round 3: Technical Interview

First half questions about react(As I selected Frontend Role)
Second half a question about string. related to arrays

Important Topics and Subtopics to Remember

DSA, String, Simple OOP and DBMS, Frontend tech if you have any experience

Sources of Preparation

Leetcode, Interviewbit, javascript.info

Jivox

Bangalore

IT

Compensation Offered (CTC) : 22 LPA

Software Engineer

CGPA: 8.04

Recruitment Procedure

Round 0: Online Assessment
There were 4 coding questions and 15 MCQs. The coding questions were standard and easy questions. The MCQs included topics like DSA, operating systems , DBMS and questions on java. Round 1: Technical Interview
This round started with a basic introduction and the Interviewer went directly into coding questions. First question was, given a statement made of English words and grammar punctuations like apostrophes, spaces and some others. Run through the statement and find all the words in the statement. The second question was a standard question, Given an array to find the number of distinct triplets having the sum to zero. The time complexity expected was o(nlogn). Both questions were to be solved and run to pass all the test cases in hackerrank platform

Round 2: Technical Interview
This round started with some questions on the projects in the resume and then coding questions were asked where the first one was on basic logic and more focus was on approach than passing all test cases. Second question was on DP and the question is, A cab is moving on a one dimensional line with passengers having pickup and drop points and money paid by them. The cab can have one passenger at a time and should pick them at their pickup point and drop at their drop point. Find the maximum money made by the cab driver on passing the passengers.

Round 3: Technical Interview
This round focused on a variety of topics like Operating system and a small system design question on a parking lot where only explanation was needed and some logical questions. This was the last round.

Important Topics and Subtopics to Remember

DSA(Dynamic programming, 2 pointers, Graphs) ,OOP

Sources of Preparation

Leetcode, Interviewbit and geeks for geeks

LTI

PAN India

IT

Compensation Offered (CTC) : 9.50 LPA

Engineer-data services

CGPA: 9.73

Recruitment Procedure

Round 1: Online test -- The online test consisted of several sections such as coding, management and decision based sections. The initial section aimed at finding out the candidate response to situations encountered in the company scenario. The questions were simple and aimed at assessing the mindset of the individual to complex scenarios in an industrial role.
The second section involved testing the candidates ability to code certain problems. The questions were easy and included questions with solutions which did not require in-depth knowledge of coding. A reasonable knowledge and background into coding is preferred for non coding based branches. The subsequent sections involved assessing the candidates communication skills such as usage of vocabulary, speaking and writing skills. The questions entailed are simple, descriptive and requires the candidate to solve them while thinking each of them critically as certain questions were repeated with different phrasings.

Round 2:Technical interview -- The interviewer was a kind, easy-going individual. He initially went through the resume and the session began with the basic self-introduction of the candidate. Being a person from a non-coding background, he questioned the necessity and interest to apply for the data services role. (Reply for the question was associated with the projects and interests stated in the resume). The next few questions were on comprehensive explanations into the projects and the analytics work associated with them.

This was followed by basic questions on statistics and math related to data science such as regression (linear, logistical and multinomial), bayes theorem and its applications , statistical sampling etc. It is required for the candidate to have a strong background in basics of statistics and other data science related concepts (fundamental level knowledge will suffice, as the questions were not in-depth). The application of these tools was also tested via application based questions with varied scenarios. A significant portion of the interview was emphasized on the mathematical and analytical ability of the candidate.

Final stage of the interview was involved with questions about API, cloud and Big data. The interview was considerate on the level of questions related to API and cloud, since I was from a non-coding background and if I was unsure of the topic, I was given the freedom to answer to the extent of my knowledge. So it is wise to answer honestly and mention your state of knowledge on the topic beforehand. The follow up

questions were brief and he asked me to explain a certain application of cloud that I was engaged with in one of my core projects during my masters.

At the end , I was given an opportunity to ask any doubts related to the company.
Answer : I had asked about the daily schedule and work life associated with data services roles within the company in-order to gain insight from an actual working professional related to the data science field. From the answer, I was able to answer a question that I was unable to answer previously during the interviews. So pay attention to the question section about the company at the end.

Round 3: HR interview -- The HR interview was smooth and it involved fundamental questions on past experiences during my undergraduate studies and it was mainly aimed at probing the mentality of the candidate to engage and work in different locations. This was followed by basic salary negotiation and the interview was done.

Important Topics and Subtopics to Remember

For a Non-coding background,
Fundamental knowledge about coding (any one language),
Using Statistical tools can be an advantage. (In my case I had knowledge of R).
Other than that, a strong base on topics such as Statistics and probability.
Also knowing about the basics and workings of various ML algorithms can come in handy too.

Sources of Preparation

For coding , Geeksforgeeks, codewars.
For data science based interview questions (towards datascience and kaggle).

Additional comments

Try to highlight the analytical portions of the projects mentioned in the resume as it might be a suitable

MediaTek

Bangalore

Electronics

Senior Physical Design Engineer

Compensation Offered (CTC) : 15 LPA

CGPA: 7.52

Recruitment Procedure

Round 1- Written Test
The test had questions on aptitude, digital design, etc.
The difficulty level of Aptitude and digital design was moderate to strenuous.
The digital design had questions from frequency divider, Verilog, logic gates etc.

Round 2 - Technical interview

The interviewer was very supportive and wanted to bring out the best in me. He gave hints also whenever I got stuck at any point.

Question 1- Draw a frequency divider circuit.
Question 2- STA concepts - how to fix setup and hold violations.
Question 3- Lots of physical design related questions. Asic flow , what are the files generated after every step in asic flow. Input and output files.

Important Topics and Subtopics to Remember

STA , VLSI design, physical design flow , design-related questions.

Sources of Preparation

Vlsi experts, Rabaey for VISI DESIGN, Physical design videos by Indranil Sengupta and PYQs.

MediaTek

Bangalore

Electronics

Compensation Offered (CTC) : 15 LPA

Senior Verification Engineer

CGPA: 7.76

Recruitment Procedure

Round 1 : Written Test
It had 3 sections - Aptitude , Basics of Engineering & Engineering Knowledge. Each section had a separate time and all questions were MCQ type .
Aptitude was a bit difficult since there was only 10 min given for that section and questions were calculative in nature.
Section 2 -Basics of Engineering was easiest of all since it had questions from basics of semiconductors , few questions which can be answered from the class 12 knowledge (example a question to identify the Schrodinger wave equation) and other fundamentals of physics were asked. Section 3 was given 40 min time since questions were little lengthy , it had questions from Verilog (Given code we need to choose appropriate output , Concepts), Digital electronics - Counters , FSMs (We were asked to find Frequency from Digital Circuits etc), CMOS , Code Converters , Boolean Algebra.

Round 2: Technical Interview -1 (Online Mode) (45 mins)
Started with my Intro and since I was from an embedded System background I was initially asked to tell all the subjects I had in my curriculum . Interviewer then asked to open the notepad and type a C program - setting a bit in for an 8 bit binary number . After I type the logic , he asked me to change the snippet I typed into a function module with necessary parameters and next asked to write another function to clear a bit .later on few questions were asked on different types datatypes in C ,slight Discussion on operators and byte vs short ,Storage Classes . I was bit nervous initially hence I typed the code asked very slowly and interviewer was friendly , he indeed helped in recollecting few concepts on storage classes

Round 3 - Technical Interview -2 (Online Mode) (55 Mins)
This Round started with an intro to my projects as mentioned in the resume . The interviewer was not curious about the projects because my projects were mostly IOT based and only 2 from VLSI Domain (which were Common type) . First question was Flip flop Vs Latch .Which is preferred mostly in VLSI design and why. For this question since it was a bit expected one I gave a very extensive explanation (more-than required with some examples which drive the interviewer towards STA actually) , He then asked me about Definition of setup and hold time and with significance . I Used this Opportunity to start with basic definitions and then asked him whether I can explain with a diagram of flipflop , as he agreed I shared my screen and drew a circuit of D flip flop using Transmission gates and explained the Setup and hold definitions and impact if they are not clearly defined w.r.t to the circuit .He asked me add Asynchronous reset logic to the same diagram . I took some time to think but i was bit nervous here and i have drawn some random logic using mux which i felt would act as asynchronous reset , but here interviewer gave an hint that my idea was correct but the implementation was wrong and he also added that can I get the same using single logic gate, i took some time and

answered that it can done using NAND /AND , he agreed and asked me to add the same circuit at the required place. Next the discussion went to Verilog - like Is For Loop exist in Verilog , if yes is it synthesizable ? I gave an extensive answer here too with different cases where the For loop is synthesizable and where it is not. At last he asked to tell the clock cycles it takes in Verilog to search a particular element in an array with 250 elements , here I explained about linear and binary search algorithms and said the no if clock cycles in both cases.

Important Topics and Subtopics to Remember

1) C programming
2) Verilog
3) Digital Circuits
4) Fundamentals of Static Timing Analysis
5) Concepts Related to CMOS , MOSFETS , Transmission gates
6)ASIC and FPGA Design Flow

Sources of Preparation

1) Verilog - Read all the important topics from the book on Verilog by Samir Palnitkar and Must to Go through all the popular questions on Verilog (Code Based) that are available online.
2) C Programming - Cover all the Concepts , MCQs , Bit manipulation Coding type available in Geeks for geeks. Searching and Sorting Concepts
3)Digital Circuits - Gate Books
4) Basic of STA and Design Flow - Watch all content available in YouTube (as per availability of time)

Additional comments

Explain the concepts slowly and clearly so that that interviewer might know our confusion and might help with a hint. Try to drive the interview into your strong areas through your explanation with appropriate examples. Good to re-confirm the question once again with the interviewer before you interpret it wrong.

Mediatek

Bangalore

Electronics

Compensation Offered (CTC) : 15 LPA

Senior Synthesis and STA Engineer

CGPA: 7.13

Recruitment Procedure

Mediatek Interview happened in two phases
1) Written Test
2) Technical Interview
1) In the written test, there were a mix of aptitude questions and digital electronics questions. Preparing DigiTS would be beneficial for it. Be Strong with digital concepts.
2/ Technical Interview - My interview went for an hour . The person who took my interview was very relaxed and also helped me to relax initially. He started with a question as to why being from Embedded I want to be In VLSI domain? I just told him that I am more interested in the digital domain.
Then he started with technical question
1) He asked to draw CMOS Characteristics and operating regions and asked what happens in different regions.
2) Then he asked me to draw the Divide by 3 or Divide by 5 frequency divider.
3) Then he asked me, what is CMOS Latch up?
4) Then he started with logic question,
You have a torch that requires 2 batteries to light up. You also have 8 batteries out of which only 4 are charged and the remaining 4 are not charged.
But you don't know which 4 batteries are charged.
However you can try different combinations of batteries to light up the torch.
PUZZLE : What is the least number of attempts you need to make, to ensure that it will light up the torch.
That was my interview.

Important Topics and Subtopics to Remember

Digital Electronics, frequency divider questions with 50% duty cycle, Basic digital question, VLSI Design
CMOS characteristics, operation regions, CMOS Latch up, Logical Question

Sources of Preparation

DigiQS - for Digital Electronics very important
VLSI Design

1) https://www.youtube.com/watch?v=HvgdMTvwUlE&list=PL0lDezr9NliRr5OgX8jyYTeoNTkMNprAq

2) Neil Weste, CMOS Kang,

3? Logical - Geeks for Geeks

Additional comment

If you have the knowledge of Particular profile the company has come for, it can help in the interview to fetch you that profile.

Mediatek india pvt Ltd

Bangalore

Electronics

Compensation Offered (CTC) : 15 LPA

Physical design engineer

CGPA: 7.11

Recruitment Procedure

Unlike in other companies ,we faced only 1 interview after the written test.
Written test consists of some puzzles,logical reasoning,vlsi concepts,digital electronics,STA concepts
As I said I faced 1 interview ,it was around 1:30 hr, they conduct no :of interviews based on the domain they will assign you in.

Interview:
Starting with my resume, the projects I did, as the 1 bit full adder layout, she asked me to explain about it ,the tools used and all,based on that project she touched physical design concepts,different input files used and libraries their definition.

After that she started with digital questions around 5-6 questions related to FSM, flip flops,clock gating cells,isolation cells,basic gates related stuff.

Then little bit about clock domain crossing,metastable states ,frequency dividers etc;

Then some questions on verilog basics,their modeling styles, some symbols/syntaxes used in verilog etc;

Asked me to write very basic C code,it is nothing actually.

Then she started to touch vlsi concepts, CMOS, all possible questions she asked,characteristics and all, mosfet basics, stick diagrams,slew,fanout definitions.
Sta Concepts all kind of questions she asked,my most of time went on these sta topics only (you need to be very good in this topic)

After at the end she started rapid fire round continuously 10-12 questions she asked about vlsi ,digital mix .

She asked about ,Linux basic commands,i told her like I will learn if it is required for the profile and at the end she asked me preference frontend /backend ,i told her I love working in backend .(But prefer telling i will flexible with both)

Suggestion: at the end don't stop your conversation,ask interviewer about your feedback/about how was the profile in company.(show interviewer that you're curious and interested about that profile/company)

Important Topics and Subtopics to Remember

1.Projects that you mention make sure you

aware it fully.
2. STA concepts
3. Vlsi design
4. Physical design concepts
5. Digital electronics
6. Verilog concepts
7. Basic c
8. Vlsi architectures
9.basics of semiconductors

Sources of Preparation

STA --- VLSI EXPERT
VLSI DESIGN --- class notes
Physical design -- course by indraneelsen Gupta
C - geeks for geeks
Vlsi architectures - class notes
Verilog - sumit palnitkar book

MediaTek India Technology

Bangalore, Karnataka, India

Electronics

Compensation Offered (CTC) : 15 LPA

VLSI (Physical Design, STA)

CGPA: 7.55

Recruitment Procedure

1st Round:

Initially, there was a written test for about 70 mins which had three sections. First section was aptitude which was a bit tough compared to the rest of the companies I have faced. Then, there was a section which consisted of basic electronics questions from what we had learnt during our Bachelors. This section was relatively easier. Last section was related to our digital domain. Questions were mostly on Verilog HDL(blocking vs non-blocking), Waveform based Questions, FSM Design, Boolean Neutral and Dual Functions, Delays in Sequential Circuits, Counter Based Sequential Design, STA-Theoretical.

Most important thing to be remembered was that there was a sectional timing cutoff. So, please keep checking your sectional time periodically.

2nd Round:

It was a Technical Interview Round. Interviewer asked me why I would like to join VLSI Field when I am from an Embedded background looking at my resume. After that he directly went on to ask technical questions. I have got questions from Latch Up in CMOS. He asked me to draw SR NAND and SR NOR Latches. He asked to draw all the six basic gates using MUX. Then, he asked me to write Verilog Codes for all the above drawn circuits. Be prepared with Verilog codes of various kinds of circuits and for various conditions. Then, he went onto test STA (definition of setup and hold times, which of them can be negative and why, does hold time not depend on frequency in all the cases). He asked to explain Physical Design Flow in detail each and every step and he questioned at every stage of my explanation why it is like that. Also, learn Verilog codes for Asynchronous Reset, FSMs, Sequence Detectors, Gray Code Counter and Universal Shift Register (Suggestion for other Companies).

Important Topics and Subtopics to Remember

VLSI Design, Verilog HDL, Static Timing Analysis, Digital Electronics(Design Related), Latch Up in CMOS, Physical Design Flow(Each Step in Very Much Detailed Way), FPGA Design Flow, SoC Design Flow, Cache Memory.

Sources of Preparation

1) Pravin Mane Sir Class Notes, Weste, Kang, Rabaey and Digital IC Design (NPTEL) from Janakiraman Viraraghavan for VLSI Design.
2) Karthik Vippala, Yash Jain, Technical Bytes, ElectroTuts, Team VLSI(Important) Youtube Channels, Udemy Course by Kunal Ghosh and VLSI Expert Website for STA.
3) vlsiuniverse(explore it deep), asic-world(read), hdlbits(practice), fpga4student(basic projects) and chipverify(read) websites for Verilog HDL. Also, vlsiuniverse website has experiences of various companies like MediaTek, Texas, ARM, Intel, Qualcomm etc. FSM based questions in this website are of a very good level to practice.
4) Verilog HDL from Component Byte, Samir Palnitkar and Indranil Sen Gupta.
5) Physical Design Flow from Maven Silicon and NPTEL Youtube Channels.
6) Digital Electronics from Unacademy Ankit Goyal and Bhima Shankar, Anand Kumar Text Book for FSMs and Counter Related Questions, GATE PYQ's and DIGI-QS Question Bank.
7) Cache Memory Concepts from Ravindra Babu Ravula CSE Channel, Patterson-Hennessy

Additional comments

Be prepared very well before the company comes. Don't prepare in hurry just in one or two days before the arrival of the company. Don't keep thinking about what is the next company that would arrive. Keep checking how much you have done and how much is yet to be done from time to time. Be well prepared very much before the arrival of a company.

MEDIATEK

Bangalore

Electronics

Compensation Offered (CTC) : 23.80 LPA

VLSI (Physical Design and STA.)

CGPA: 7.22

Recruitment Procedure

First Round -

It was a written test of about 75 mins. It consists of three parts. First was aptitude which was moderate to tough. Then there was basic electronics which consisted of basic questions related to analog, digital, edc and network theory. They were pretty easy. Last round was related to domain (In this case, it was VLSI). Questions were mostly on FSM Design, Counter Design, STA, delay/Hazards(waveform based) and FIFO. Questions were lengthy and on a tougher side.

There was sectional timing cutoff but one can switch anytime between sections and no negative marking

Second Round

It was a technical cum HR interview. Started from basic introduction and then the interviewer asked me why I wanted to join VLSI being from embedded background. After that he shifted to technical domain and asked questions from FSM (difference between mealy and Moore and reason for each difference). STA (definition of Setup and Hold time, Which of them can be negative and why, What is the effect of PVT on setup and hold on STA). Then he asked me two puzzles which took about 25 mins. After that he gave me a case asked to draw its fsm. Then some general technical questions(difference between digital and discrete signals) and at last, we had a general discussion like my family background, if I will be comfortable in script writing, scene of covid at my native, my experience in bits and like wise.

Total it lasted around 75 mins.

Important Topics and Subtopics to Remember

Important topics specific to my interview

FSM's, Verilog, STA, CMOS circuits, ASIC design flow and Clock Domain Crossing

Sources of Preparation

Digital Electronics-DIGI-QS book and Gate PYQ's, Verilog- Samir Palnitkar and Verilog FAQ by Shivkumar, VLSI Architecture- Gurunarayan Sir's Lectures, VLSI Design-NPTEL lectures by Jankiraman Sir, Physical Design and STA- NPTEL Lecture by Indranil Sen Gupta Sir. Apart from that there are various good YouTube playlists(Karthick Vippala, Technical Bytes, Team VLSI etc.) and Udemy courses(Kunal Ghosh) which are useful for interview specific questions.

Additional comments

Try to explain answer in as simple way as you can.
Never try to bluff. If you don't know anything say politely that you can't recall it. They check attitude more than aptitude so it's still fine if you can't answer everything
Be confident and calm always.

MEDIATEK

Bengaluru

Electronics

Compensation Offered (CTC) : 23.80 LPA

Physical Design and STA

CGPA: 7.1

Recruitment Procedure

Round 1 : Online test. It consisted of two sections. In the first section aptitude and reasoning was there and in the second section most of questions were from digital electronics alongwith basics of analog and RLC circuits.
Round 2 : It was technical cum HR round. Interviewer was very cooperative. It was more of conversastion. Questions on flip-flops,FSM and STA were asked. He also asked me to solve few puzzles.

Important Topics and Subtopics to Remember

FSM,STA,Verilog,Digital Electronics,Digital VLSI Design

Sources of Preparation

DIGI QS , Verilog faq by shivakumar

Keep smilling , be expressive , don't hesitate to ask and be honest while answering.

MediaTek

Electronics

STA/Synthesis Engineer

Bangalore

Compensation Offered (CTC) : 14.80 LPA

CGPA: 8.06

Recruitment Procedure

Round 1: Online Test
The test had three sections with increasing level of difficulty. Aptitude, Basic Digital and then Advanced Digital Electronics.

Round 2: Technical Interview
There were two panelists in the interview and one of them was the manager. He started with the first question as 'You are from ME Embedded Systems, what have you learnt in the field of digital electronics to apply for this profile ?'. He also asked me why I left my first job, what was the good part and bad part there etc.
Then they started with technical questions. Topics were -
Setup time and Hold time in detail, Logic gate design using Mux, Static and Dynamic power in VLSI, What contributes to dynamic power, How to reduce the power consumption, Power and Area requirements of using four 8:1 Mux vs using one 32:1 Mux, Clock gating.
He asked me to design a digital circuit for clock gating and then gave some clock signal and then asked me to modify it in such a way that clock gating will take place only at the posedge of clock. RISC Processor, Project explanations, Design of a Sequence detector.

Puzzle Question: A moderately difficult question based on Rubik cube's edges and faces.

Important Topics and Subtopics to Remember

VLSI Architecture
VLSI Design
Digital Electronics
Verilog HDL
In and outs of your resume

Sources of Preparation

Digi_Qs_full.pdf given by the seniors,
NPTEL lectures for Verilog and RISC,
VLSI Design lectures
PU Chronicles

Additional comments

Only two things matter in the placements - Your preparation and your luck !!
We cannot do anything about the second but the first one is certainly is in our hands. Be prepared for each and every interview. My luck was in favor for other two companies also, but I wasn't fully prepared so I missed those opportunities. (And the packages of those two companies were more than this company by 10 LPA !!). There is no point in having regret later because the opportunity is missed by that time, so you have to be prepared for each and every interview/test.
Once you are prepared, the key to crack the interview round is simple - Just enjoy each and every interview ! Have fun in the interviews and the job offer will follow.
PS - In case of online interviews, use pentablet with Google Jamboard or OneNote to explain the circuits.

MEDIATEK

Bangalore

Electronics

Compensation Offered (CTC) : 14.80 LPA

Physical Design & STA Engineer

CGPA: 8.54

Recruitment Procedure

Round1: Written test
Includes questions on Digital electronics, General Aptitude (Aptitude part was a bit difficult because of time constraint. we had to solve 8 qns in 10 minutes) and basics of VLSI design It had three sections 1. Aptitude 2. Digital electronics 3. Hardware(combination and sequential circuits based questions)
Round2: Technical Interview
I had only 1 interview while some of my batchmates had two. My interview lasted for 1hr 35mins or so. He started with introduce yourself and went on testing me with questions on Digital electronics.
Question1: A circuit implementation using only NAND gates
Question2: XOR gate implementation using MUX
Question3: Gave some verilog snippet and asked me the hardware synthesized by the code Question4: Difference between case and if else in verilog. Based on the hardware synthesized Question5: Difference between Blocking and Non Blocking statements in verilog Question6: Gave a verilog code and asked me if the usage of Blocking statement in the context of adding delay as per a circuit's requirement was satisifed or not
Question7: on physical design...asked me questions on backend part of ASIC Design flow as to when and where timing analysis is done in the flow.
Question8: on Clock tree synthesis and buffer insertion
Question: Setup hold violations.....when do they occur and how to rectify them
Question9: How to reduce delay in VLSI Design....he asked me various methods to reduce the delay....one of my answers was to use different threshold voltage cells depending on the requirement Question10: He asked me to explain further on HVT SVT and LVT cells and how does that effect delay...he was satisfied with my answer
Question11: Which is the dominant power dissipation in low power circuits
Question 12: Question on clock domain crossing and synchronizers
Question 13: what is metastability
Question14: Use of one-hot encoding
Question15: question on FIFO max data transfer rate given a burst size

So these are most of the questions that were asked to me during my interview...I might've missed out on a few of them.

Puzzles and Analytical ability:
He tested me on logical puzzles(Analytical ability as he called it) in between the technical questions..i had some 4-5 questions like 1)qn on egg dropping problem from geekforgeeks, 2)orange apples in a basket with wrong labels how to identify the correct baskets in one go. 3)How long can a bike travel with one spare tyre. 4)question on two liquid containers to measure a quantity in minimum steps(i dont remember the exact qn). In between he used to pose general background related qns (HR type) like tell me about your BTech and leadership skills. (I had managed an event during techfest in my college....he asked me about it..) and non academic activities. He also asked me as to why there was a dip in my Btech. percentage compared to previous studies...i told him I was much into sports back then, he was okay with it and told me that there are a lot of sporting opportunities in the company and was making me really comfortable..15mins into the interview it was more like a friendly discussion. He also asked me what i knew about the company and some general questions about the industry trends etc

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Important Topics and Subtopics to Remember

Be thorough with your basics of digital electronics and VLSI Design. Apart from these, focus on all the subjects you've learnt as part of the curriculum like CAD for IC design and VLSI Architecture. I wasn't questioned on my projects but most often you will be questioned on them.

Sources of Preparation

Solve digiQS pdf. it's the ultimate compilation of all the good and most probable qns during the interview and written tests. It would give you lots of insights into the type of questioning. Apart from these, revising your basic concepts of all the subjects you've learnt will suffice.
For VLSI Design part refer to vlsiexpert.com.
There are lot of sources to prepare CAD and physical design portions. Apart from these, know about the complete ASIC Design flow and should be able to explain all the intermediate steps in detail. For logical puzzles solve puzzles given in geeksforgeeks. that would be sufficient

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Additional comments

Believe in yourself and be confident. Keep your calm even if you give wrong answers to some of the qns. They mainly check your approach and the interviewer will try to maintain a friendly atmosphere and make you feel comfortable. Speak through your points when you're solving a qn on paper. Be interactive. i had an online interview on webex, where i had to solve the qns and show him my answer sheet Also, you got to know every bit of your Resume and mention only the stuff you are comfortable with

MediaTek

Bangalore

Electronics

Compensation Offered (CTC) : 23.80 LPA

Physical design engineer

CGPA: 7.32

Recruitment Procedure

The Process consisted of 2 rounds ie, Written round and Technical+ Hr Interview.
Round 1:
Written Round:
It consisted of 53 questions time limit was 65 minutes. It had no negative marking. It had 3 sections
1. Aptitude
2. Basic digital electronics
3. Hardware specific section(Verilog, STA etc.)
Each section had its own timer separately. You have to give the answer in the stipulated time. The questions were basic to moderate level . Solve DIGI QS and be thorough with Verilog basics . It can be cleared easily only factor is time the aptitude section was a bit difficult. Speed and accuracy are key. Basics of STA questions VLSI design Verilog FSM were asked.

Round 2:
Personal Interview: It was a single round of interview which combined both technical and HR questions. The questions were mainly from STA and backend mostly. I am listing down the questions below. 1. Explain the whole ASIC design flow in detail.
Describe each step properly with STA mentioned each step from Synthesis to last.
2. What you learnt about each step in your courses.
Tell the Cad for IC course details.
3. Explain your project of Multicarrier communication and draw block level diagram. This was my RP and it was based on %g communication basics. Only Mediatek asked me about this. Other companies did not care about it as it was from other domain. Be through with your projects and RP.

4. Draw cmos inverter. What will happen if u interchange both NMOS and PMOS? It will be a buffer.
5. Draw NAND using CMOS logic and also size it and explain sizing procedure. 6. Draw CMOS NOR gate. Tell what is preferred to use? NAND or NOR?
7. What happens in placement and floor planning step?
8. Why we need STA when you can get slack information in tool output?

To check that each and every path is conforming to timing constraints.
9. STA basics.
10. What is setup time what is hold time. What will happen if we violate it?
11. Write the setup and hold time constraints and explain.
12. What is false path ?
13. What is multicycle path ?
14. What is time borrowing why we need this?
15. What is OCV what is PVT in library
16. What is lib and lef file
17. What is DFT?
18. One ckt was given of AND gate with one i/p =1 and other as clock and other given with latched i/p and output ANDed which should you choose and why?
19. What is crosstalk how to remove that?
20. Given the clck /2 ckt asked to write Verilog code for exactly that ckt.
21. Write a simple Verilog code in data flow and behavioral mode. Why we need data flow and why behavioral mode.
22. Write a basic C prog to get a basic arithmetic operation.
23. Draw XNOR gate. Implement it with 2:1 MUX.
24. What is Enhance mode MOSFET and depletion mode MOSFET.
25. How to solve setup and hold violation?
26. What are typical types of cell in library ;like hvt lvt and svt
27. How to use these cells to reduce violation?
28. Asked about UVM and UNIX command I said don't know asked about perl I did not know. Its ok if you don't know just tell honestly.
29. Why we need to reduce setup and hold violation?
30. When the physical verification happens?
HR questions:
1.Why do you have gap years?
Told about my health issues
2. Are you comfortable in Backend role?
3. Asked abt my role in previous job.

Important Topics and Subtopics to Remember

STA
VERILOG Concepts
ASIC Flow
CAD course

Sources of Preparation

For written test DIGI QS is sufficient . Just practice it properly.
For aptitude you can see online websites like TESTBOOK or any other platform
For STA vlsiexpert.com. Its absolutely necessary. Read it thoroughly.
For Vlsi architecture the class notes are good enough.
For Vlsi design questions Rabey book and class notes and Weste book is good enough.

Additional comments

In placements your preparation as well as luck plays a important role. Remember you may get rejected even after answering all questions in interview (personally happened with me in WD) so never doubt yourself. Keep preparing. All you need is one job. Do not lose hope. And if you have gap please justify it confidently.
Be ready for any question on your RP and projects.
If you feel low never hesitate to contact your seniors over phone. It matters alot, speaking from personal experience. We are all here to help.
All The BEST.

Navi

Bangalore

IT

SDE1

Compensation Offered (CTC) : 29 LPA

CGPA: 7.69

Recruitment Procedure

Round 1: Coding Round:
Test had 3 sections with only MCQ's in them.(Aptitude, CS Fundamentals etc) and there was a specific timer for each section. The 4th section had 2 easy coding questions. one was DP and the other one was based on the 1D banker's algorithm. Last section also had 1 medium coding question with 40 min in hand.

Round 2: Technical Interview:
Interviewer started with the introduction of the company and after that he asked me a really basic question: To find avg of 2 numbers without using any other data type. So we actually spent some time on this question, I gave many solutions for the problem and then he asked me to code that in python and c++. So as per our discussion we were expecting different answers in both the languages for the same code.Finally after some tuning he was satisfied with the solution. Next he asked me an another adhoc question,
Q2 : Given patterns like this A, B, C...Z, AA, AB, AC.....BA, BB, BC.....AAA..... find the nth element.
I was given only 10 minutes for this question. (Because most of the time was spent during discussing solutions for first question)

Round 3: Managerial Round:
After Introduction, Interviewer asked me to design twitter with many features like Retweets, Post, Reactions on post, etc. So he asked me to write a code on google docs and we discussed all the data structures and time complexities. After this he asked me about my internships and projects.

Round 4: HR:
Common HR Questions to find if a candidate is a good fit for the company or not. Likes and Dislikes in general. Difficulties faced during the projects etc.

Important Topics and Subtopics to Remember

DSA, OOP, DBMS and other CDC's as well if your resume is related. Practice some Designing questions as well.

Sources of Preparation

Leetcode and Interview Bit for DSA and Love babbar Whimsicals for CDC's (you can find them on his youtube channel)

Navi

Bangalore

IT
SDE 1

Compensation Offered (CTC) : 29 LPA
CGPA: 8.48

Recruitment Procedure

Coding Round
1. There were 45 MCQs related to Aptitude (around 110 minutes).
2. There were 2 coding questions (around 35 minutes) :
2(a) A bucket with some capacity is given. There is a certain amount of water passed to it (given in form of array).Need to calculate total overflow (easy,greedy).
(b)Don't remember exactly but it boiled down to the basic array subtraction problem (cake-walk,implementation). Problem statement was big.
3. Another coding question. Story of problem reduced to : Tree and one node (not necessarily the 0th node) is given (constraint 1<=n<=1e5, n is number of nodes) and Q queries are asked (1<=Q<=1e5). In each query 2 nodes are given and you need to find the 4th node whose sum of distance to all three nodes is minimum. Can be solved using Binary Lifting.
Solution: Root the tree to the node which is given as input. The answer will be LCA of 2 nodes given in the query. ((n+q)logn complexity). Try to Justify it.

Interviews

Round1 :
1. Given a list of prices of tickets and corresponding days till which they are valid, return the minimum cost one needs to spend for a given number of days. One can buy multiple tickets of the same type.
Solution : We can use n*m dp where n is number of days and m is total types of tickets.
2. Data provided : Friends, things they will spend money on (traveling, money, food etc). Say 4 friends A, B, C, D. Data of form that A spends 50 rupees of C, D on food. B spent 100 rupees on traveling by B, A provided. Find the most efficient way to store the data. I provided a solution using vectors in a way so that less memory is used and there is no loss of data and access is fast.

Round2 :
1. Questions on my work experience.
2. One of my work was based on Dependency Injection. He asked me to design my own and how I will do constructor injection. How I will inject in cases of multiple implementations of the same interface class.
3. What innovative thing I did in my Internship.

Round 3 (cultural fit round):
Why I took coding, when I decided to, what I want to do if I have a lot of money etc.

Important Topics and Subtopics to Remember

DSA, Aptitude, OOP and DBMS questions.

Sources of Preparation

GFG interview archives and last minute notes. Interviewbit last minute notes. Design videos on YouTube. Competitive Coding, Leetcode, InterviewBit for DSA round.

Additional comments

Don't be overconfident, Nervous. Coding questions have more weight usually than MCQ's. Don't talk about things like how challenging your internship was but what you did finally is the only thing that matters.

NXP Semiconductors

Noida

Electronics

Compensation Offered (CTC) : 15 LPA

Design Engineer

CGPA: 7.9

Recruitment Procedure

Round 1: Paper:
1. Contains subjective and objective questions.
2. Try to solve DigiTS provided by BITS
3. Also, don't only answer the questions but also remember why you answered only those questions, Interviewer asks you about the questions you answered like don't blatantly guess any answer they will ask you why you answered this question
4. Try to do the digital and analog both part to get more in the game

Round 2: Technical Interview:
1. Interview will be of fixed hours so be crisp with your answers
2. Do not try to answer every question with anything random; they won't be impressed by that.
3. Be clear about your projects they'll ask you deeply about them
4. Try to practice sample verilog questions and how to answer them in interviews
5. Important topics like STA, MIPS, Pipelining and other concepts should be on tips to always be answered.

Important Topics and Subtopics to Remember

STA, MIPS, Pipelining, LOGIC FAMILY, Gates,

Sources of Preparation

Try to prepare with all the materials provided by BITS

Additional comments

Also go for J.M. RABAEY for expertise in digital

Paypal

Bangalore

IT

Compensation Offered (CTC) : 12 LPA

SDE

CGPA: 8.48

Recruitment Procedure

1. Coding Round (2 questions, 1.5 hr)
First question was basic backtracking + depth first search problem, very similar to the rotting oranges problem (https://leetcode.com/problems/rotting-oranges/) from leetcode, but slightly difficult as compared to this problem.
Second was a hard problem of Recursion, but recursive code was not efficient, I tried memoization also but certain edge cases were not passing. Only a few students were able to solve it completely.
Those who were able to solve 1.5 questions were selected for Interviews.
2. 1st round: Technical Interview (1hr)
Only DSA questions were asked in this.
First Question : Given a string containing Parentheses print the length of the longest substring which has a sequence of valid parenthesis.
eg : “()({[]}[]))()” , ans: “()({[]}[])”
This problem is the combination of (https://leetcode.com/problems/valid-parentheses/) + (https://www.geeksforgeeks.org/print-longest-substring-without-repeating-characters/)
First she asked me to write the code to get the length and later she modified the question to print the substring.
Second question was also the variation of the first question, I have to print all the possible longest substring with valid parenthesis.
3. 2nd Round: Technical Interview (1hr)
This round was taken by the senior level manager. Firstly he asked me about the first round and my approach to solve it. Then he asked me about Stacks and asked me to implement it. Then, he asked me to implement heaps and merge sort algorithms. Later the implementation of hash maps with some variations. After that he jumped on my projects. One of my projects was on reverse shell scripting, so he asked the basics of networking and socket programming along with some cyber security related questions and some OOP related questions.
4. 3rd Round: manager + DSA round
This round was very short, about 20 mins. Interviewer asked me to introduce myself. And asked a single DSA question which was based on making a custom comparator for sorting an array, and that’s it.
At the end of all the interviews, I was given time to ask the interviewer a few questions. So prepare some good questions. Please please!! don’t ask about the work life balance.

Important Topics and Subtopics to Remember

Must : OOP, DSA
For Non CS people, companies don't ask about OS and CN but if you are sitting for companies like CISCO, you should know the basics of OS and CN.

Sources of Preparation

Leetcode, GFG, BinarySearch.com, PU IT placement questions sheet

PhonePe

IT

Bangalore/Pune

Compensation Offered (CTC) : 30.5 LPA

Software Engineer

CGPA: 8.9

Recruitment Procedure

Round0 : Coding Test
Coding test had 3 questions with 100, 300, 300 points distribution. 300 point questions were quite difficult to solve.

Round1 : Problem Solving and Coding
This round I was asked 4 questions, most of them were of difficulty level similar to Leetcode medium level questions

1. Minimum number of meeting rooms required to finish all meetings (Meeting Rooms II)
2. Given a (unbalanced) BST, select a random node such that all nodes are equally likely to be selected.
3. You are asked to convince your family for something. However each family member has conditions such that if some x, y, z other relatives are convinced only then can they be convinced. Eg. Person B might say that they will be convinced only if Person A and C are convinced. Find if it is possible to convince everyone.
4. Given a graph, detect if it has a cycle or not.

Round2 : Problem Solving and Coding
This round I was asked 3 questions, most of them were of difficulty level similar to Leetcode hard level questions.

1. Divide an array in k subarrays such that the maximum sum of any subarray is minimum.
2. Your college has daily assignments, and the time required for assignment on each day is provided in an array. You have figured out a way of hacking the system and submitting the assignment without doing any work (ie. spending 0 minutes that day). However to avoid suspicion you have decided to not hack more than k consecutive days. Find the minimum amount of time you have to spend doing assignments while not raising suspicion.
3. Given a graph with n nodes and m edges and some k special nodes (1 <= k <= n). Find the minimum distance between any two special nodes. (I wasn't able to arrive at the optimal approach for this question and struggled with its time complexity calculation)

Round3 : Hiring Manager
This round was very chill.
He first asked me to introduce myself, and asked about how my previous rounds were? Asked me about my work experience that I had on my Resume. What tech stack had I worked with?
What was something that could have been improved in any of my previous internships?
What are my Top 2 dream companies?
Even if PhonePe is not my dream company, why was I interested in joining them?
What are my plans in career and how does PhonePe help me? etc.

Important Topics and Subtopics to Remember

DSA

Sources of Preparation

Preparation material provided by PU.
Leetcode
pramp.com

Additional comments

For HM round, have clarity about your goals and be prepared to answer some tough questions that will make you think. Answer them with honesty.

PhonePe

Bangalore

IT

Compensation Offered (CTC) : 30 LPA

Software Engineer

CGPA: 8.48

Recruitment Procedure

Coding Round :
1. Some graph problems checking if can come back to the node and traverse all other nodes.
2. Queries given. Either insert element or find the median or delete element. (Can be solved using multiset, note we could also use priority queue incase delete query was not part of the problem).
3.Problem reduced to finding the number of components in the matrix.
4. Problem reduced to binary search. Some points were given and minimum or maximum distance was to be calculated.

1st Interview:
1.array given, print corresponding answer array where at ith position we need to print kth largest element. For example in an array [4, 3, 2, 5, 6, 7, 1, 0, -4] and the k=4 answer array will be [-1, -1, -1, 2, 3, 4, 4, 4, 4]. Can be solved using priority queue or set in nlogn. I was asked to code it.
2.Transaction problem. We can buy and sell stock (and can buy only after selling). You can do this and you will find the problem.
3.Skyline problem. Google this also. You will find it on the web. Could be solved in nlogn.

2nd Interview:
1. Implement BST with find, insert and return random nodes.
2. Some sequences are given say [2, 3], [2, 4, 3]. You need to print the answer array here 2,4,3. Here the input relation is defined. So in [2, 3], [2, 4, 3] we are told that 2 should come before
3. 4 should come after 2. 4 should come before 3.
Now you need to check if the answer will be unique. For example in input [2, 3], [2, 4] output can be [2, 3, 4] as well as [2, 4, 3]. So here we will return false. In the previous example the answer was true.
It can be solved using topological sort in O(n). You can remove edges and at any moment two nodes with outdegree 0 should not be present.

3rd Interview:
1.My project explanation. Interviewer developed some questions on my project domain and asked me.
2.Asked to design data structures which can efficiently answer 2 types of queries. In both queries I will give a person name. In the first query I need to print all people whose contacts have been stored in that person. In the second query I need to print all people who have contact with this person in their phonebook.
Then I was asked if there would be any problem if there are simultaneous read operations in the data structure and any problem if there is both read and write. How will I resolve it ? (It can be done using locks : semaphore or mutex).
Then I was asked some HR type questions like what type of work I like etc.

Important Topics and Subtopics to Remember

DSA (very Important for all day 1 companies including PhonePe) >>>>OS==DBMS==OOP >>CN .

Sources of Preparation

Codeforces, Codechef, Atcoder, Leetcode, Interviewbit, GFG archives, GFG last minute notes,Interviewbit important OOP/DBMS/OS questions. Youtube videos on design.

Additional comments

Don't be over nice, desperate, rude. Most companies give job only on basis of how much you solve. Coding round ranks can be important and have weight even during interviews in some companies. Having good company on resume can help. But if you don't have these things, don't worry, as long as you have prepared well you will get into one of good companies of your choice.

Many people suggest that keep talking while solving. I experimented this with few companies. And with few other companies I first remained silent for 5 minutes, solved on paper and then started discussing/telling the approach and Interviewer were more impressed in this case. No point in speaking anything coming to your mind. Take your time and then explain.

Qualcomm

Bengaluru

Electronics

Compensation Offered (CTC) : 21 LPA

Associate Hardware Engineer

CGPA: 8.01

Recruitment Procedure

Round 0: Online Test
3 Sections in the test - 20 questions each section (90 min)
1. Aptitude - General questions based on logic and graphs. Not very difficult. Practice a few tests before hand just get a feel of questions
2. C Programming - MCQ type test with questions based on syntax of C, if, for loops, pointers questions 3. Communication/Digital - Questions on SAS, DD, CompArch topics

Round 1: Technical Interview
Asked about my favorite course in BITS, basic DD questions like build universal gates from MUX, what is a state machine etc. Then asked to elaborate on any one of the projects I had done. The interview lasted for an hour and wasn't very technically intensive.

Round 2: Technical interview
This round lasted for 90 min and was more in depth than the previous one. The interviewer started by asking me what is a flip flop, build a JK flip flop using other RS flip flop, D flip flop. Then he asked about async and sync counters. Then he asked questions on FIFOs and their functioning. Then I had to do live verilog coding of a blackbox which takes certain inputs and gives desired outputs. I did not know the OOP concepts which he asked about, so I told him that I hadn't taken the OOP course. Overall, be honest with the interviewer and he/she will guide you if you are stuck. Keep talking about what your thought process is.

Round 3: HR Call
The HR called and asked about my interview process and my office location preference. This was a 10 min call where she elaborated the CTC details

Important Topics and Subtopics to Remember

Digital Design (Counters, FlipFlops, StateMachines), C Programming, ADVD, Verilog, Static Timing Analysis, Computer Architecture

Sources of Preparation

Digital Design - This is the most important CDC for digital preparation. Go through Morris Mano textbook till Chapter 6 fully and try to solve all questions
Verilog - Use Morris Mano and its content to revise verilog. ComponentByte YouTube channel might also be useful

Static Timing Analysis - http://www.vlsi-expert.com/p/static-timing-analysis.html go through chapter 1-3 on this website

ADVD - Revise CMOS NAND, NOR concepts and about how circuits are built

Computer Architecture- You just need basic knowledge of MIPS Architecture and pipelining C -

Use the blogs and quizzes on GeeksForGeeks, they should be enough

NPTEL for some topics might be useful

Additional comments

Be thorough with whatever you know. Practice questions given by PU and also look at previous year chronicles. Solving questions real time is the key, so try solving as many questions beforehand as you can. Trust yourself and good luck!

Qualcomm

Banglore

Electronics

Compensation Offered (CTC) : Company

Hardware Engineer

CGPA: 7.71

Recruitment Procedure

Written Test: 3 sections were in the written test: aptitude, c programming and digital electronics.
Round 1 interview: 5 bit sequence detector both mealy and moore design was asked to be solved with a timer on to note the time taken to solve, frequency divider circuits were asked, overview of any project, basic Verilog questions, basic digital questions like minimum number of gates required to implement a particular function, typical HR questions.

Important Topics and Subtopics to Remember

Verilog, digital electronics

Sources of Preparation

Verilog : nptel lectures of indranil Sen Gupta, hdl bits
Digital electronics: gate notes, digi ques pdf by srikanth alaparthi
STA : Chetan sir lectures (BITS Hyderabad professor), Udemy lectures by Kunal ghosh
Vlsi Design : nptel lectures by Janakiraman
Physical design : nptel lectures by Indranil Sen Gupta

Qualcomm

Bangalore

Electronics
Engineer

Compensation Offered (CTC) : 21 LPA

CGPA: 9.3

Recruitment Procedure

Round -1
1. Questions from pipelining, 5 stage pipelines.
2. Programming logic - string manipulation
3. 3 ants puzzle to find probability of crossing

HR
1. Willing to relocate
2. Strengths and weakness

Important Topics and Subtopics to Remember

VLSI design concepts - STA, CDC
Pipeline in processors

Sources of Preparation

Online materials, lecture notes, reference text suggested by faculty.

Qualcomm

Hyderabad

IT

Compensation Offered (CTC) : 21 LPA

Engineer

CGPA: 7.9

Recruitment Procedure

round 1:
introduce yourself. Then he went on to ask me about my BTech project. Then he started with OS questions. all basic questions from os like deadlock,synchronization,readers writers problem with code. Then he asked me a very simple question of creating a linked list from scratch and then deleting the nth element.

round 2:
introduce yourself. some discussion on projects from my resume. Then he started asking coding questions. three questions were asked. zigzag level order traversal, finding minimum in stack in o(1) and find length of longest increasing subsequence. Then he asked questions like round 1 and at last the concept of pointers, oops questions.

Important Topics and Subtopics to Remember

Operating system is a very important subject and one must prepare it thoroughly besides DSA. OOPS is also important.

Sources of Preparation

The leetcode for DSA was enough for me. core cs subjects from gate notes were sufficient.

Qualcomm India Pvt. Ltd.

Bengaluru

IT

Compensation Offered (CTC) : 30 LPA

Software Engineer

CGPA: 9.27

Recruitment Procedure

Aptitude Test: Simple Quantitative Aptitude Questions, Moderate level C based MCQs

Round 1: Technical Interview (30 min)
- Introduction, 2-3 Simple OOP questions, One puzzle question(GFG puzzles will be great place to prepare), Questions on OS and C
e.g. Inline vs. Macro in C, Static inline function, Bit Manipulation(3-4 questions), etc.

Round 2: Technical Interview (50 min)
- Introduction, One puzzle question(from GFG), 2-3 simple OS questions, FLow of Compilation of C program, Mutex and semaphores, Straight dive into projects(please have deep understanding of your projects),
Significant amount of discussion on my previous job experience(Full stack development).

Round 3: HR
- It seemed it was just a formality. It lasted for 5 min only.

Important Topics and Subtopics to Remember

Majorly OS concepts
- Semaphore, Mutex, Spinlock and examples with codes. Where can mutex be used but not spinlock and vice versa?
- Page invalid bit
- Real Time Systems: Hard, Soft, Firm with example. Priority Inversion, Priority Inheritance, Priority Ceiling
- Memory Management Unit(just concept)
- Priority Inversion and ways to solve
- Memory map/layout of C program

- Virtualization theory
- How to avoid segmentation faults?
- Function pointers
- Binary semaphore vs Mutex, choose one, why?
- Interrupt Service Routine(ISR)
- How to alter volatile variables?
- Race condition? Write a program to show a race condition.
- Virtual Function Table
- Dynamic Memory Allocation in C, Structures, Unions,
- What happens during a system call?

Sources of Preparation

LeetCode(Coding: Basic to Moderate),
InterviewBit(Coding: Moderate to Hard),
GFG(for interview experiences, puzzles)

Additional comments

No questions on DBMS,
Don't panic during interview. Just answer what you know and inform the interviewer if you don't know, clearly(in case of theory question). Interviewer will help you if you try to solve the problem(in case of coding question)

QUALCOMM

Bangalore

Electronics

Compensation Offered (CTC) : 11.50 LPA

ASSOCIATE ENGINEER

CGPA: 8.34

Recruitment Procedure

Round 1 – Online test consisted of 3 sections: Aptitude, C programming, and questions related to the Communication engineering field.

Round 2 – Technical interview 1 (lasted for 1 hr)
(Observation – since my resume pointed out in digital domain the interviewers for both Round 2 and Round 3 were from design verification domain, and it was different for other applicants) The interviewer asked me to introduce myself, talk about the courses I have done, and asked the domain I was interested in. He asked to use a Microsoft whiteboard/one note to draw/write the solution and share the same in the meet. Then he started with the technical round by asking questions that are as follows: 1. You are provided with eight identical balls and a weighing instrument. 7 out of the 8 balls are equal in weight, and 1 of the eight balls is defective. The task was to find the defective ball (either heavier or lighter in weight but the defect was not mentioned) in optimal steps. (Only 5 mins were given to solve it) (The interviewer expected a tree-like structure that would depict the path taken and would branch into multiple nodes depending on the conditions shown by the weighing pan, less in weight, more in weight, and equal in weight).
2. Draw the truth table for two input XOR and XNOR gates. Illustrate these two input XOR and XNOR gates using 2:1 multiplexer only.
3. Write a Verilog code for two-input AND gate and also write a testbench for the same. It should be a proper code following Verilog syntax (starting from module declaration and ending with end module) and not a pseudo code. (In the code for testbench, he expected proper statements that would check whether the outputs of the AND gate were correct or not and then display the result accordingly) 4. Write/explain the chip fabrication process.
5. Swap two variables using C programming using two different techniques. 6.
Draw a divide by two counter using D flip flop.
7. Draw a divide by four counter using D flip flop.

After this, the technical questions were over, and the interviewer asked a few other questions like
1. What do you know about Qualcomm?
2. Will you go for masters? If not, then why?
3. Why should I hire you?
4. Where do you see yourself in the next five years?

After this, the interviewer asked me if I had any questions for him and answered my queries, and the interview was over.
Round 3 - Technical interview 2 (approx. 1 hr)
The interviewer again asked me to introduce myself.
After that, he looked at my Resume and asked few questions related to it – I had mentioned 3 projects related to digital, 1 related to Analog and 1 related to PS1 as an internship, so he told me that almost all my courses and projects pointed that I have an interest in hardware, but there was some work related to web development (which I had done in my PS1), so he asked me to explain why I did web development project if I had an interest in hardware (so make sure you have an answer for everything related to things mentioned in your resume). After explaining it, he asked me to explain the MIPS pipelined processor (it was one of the mentioned projects in my Resume).

Next, he asked me to write a simple C programming code to add two variables and store the result in a third variable. After this, he asked me how the C programming code will be implemented by the processor, which I had mentioned above. (He expected the Ans that the compiler would convert the above C code into machine understandable code and etc). He then asked me to write ASM code (since I had mentioned it in skills and TAship) for the same, i.e., adding two variables and storing it in 3rd variable.

Next he asked me to write a Verilog code (with proper syntax) for a 2-bit adder that will add the inputs only at the positive edge of the CLK cycle and give the output. After that he asked to modify the code so that the output does not overflow (get truncated) if the sum of the numbers exceeds the size of the destination.
Next he asked to explain the different types of counters (ripple and synchronous and the difference between them).

For the next question, he provided a black box that gave the output equivalent to a 2-bit counter and input as CLK and Reset and asked to make a 4-bit counter.
Next, he asked to draw a CMOS design for the NAND gate and explain how the circuit works for different input combinations.
At last, he asked to draw a AND gate using a 2:1 multiplexer.

After that, since he had time, he had a casual conversation with me, wherein he asked about when would I get graduated, what I would be doing in my final year and some questions related to acads, and lastly, he asked if I had any questions for him.

Round 4 – HR Round
It was a short telephonic interview that lasted for around 10 mins. The interviewer took feedback of the entire interview process. Then she asked me whether I had any plans to pursue Masters? And the reason if not going to pursue it. Lastly, she asked about location preference and if I had any other questions for her and the interview was over.

Important Topics and Subtopics to Remember

All the concepts related to DD (able to make simple circuits using basic combinational circuits and gates), Verilog programming, C programming (usefull in the online test), Concepts from Mup and Comp Arch.

Sources of Preparation

The textbooks and reference books used for Courses like DD, ADVD, Comp arch are very usefull. There are a lot of online sources as well for practising the concepts like asic.co.in, hdlbits (for verilog), indiabix, testbook, gatepaper, etc. and youtube channels like technical bytes, NANDland, Neso Academy, and VLSI expert (for STA). Previous year online test question papers and question bank containing the questions asked in previous interview rounds.
https://docs.google.com/document/d/15Pzw4dFGseI2JHNAAH3sozsVfRVntMYiNjZFDEDjdHE/edit?usp=sharing

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Additional comments

Explain the interviewer whatever you are thinking, even if you dont have an answer/optimal answer, they usually look towards your approach, and may even guide you incase you are stuck. This is really helpful incase of an online interview. And let them know if you dont know any particular topic, so that you can move on to the next question instead of wasting your time.

Qualcomm

IT

Engineer (Software)

Anywhere in India

Compensation Offered (CTC) : 30 LPA

CGPA: 8.1

Recruitment Procedure

Round 0: Written Round
This round had 3 sections
Aptitude
C programming
DSA
Aptitude difficulty was majorly medium.
C programming questions were mainly on pointers, recursion, structures, output-basd. The difficulty level was medium to hard.
DSA questions were similar to GATE level questions from arrays, linked list, and Trees.

After the written round, almost 20 students got shortlisted for round 1 interviews from the whole M.E computer science.

Round 1: Technical Interview 1
The first technical interview was conducted by the Director of Engineer in Qualcomm (I check his profile on Linkedin before the interview). The whole interview mainly revolved around my concepts in C programming, Operating systems, and somewhere recursive programming.

The Memory layout of the C program. The complete compilation process and loading of the C program.

He asked me to find the output of some C-programs shared with me during the interview. (I assume it was to check my C concepts)

To allocate memory of NxM 2D array dynamically using the minimum number of malloc. (Answer is 1).

Process Synchronization was asked during the interview. Difference between semaphores and mutex.

The interview asked me about my previous experience before BITS. He asked me to explain the OSI model in computer networks in-depth(I have projects based on networks)

The interviewer asked me to print the N-Fibonnaci series in 2 different ways i.e sequential and recursive.

This round didn't focus on any particular DSA questions for me. The other candidate may have a different experience based on their allotted interviewer.
The round was expected to be of 40 minutes duration but it took around 1.5 hours.

Round 2: Technical Interview 2
The second round was conducted by a staff Engineer in Qualcomm.
He directly asked me to clone a LinkedList with random pointers (Standard Question on LeetCode), the interviewer was only interested in the approach and some basic implementation.

He asked me one more question on LinkedList (I don't remember that)

He then asked me to code the substring function, string copy function with overlapping memory constraints (for example copying on memory location of a string with the same memory location of the same string).

I successfully gave all the answers and the interviewer seems to be satisfied and completed the interview in 20 mins only.

Only 5-6 students were selected at the end of this round.
All the best to all.

Important Topics and Subtopics to Remember

C programming, OOPS, Operating System, Computer Networks, Arrays, LinkedList, and Trees.

Sources of Preparation

LeetCode, GFG, Gate Notes, GFG Mock Quizes, InterviewBit.

Q2EBanking

IT

SDE

Bangalore

Compensation Offered (CTC) : 14 LPA

CGPA: 7.47

Recruitment Procedure

Round 1: was coding round + MCQ
Round 2: Then gave an easy topic for GD. General knowledge topic
Round 3: Technical interview. Asked SQL questions. 1 DSA question.
Round 4: Hiring manager round. Asked about my resume in detail. Asked if I had any questions.
I asked about their what is the growth like in the company
Round 5: Was HR round. Asked basic HR questions. What do you want to join this company? These type of questions

Note Round 1 and 2 were on 1 day
Round 3, 4 and 5 on another day

Important Topics and Subtopics to Remember

DSA, SQL and OOP

Sources of Preparation

PU material . Which included Leetcode and do SQL questions from GFG

Q2ebanking

Bangalore

IT

Compensation Offered (CTC) : 14 LPA

Associate Software Engineer

CGPA: 6.82

Recruitment Procedure

Round 1: Group Discussion
Here we were given a topic on digital payments and given 5 mins time.

Round 2: Technical Interview
q1. String related programming question(Easy)
q2. 1 array question(Easy)
q3. OOPs related question.
q4. Are Strings in Python Immutable? The interviewer asked me this because I used to code in Python. Q2ebanking prefers JAVA because the work here is in JAVA.

Round 3:
Questions on Dbms and Sql.
I was given to write a Sql query(Easy, Important)

Round 4: HR (15 mins)
Tell me something about yourself.
What do you know about q2?
Where do you see yourself in 5 yrs?

Overall, the interview experience was good. The interviewers was okay if we needed some hints.

Important Topics and Subtopics to Remember

Database, SQL, JAVA , DSA

Sources of Preparation

GFG, Leetcode, Interviewbit

Sedemac Mechatronics

Pune

Mechanical/Design

Compensation Offered (CTC) : 13 LPA

R&D

CGPA: 8.13

Recruitment Procedure

Round 1: Aptitude Test
This test involved questions related to mental ability, very similar to what we learned while preparing for NTSE and BITSAT examination. For example: pipes and cisterns, Time and Work, Number system (including various divisibility rules), fractions etc. There were 4-5 questions of permutation and combination. (Easy only when fundamentals are strong)
The main thing to keep in mind while solving the questions is that you need to be fast and accurate because time is one of the major factor here. Only with practice one can minimize the silly mistakes.

Round 2: Technical Test
This test was heavily based on electric circuits and classical mechanics. Concepts of class 11th and 12th mechanics can come handy. Electrical science from 1st year was very useful in solving the circuit based problems. The questions were based heavily on applications side.

Round 3: Technical Interview-1
There were 4 questions asked, to which I had to explain the thought process And also solve it on paper.

Question 1:
This question was entirely based on rotational mechanics. Involved a omega vs torque graph And we were supposed to find omega as a function of time. This also involved the basic concepts of integration as well.

Question 2:
This question was very simple and entirely based on the properties of rotation matrix And some concepts of CAD course, which is a CDC of mech. We were asked to rotation a vector in a way which was giving there.

Question 3:
This was a question based on our understanding of concepts. I was asked how can I find torque practically. By using the concepts of pulley And disk And measuring omega with a tacometer I was able to show them One of the way to get the desired result.

Question 4:
This question was very straight forward, in which I was asked to prove the divisibility rule of 3.
My panel consisted of 2 people And they were very Nice And understanding in nature.

After this round 11 people were selected

Round 4: Technical Interview-2

There were 4 questions asked, to which I had to explain the thought process And also solve it on paper. This interview involved questions from electrical science.

Question 1:
This was based on AC circuit And how to get combined waveform. The concept of clippers and clampers from ES course was very useful here.

Question 2:
This question was based on the time dependent circuit And RC circuit. I was supposed to find the current in the capacitor branch And resistor branch as a function of time.

Question 4:
This question was based on the start Delta formation of resistors And the current in it, which can be found using kvl And kcl.

Again my panel consisted of 2 people, who were extremely supportive throughout the interview.

Finally after this interview 3 students were offered the Job. And receiving a personal call from PU was such a delight!

Important Topics and Subtopics to Remember

Rotational Mechanics
Electrical Science (The course we did in our first year)
Differential Equations
Basic aptitude

Sources of Preparation

Class 11th and 12th Physics NCERT
BITS Lecture notes and slides
NPTEL

Additional comments

Don't mug up anything. Just know your concepts very well And always have faith in yourself. Plus, never ever lie in an interview process. What I think is that they also look for how much honest the student is.

ServiceNow

Hyderabad/Bangalore

IT

Compensation Offered (CTC) : 23 LPA

Associate Software Engineer

CGPA: 7.13

Recruitment Procedure

Round 0 : Coding Test (60 mins) -
The test had 15 MCQs from CS Fundamentals - OOP(Java), OS, DBMS. There was only one coding question. It was a knapsack variation, with weights only. Not very tough, but I could not get the last 2 test cases with O(n^2). Got a majority of MCQs right and 8/10 test cases. Around 20 people were shortlisted for interviews including M.E. students.

Round 1 and 2 did not follow any structure for me, for some others it was 2 DSA questions and fundamentals.

Round 1 : Interview - CS Fundamentals + DSA (60 mins) -
The interviewer just asked my name and branch and started with questions. It felt like a rapid fire. He started with OS since that was on my resume and I had done the course. Questions- What is scheduling? What are some scheduling algorithms? What is paging? What are some paging algorithms? Why is virtual memory needed?
Then he switched to OOP. Questions- Explain 4 basic concepts. What is virtual pointer?
He asked if I knew about compilers. For EEE folks, the best response to these questions is that you haven't done the course but you can try and answer logically. He started asking questions, some of which could be answered with a basic understanding of CS (compilers, interpreters, assembly code etc.) When he asked a more theoretical question I replied with I don't know. This was followed by DBMS, asked why normalization is needed and what are the normal forms. I couldn't answer after a point and he moved on to DSA. I was asked around 8-10 questions in total and I had to code only the last one. Initial 6-7 questions were leetcode easy-medium level questions, I had to only understand the problem, clarify assumptions, state logic and then he would ask follow up questions with variations. Questions from arrays, linked lists, stacks, queues, trees. The last question was a DP question - min cost path in 2D matrix. He just switched the corners to work with and expected clean, working code. This ended the interview. I probably gave 1-2 wrong answers in the fundamentals portion which I corrected immediately after. Around 15 people were shortlisted for the next round.

Round 2 : Interview - CS Fundamentals + DSA (80 mins) -
The interviewer was a senior software engineer and was relatively chill. Interview started with a proper introduction and moved on to my resume. I had a choice to explain one project of my liking. In all

interviews I chose my summer internship project (software, early-stage startup) since it is relatively easier to take the interview into behavioral questions for which you have prepared answers and there is a lot to talk about if you worked in a team. Questions were around my understanding of the product, my role and the challenges I faced. I had answers prepared beforehand. Then he asked what had already been asked in the previous round (best to answer it honestly). The questions followed a similar flow, jumping across topics and asking new questions/variations. At some point in between a codeshare link was given which had my previous round's code. I had to explain the problem and my approach. He then gave two questions, one was a standard BFS question - a transforming strings variation. I had to explain the approach, write pseudocode and explain the time and space complexities. Gave a standard O(length) solution, he was satisfied and in fact helped a lot, almost like a code pair session. Then he gave a tree-DP question- House Robber 3 from leetcode. I got lost somewhere while writing code but he was satisfied with the approach and asked me to dry run for some testcases. Then he asked a standard data structure based design question (parking lot and some follow-ups on that). This followed some questions on DSA theory- what are segment trees, what are red-black trees, hashing, open hashing, closed hashing. Could answer everything (you can refer to notes from the DSA on-campus course for prep). By the end it had almost turned into a discussion about a lot of CS topics. He asked if I had any questions and I asked about his team, challenges he faced and what he likes most about the company. Around 10-12 people were shortlisted for the next round.

Round 3: Hiring Manager Interview - Behavioral + DSA (60 mins) -
The interviewer was the manager of the team which was hiring. The interview started with introductions and moved on to the resume. I talked about the same project again. I was asked more behavioral questions - my takeaways from the project, challenges faced etc. This was followed by some general questions - what is an engineering skill you've picked up recently? what is something you like doing on a break? Then she moved on to DSA. The questions were on hackerrank's interview platform with test cases already present and only some of them visible. I had to understand/clarify the problem, write clean code/debug properly.
The first question was a very standard sliding window question, I could solve this one pretty quickly without any help.
This was followed by a DP question. It was a variation of longest increasing subsequence. I was talking out loud and was given a hint to look at the sample test cases and try to identify a pattern which could simplify the problem to something I knew (longest increasing subsequence). I solved the question in O(n^2), had to debug quite a bit towards the end using the given edge cases. It gave TLE on 4 cases. I told that it can be done in O(nlogn) by optimizing LIS using upperbound and she was satisfied with only the approach. Asked me if I had any questions, I had read up about a recent acquisition by ServiceNow. We had a small discussion on that.

Finally 5 people received offers.

Important Topics and Subtopics to Remember

DSA, OOP, OS, DBMS for non-CS. For CS students I'd recommend revise a bit of everything else as well. Do not ignore the theory taught in DSA (I was asked questions on this in other interviews as well)

Sources of Preparation

Leetcode is enough for a lot of companies. For fundamentals and theory-GFG and class notes are more than enough. There are some decent YouTube channels you can refer to as well.
GFG interview experiences and PU Chronicles helped know more about the process.
Mock tests and interviews from PU/Bootcamps are very important.

Additional comments

Give at least 3 mock interviews incase you are new to tech interviews. There is a rhythm to these interviews which can very well be learnt and would give you a lot of confidence

SIEMENS

Pune

IT

Compensation Offered (CTC) : 14 LPA

GTE

CGPA: 9.02

Recruitment Procedure

Round 1: Written MCQ test
Python, C, C++, JAVA language related questions. There were some logical questions as well. I did not know C++ or JAVA language but still got through the test.
Round 2 : Technical Interview
Interviewers asked for the Introduction.
Then they asked me why I wanted to shift from a Mechanical background to the IT sector. Then they asked me if I have some coding background. I knew python at that time. So they asked me to write a sample code. They basically tested the logic. Then they asked me 1 2 puzzles.
They asked me some mechanical questions as well like the 'equation of state' and if it is valid for ideal and non-ideal gasses. The interviewers were chill. At the end they started explaining how things work in the company.
Round 3 : HR interview
The HR round was very casual. First she made me comfortable by asking some introductory questions.Then she asked me a puzzle. She also asked me if I do coding and how I will be able to shift from mechanical to IT. If i will be able to learn new languages while working. She even asked me about my daily routine. Overall it was a very interactive type interview.

Important Topics and Subtopics to Remember

Thermodynamics, Python, Basics of C or C++

Sources of Preparation

According to the GATE book, Youtube tutorials for the languages.

Additional comments

You should be up to the point and crisp. Communicate well. They test logical things at every point so practice some puzzles online.

Silicon Labs

Hyderabad

Embedded
Software Engineer - I

Compensation Offered (CTC) : 22.50 LPA

CGPA: 7.68

Recruitment Procedure

Round 1: Online Written Test:

A day before the exam, we were given 3 profiles to choose from and we could pick 2 from the choices based on our interests. I have opted for "Software Engineering - Embedded Wireless" as my first option and "Validation Engineering" as my second option. As "Software Engineering" was my first option, questions in the written test were testing my programming skills. The test consisted of 15 questions, 3 coding related questions and the rest 12 were multiple-choice questions(related to programming).

Round 2: Technical Round:
Time: 1hr
The round was more like a discussion. I had 4 yrs of IT experience before joining BITS. So the interviewer asked me the reason for opting for masters after 4 yrs. He asked what I was working on and he also asked me regarding the projects if I had done anything related to embedded systems during these 4 yrs. Told about the projects I have worked on and the rest of the interview went on discussing how I have implemented it. Later he gave me a scenario and asked me to design a system around it. The question was slightly tricky for which I had to use both my embedded project knowledge and knowledge related to my work experience to come up with the solution. Later he asked me questions on OS concepts like semaphores, mutexes etc.

Round 3: Managerial Round:
Time: 45min
This round focused on managerial questions. He asked me to introduce myself. Later he gave me scenarios and asked how I would be managing those (Typical Managerial Round questions). Later he asked a few technical questions based on time complexities and asked me to write the program for quicksort. Later he asked me why I was not opting for a PhD.

Round 4: HR
Time: 30 Min

Typical HR Questions like "where do you want to see yourself after 5 yrs?". Questions related to

the company and products on which the company is currently working. He asked me to suggest 5 creative uses of a pen. and 5 creative uses of a Water bottle for which I was not able to answer properly. Don't expect only company-related questions will be asked in HR Rounds be prepared for unconventional
questions like these.

Important Topics and Subtopics to Remember

OS Concepts, C Programming, Time complexities of various sorting techniques, Not only for this company but being a master's student in embedded systems, companies are expecting knowledge on OS and Programming during the interviews.

Sources of Preparation

Try to solve Questions related to data structures in GeeksForGeeks, LeetCode, Hackerrank as much as you can.
https://www.geeksforgeeks.org/data-structures/

This course by Abdul Bari on Udemy will help in preparing for Data Structures.
https://www.udemy.com/course/datastructurescncpp/

OS Concepts like semaphores, deadlocks etc. and their implementations in any one of the programming languages you are comfortable in.

Apart from these "must-do-coding questions" from GFG will help in written tests.

Additional comments

Most of the interview discussions will be on the project, I would suggest being thorough with the projects you have mentioned in your resume. You should be ready to write the code for the projects you have mentio

Silicon Labs

Hyderabad

Electronics

Compensation Offered (CTC) : 19 LPA

Associate Validation Engineer

CGPA: 8.52

Recruitment Procedure

There were three rounds of interview;
Technical, Hiring Manager, and HR round respectively.

Technical:- This round consisted mainly of projects and work experience that I mentioned in my resume and asked questions on basic transistor level design and Static timing Analysis because that was my project specialization. He was more interested in the approach rather than the solution and asked me to show my work for each question.

Hiring Manager:- He asked the basics of Communication concepts (Modulation Techniques, FFT, sampling/quantization and signal encoding). My experience with tools like Cadence and CST Studio suite also helped here as it highlighted my skills.

Important Topics and Subtopics to Remember

MuE, ADVD, DSP, CommSys, EFME and Communication Networks

Good command over these topics will make the process easier for you and don't stress much over programming languages as that won't be the primary thing your recruiter is eyeing for.

That being said, maintain a decent proficiency on languages like Python, Matlab and C (till pointers, objects and classes would be more than enough)

Sources of Preparation

Razavi for RF and ADVD (along with Chembiyan Sir's lecture series)
Sarang Sir's lectures are more than enough for DSP concepts

Additional comments

Take a 2 min pause and answer with confidence. Wrong answers with a correct approach will still leave a greater impact than plain "I don't know".
It's okay to ask for help when stuck, rather than wasting precious interview time.

Goodluck for your interview process :D

Silicon Labs

Hyderabad

Electronics

Compensation Offered (CTC) : 20 LPA

Validation Engineer

CGPA: 7.56

Recruitment Procedure

Round 1: Written Test : It was approximately 1 hour, questions were mostly from EMFT (Transmission line, waveguide), Digital Electronics and Aptitude.

Round 2: Technical Interview : The interview started with very basics c programming questions eg. Why is the C language preferred in embedded systems? Difference between structure and union. Write a simple structure code, write the C code of finding factorial using function, file handling in C and some basic python questions (what is list, tuple , dictionary).
After this interviewer asked about my project (FPGA Project) in which first he asked about the FPGA design flow in Xilinx vivado then he asked about working of project, he told me to write the Verilog code of clock divider circuit and asked me to explain that, he also asked whether i can suggest any other approach to divide the clock. Some more questions were asked about the other features of FPGA which I couldn't answer, then he asked what will be the effect on the FPGA board if you keep it in -40 Deg Celcius Temp, how will you do the debugging in hardware.

Round 3: Technical + Managerial Interview : The interviewer first opened my resume and asked about my previous studies , my gate rank, why do you have a gap between B.Tech and M.tech?, why did you not join IIT? etc, after this he asked about my cadence project in which he asked about DRC, LVS, parasitic extraction etc, then he moved towards my branch and asked about the architecture of LPC 2378 , Ram , peripherals and other basic questions related to LPC, then he asked about my another FPGA project and asked me to explain it, he also asked whether do you have knowledge about automation using python in the end he told me about the job profile and location.

Round 4: HR Round : this duration of this round was very short ,HR asked some basic questions related to the company and me.

Important Topics and Subtopics to Remember

Digital Electronics, C prog, Python, knowledge about ARM architecture and any one ARM based microcontroller.

Sources of Preparation

Follow some YouTube channels like Back to Basics, Digital Sri, NandLand, Technical byte, component byte for interview preparations.

Tejas Networks

Bengaluru

Embedded
Hardware Engineer

Compensation Offered (CTC) : 11 LPA
CGPA: 7.22

Recruitment Procedure

Round-1: Written Test': Duration:-90 minutes
There were aptitude, digital, analog and network questions. Total 35 questions were asked in which 10 were aptitude questions and the rest were digital, analog and network questions.

'Round-2:Technical Interview': Duration:-40 minutes
1.Introduction about yourself and what i know about tejas networks?
2.Project related to FPGA was asked in detail having deep discussion and also a part of verilog code was told to write.
3.Question related to STA. What is setup time, hold time? How to remove setup violation, hold violation?
4.Questions related to zener diodes.

'Round-3: Technical Interview': Duration:-60 minutes
1.Project on MIPS pipelined processor was asked in detail.
2.Interviewer opened the written test questions and asked some questions. He mainly asked STA questions.
3.Interviewer also opened a pdf and asked a STA question from it. In which he asked about setup time violation, hold time violation etc.
4.Verilog code of mux, counter, frequency divider were asked.
5.Questions on PVT variation in STA were asked.
6.Questions related to digital circuits (e.g. mux, frequency divider) were asked.

Important Topics and Subtopics to Remember

MIPS Processor Design, STA, Verilog, Frequency Divider, Zener Diode

Sources of Preparation

vlsiexpert.com, GATE Notes, Verilog from nptel Indranil sengupta IIT Kharagpur

Tekion

Bengaluru

IT

Compensation Offered (CTC) : 25 LPA

Associate Software Engineer

CGPA: 8.2

Recruitment Procedure

Round 0 :Coding Round
Duration:1 Hr
15 MCQs on basic Aptitude and Computer Science fundamentals
3 coding questions all related to Dynamic Programming
Q1: Similar to paint houses 2 on leetcode
Q2:You are given a string S of the length n consisting of only lowercase English alphabets. If the two consecutive characters in a subsequence have a difference that is no more than k, then it is called a special subsequence. Find the length of the longest special subsequence. Q3:Similar to largest Sub Number on hackerearth
link:
https://www.hackerearth.com/practice/basic-programming/implementation/basics-of-implementation/practice-problems/algorithm/the-next-clue-764ccadf/

Round 1:Technical Round 1
Duration 1.5hrs
Interviewer started by grilling on the resume asking details of my summer internship and other projects that i had mentioned
Q1:Write a production level code for converting a string to int
Interviewer had asked not to use any stl functions and implement a try catch block and handle the exceptions and throw appropriate errors.
Q2:Write a program to print the boundary of the tree.
Cross questions on implementation of struct and how to generalize it and how template actually works
Q3: Basic concepts of OOP:Encapsulation,Inheritance,Diamond lock problem in java

Q4: Question on Operating Systems: Deadlock and its conditions

Round 2:Technical Round 2
Duration 1hr
This interview also started off by discussing my internships
Q1: Longest common subsequence in two strings
Q2: Print the matrix in spiral order without any extra space.
Interviewer stressed a lot on doing it in constant space and was not interested in looking at

other solutions.
Q3:Trapping rainwater problem. He wanted to solve this specifically from stack.
Q4: Question on Databases:
What are indexes?
What are keys and define different types of keys?(lot of cross questions were asked on this and he wanted to know the difference between different keys)
Q5: Questions on Operating Systems
Difference between threads and processes.
Process Synchronization and Semaphores(different types of Semaphores)

Round 3: HR
Duration 30 mins
The interviewer liked one of my projects so she wanted to ask questions on them instead of asking DSA problems which she told me she was planning to ask and she grilled me for good 30-35 mins on one project only and she had asked me every minute detail followed by some basic oops questions

7 students got the offer.
My Experience:
Try to get one good project or internship on your resume since that allows you to avoid some tough questions and you should never lie on your resume you will be asked a lot of questions on them and lying leaves a real bad impression.In my case one of my projects was picked up in almost every interview which helped me avoid some dsa problems.
Interact with interviewer as much as you can and be honest if you are not able to think of something tell him he gives you hints that might unblock you.

Important Topics and Subtopics to Remember

DSA
DBMS
OOPS
OS
Basics of Computer Networks

Sources of Preparation

DSA:Leetcode,Interviewbit
DBMS:Sanchit Jain videos
OOPS:GFG
OS:Class notes/GFG
CN:GFG

Tekion

Bangalore

IT

Compensation Offered (CTC) : 25 LPA

SDE

CGPA: 8.11

Recruitment Procedure

Round 1: Coding Round

15-20 MCQs + 3 Coding questions of different weightage on hackerearth.

MCQs were based on OOP/DSA/DBMS/Networks/OS.
Question 1: based on modular arithmetic and xor.
Question 2: based on DP.
Question 3: Don't remember.

Round 2: Technical Interview

The interviewer asked me about my projects, what tech stack they used and the reasons for choosing them. He moved on to other basic questions like what is Round robin scheduling, difference between Http & Https etc. He then proceeded to DSA questions:
Question 1: Find if 2 LinkedList intersect.
Question 2: In an array whose elements are only either a or b (a and b are given), sort the array in-place using swaps only. This he also made me implement on my local ide.
Question 3: A array is valid if there is at max 1 instance where arr[i]>arr[i+1]. Find if the given array is valid. Question 4: Build a BST from a sorted array.

Round 3: Technical Interview

Interviewer asked me about my internship project. He asked me basic questions on function overloading/overriding and polymorphism. Questions about memory management in OS (paging and Virtual memory) were also asked.
DSA Questions:
Question 1: https://leetcode.com/problems/generate-parentheses/
Question 2: https://leetcode.com/problems/house-robber/

Round 4: HR Interview

Asked me few situation based questions and some questions related to product management. I had interests in ML so he asked how it could potentially be beneficial to the company. It is important to know basic background of the company and the products
it is offering.

Important Topics and Subtopics to Remember

OOP, OS, DSA, Computer Networks

Sources of Preparation

Leetcode, GFG

Additional comments

Texas Instruments

Bengaluru, Karnataka

Electronics
Digital Engineer

Compensation Offered (CTC) : 22 LPA
CGPA: 9.11

Recruitment Procedure

Round 1: Written Test:
It consisted of Aptitude and Digital sections. The difficulty level of the aptitude section was moderate. Digital section required a good understanding of B.E (digital electronics) and M.E (VLSI design, EDC) concepts.

Round 2: Technical Round:
The panel consisted of 2 people. They asked me to present my resume and go through it briefly. There was just 1 round of interview for a duration of 45 mins. They 1st asked me to briefly summarize all the projects written in my resume. I explained the projects along with its applications. They wanted to test my concepts more than my understanding of the projects (depends on who takes your interview). They asked me to write verilog code for a bidirectional 4 bit shift register and then asked me to write its circuit. I was asked the difference between inertial and transport delay. Based on these two delays they gave me a verilog code and told me to write the waveforms. I was given a verilog code (blocking and non blocking statements) and was asked to write the synthesized circuit. I was asked to design a circuit for a 25% duty cycle. I wrote the circuit and they asked me if the circuit would give 25% duty cycle in a practical scenario and if not told me to draw the waveform. I was asked to draw a divide by 2 circuit without T flip flop. I was asked to derive setup and hold constraints for the flip flop based system. Then I was asked to design an inverter with equal rise and fall time constant. Finally I was asked to design a state machine (I chose to do it as a moore machine) whose output is high when the input has three consecutive 1s or 0s. They asked me to draw for both overlapping and non overlapping cases.

Round 3: HR
Whoever got the HR call, all of them were hired. I was asked to introduce myself and then the HR stopped me and asked to say something that is not in my resume. I was not prepared for such a question but still I somehow managed by talking about my hobbies.

Important Topics and Subtopics to Remember

Clock divider circuits
STA
State machine
Verilog code synthesis and delays
Inverter

Sources of Preparation

VLSI expert for STA
Rabaey for inverter
Textbook by Shivkumar for verilog code synthesis and delays

Additional comments

The interviewers want to see your approach to the final answer. So do not directly give the final answer even if you know it.

Texas Instruments

Bangalore

Electronics

Compensation Offered (CTC) : 22LPA

Analog Engineer

CGPA: 8.71

Recruitment Procedure

Round 1: Online Test
There were questions depending on what you have chosen to give the test for – Analog, Digital, Test had both questions on Analog electronics and Aptitude. The time was less so I needed to have practice. Questions were mostly numerical types in the analog section like analysis of RLC circuits, Op-amps, Mosfets, poles, zero, 3db frequency , gain , etc. calculation. Giving PU practice tests is a good idea but they are limited in no. Aptitude questions could be practiced from material provided by PU. Round 2: Technical Interview – 1hr 20min
It started with 2 Interviews asking about me and my resume just a bit, then they jumped on to questions. They were helpful and friendly.
You need to draw responses on the screen using a mouse, pen tablet. There was some problem in webex at my time so I drew on paper to keep it also ready.

Part 1-They started by questions on Electrical Sciences like how would this RC circuit respond to a step input then modified the question to impulse input or changed an element of circuit like open a connection or remove a capacitor and you needed to draw the for various nodes in circuit and specify the time constants at those nodes. All this has to be done intuitively. Your basics need to be very clear for this and Chembiyan Sir's videos are a must for this. There were about 3 questions like this all modified and then re-questioned. Inductors and diodes questions were also asked which my friend later told me.

Part 2- Response of a RC circuit to square wave current input (0 mean) input this could be confusing at times but it was in PU practice material voltage response had to be drawn, the response had abrupt changes in it due to current source they at time tried to confuse me by rehearsing my answer in wrong way so you need to be confident at times. Then they cross questioned that would the voltage go to infinity and if not why so. Ans- square wave has a 0 mean so the same amount of charge is given to the capacitor and then taken.

Part 3-RC circuit in which a capacitor is introduced with a new metal plate, voltage response needed to be drawn with time. You can also ask questions to be sure you go in the right direction. I asked if this introduction of metal plates was instantaneous. I was a bit confused so they helped me by asking me to draw the circuit before and after the metal plate was introduced which made it really easy.

Part 4- Analog electronics
Two op-amp circuits were given one with positive and other with negative feedback. Virtual short concept needed to be applied on negative feedback case to get answer and in positive feedback it would jump to one of Vsat depending on circuit. I gave a detailed explanation of how the negative and positive works like if V+ is not equal to V- in negative feedback the output voltage is such that its (V+ - V-) is reduced, if still it is not equal it keeps on happening till both are equal and Virtual short prevails. This was cross questioned that why the output does not keeps on jumping between +Vsat and -Vsat the answer was slew rate(revising class notes could help) that it takes finite time for voltage to change on output so this jump behavior does not happen. Similar explanation was given for positive feedback that (V+ - V-) is increased till it reaches any of the Vsat.

Part 5- Aptitude
First question was of an ant to go from one corner of the cube to another and the shortest path was to be calculated. It is a common aptitude question.
Second question was to calculate 45 min from 2 candles which could burn for 1hr. I found it very difficult. It took me more time to solve it than any other question. I asked the interviewer for a hint so they asked me to calculate the 90 min mark first. The answer was to burn one candle from both ends and other candle from one end when then candle burnt with both ends is exhausted it would have measured 30 min (half of 1 hr as burnt from both ends) and 30 min time is left for one side burnt candle so now burn it from other end as well so it would measure 15 min. Therefor 30 + 15= 45min
This was a really difficult one but the hint really helped me as it made it a bit simple, this was not a conventional aptitude question so you should be ready for anything in this section.

Round 3- HR Interview
Basic HR interview asked about me,
The semester was online so did it affect your practical, I explained that practical's were taken on software and I used some instruments while doing my projects.
What do you plan to do after this Masters, MTech, MBA etc.
At the end he said that I am recruited.

Important Topics and Subtopics to Remember

ES, Analog Electronics, Microelectronics are most important
ADVD, SAS, Control Sys, ED can also be asked.

Sources of Preparation

Chembiyan Sir's videos.
https://www.youtube.com/channel/UCbASDVRKAJByMa5rz6Uv_lw/playlists
The ES taught is a bit different than what is asked (intuitive analysis for interview) .
Chembiyan Sir's videos are great for that.
Mane Sir's Video for Amplifiers and Frequency Response
https://www.youtube.com/channel/UCK3QxJzyv3adijclAPcZc2w/videos
Behzad Razavi - Fundamentals of Microelectronics
PU preparation material.
https://drive.google.com/drive/folders/1bMR5t_KNBuEaVQdKJgvM_YPUrRRQ-JLe PU mock tests
Class notes.

Additional comments

There are a very few analog profile companies and also they recruit very few students. So it will be a good idea to keep a backup option eg- Digital profile etc.

Please keep in mind there are both Online tests (numerical based) and interviews (intuition based) so be prepared for both. Intuitive analysis, how you get the answer and strong fundamentals are also important
as there would be a lot of cross questioning and modification to questions. Participate in mock interviews by PU and with your peers, be very clear with basics and be confident.
All the best.

Texas Instruments

Bangalore

Electronics

Compensation Offered (CTC) : 24 LPA

Digital Engineer

CGPA: 7.87

Recruitment Procedure

Round 1: Written Test

Divided into three parts (Analog, Digital, Aptitude). I only attempted Digital and Aptitude since I was applying only for a Digital profile. The Digital part mainly contained questions based on DD, Verilog, CompArch, and ADVD (Digital Part). Taking calculated guesses worked the best for me as some of the questions could be answered by looking at the options and seeing which one fits (instead of solving everything from scratch). The Aptitude part had standard aptitude questions which were easy.

Round 2: Technical Interview

I had only one technical interview round, it could be more depending on how they decide to interview that year. Since it was a Digital interview, the questions were almost all based on DD for me.

Initially, they looked through my resume and asked about a project I did. It was a device related project and didn't really ask me anything further on it apart from seeming interested that I had experience in using Cadence Virtuoso.

There were four questions that they asked me in the interview.
Q1 was to design a certain frequency divider (I think divide-by-3) with any flip-flops of my choice. I had to design it again using a 50% duty cycle.
Q2 was to code up a basic counter in Verilog (to which they made me add basic features later like make it an up-down counter, include an asynchronous/synchronous reset, etc.)
Q3 was a boolean algebra question where they wanted me to get a complement of a string (don't remember if it was 1s or 2s) using only certain two operations (I don't remember which ones but it wasn't a difficult question if you knew the basic boolean stuff.)
Q4 was a very basic question on FIFO depth. It was phrased in a bit of a tricky manner initially but after getting stumped for a bit and getting a hint, I saw that the solution was very simple.

Overall, all the questions were actually pretty basic and I definitely encountered similar ones while preparing. It's important to keep calm and keep verbalizing your thought process to the interviewer even if you think you are stuck at some point while solving the problem. When they provide you a hint or additional information, you need to be quick to act on it.

Important Topics and Subtopics to Remember

DD, ADVD, Verilog. CompArch and MuP basics are important too but I wasn't asked about them.

Sources of Preparation

DD: Morris Mano
ADVD (Digital): I used Jan Rabaey but whichever textbook used in the ADVD course works
Verilog: Google/YouTube/Documentation. I think the NPTEL Verilog course on YouTube was what I used
CompArch and MuP: I've heard slides are enough but I'm not very sure

Previous year GATE papers, DD/ADVD Tutorials/Compres/MidSems, and PU-shared interview questions are all helpful for practice

Texas Instruments

Banglore

Electronics

Compensation Offered (CTC) : 25.50 LPA

Digital Engineer

CGPA: 9.41

Recruitment Procedure

Round 1:
Written test with 3 parts - Digital, Analog & Aptitude. Different shortlist for Analog and Digital depending on your performance in those parts. For the Digital part, questions asked are covered in DD course: Mux, K-maps, Logic gates and simplification, making gates using CMOS etc. 2 topics which aren't covered in DD: Glitch, FIFO. I barely solved 3-4 Analog questions. Digital had solved 16 of 20. Aptitude is pretty easy, just need to be quick.

Round2:
Technical interview:(50 mins)
Questions entirely based on DD:
Q1. What are Universal gates? Is Mux a universal gate? Make a NAND gate using a 2-1 Mux.
Q2. Make 3 input, 4 input, 5 input NAND from 2 input NAND. Derive the general formula for the number of gates needed for a n input NAND.
Q3. Make a divide by 3 frequency divider with and without 50% duty cycle. Draw timing diagrams for the input and output.
Q4. Make a digital circuit for the equation Y(t)=A*X(t) + B*X(t-2) + Y(t-1). I made the circuit using D flip flops to store the previous stage. He asked me about the max number of binary digits on each wire too as A, B and X are 4 bit numbers.

I was able to answer all the above questions. For the last question he asked me had I seen these kinds of equations before in courses like SAS and ComSys. I told him that it's been a while since I studied those subjects and didn't remember much right now.

Round3:
Technical Interview:(30 mins)
Was asked to make a circuit such that it will count the number of 1's in a seven digit binary number and give that as the output. Eg: For input of 1100111 the output should be 101 i.e. 5. The circuit was to be made only using full adders. I was stuck and asked for a hint which he helped me with. I gave an approximate solution without using the carry input of the full adder. He later said that the solution can be much simpler if I use the Carry input too and ended the interview.

Round4:
HR interview:(5 mins)
Basic questions about my future plans and would I like to work at TI. Asked me if there was something I wanted to ask about. I asked a little about the kind a of work I might get to do as a Digital Engineer TI

Important Topics and Subtopics to Remember

1) Revise DD completely
2) Solve questions on STA and Frequency divider circuits
3) Be through with concept of universal gates
4) Solve questions on FSM, Moore & Mealy circuits
5) Revise making logic gates using CMOS
6) If possible read up on glitch and FIFO - not asked in interviews but useful for written test
7) Revise Verilog too.

Sources of Preparation

1) Morris Mano DD textbook
2) Online videos for Frequency divider circuits
3) For STA - http://www.vlsi-expert.com/2011/03/static-timing-analysis-sta-basic-timing.html
4) STA and CMOS is covered in Digital portion of ADVD too
5) Solve random questions online for FSM

Additional comments

Be calm during interviews. Let the interview know about your thinking process i.e. say out your thoughts loud while solving questions. If stuck somewhere can ask for a hint if you feel the question is tough. The interviewers are generally helpful and want to know about the process rather than the final answer.

Texas Instruments

Bengaluru

Electronics
Digital Engineer

Compensation Offered (CTC) : 25.50 LPA

CGPA: 8.98

Recruitment Procedure

Round 1: Written Test
It was an MCQ test with three sections: Analog, Digital and Aptitude.
Part-1 Analog Electronics: There were 20 questions in this section consisting of basic R/L/C Circuits, a few basic Mosfet-BJT configurations, 3-4 questions on Bandwidth calculations of different circuits, opamp-based circuits and a few circuits consisting of diodes. These questions do not require many calculations, just focus on fundamentals.
Part-2 Digital Electronics: Again, 20 questions are in this section. Basic digital circuits, 2-3 questions on FSM, 2-3 questions on STA, 2 questions on FIFO Depth Calculation, questions on fault detection-'gates stuck at 0/1', SRAM/DRAM, and remaining questions were on Combinatorial Logic. Part 3 General Aptitude: Basic question one can find in Geeks for Geeks

Round 2: Technical Interview- We only had one comprehensive interview, which lasted about 1.5 hrs. Interviewers asked for an introduction followed by my area of interest. I was asked to present my Resume and elaborate upon all my projects & prior experiences. After that, we jumped directly to the question. I remember a few of the questions

1)Explain Johnson Counter. I was asked to draw the circuit and write a Verilog code on this. I was then asked about Blocking and Non- Blocking assignments. How the output of the code will change in each case. Next, I was told to add intra assignment delays and was questioned on Timing violations due to the delays added and the expected outputs.

2)Explain Moore Machine and Mealy Machine. Advantages and disadvantages in each case. Draw a FSM for detecting a sequence (0 1 1 .....1 0).

3)Implement an EXOR gate using NAND, using 2:1 Mux. Explain CMOS Logic.

4)For a given circuit, what gate would you prefer NAND or NOR? Explain using CMOS logic. Explain the working of SRAM/DRAM.

5)Given two fabricated chips, one with setup time violation and the other with hold time violation which chip is unusable. How to fix the other chip without making changes to its hardware implementation? Also, discussed about few problems that arise during fabrication of I/Cs. Lastly, my interview ended with a few HR type questions.

Important Topics and Subtopics to Remember

Analog: Basic RLC, Microelectronic Circuits and ADVD, Gain and Bandwidth Calculation, Opamp Circuits, Analog Electronics
Digital: Digital Design, CMOS Digital VLSI, Static Timing Analysis, Verilog, CompArch Basics,

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Sources of Preparation

1) Basic RLC Circuits (Chembiyan Sir's Playlist):
https://youtube.com/playlist?list=PL6qRG5-NfbLvagdQOwShX9FMrzb5hSvrq

2) Digital Design: Morris Mano - Combinatorial, Sequential Circuits, FSM, State Reduction, Memory- PLA, PAL, Counters, Timing Diagrams, Metastability,

3) CMOS Digital VLSI: MOSFET basic, Combinational Circuits, basic Inverter properties, Sequential circuits, Transmission Gates, Registers, Latches, Flipflops, Clocks(Skew and Jitter), SRAM/DRAM, Static Timing Analysis , Clock Domain Crossing
Books: Kang, Neil Weste, Rabaey
https://youtube.com/playlist?list=PLLy_2iUCG87Bdulp9brz9AcvW_TnFCUmM

4) MuP Basic and Comparch Basic: ISA Basics, Pipeline, Datapath, Cache basics, Cache Coherence, Virtual Memory
Books:Computer Organization and Design The HardwareSoftware Interface Patterson, John L.

Hennessy 5) Verilog: Verilog HDL by Samir Palnitkar & https://hdlbits.01xz.net/wiki/Problem_sets 6)

BJT& Mosfets: Razavi Electronics 1 & 2

7) Analog Electronics: L.K Maheswari Analog Book

Digital Preparation Material compiled by my friends and me:
https://docs.google.com/document/d/1w_4535JQptPlnh9sgjWy5f8kNc8EUEdZwXXTAr471LI/edit?usp=sharing

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Texas Instruments

Bengaluru

Electronics
Digital Engineer

Compensation Offered (CTC) : 25.50 LPA

CGPA: 8.7

Recruitment Procedure

Round 1: Written test
Aptitude: Easy. Logical questions like ones in this link can sometimes get tricky. https://www.freeaptitudecamp.com/logical-reasoning-puzzles/

Digital: Topics included FIFO depth(2Qs), cross talk reduction techniques,(2Qs), analysis of sequential circuits with 2-3 FFs(2-3Qs), setup time(1Q), use of Mux as gates, self dual functions.

Round 2: Technical interview
The interviewer asked for a brief description of my projects. He did not ask follow-up questions but moved on to ask questions on DD.

Question 1: You have 2 ROM which are 1K x 8 each. Implement a ROM that is 2K x 8. Easy question. I made the diagram on my digital pad. The lower 10 bits are fed to ROM address pins and MSB and MSB' are given respectively to enable port of the 2 ROMs.

Question 2: Write code for 1011 overlapping detector
Interviewer expected me to directly write code instead of state diagrams and equations. So I implemented using a shift register. He told me to not use any instantiations of modules/gates in the detector module which meant I could not define a module for DFF. So, I came up with a purely behavioural model. He also asked me to take a sequence and do a dry run.

Question 3: You have a comparator module with two inputs A and B. It has 2 outputs G and S where G is the larger of 2 nos. and S is smaller of 2 nos. Design a circuit to sort four nos. using such modules. The logic used in the question is very similar to writing a C++ code to compare 4 numbers using if-else.

Question 4: Puzzle: You are blindfolded and have to split a pile of 50 coins that has 10 coins head up such that no. of heads in two piles are same.

Solution: https://www.geeksforgeeks.org/puzzle-39-hundred-coin-puzzle/

Round 3: HR round
The interviewer was very friendly and asked me to introduce myself. I talked about my brief family background, schooling and hobbies.I ensured I did not tell something already on the resume.

Important Topics and Subtopics to Remember

Digital design - STA, use of multiplexer as gates, construction of 2^n mux from 2:1 mux, frequency dividers etc.
Verilog - focus both on theory(blocking and non blocking statements, continuous and procedural statements, all keywords) and coding of any combination or sequential block using different styles. Computer architecture

Sources of Preparation

For DD, I referred to the book by Morris Mano. Further, I supplemented it with following books. These books are extensive but try to cover questions on relevant concepts.
1. Contemporary Logic Design - Randy H. Katz
2. Static Timing Analysis Interview Questions with Answers - Sam Sony
3. Cracking Digital VLSI Verification Interview - Ramdas

PU preparation material
Neso academy on Youtube, especially the videos on state machine.
GATE questions
Verilog - Mane Sir's notes, hdlbits website.
Comparch - Hennessy & Patterson textbook

Texas Instruments

Bangalore

Electronics

Compensation Offered (CTC) : 22 LPA

Digital Engineer

CGPA: 8.01

Recruitment Procedure

There were 4 profiles that Texas Instruments came for - Analog, Digital, Software and EDA(Electronics Design Automation)

Round 1 : Online test consisted of 4 sections (Aptitude (30min), Analog(45 min), Digital(45 mins) and Software (45mins) and based on the profiles applied the sections need to be attempted.

Round 2: Round 2 was a technical interview which was taken by a panel of 2 people. Both the interviewers had a background in Digital Verification and embedded systems. They asked me to use a Microsoft whiteboard/one note to draw the solutions.
The interviewer asked me to introduce myself and based on my introduction and interest in robotics they asked me to design a cleaning robot.
Based on the design the interviewer were cross questioning -
How will the interrupts be used in the robot
The kind of wheels used and the algorithms to be implemented.
How will the robot know which places to clean in a room?

As I had done some work on the processor design and architecture they asked me about the ways to increase the throughput in a processor (Anwer Pipelining) and how pipelining works. Next she asked about implementation of jmp instruction in the pipeline.
As I explained about the jmp instruction and the hazards associated with it she asked me about the ways to minimize control hazards.
What is a cache and how would cache work in a multiprocessor system ?
Explain cache coherence ?
Now the second interviewer took over the interview and they both started asking me questions related to digital electronics.
What is the difference between sequential and combinational circuits and also the difference in their verilog implementation?

Draw a clock divide by 8 circuit and mention its duty cycle ?.
The difference between asynchronous and synchronous circuits ?
Explain clock domain crossing and draw the circuit to synchronize 2 clocks A and B using a synchronizer?
What are the timing constraints in a circuit and give a practical example of a circuit which has both setup and hold violation ?
Draw a state machine which detects 111 in a sequence and also explain mealy vs moore machines ?
What are the encoding schemes for the states in the FSM?
Explain the structure of the verilog code for the above FSM and how would you handle the don't care states ?
Draw a circuit for a number divided by 16 ? (not a divide by 16 counter). The working should be such that the number should be divided by 2 in every clock cycle.
At last she asked me to write the mathematical expression for XOR gate without using any operators?

After that they ended the technical question and asked me if I had any questions for them. I asked about the requirements of the profile and what domain I will be working on if selected. After this my interview was over and they asked me to leave.

Important Topics and Subtopics to Remember

Digital Design(Gates conversion, MUX, latches flip flop designs), Analog and Digital VLSI Design, Computer Architecture(Cache design, pipeline system, STA(Static Timing Analysis)

Sources of Preparation

Advanced Digital design (playlist by Karthik Vippala) – 5hr 7min
https://www.youtube.com/watch?v=4hOo1NeLVUE&list=PLdcY8Cf-O1ZrW51cabfrAjSvbIG0URQ9_&index=13
Moore and Mealy Machines (playlist by Neso Academy) – 2hr 42min
https://www.youtube.com/playlist?list=PL7EBRjpOD5oMfVfP0Ub5j2u4pyWBbXdi5
Static timing analysis (STA playlist by Technical Bytes) – 1hr 33min
https://www.youtube.com/playlist?list=PLPmSCnkkX4qu3y6qEJ8xptEQKKG2_NnDj
Digital Design Interview Questions (playlist by Technical Bytes) – 2hr 1 min
https://www.youtube.com/playlist?list=PLPmSCnkkX4quw-EYO1k_vG04OFVaKvWIC
Flip flops and latches (playlist by Technical Bytes) – 1hr 47min
https://www.youtube.com/playlist?list=PLPmSCnkkX4qvMfSrFZ70uXzUxmSdjU84c

Clock Frequency Divider (playlist by Technical Bytes) – 1hr 3min
https://www.youtube.com/watch?v=AfINILc0WEg&list=PLPmSCnkkX4qtFcm8FZpwHEawvq5eULxwf
Verilog coding : https://hdlbits.01xz.net/wiki/Problem_sets
STA (one of the best site to learn STA) :
http://www.vlsi-expert.com/2011/03/static-timing-analysis-sta-basic-timing.html

Drivelink for Previous Years placement Round 1 (online/written test) for all the electronics companies
https://drive.google.com/drive/u/0/folders/1EYE4SaTF3edNpLUXdyxSPZv9naXY-ODO

Additional comments

The company looks closely at your resume so all the projects and courses mentioned are very important
Many companies follow the same trend and topics of questions which they had followed previously, like asking puzzles.
Resume projects are very important. The interviewer can point out any project of his choice and ask you to explain it completely from the hardware point of view even if it is a simulation project. You should be aware of all the languages that you have mentioned in your resume, if you did your MUP project in Assembly language then you should be familiar with writing basic ALP programs.

Western Digital Corporation

Bangalore

Electronics

Compensation Offered (CTC) : 19 LPA

Product Engineer - Memory Reliability and Testing

CGPA: 9.39

Recruitment Procedure

Written Test: It has 4 sections (aptitude, programming, embedded, electronics). Aptitude is a mandatory section. Among the remaining 3 sections, either 2 or all 3 can be chosen and answered based on time. 20 questions in each section and the duration of the test is 1hr. Correct answer gets 1 mark and the wrong one gets a penalty of 0.25 marks. Questions were simple and focused mostly on basics of the subject.

Round1:
She asked me to introduce myself where I also spoke about my past work experience. So she then asked questions on what I did in my past work experience, what were the challenges I faced in the workplace, and how did I overcome them. I explained her 1-2 instances, she then asked me to explain my project in the resume. I explained my entire project clearly, later she went on to ask 3 questions. one was a simple puzzle, 2nd was about body effect in mosfet and third one was a basic question regarding IC testing. The 3rd was asked because she was from the IC testing team and wanted to check my approach on how I would think of it.

Round2:
Asked to explain my project. I explained my MIPS processor design. He had a couple of questions on how I designed certain modules. So, he asked them and I explained to him how I did that. He then picked up one module in my design and asked me to draw a block level design of that one module. That block level design had muxes and adders. So he then asked me to implement full adder using nand gates. Then nand gate circuit design using mosfets. He then asked me to explain how each transistor responds for each input combination in the circuit. Then he asked me to explain device physics and functioning of nmos and vgs vt vds relations. He then asked me about sram and its functioning and basic questions on noise margins.

Round3:
Here he again picked up 2 of my projects and asked me to explain them and then asked about some real time issues...then showed me the circuits of voltage divider and low pass filter, asked the step response of low pass filter and the output equation. Then he asked me about how

noise can be removed from input signals and some discussion about noise went on. He then explained to me the job profiles available.

Round 4:
This was just explaining job profiles and knowing my interests
Round 5 was a typical HR round.

Important Topics and Subtopics to Remember

Memories (SRAM, DRAM, FLASH), MOSFET functioning and device physics, Basic C programs, CMOS circuit working and noise margins, Digital electronics, Digital VLSI Basics, Verilog HDL, Embedded C basics, Embedded Protocols, ARM Architecture, Data Structures.

Sources of Preparation

Digital Electronics - Gate syllabus revision, DIGI_QS by Srikanth Alaparthi
Digital VLSI - Gate level basics, VLSI Design Class notes,
Verilog HDL - NPTEL lectures by Indranil Sen Gupta, HDL Bits
Embedded - Anupama mam class notes of ESD, Bharatacharya ARM notes, Embedded C by Fastbit academy in Udemy
C programming - geeks for geeks
Data Structures - My code school

Additional comments

All the projects mentioned in the resume must be thoroughly prepared and explained clearly. Project explanation plays a major role in the selection. Make sure to explain them clearly. Certain questions are asked by the interviewers just to check the approach and not for the perfect answer, so even if you don't know the final answer, explain your thoughts on the question and never stay silent. Explain things confidently and clearly.

Western Digital

Bengaluru

Electronics

Compensation Offered (CTC) : 19 LPA

ASIC Development Senior Engineer

CGPA: 8

Recruitment Procedure

Round 1: Technical Interview
He asked me about the memories, its architecture in detail and asked about all the projects I mentioned in my resume.

Round 2: Technical Interview
This round is purely coding based. He asked questions on cache, semaphore, and OS based. Then he asked me about linked lists and to write a flow of coding for doubly circular linked lists.
After that he asked me to write a code:
Ques: write a code to access a content present in a memory location and check whether the 3 and 7 bits of the data present in that location are 1 or 0. If 1, then alter that bit.
After this is he asked me a puzzle on GP

Round 3: Technical Interview
This is purely vlsi based. I mentioned a project on MIPS architecture, he asked everything about it like what is pipelining, how I have incorporated it and how I am managing pipelining hazards.
He also asked me how mosfet works from basic to intermediate like mos capacitor.
Also the ASIC flows in detail.
What are ways to reduce power.
After this a puzzle.

Round 4: HR Round
This round is a chill round. He only asked about my passion and all.

Important Topics and Subtopics to Remember

Mosfet in detail, DSA, ASIC/FPGA flow, Static Timing Analysis, Embedded C
What is volatile means in embedded C like that
Metastability, fsm

Sources of Preparation

Notes given by PU, previous year experience, vlsi expert and DSA and embedded C from udemy

Western Digital

Bengaluru

Embedded

Compensation Offered (CTC) : 19 LPA

Senior Engineer, Firmware Engineering

CGPA: 8.66

Recruitment Procedure

Round 1: Written Exam
The written exam consisted of 4 sections: 1:Reasoning and aptitude, 2:Digital Electronics, 3:Analog Electronics and 4:C programming and firmware basics.

Round 2: Technical Interview 1
This interview started with some questions about my work experience and why I decided to go for masters in Embedded systems and not in Microelectronics. Next the interviewer started going through my resume and started asking about all the Embedded systems related projects in detail. For example, one question was why I had used an internal RC oscillator for the clock in one of the projects that used LPC2378 instead of an external crystal oscillator as the crystal oscillator has higher accuracy.
Similarly all the projects were discussed in detail and he made me explain the design and also cross questioned me on the design choices that were made for that project.

Round 3: Technical Interview 2
This round started with formal introduction, followed by some questions on C programming concepts.
Some questions were:
What will happen if a char type variable is initialized with a 16 bit hexadecimal value ? Will it give a compilation error ? Will it give a warning ? if it compiles successfully, what value will be stored in the variable ?
What will happen if the condition check in a for loop will compare a character type variable to an unsigned int type variable ?

Next I was asked some questions about i2c protocol:
What is the first step to be considered while developing a driver for i2c ?
If the the i2c slave sees a constant 1 on the SCL line. If you are sure that the driver and the hardware is working properly at both the devices, then what can be the issue ? How will you debug this issue ?

Next he asked some questions about Python programming.

Round 4: Manager interview
This round started with basic introduction, family background and questions about my work experience. Why did I leave that job and decide to go for masters? Next the manager explained about the job profiles that she was hiring for and asked me which profile I would like to work in. One of the questions she asked was: Suppose you are working on a very interesting development project and after that project, you are asked to work on the documentation of some project as the next assignment, what would your approach be and what would you do next ? She also had some questions that could be prepared for by going through common managerial questions on the internet.

Round 5: HR Round
This round started with a basic introduction, discussion about my family background etc.
Next question was to explain any one project in my resume on a high level, and then explain some project or group activity that I had undertaken that demonstrated some leadership quality. This concluded the process with the HR executive telling me that the interview process is done and the results will be declared soon.

All the interviewers were very warm and friendly. They encouraged me to come up with my own solutions, and helped me if they felt that I was stuck at some point.

Important Topics and Subtopics to Remember

C programming, digital electronics, communication protocols like i2c, SPI, UART etc. , and in-depth knowledge about all the projects mentioned in the resume.

Sources of Preparation

C programming: C quiz from GeeksForGeeks, YouTube channel: mycodeschool
Digital electronics: Gate Notes and Digi_QS
Some YouTube channels like nandland, Back To Basics
Embedded systems design course content for communication protocols.

Additional comments

The written exam is designed in such a way that we need to attempt each question in less than a minute. So don't be stuck at a single question and keep moving to the next questions if you don't know the answer to any question.

In the interview, always keep a smiling face and answer the questions confidently.
In case you don't know the answer to a question:
Try to give the answers to the questions even if you know some part of it, but are not sure about the exact answer, as mostly the interviewer doesn't expect you to know everything, but it is the approach that matters in the interview. Only in the case where you have utterly no idea what the question is about, say that you don't know the answer, otherwise try to take the discussion (interview) forward with whatever knowledge you have. In such cases you may also start your answer by saying that you are not entirely sure about this topic but would try to answer with whatever knowledge you have.

Western Digital - Sandisk

Bangalore

Embedded
Firmware

Compensation Offered (CTC) : 21 LPA
CGPA: 8

Recruitment Procedure

Round 1:Written test: The exam was of 1hr with 4 sections :Aptitude, c programming, electronics, firmware each section having 15 questions. Aptitude is simple , Electronics section mainly has gate digital and analog questions.
Round 2:Technical interview1: Questions were asked on pointers(how much pointer increments for various data types, finding size of data type without using size of operator), Basic string operations (if string is a palindrome). Many questions were asked on bitwise operators (number is even or not, number of ones in a binary format of a number and went on with few more questions) and linked list (find middle node in linked list, remove duplicate node, delete the node whose address is given without the header pointer).Questions on memory, how is data stored ,various memories ,malloc, free and how does free go to the location to delete.
Round 2: In this round the i was given questions to write code which were also on linked list, strings. He asked me explain projects and asked some questions about them.
Round 3: This round was like a discussion. He drew a circuit with voltage source and ammeter, current source and voltmeter asked me how to avoid having infinite current and voltages in the respective circuits and went to clippers . He gave a gist of all the areas of work in the company.
Round 4: It was also kind of HR. He asked me explain a project.
Round 5: it is a complete HR. It was a normal discussion about hobbies, reallocation ,family background and some personality check questions.

Important Topics and Subtopics to Remember

c programming, Data structures , bitwise operators and projects are most important. Go through digital, analog and networks basics.

Sources of Preparation

For c refer geeksforgeeks(written : snippets and theory, interview: coding questions) and Udemy course is good for basics. For data structures mycodeschool youtube videos and try to cover the concept of all possible questions on the linked list.

Additional comments

Beconfident. Even if you don't know anything after giving a thought to the interviewer,he will give hint or move to the next topic.

Western Digital (WDC) - Sandisk

Bangalore

Electronics

Compensation Offered (CTC) : 27.20 LPA

Senior Engineer

CGPA: 7.58

Recruitment Procedure

Round 0: Written Test
The written test was MCQ type and had 4 sections: Aptitude, C, Electronics and Embedded, out of which, minimum 3 had to be attempted. Aptitude and C were mandatory and from the remaining two, any 1 can be solved. Each section has around 15 questions and the total duration is around 1 hour. The questions were between easy to moderate level.

Round 1: Technical Interview
This interview was moreover like an interaction. There was one panelist. He asked me questions from my resume. I was asked to explain my projects and he asked some questions about it. He also asked some questions from Verilog. This interview went for around 50 mins.

Round 2: Technical Interview
This interview was specific to the profile. There was one panelist. He asked me questions on Digital Electronics, Digital VLSI design and some questions on Verilog. The questions were of moderate level. After that, he asked me to write a C code for the given problem
statement. He first told me to explain the logic/Approach I used to solve the problem and then asked me to write the code. After this, he asked me some questions like "Why this field ?", "Where do you see yourself after 5 years ?" etc. The interviewer was helpful and
was giving me hints whether I am thinking in the right way or not. This interview went for about 1 hour.

Round 3: HR Interview
This was a complete HR interview and I was asked normal HR questions like my introduction, Why left my previous job ?, Any leadership experience ?, Work management etc. This interview went for about 30 mins.

After that, Results came out and I got shortlisted. Total 10 people were shortlisted by the company for 3 job profiles.

Important Topics and Subtopics to Remember

Be thorough with your basic Digital Electronics and from Digital VLSI Design, Cover important topics like Setup and Hold time, Types of Power Dissipation in CMOS circuits, crosstalk noise and crosstalk delay. Also, practice Verilog.

Sources of Preparation

Digital Electronics :- Gate Notes, Morris Mano and Digiqs question bank.
Verilog :- Sameer Palnitkar Book, IN Sengupta NPTEL.
ASIC Design Flow :- CAD for IC Design course notes.
Digital VLSI Design :- Janakiraman IIT Madras NPTEL, Weste and Harris Book.
VLSI Architecture :- Patterson Book.

WESTERN DIGITAL (WDC)- SANDISK Bangalore

Embedded

Compensation Offered (CTC) : 21.20 LPA

ASIC Development engineering

CGPA: 8.35

Recruitment Procedure

Written Exam: 4 Sections- 1) Reasoning and Aptitude 2) Firmware 3) C Programming 4) Analog/ Digital. All questions were mcq based and level of questions was easy to moderate.

ROUND 1: TECH:
Interviewer was polite and first he asked me to introduce myself. Then I was asked about my project RISC processor design. he started drilling the questions like how much you have incremented the program counter. why you have not make 8-9 cycle why only 4. then he asked me if i had 2 instructions then how much time they will take to execute in pipelined and w/o pipelined processor. so my Ist round was about 30-40 minutes.

ROUND 2: TECH:
In the second round he asked me from OS, specially m/o management , how processor and microcontroller boots, ISR execution , what is the toughest code you have written , binary search, remove repeating elements in an array.

ROUND 3: TECH + MANEGERIAL:
In third round interviewer gave me a scenario like if we are given 2 blocks with completely different clock then how they can transfer data from one another, and few basic VLSI design questions than he started talking about his work in the company and he shared his experience.

ROUND 4: HR
Only basic questions were asked like introduce yourself, hobbies, strength and weakness, have you performed any role where u have shown your leadership qualities in your past life, etc. Than he also talked about my role in the company and some work life, etc.

Important Topics and Subtopics to Remember

1. Be thorough with your projects.
2. Good knowledge in RC, VLSI design, and VLSI arch. is required.
3. Basic understanding of Sequential Circuits, and STA.
4. C programming

Sources of Preparation

1. For the VLSI ARCH:- Class Notes, and nptel lectures, Computer Organisation and Design by Patterson & Hannessy.
2. For VLSI design : Follow Kang and Neil Waste.
3. For Verilog: Prof. Indranil lec IIT Kharagpur(Youtube), and Palnitkar Book.
4. C programming: Geeks For Geeks and Tutorials Point.

ZS Associates

Consulting
BOA

Gurgaon or Pune

Compensation Offered (CTC) : 13 LPA

CGPA: 8.47

Recruitment Procedure

Round 1: Automated Round
1.1 - Aptitude - General Apti questions + some English. Basic aptitude prep sufficient 1.2 - Case Study: Had a market entry case with MCQ questions
Based on some given data, recommended steps were asked. Requires some business acumen
1.3 - Video Round: 1 Guesstimate + 1 Behavioral question. Speaking skills, posture, body language, and quality of answers checked

Round 2: Case study
2.1 - Briefing with HR on the basics of the case to be solved
2.2 - 60 minutes are given to solve the case study. Basically have to draw inferences from data, graphs and tables and solve the problems(generally 4). Time-consuming, so need to be quick
2.3 - Case Interview - Happens after case study solving and takes an hour to complete. Discussion on your thought process behind solving each problem in the case study. Mention each and every small detail. Also a few puzzles are asked (prepared from GFG).

Round 3: EBI/FIT Round
Sort of HR round. Questions on resume, basic behavioral questions, why ZS and all. Also, some people were asked to guesstimate in this round.

Important Topics and Subtopics to Remember

Aptitude
Guesstimates
Case Study

Behavioral Questions

Sources of Preparation

Google for everything
Puzzles from GFG

Additional comments

Read about what ZS does, its work culture and people before the interview.