BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI HYDERABAD CAMPUS
FIRST SEMESTER 2024-2025

Course Handout Part II

Date: 01-08-2024

In addition to part I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

***Course No*.** **: EEE F313/INSTR F313**

***Course Title*: ANALOG AND DIGITAL VLSI DESIGN**

***Instructorincharge*: Syed Ershad Ahmed**

Lecture Instructor: **: Syed Ershad Ahmed**

***Tutorial Instructors*: Surya Shankar Dan, Syed Ershad Ahmed and Chetan Kumar**

1.Scope and Objective of the Course:

The objective of this course is to provide an introduction to the fundamentals and practical considerations pertaining to the design of integrated circuits. The scope encompasses both theoretical and practical aspects of analog and digital integrated circuits starting from the basic concepts of MOSFET to major analog and digital building blocks; The importance of CAD tools in IC system design process is also acknowledged and stressed upon accordingly.

2. Course Description:

Moore's Law, Y chart, MOS device models including Deep Sub-Micron effects; an overview of fabrication of CMOS circuits, parasitic capacitances, MOS scaling techniques, latch up, matching issues, common centroid geometries in layout. Digital circuit design styles for logic, arithmetic and sequential blocks design; device sizing using logical effort; timing issues (clock skew and jitter) and clock distribution techniques; estimation and minimization of energy consumption; Power delay trade-off, interconnect modelling; memory architectures, memory circuits design, sense amplifiers; an overview of testing of integrated circuits. Basic and cascaded NMOS/PMOS/CMOS gain stages, Differential amplifier and advanced OPAMP design , matching of devices, mismatch analysis, CMRR, PSRR and slew rate issues, offset voltage , advanced current mirrors; current and voltage references design, common mode feedback circuits, Frequency response, stability and noise issues in amplifiers; frequency compensation techniques.

3. Text Book :

T1: Jan M. Rabaey; Anantha Chandrakasan; Borivoje Nikoli´c, "Digital Integrated Circuits - A Design Perspective", (Second Edition) Prentice-Hall Electronics and VLSI Series. (2003).

T2: Behzad Razavi,"Design of Analog CMOS integrated circuits", McGraw Hill International Edition. 2001.

4. Prime Reference Books

R1: Neil H.E. Weste, David Harris, Ayan Banerjee, "CMOS VLSI Design", 3rd Edition Pearson Education.

Other Reference Books:

R1) Kang. S.M and Leblebici Y., "CMOS Digital Integrated Circuits: Analysis and Design, McGraw Hill International Editions 3rd Edition 2003.

R2) Pucknell D.A., Eshraghian K.,"Basic VLSI design, systems and circuits", Third edition, Prentice Hall of India Pvt. Ltd.

R3) Fabricius E.D., "Introduction to VLSI design", McGraw Hill international editions.

R4) Gregorian R., Temes G.C.,"Analog Mos integrated circuits for signal processing", Wiley interscience publication.

R5) Sze S.M.,"VLSI Technology", Second edition, McGraw Hill International Edition.

R6) IEEE Journals of solid state circuits, VLSI system.

R7) Martin. Ken, "Digital Integrated Circuit Design", Oxford University Press, Inc.

R8) Johns. David A. and Martin K, "Analog Integrated Circuit Design," John Wily & Sons. Inc. 2002.

R9) Michael. L. Bushnell and Vishwani. D. Agrawal, "Essentials Of Electronic Testing For Digital, Memory And Mixed Signal VLSI Circuits. Kluwer Academic Publishers, Third Edition, 2004

5. **Notices:** All notices will be put up on the CMS

6. **Course Plan :**

No of Lec.	Topic To be Covered	Learning Objectives	Ref. to Text Book
	Common Topics		
2	1. Introduction to VLSI Design Methodologies	Moore's Law, Y chart, Quality Metrics of Digital Design. VLSI Design flow	Chapter-1**(T1)** /Chapter-1 (R1)
5	2. CMOS Technology, Design Rules, MOS Capacitances, Scaling	MOS device modeling, parasitic capacitances, MOS scaling techniques, latch-up, matching issues, An overview of fabrication of CMOS circuits, layout, and interconnect modeling;	Chapter-2,3,4 **(T1)**/Chapter-2,3, (4.5) (R1) + Class Notes
	Digital Design I:		
6	3. CMOS Inverter and combinational logic circuits.	Digital circuit design styles for logic, Combinational blocks design.Device sizing using logical effort;	Chapter-5,6**(T1)** /Chapter-4,6 (R1) + Class Notes
5	4. Synchronous system and Sequential circuits design	Synchronous design, timing metrics, Design of flip-flops, Timing issues (clock skew and jitter) and clock distribution techniques;	Chapter-7,10**(T1)** /Chapter-7 (R1) + Class Notes
	Analog Design		
6	5. Advanced Current Sources & sinks; Current Reference circuit,	Basic and cascaded NMOS /PMOS /CMOS gain stages. Advanced current mirrors; current and voltage references design.	Chapter-3,4.5**(T2)** + Class Notes
6	6. Operational amplifier architectures and Feedback circuits.	Differential amplifier and advanced OPAMP design, matching of devices, mismatch analysis, common mode feedback circuits	Chapter-8,9**(T2)** + Class Notes
5	7. Frequency Compensation and Noise	Frequency Response stability and noise issues in amplifiers; frequency compensation techniques.	Chapter-7, 10**(T2)** + Class Notes
	Digital Design II:		
1	8. Arithmetic Block Design	Designing of adders, multipliers, and shifters (to be covered in Flip mode)	Chapter-11 (**T1**)
2	9. Memory Circuits Design	Design of SRAM, DRAM, decoders, sense amplifiers (to be covered in Flip mode)	Chapter-12**(T1)** /Chapter - 9 (R1) + Class Notes
3	10. Design verification & test	An overview of design verification and testing of Integrated circuits.	Chapter-15 (R1) + Class Notes

7. **Evaluation Scheme :**

#	Component	Duration	Weightage	Full marks	Date & time	Nature
1	Quizzes	To be announced	30 %	60	To be announced later	Closed book
2	Midterm	90 min	30 %	60	05/10 - 4.00 - 5.30PM	Open Book
3	Comprehensive	180 min	40 %	80	07/12 AN	Closed book**

** Though the comprehensive exam is a closed book, one A4 handwritten (both sides) formula sheet will be allowed for the entire duration of the comprehensive exam. Only formulas in the sheet are allowed.

8. **Chamber Consultation Hour:** To be announced in the class

9. **Make-up Policy:** Requests for makeup examination will be considered ONLY for extremely serious cases where:

a. Parents of the concerned student have to request the course IC in a signed document for the makeup of their son/daughter.

b. Written & signed documentary evidence needs to be furnished by the Hostel Warden/ID confirming the reason for absence from the scheduled examination.

c. In case of medical emergencies, students must produce documentary evidence from the doctor.

11. **Notices:** All notices for the course will be announced in class and displayed on the CMS simultaneously.
12. **Academic Honesty and Integrity Policy:** Academic honesty and integrity are to be maintained by all the students throughout the semester and no type of academic dishonesty is acceptable.

InstructorInCharge
EEE F313/INSTR F313