Birla Institute of Technology & Science, Pilani
Hyderabad Campus

FIRST SEMESTER 2024-2025

Course Handout Part II

Date: 01-08-2024

In addition to part-I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

Course No.	: EEE F348
Course Title	: FPGA Based System Design Laboratory
Instructor-in-Charge	: Anakhi Hazarika
*Instructor*s	: Aditi Sood

Scope and Objective of the Course:

HDL (hardware description language) and FPGA (field-programmable gate array) devices allow designers to quickly develop and simulate a sophisticated digital circuit, realize it on a prototyping device, and verify the operation of the physical implementation. It combines together the flexibility of a microprocessor and the high performance of an Application Specific Integrated Circuit (ASIC). The ease of programming and debugging with FPGAs, as compared to ASICs, decreases the overall non-recurring-engineering (NRE) costs and time-to-market of FPGA-based products. In this lab-oriented course, students will develop their skills by working on more challenging digital system designs using Verilog hardware description language (HDL) in an industry-standard design environment. Students will also implement real-world designs in field programmable gate arrays (FPGAs) as well as test and optimize the FPGA-implemented systems.

Textbooks :

1. FPGA prototyping by Verilog examples By Pong P. Chu., Wiley, 2008
2. FPGA tutorial by Xilinx (http://www.xilinx.com/training/fpga-tutorials.htm#ISE)
3. Wolf Wayne, FPGA Based System Design, Pearson Edu, 2004.
4. Verilog HDL: A Guide to Digital Design and Synthesis Book by Samir Palnitkar

Course Plan:

The practices are intended to provide hands-on experience on the simple Verilog code writing to implement on FPGA. Further, real-life examples with some interfacing devices will be performed. Finally, some complex problems will be assigned to the students in project mode.

List of Experiments

Intro LAB: Introduction to FPGA-Based System Design and Basic Verilog (1 to 2 classes)
Exp 1a: Demonstration of Design and Synthesis of digital block using Verilog
1b: Verilog modeling style and synthesis results
Exp 2: Implementation of simple combinational design in Xilinx ZED Board
Exp 3: Implementation of simple Sequential design in Xilinx ZED Board
Exp 4: Design of A Counter Using the On Board Clock
Exp 5: Design and implement Finite State Machine (FSM)
Exp 6: Design and implement a traffic light control circuit
Exp 7: Demonstration of IP Integrator
Exp 8: FPGA System Design Using IP Integrator
Exp 9: Hardware Debugging using VIO
Exp 10: Design of an ALU and hardware debugging using VIO
Exp 11: Integrated logic analyzer (ILA) core for hardware debugging
Exp 12: Creating a MAC Using the Xilinx System Generator and Implementation on Hardware

Assignment

Final Project

Evaluation Scheme:

Component	Duration	Weightage (%)	Date & Time	Nature of Component
Regular Lab	2 hours/ week	35%	Regular lab Performance	Open book
Project/Assignment		30%	Will be announced	Open book
Lab Quiz		20%	Will be announced	Closed book
Lab Exam		15%	Will be announced	TBA

Chamber Consultation Hour: Chamber consultation hours of Instructors will be announced separately.
Notices: All notices of this course will be displayed in CMS
Make-up Policy: No makeup is allowed for lab evaluation. The **best n-1** labs will be considered, where **n** is the total number of labs that will be conducted. However, a student can perform the missed experiment in a free time slot available in the lab.
Academic Honesty and Integrity Policy: Academic honesty and integrity are to be maintained by all the students throughout the semester, and no type of academic dishonesty is acceptable.

INSTRUCTOR-IN-CHARGE