

## 1) Clock Divider

### Verilog code:-

```
module clock_divider (  
    input wire clk,  
    input wire reset,  
    output reg clk_div  
);  
  
    reg [3:0] counter;  
  
    always @(posedge clk or posedge reset) begin  
        if (reset) begin  
            counter <= 4'b0000;  
            clk_div <= 1'b0;  
        end else begin  
            if (counter == 4'b1000) begin  
                counter <= 4'b0000;  
                clk_div <= ~clk_div;  
            end else begin  
                counter <= counter + 1'b1;  
            end  
        end  
    end  
  
endmodule
```

## **Testbench:-**

```
module tb_clock_divider;
```

```
    reg tb_clk;
```

```
    reg tb_reset;
```

```
    wire tb_clk_div;
```

```
    clock_divider uut (
```

```
        .clk(tb_clk),
```

```
        .reset(tb_reset),
```

```
        .clk_div(tb_clk_div)
```

```
    );
```

```
    always begin
```

```
        #5 tb_clk = ~tb_clk;
```

```
    end
```

```
    initial begin
```

```
        tb_reset = 0;
```

```
        #10 tb_reset = 1;
```

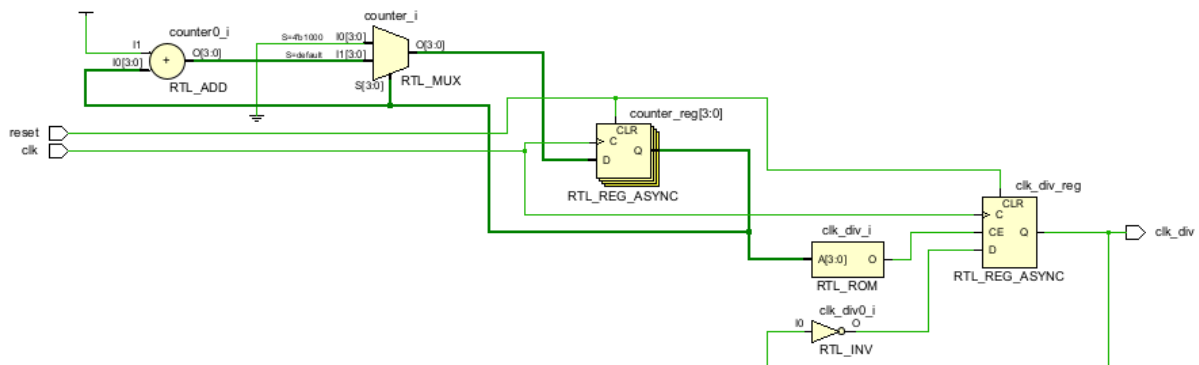
```
        #100;
```

```
        $stop;
```

```
    end
```

```
endmodule
```

## RTL schematic:-



## Synthesis report:-

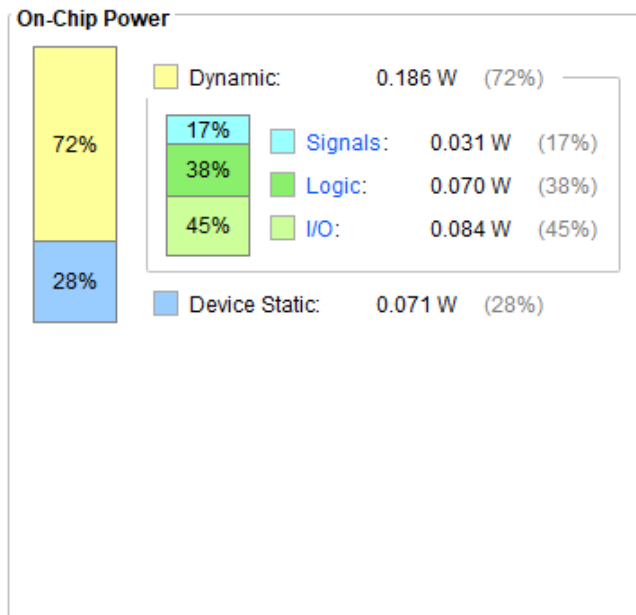
Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/7/23, 3:43	9.0 KB
synthesis_report			9/7/23, 3:43	14.3 KB
Implementation				
impl_1				
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## power report:-

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

**Total On-Chip Power:** 0.256 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 26.3°C  
**Thermal Margin:** 58.7°C (11.7 W)  
**Ambient Temperature:** 25.0 °C  
**Effective  $\theta_{JA}$ :** 5.0°C/W  
**Power supplied to off-chip devices:** 0 W  
**Confidence level:** Low

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## Output:-



## **2) Johnson Counter:-**

### **Verilog code:-**

```
module johnson_counter_structural (  
    input wire clk,  
    input wire reset,  
    output reg [3:0] counter_out  
);  
    wire q0, q1, q2, q3;  
  
    d_flip_flop DFF0 (.D(reset), .clk(clk), .Q(q0));  
    d_flip_flop DFF1 (.D(q0), .clk(clk), .Q(q1));  
    d_flip_flop DFF2 (.D(q1), .clk(clk), .Q(q2));  
    d_flip_flop DFF3 (.D(q2), .clk(clk), .Q(q3));  
  
    always @* begin  
        counter_out = {q3, q2, q1, q0};  
    end  
endmodule  
  
module d_flip_flop (  
    input wire D,  
    input wire clk,  
    output reg Q  
);  
    always @(posedge clk) begin  
        Q <= D;  
    end  
endmodule
```

## **Testbench:-**

```
module tb_johnson_counter_structural;

reg tb_clk;

reg tb_reset;

wire [3:0] tb_counter_out;


johnson_counter_structural uut (
    .clk(tb_clk),
    .reset(tb_reset),
    .counter_out(tb_counter_out)
);


always begin
    #5 tb_clk = ~tb_clk;
end

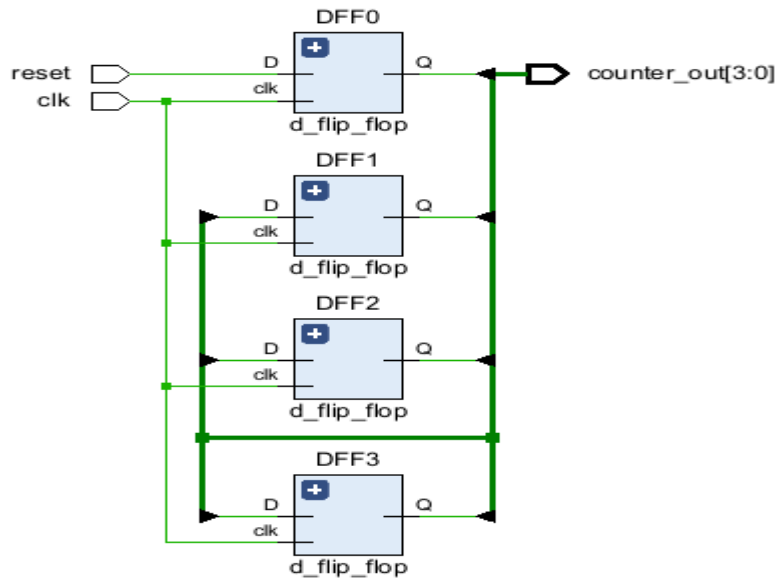

initial begin
    tb_reset = 0;
    #10 tb_reset = 1;
    #30;

    $display("Counter Output: %b", tb_counter_out);

    $stop;
end


endmodule
```

## RTL schematic:-



## Synthesis report:-

Report	Type	Options	Modified	Size
▼ Synthesis				
▼ Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/10/23, 12:01	7.8 KB
synthesis_report			9/10/23, 12:01	14.5 KB
▼ Implementation				
▼ impl_1				
▼ Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
▼ Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
▼ Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## power report:-

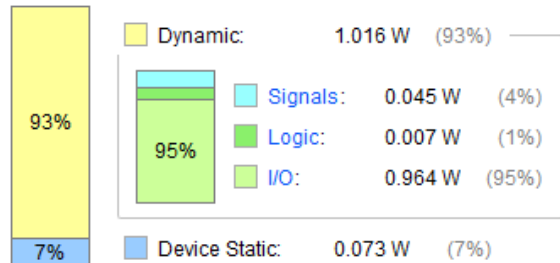
### Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

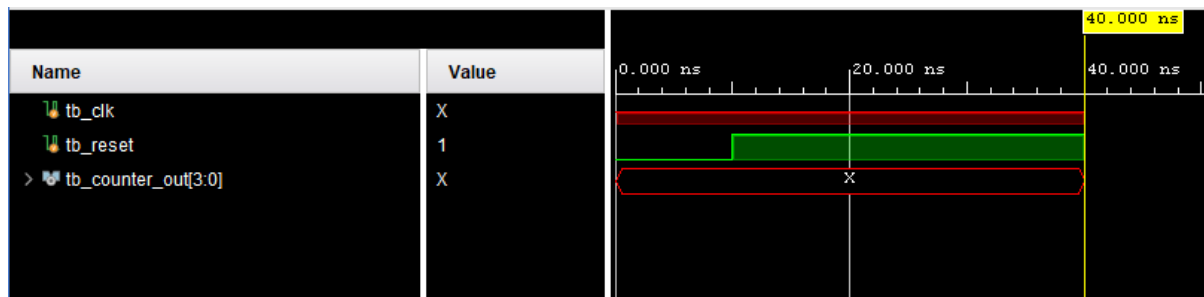
**Total On-Chip Power:** 1.088 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 30.4°C  
Thermal Margin: 54.6°C (10.8 W)  
Ambient Temperature: 25.0 °C  
Effective  $\theta_{JA}$ : 5.0°C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: Low

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### On-Chip Power



## Output:-





### **3) 5 Input Majority Circuit**

**Verilog code:-**

```
module majority_circuit_5input (  
    input wire a, b, c, d, e,  
    output reg y  
);  
  
    always @* begin  
        if ((a & b & c) | (a & b & d) | (a & b & e) | (a & c & d) | (a & c & e) | (a & d & e) |  
            (b & c & d) | (b & c & e) | (b & d & e) | (c & d & e))  
            y = 1'b1;  
        else  
            y = 1'b0;  
        end  
    endmodule
```

## **Testbench:-**

```
module tb_majority_circuit_5input;

reg tb_a, tb_b, tb_c, tb_d, tb_e;

wire tb_y;

majority_circuit_5input uut (

    .a(tb_a),

    .b(tb_b),

    .c(tb_c),

    .d(tb_d),

    .e(tb_e),

    .y(tb_y)

);

initial begin

    tb_a = 1; tb_b = 1; tb_c = 1; tb_d = 1; tb_e = 1;

    #10;

    $display("Input: %b %b %b %b %b, Output: %b", tb_a, tb_b, tb_c, tb_d, tb_e, tb_y);

    tb_a = 0; tb_b = 0; tb_c = 0; tb_d = 0; tb_e = 0;

    #10;

    $display("Input: %b %b %b %b %b, Output: %b", tb_a, tb_b, tb_c, tb_d, tb_e, tb_y);

    tb_a = 1; tb_b = 1; tb_c = 1; tb_d = 0; tb_e = 0;

    #10;

    $display("Input: %b %b %b %b %b, Output: %b", tb_a, tb_b, tb_c, tb_d, tb_e, tb_y);

    tb_a = 1; tb_b = 1; tb_c = 0; tb_d = 0; tb_e = 0;

    #10;

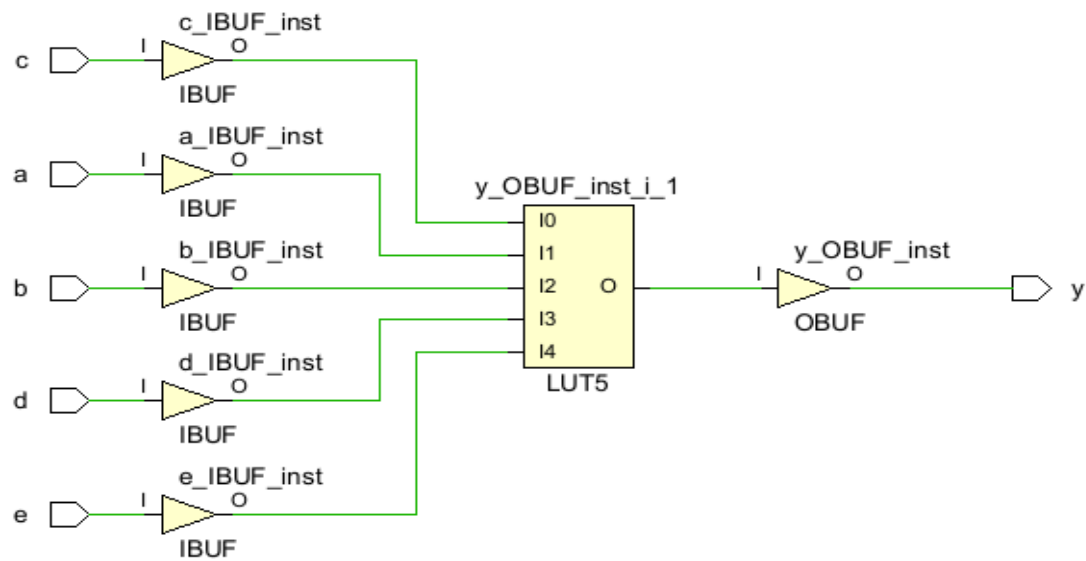
    $display("Input: %b %b %b %b %b, Output: %b", tb_a, tb_b, tb_c, tb_d, tb_e, tb_y);

    $stop;

end

endmodule
```

## RTL schematic:-



## Synthesis report:-

Report	Type	Options	Modified	Size
✓ Synthesis				
✓ Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/10/23, 11:4	7.8 KB
synthesis_report			9/10/23, 11:4	13.8 KB
✓ Implementation				
✓ impl_1				
✓ Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
✓ Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
✓ Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
✓ Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
✓ Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
✓ Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
✓ Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
✓ Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
✓ Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

power report:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:

0.475 W

Design Power Budget:

Not Specified

Process:

typical

Power Budget Margin:

N/A

Junction Temperature:

27.4°C

Thermal Margin:

57.6°C (11.5 W)

Ambient Temperature:

25.0 °C

Effective θJA:

5.0°C/W

Power supplied to off-chip devices:

0 W

Confidence level:

Low

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On-Chip Power

85%

15%

Dynamic: 0.404 W (85%)

96%

Signals: 0.010 W (3%)

Logic: 0.003 W (1%)

I/O: 0.390 W (96%)

Device Static: 0.071 W (15%)

Output:-

Name	Value
tb_a	1
tb_b	1
tb_c	0
tb_d	0
tb_e	0
tb_y	0

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## **4) Parity Generator:-**

### **Verilog code:-**

```
module odd_parity_generator (  
    input [7:0] data,  
    output reg parity  
);  
  
    always @* begin  
        parity = ^data;  
    end  
  
endmodule
```

### **Testbench:-**

```
module tb_odd_parity_generator;  
    reg tb_data [7:0];  
    wire tb_parity;  
    odd_parity_generator uut (  
        .data(tb_data),  
        .parity(tb_parity)  
    );  
    initial begin  
        tb_data = 8'b10101010;  
        #10;  
        $display("Input Data: %b, Parity: %b", tb_data, tb_parity);  
        tb_data = 8'b11110000;  
        #10;  
        $display("Input Data: %b, Parity: %b", tb_data, tb_parity);  
    end  
endmodule
```

```

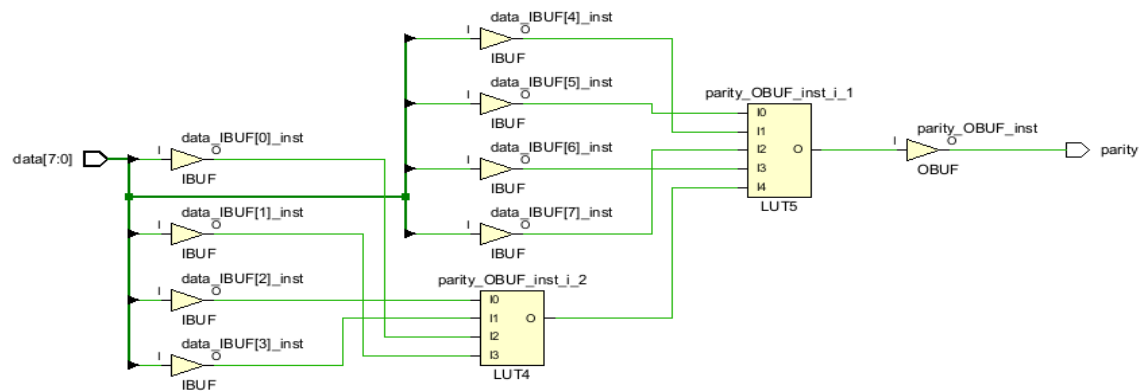
$stop;

end

endmodule

```

## RTL schematic:-



## Synthesis report:-

Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/11/23, 7:31 PM	7.8 KB
synthesis_report			9/11/23, 7:31 PM	12.7 KB
Implementation				
impl_1				
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc		9/11/23, 7:35 PM	4.6 KB
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io		9/11/23, 7:35 PM	72.3 KB
Utilization - Place Design	report_utilization		9/11/23, 7:35 PM	9.6 KB
Control Sets - Place Design	report_control_sets	verbose = true;	9/11/23, 7:35 PM	3.6 KB
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Route Design (route_design)				
DRC - Route Design	report_drc		9/11/23, 7:36 PM	4.6 KB
Methodology - Route Design	report_methodology		9/11/23, 7:36 PM	1.5 KB
Power - Route Design	report_power		9/11/23, 7:36 PM	8.0 KB
Route Status - Route Design	report_route_status		9/11/23, 7:36 PM	0.6 KB
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;	9/11/23, 7:36 PM	12.5 KB
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization		9/11/23, 7:36 PM	6.7 KB
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;	9/11/23, 7:36 PM	1.1 KB
implementation_log			9/11/23, 7:36 PM	25.7 KB
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

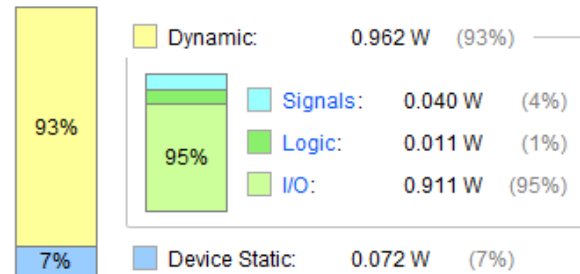
## power report:-

### Summary

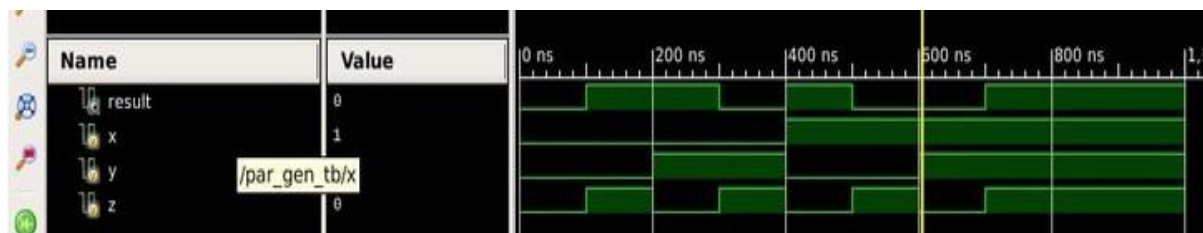
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** **1.034 W**  
**Design Power Budget:** **Not Specified**  
**Process:** **typical**  
**Power Budget Margin:** **N/A**  
**Junction Temperature:** **30.2°C**  
**Thermal Margin:** **54.8°C (10.9 W)**  
**Ambient Temperature:** **25.0 °C**  
**Effective  $\theta_{JA}$ :** **5.0°C/W**  
**Power supplied to off-chip devices:** **0 W**  
**Confidence level:** **Low**  
[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

### On-Chip Power



## Output:-



## **5) Binary to One Hot Encoder:-**

### **Verilog code:-**

```
module binary_to_one_hot_encoder (  
    input [3:0] binary_input,  
    output reg [15:0] one_hot_output  
);  
  
    always @* begin  
        case (binary_input)  
            4'b0001: one_hot_output = 16'b0000000000000001;  
            4'b0010: one_hot_output = 16'b0000000000000010;  
            4'b0100: one_hot_output = 16'b0000000000000100;  
            4'b1000: one_hot_output = 16'b0000000000001000;  
            default: one_hot_output = 16'b0000000000000000;  
        endcase  
    end  
  
endmodule
```

### **Testbench:-**

```
module tb_binary_to_one_hot_encoder;  
    reg [3:0] tb_binary_input;  
    wire [15:0] tb_one_hot_output;  
    binary_to_one_hot_encoder uut (  

```



```

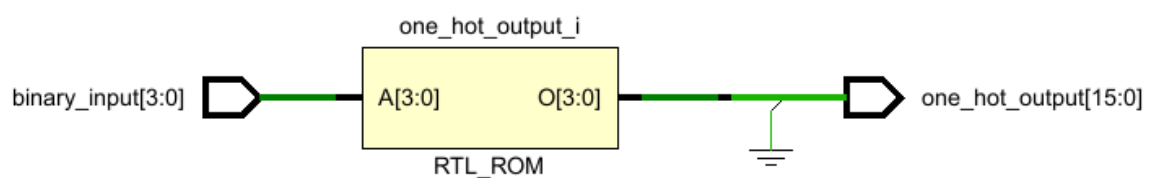
        .binary_input(tb_binary_input),
        .one_hot_output(tb_one_hot_output)
    );

    initial begin
        tb_binary_input = 4'b0001;
        #10;
        $display("Binary Input: %b, One-Hot Output: %b", tb_binary_input, tb_one_hot_output);
        tb_binary_input = 4'b0100;
        #10;
        $display("Binary Input: %b, One-Hot Output: %b", tb_binary_input, tb_one_hot_output);
        tb_binary_input = 4'b1010;
        #10;
        $display("Binary Input: %b, One-Hot Output: %b", tb_binary_input, tb_one_hot_output);
        $stop;
    end

endmodule

```

### **RTL schematic:-**



## Synthesis report:-

Report	Type	Options	Modified	Size
▼ Synthesis				
▼ Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/11/23, 8:06 PM	9.0 KB
synthesis_report			9/11/23, 8:06 PM	14.5 KB
▼ Implementation				
▼ Impl_1				
▼ Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Opt Design (opt_design)				
DRC - Opt Design	report_drc		9/11/23, 8:07 PM	2.6 KB
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
▼ Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
▼ Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

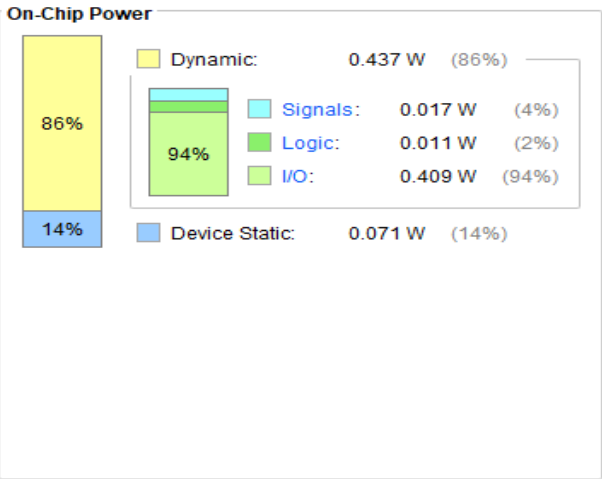
## power report:-

Summary

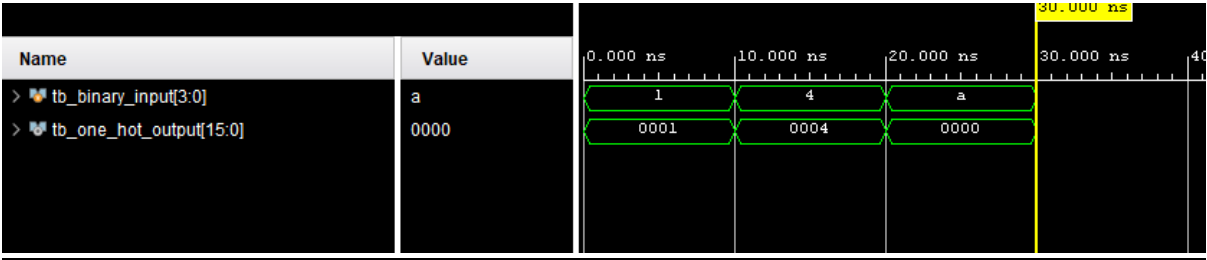
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

**Total On-Chip Power:** 0.508 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 27.5°C  
Thermal Margin: 57.5°C (11.4 W)  
Ambient Temperature: 25.0 °C  
Effective  $\theta_{JA}$ : 5.0°C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: Low

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Output:-



## **6) N-bit Comparator:-**

### **Verilog code:-**

```
module n_bit_comparator (  
    input [7:0] A,  
    input [7:0] B,  
    output equal,  
    output greater,  
    output less  
);
```

```
    assign equal = (A == B);
```

```
    assign greater = (A > B);
```

```
    assign less = (A < B);
```

```
endmodule
```

### **Testbench:-**

```
module tb_n_bit_comparator;
```

```
    reg [7:0] tb_A;
```

```

reg [7:0] tb_B;

wire tb_equal;

wire tb_greater;

wire tb_less;

n_bit_comparator uut (
    .A(tb_A),
    .B(tb_B),
    .equal(tb_equal),
    .greater(tb_greater),
    .less(tb_less)
);

initial begin

    tb_A = 8'b01010101;

    tb_B = 8'b01010101;

    #10;

    $display("Input A: %b, Input B: %b, Equal: %b, Greater: %b, Less: %b", tb_A, tb_B,
tb_equal, tb_greater, tb_less);


    tb_A = 8'b10101010;

    tb_B = 8'b01010101;

    #10;

    $display("Input A: %b, Input B: %b, Equal: %b, Greater: %b, Less: %b", tb_A, tb_B,
tb_equal, tb_greater, tb_less);


    tb_A = 8'b01010101;

    tb_B = 8'b10101010;

    #10;

```

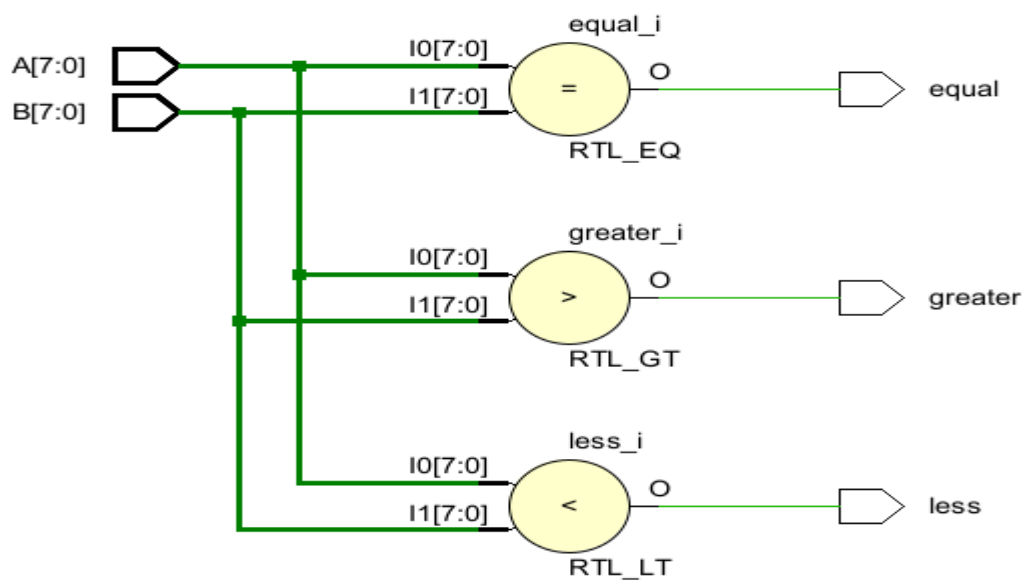
```
$display("Input A: %b, Input B: %b, Equal: %b, Greater: %b, Less: %b", tb_A, tb_B,  
tb_equal, tb_greater, tb_less);
```

```
$stop;
```

```
end
```

```
endmodule
```

### RTL schematic:-



### Synthesis report:-

Report	Type	Options	Modified	Size
▼ Synthesis				
▼ Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/11/23, 11:33 PM	7.9 KB
synthesis_report			9/11/23, 11:33 PM	12.1 KB
▼ Implementation				
▼ impl_1				
▼ Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
▼ Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
▼ Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## power report:-

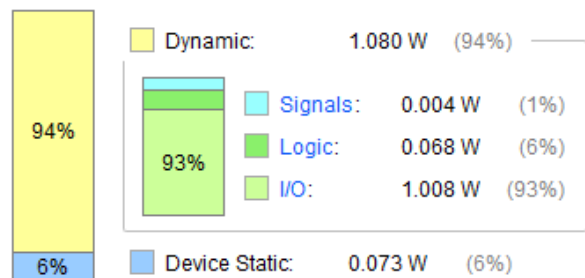
### Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

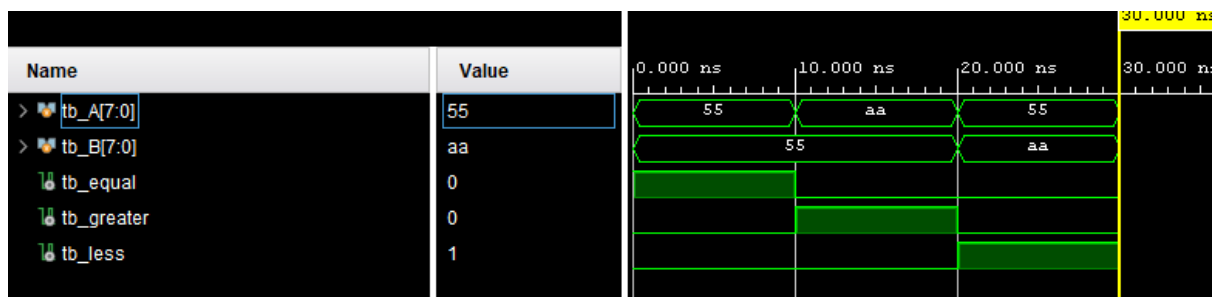
**Total On-Chip Power:** 1.153 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 30.8°C  
**Thermal Margin:** 54.2°C (10.8 W)  
**Ambient Temperature:** 25.0 °C  
**Effective θJA:** 5.0°C/W  
**Power supplied to off-chip devices:** 0 W  
**Confidence level:** Low

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### On-Chip Power



## Output:-



## 7) Fixed Point Restoring Division

### Verilog code:-

```
module fixed_point_restoring_division (  
    input signed [7:0] dividend,  
    input signed [7:0] divisor,  
    output reg signed [7:0] quotient  
);
```

```
    reg signed [7:0] remainder;
```

```
    reg [3:0] count;
```

```
    reg sign;
```



```

always @* begin
    count = 4'd0;
    remainder = dividend;
    sign = (dividend < 0) ^ (divisor < 0);

    while (count < 4'd64) begin
        if (remainder[7] == 1) begin
            remainder = remainder + (divisor >> count);
        end
        else begin
            remainder = remainder - (divisor >> count);
        end
        count = count + 1;
    end
    if (sign) begin
        quotient = -remainder;
    end
    else begin
        quotient = remainder;
    end
end

endmodule

```

### **Testbench:-**

```

module tb_fixed_point_restoring_division;

    reg signed [7:0] tb_dividend;
    reg signed [7:0] tb_divisor;
    wire signed [7:0] tb_quotient;

```

```

fixed_point_restoring_division uut (
    .dividend(tb_dividend),
    .divisor(tb_divisor),
    .quotient(tb_quotient)
);

```

```

initial begin

```

```

    tb_dividend = 8'b000000110;

```

```

    tb_divisor = 8'b000000010;

```

```

    #10;

```

```

    $display("Dividend: %b, Divisor: %b, Quotient: %b", tb_dividend, tb_divisor, tb_quotient);

```

```

    $stop;

```

```

end

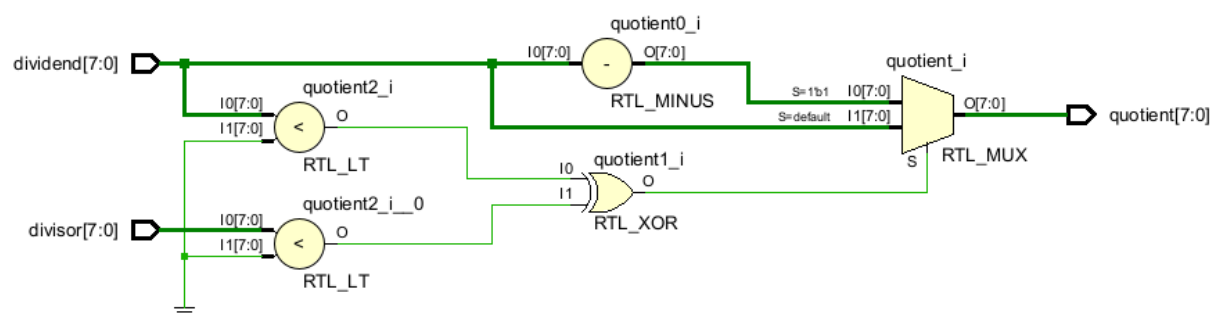
```

```

endmodule

```

## RTL schematic:-



## Synthesis report:-

Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/12/23, 12:14 AM	7.9 KB
synthesis_report			9/12/23, 12:14 AM	12.6 KB
Implementation				
impl_1				
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc		9/12/23, 12:16 AM	4.7 KB
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io		9/12/23, 12:16 AM	72.3 KB
Utilization - Place Design	report_utilization		9/12/23, 12:16 AM	9.8 KB
Control Sets - Place Design	report_control_sets	verbose = true;	9/12/23, 12:16 AM	3.6 KB
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Route Design (route_design)				
DRC - Route Design	report_drc		9/12/23, 12:16 AM	4.7 KB
Methodology - Route Design	report_methodology		9/12/23, 12:16 AM	1.6 KB
Power - Route Design	report_power		9/12/23, 12:16 AM	8.2 KB
Route Status - Route Design	report_route_status		9/12/23, 12:16 AM	0.6 KB
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;	9/12/23, 12:16 AM	34.0 KB
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization		9/12/23, 12:16 AM	6.7 KB
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;	9/12/23, 12:16 AM	1.2 KB
implementation_log			9/12/23, 12:16 AM	26.5 KB
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## power report:-

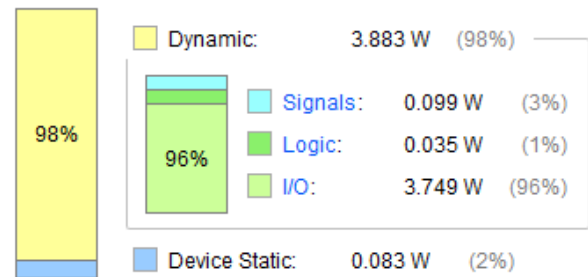
## Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

**Total On-Chip Power:** 3.966 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 44.8°C  
**Thermal Margin:** 40.2°C (8.0 W)  
**Ambient Temperature:** 25.0 °C  
**Effective  $\theta_{JA}$ :** 5.0°C/W  
**Power supplied to off-chip devices:** 0 W  
**Confidence level:** Low

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### On-Chip Power



## Output:-

Name		Value	10,000 ps			
			9,997 ps	9,998 ps	9,999 ps	10,000 ps
> tb_dividend[7:0]		06	06			
> tb_divisor[7:0]		02	02			
> tb_quotient[7:0]		06	06			

## 8)DAY TO BCD

### **Verilog code:-**

```
module bcd_to_7seg_decoder (  
    input [3:0] bcd_input,  
    output reg [6:0] seg_output  
);  
  
    always @* begin  
        case(bcd_input)  
            4'b0000: seg_output = 7'b0111111;  
            4'b0001: seg_output = 7'b0000110;  
            4'b0010: seg_output = 7'b1011011;  
            4'b0011: seg_output = 7'b1001111;  
            4'b0100: seg_output = 7'b1100110;  
            4'b0101: seg_output = 7'b1101101;  
            4'b0110: seg_output = 7'b1111101;  
            4'b0111: seg_output = 7'b0000111;  
            4'b1000: seg_output = 7'b1111111;  
            4'b1001: seg_output = 7'b1101111;  
            default: seg_output = 7'b0111111;  
        endcase  
    end  
  
endmodule
```

### **Testbench:-**

```

module tb_bcd_to_7seg_decoder;

    reg [3:0] tb_bcd_input;
    wire [6:0] tb_seg_output;

    bcd_to_7seg_decoder uut (
        .bcd_input(tb_bcd_input),
        .seg_output(tb_seg_output)
    );

    initial begin

        tb_bcd_input = 4'b0010;
        #10;
        $display("BCD Input: %b, 7-Segment Output: %b", tb_bcd_input, tb_seg_output);

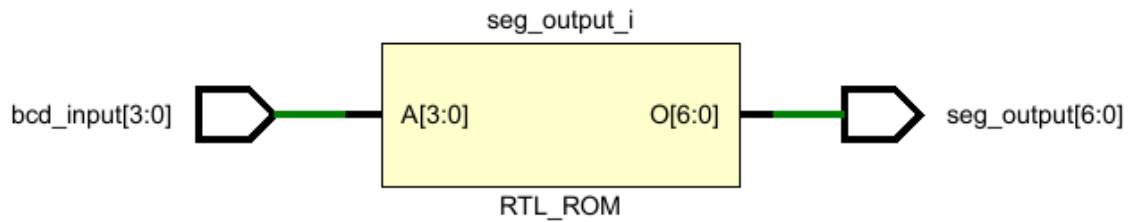
        tb_bcd_input = 4'b1001;
        #10;
        $display("BCD Input: %b, 7-Segment Output: %b", tb_bcd_input, tb_seg_output);

        $stop;
    end

endmodule

```

## **RTL schematic:-**



## Synthesis report:-

Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/12/23, 9:32 PM	7.8 KB
synthesis_report			9/12/23, 9:32 PM	11.9 KB
Implementation				
impl_1				
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## power report:-

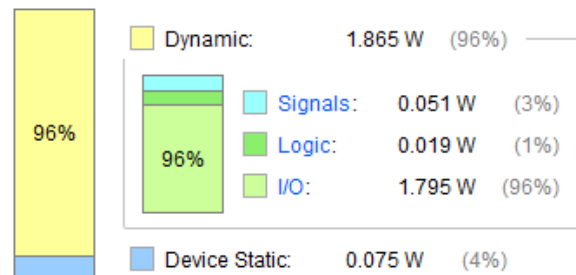
## Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** 1.94 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 34.7°C  
**Thermal Margin:** 50.3°C (10.0 W)  
**Ambient Temperature:** 25.0 °C  
**Effective  $\theta_{JA}$ :** 5.0°C/W  
**Power supplied to off-chip devices:** 0 W  
**Confidence level:** Low

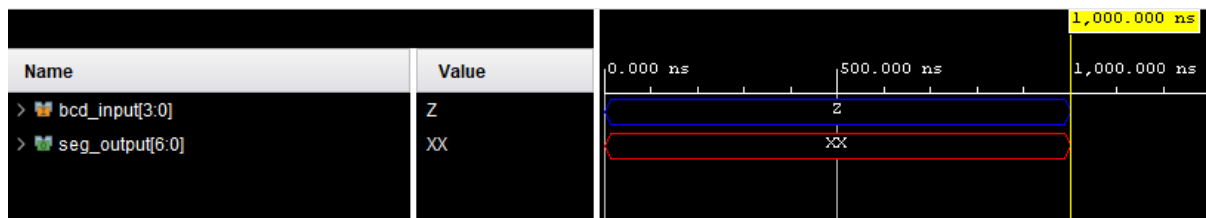
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### On-Chip Power



User specified ambient temperature of the surrounding air in which the device is expected to operate.

## Output:-



## 9)Positive Edge Detector:-



**Verilog code:-**

```
module and_gate (input a, input b, output y);
```

```
    assign y = a & b;
```

```
endmodule
```

```
module or_gate (input a, input b, output y);
```

```
    assign y = a | b;
```

```
endmodule
```

```
module not_gate (input a, output y);
```

```
    assign y = ~a;
```

```
endmodule
```

```
module positive_edge_detector (input clk, output reg pos_edge_detected);
```

```
    wire clk_n;
```

```
    wire pos_edge;
```

```
    not_gate u1 (.a(clk), .y(clk_n));
```

```
    and_gate u2 (.a(clk), .b(clk_n), .y(pos_edge));
```

```
    always @(posedge clk) begin
```

```
        pos_edge_detected <= pos_edge;
```

```
    end
```

```
endmodule
```

**Testbench:-**

```

module tb_positive_edge_detector;

    reg tb_clk;
    wire tb_pos_edge_detected;

    positive_edge_detector uut (
        .clk(tb_clk),
        .pos_edge_detected(tb_pos_edge_detected)
    );

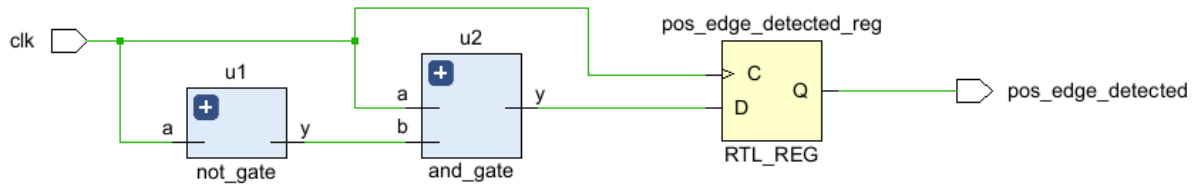
    always begin
        #5 tb_clk = ~tb_clk;
    end

    initial begin
        tb_clk = 0;
        #10;
        #5 tb_clk = 1;
        #10;
        $display("Positive Edge Detected: %b", tb_pos_edge_detected);
        #5 tb_clk = 0;
        #10;
        $display("Positive Edge Detected: %b", tb_pos_edge_detected);
        $stop;
    end

endmodule

```

### **RTL schematic:-**



## Synthesis report:-

Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/12/23, 9:	7.7 KE
synthesis_report			9/12/23, 9:	12.3 K
Implementation				
impl_1				
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## power report:-

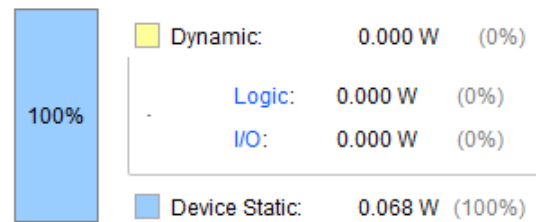
## Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

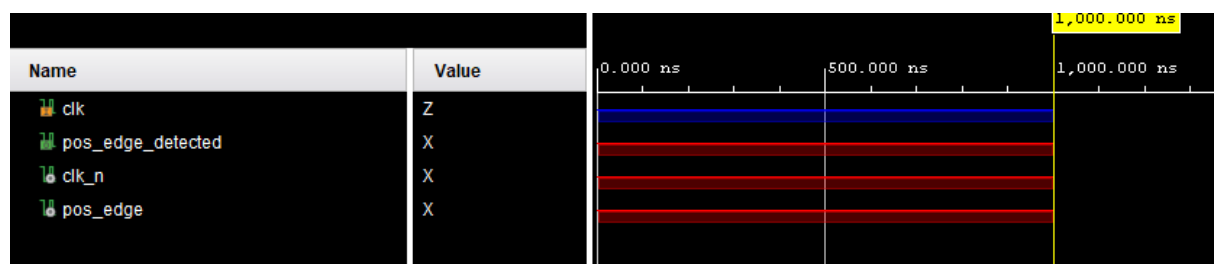
**Total On-Chip Power:** 0.068 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 25.3°C  
**Thermal Margin:** 59.7°C (11.9 W)  
**Ambient Temperature:** 25.0 °C  
**Effective  $\theta_{JA}$ :** 5.0°C/W  
**Power supplied to off-chip devices:** 0 W  
**Confidence level:** High

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### On-Chip Power



## Output:-



## 10)4-Bit Carry Select Adder

### Verilog code:-

```
module carry_select_adder (  
    input [3:0] A,  
    input [3:0] B,  
    input Cin,  
    output [3:0] S,  
    output Cout1,  
    output Cout2  
);  
  
    wire [3:0] S1, S2;  
    wire Cout_intermediate;  
  
    full_adder u1 (.A(A[0]), .B(B[0]), .Cin(Cin), .S(S1[0]), .Cout(Cout_intermediate));  
    full_adder u2 (.A(A[1]), .B(B[1]), .Cin(Cout_intermediate), .S(S1[1]),  
.Cout(Cout_intermediate));  
    full_adder u3 (.A(A[2]), .B(B[2]), .Cin(Cout_intermediate), .S(S1[2]),  
.Cout(Cout_intermediate));  
    full_adder u4 (.A(A[3]), .B(B[3]), .Cin(Cout_intermediate), .S(S1[3]), .Cout(Cout1));  
  
    full_adder u5 (.A(A[0]), .B(B[0]), .Cin(Cout1), .S(S2[0]), .Cout(Cout_intermediate));  
    full_adder u6 (.A(A[1]), .B(B[1]), .Cin(Cout_intermediate), .S(S2[1]),  
.Cout(Cout_intermediate));  
    full_adder u7 (.A(A[2]), .B(B[2]), .Cin(Cout_intermediate), .S(S2[2]),  
.Cout(Cout_intermediate));  
    full_adder u8 (.A(A[3]), .B(B[3]), .Cin(Cout_intermediate), .S(S2[3]), .Cout(Cout2));  
  
    assign S = {S2, S1};  
endmodule
```

```

module full_adder (
    input A, B, Cin,
    output S, Cout
);

    xor_gate u1 (.a(A), .b(B), .y(S));
    xor_gate u2 (.a(S), .b(Cin), .y(S));

    and_gate u3 (.a(A), .b(B), .y(C1));
    and_gate u4 (.a(S), .b(Cin), .y(C2));
    and_gate u5 (.a(A), .b(Cin), .y(C3));

    or_gate u6 (.a(C1), .b(C2), .y(C4));
    or_gate u7 (.a(C3), .b(C4), .y(Cout));

endmodule

module xor_gate (input a, input b, output y);
    assign y = a ^ b;
endmodule

module and_gate (input a, input b, output y);
    assign y = a & b;
endmodule

module or_gate (input a, input b, output y);
    assign y = a | b;
endmodule

```

### **Testbench:-**

```

module tb_carry_select_adder;

    reg [3:0] tb_A;
    reg [3:0] tb_B;
    reg tb_Cin;
    wire [3:0] tb_S;
    wire tb_Cout1;
    wire tb_Cout2;

    carry_select_adder uut (
        .A(tb_A),
        .B(tb_B),
        .Cin(tb_Cin),
        .S(tb_S),
        .Cout1(tb_Cout1),
        .Cout2(tb_Cout2)
    );

    initial begin
        tb_A = 4'b0101;
        tb_B = 4'b0011;
        tb_Cin = 1'b0;

        #10;

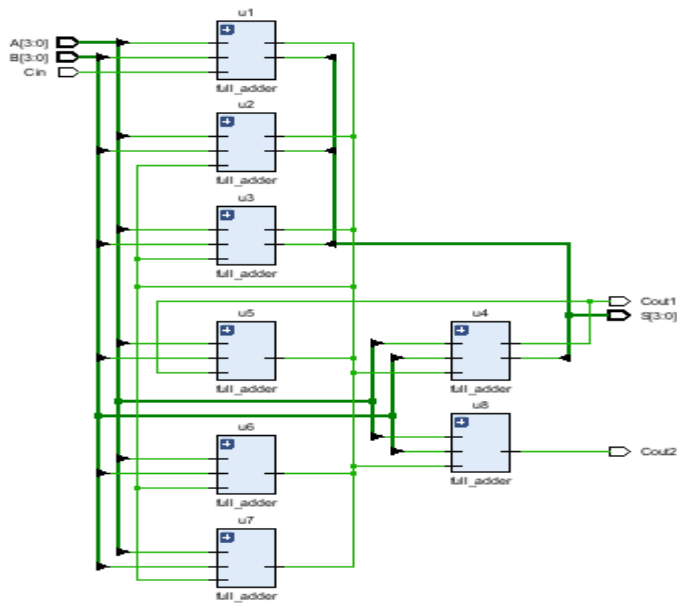
        $display("A: %b, B: %b, Cin: %b, S: %b, Cout1: %b, Cout2: %b", tb_A, tb_B, tb_Cin, tb_S,
        tb_Cout1, tb_Cout2);

        $stop;
    end

endmodule

```

### **RTL schematic:-**



## Synthesis report:-

Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/12/23, 11	7.8 KE
synthesis_report			9/12/23, 11	17.9 K
Implementation				
impl_1				
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## power report:-



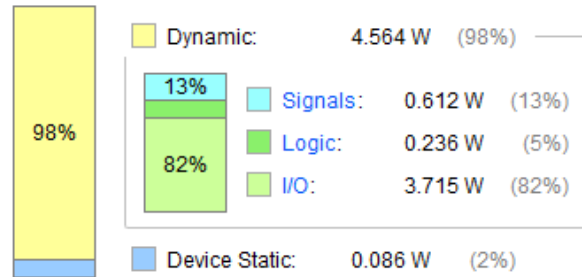
## Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

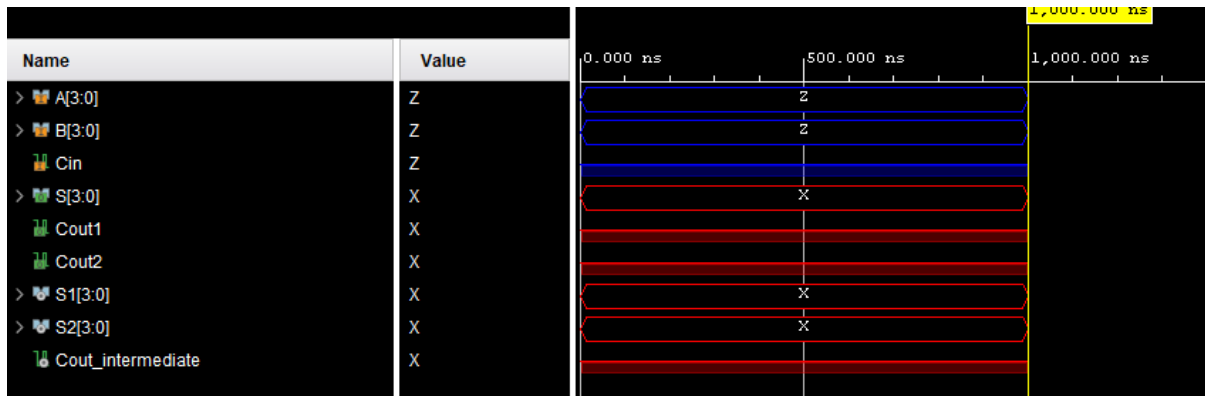
**Total On-Chip Power:** 4.65 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 48.2°C  
Thermal Margin: 36.8°C (7.3 W)  
Ambient Temperature: 25.0 °C  
Effective  $\theta_{JA}$ : 5.0°C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

### On-Chip Power



## Output:-



## 11) Moore FSM which detects 1010 Sequence

Verilog code:-

```

module fsm_1010_detector (
    input wire clk,
    input wire rst,
    input wire in_data,
    output reg detect
);

parameter S0 = 2'b00;
parameter S1 = 2'b01;
parameter S2 = 2'b10;
parameter S3 = 2'b11;

reg [1:0] state, next_state;

always @(posedge clk or posedge rst) begin
    if (rst) begin
        state <= S0;
    end else begin
        state <= next_state;
    end
end

always @* begin
    case(state)
        S0: next_state = (in_data == 1'b1) ? S1 : S0;
        S1: next_state = (in_data == 1'b0) ? S2 : S0;
        S2: next_state = (in_data == 1'b1) ? S3 : S0;

```

```

    S3: next_state = (in_data == 1'b0) ? S0 : S0;
    default: next_state = S0;
endcase
end

always @* begin
    detect = (state == S3);
end

endmodule

```

### **Testbench:-**

```

module tb_fsm_1010_detector;

    parameter CLK_PERIOD = 10;
    parameter SIM_TIME = 100;

    reg clk, rst, in_data;
    wire detect;

    fsm_1010_detector uut (
        .clk(clk),
        .rst(rst),
        .in_data(in_data),
        .detect(detect)
    );

    always #((CLK_PERIOD / 2)) clk = ~clk;

```

```
initial begin
```

```
    clk = 0;
```

```
    rst = 1;
```

```
    in_data = 0;
```

```
    #10 rst = 0;
```

```
    #10 in_data = 1; // State S1
```

```
    #10 in_data = 0; // State S2
```

```
    #10 in_data = 1; // State S0
```

```
    #10 in_data = 0; // State S0
```

```
    #10 in_data = 1; // State S0
```

```
    #10 in_data = 1; // State S1
```

```
    #10 in_data = 0; // State S2
```

```
    #10 in_data = 1; // State S3
```

```
    #10 in_data = 0; // State S0
```

```
    #10 in_data = 1; // State S1
```

```
    #10 in_data = 0; // State S2
```

```
    #10 in_data = 1; // State S0
```

```
    #10 in_data = 0; // State S0
```

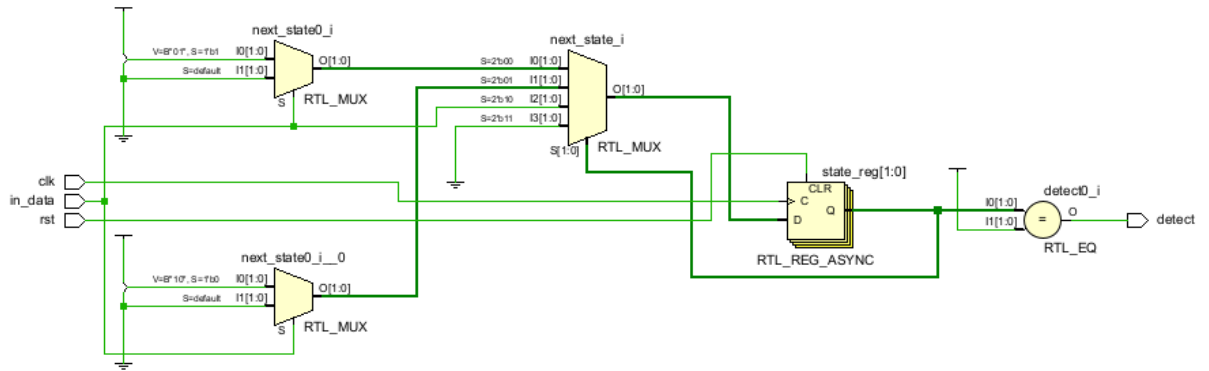
```
    #10 in_data = 1; // State S0
```

```
    #10 $finish;
```

```
end
```

```
endmodule
```

**RTL schematic:-**



## Synthesis report:-

Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization			
synthesis_report				
Implementation				
impl_1				
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## power report:-

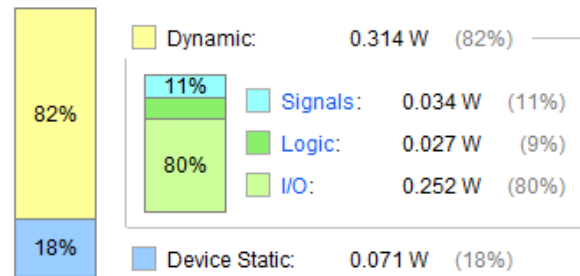
## Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

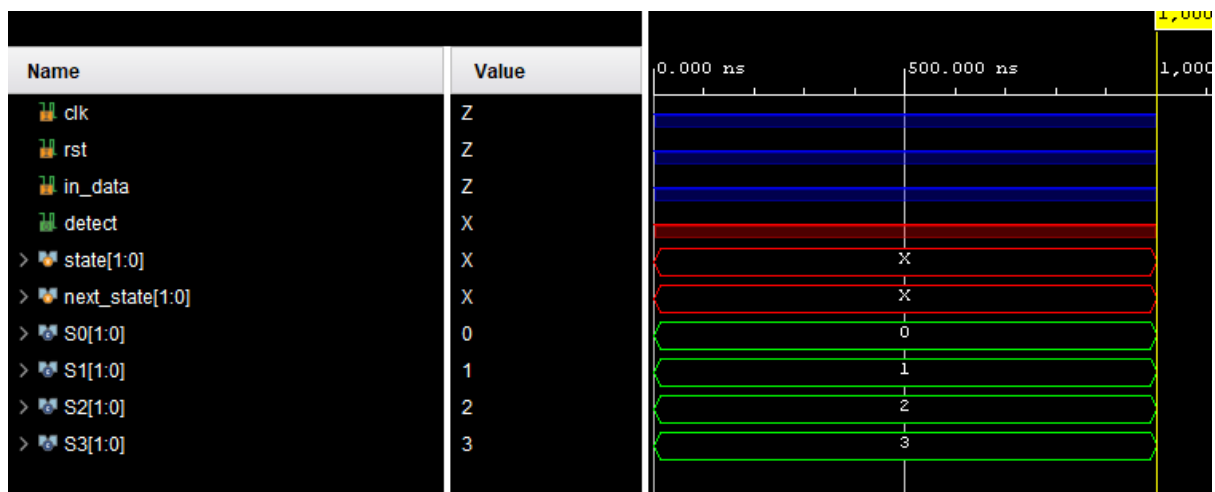
**Total On-Chip Power:** 0.385 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 26.9°C  
**Thermal Margin:** 58.1°C (11.6 W)  
**Ambient Temperature:** 25.0 °C  
**Effective  $\theta_{JA}$ :** 5.0°C/W  
**Power supplied to off-chip devices:** 0 W  
**Confidence level:** Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

### On-Chip Power



## Output:-



## 12)N:1 Multiplexer

### **Verilog code:-**

```
module mux_4to1 (  
    input wire [3:0] data_in,  
    input wire [1:0] sel,  
    output reg out  
);  
  
always @* begin  
    case(sel)  
        2'b00: out = data_in[0];  
        2'b01: out = data_in[1];  
        2'b10: out = data_in[2];  
        2'b11: out = data_in[3];  
        default: out = 1'b0;  
    endcase  
end  
  
endmodule
```

### **Testbench:-**

```
module tb_mux_4to1;  
  
    parameter CLK_PERIOD = 10;  
    parameter SIM_TIME = 100;  
  
    reg [3:0] data_in;  
    reg [1:0] sel;  
    wire out;
```

```
mux_4to1 uut (  
    .data_in(data_in),  
    .sel(sel),  
    .out(out)  
);
```

```
initial begin
```

```
    data_in = 4'b0000;
```

```
    sel = 2'b00;
```

```
#10 sel = 2'b00;
```

```
    #10 data_in = 4'b1010;
```

```
#10 sel = 2'b10;
```

```
    #10 data_in = 4'b0110;
```

```
#10 sel = 2'b01;
```

```
    #10 data_in = 4'b1100;
```

```
#10 sel = 2'b11;
```

```
    #10 data_in = 4'b0011;
```

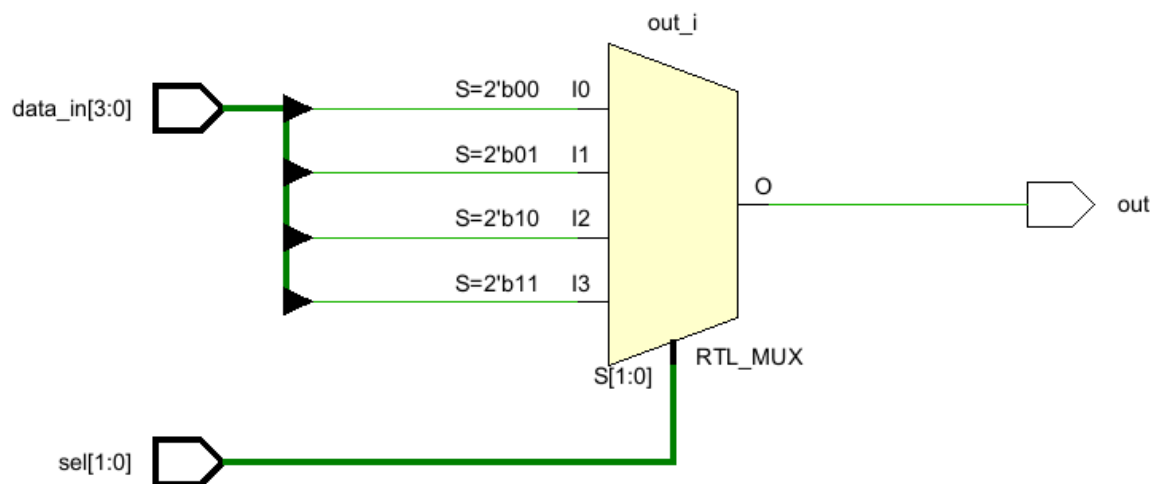
```
#10 $finish;
```

```
end
```

```
endmodule
```

**RTL schematic:-**





## Synthesis report:-

Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/12/23, 10:28 PM	7.7 KB
synthesis_report			9/12/23, 10:28 PM	11.9 KB
Implementation				
impl_1				
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
Implementation Log				
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## power report:-

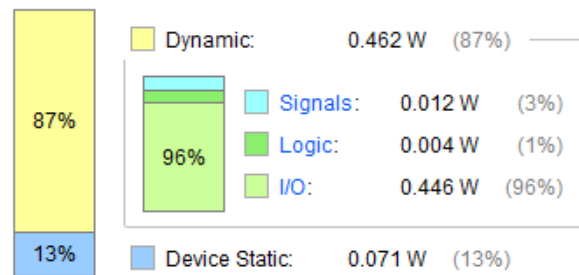
## Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

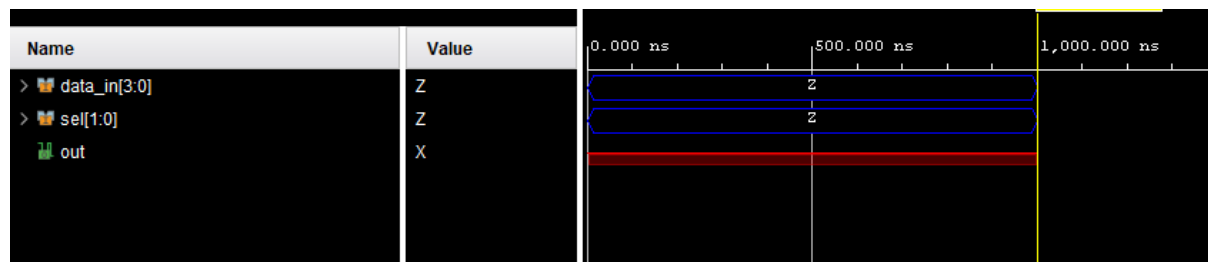
**Total On-Chip Power:** 0.533 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 27.7°C  
**Thermal Margin:** 57.3°C (11.4 W)  
**Ambient Temperature:** 25.0 °C  
**Effective  $\theta_{JA}$ :** 5.0°C/W  
**Power supplied to off-chip devices:** 0 W  
**Confidence level:** Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

### On-Chip Power



## Output:-



## 13) Write RTL code for a BCD counter

### Verilog code:-

```
module bcd_counter_24hr (  
    input wire clk,  
    input wire rst,  
    output reg [3:0] hr,  
    output reg [3:0] min,  
    output reg [3:0] sec  
);  
  
    reg [3:0] count_hr, count_min, count_sec;  
  
    always @(posedge clk or posedge rst) begin  
        if (rst) begin  
            count_hr <= 4'b0000;  
            count_min <= 4'b0000;  
            count_sec <= 4'b0000;  
        end else begin  
            if (count_sec == 4'b1001) begin  
                count_sec <= 4'b0000;  
                if (count_min == 4'b1001) begin  
                    count_min <= 4'b0000;  
                    if (count_hr == 4'b0011) begin  
                        count_hr <= 4'b0000;  
                    end else begin  
                        count_hr <= count_hr + 4'b0001;  
                    end  
                end else begin  
                    count_min <= count_min + 4'b0001;  
                end  
            end  
        end  
    end  
end
```

```
    end else begin
        count_sec <= count_sec + 4'b0001;
    end
end
end
```

```
always @* begin
    hr = count_hr;
    min = count_min;
    sec = count_sec;
end
```

```
endmodule
```

### **Testbench:-**

```
module tb_bcd_counter_24hr;

    parameter CLK_PERIOD = 10;
    parameter SIM_TIME  = 1000;

    reg clk, rst;
    wire [3:0] hr, min, sec;

    bcd_counter_24hr uut (
        .clk(clk),
        .rst(rst),
        .hr(hr),
        .min(min),
```

```
.sec(sec)  
);
```

```
always #((CLK_PERIOD / 2)) clk = ~clk;
```

```
initial begin
```

```
    clk = 0;
```

```
    rst = 1;
```

```
    #10 rst = 0;
```

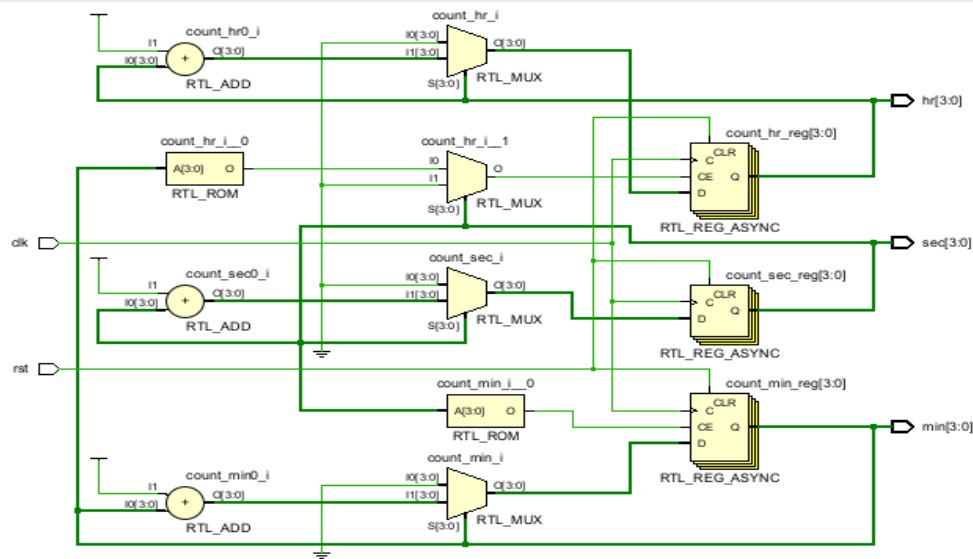
```
    #SIM_TIME;
```

```
    #10 $finish;
```

```
end
```

```
endmodule
```

## RTL schematic:-



## Synthesis report:-

Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/12/23, 10:39 PM	8.0 KB
synthesis_report			9/12/23, 10:39 PM	12.2 KB
Implementation				
impl_1				
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
Implementation Log				
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
Write Bitstream (write_bitstream)				
report_webtalk				
Implementation Log				

## power report:-

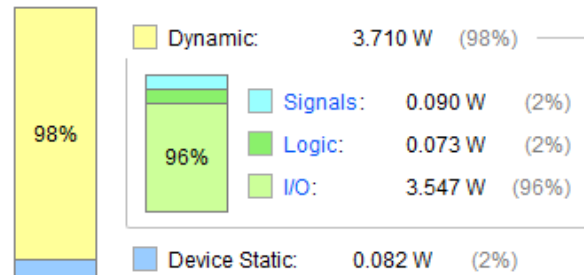
### Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** 3.792 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 44.0°C  
Thermal Margin: 41.0°C (8.2 W)  
Ambient Temperature: 25.0 °C  
Effective  $\theta_{JA}$ : 5.0°C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

### On-Chip Power



## Output:-



## **14)3-to-1 1-bit MUX with a 1-bit latch**

### **Verilog code:-**

```
module mux_3to1_with_latch (  
    input wire a,  
    input wire b,  
    input wire c,  
    input wire sel,  
    input wire en,  
    output reg out  
);  
always @(a, b, c, sel) begin  
    case (sel)  
        2'b00: out = a;  
        2'b01: out = b;  
        2'b10: out = c;  
        default: out = 1'b0;  
    endcase  
end  
always @(posedge en) begin  
    if (en) begin  
        case (sel)  
            2'b00: out <= a;  
            2'b01: out <= b;  
            2'b10: out <= c;  
            default: out <= 1'b0;  
        endcase  
    end  
end  
endmodule
```



## **Testbench:-**

```
module tb_mux_3to1_with_latch;
```

```
    parameter CLK_PERIOD = 10;
```

```
    reg a, b, c, sel, en;
```

```
    wire out;
```

```
    mux_3to1_with_latch uut (
```

```
        .a(a),
```

```
        .b(b),
```

```
        .c(c),
```

```
        .sel(sel),
```

```
        .en(en),
```

```
        .out(out)
```

```
    );
```

```
    initial begin
```

```
        a = 0;
```

```
        b = 1;
```

```
        c = 0;
```

```
        sel = 2'b00;
```

```
        en = 1;
```

```
        #10 sel = 2'b00;
```

```
#10 a = 1;
```

```
#10 sel = 2'b01;
```

```
#10 b = 0;
```

```
#10 sel = 2'b10;
```

```
#10 c = 1;
```

```
#10 en = 0;
```

```
#10 c = 0;
```

```
#10 a = 1;
```

```
#10 b = 1;
```

```
#10 en = 1;
```

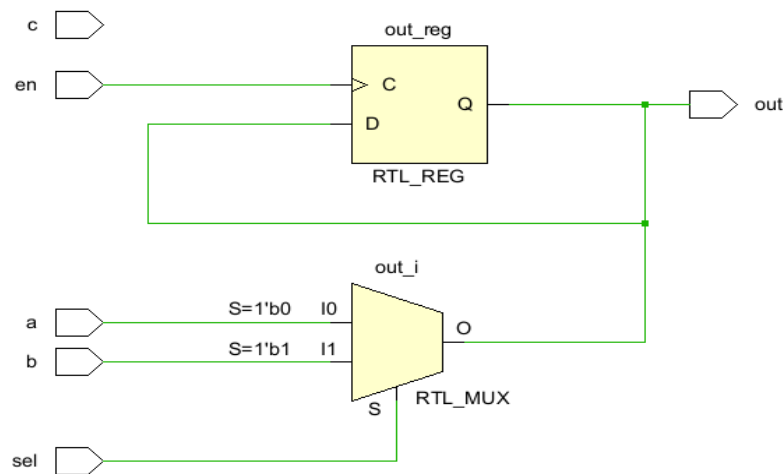
```
#10 b = 0;
```

```
#10 $finish;
```

```
end
```

```
endmodule
```

## RTL schematic:-



## Synthesis report:-

Report	Type	Options	Modified	Size
✓ Synthesis				
✓ Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/12/23, 10:4	7.8 KB
synthesis_report			9/12/23, 10:4	13.5 KB
✓ Implementation				
✓ impl_1				
✓ Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
✓ Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
✓ Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
✓ Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
✓ Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
✓ Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
✓ Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
✓ Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
✓ Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

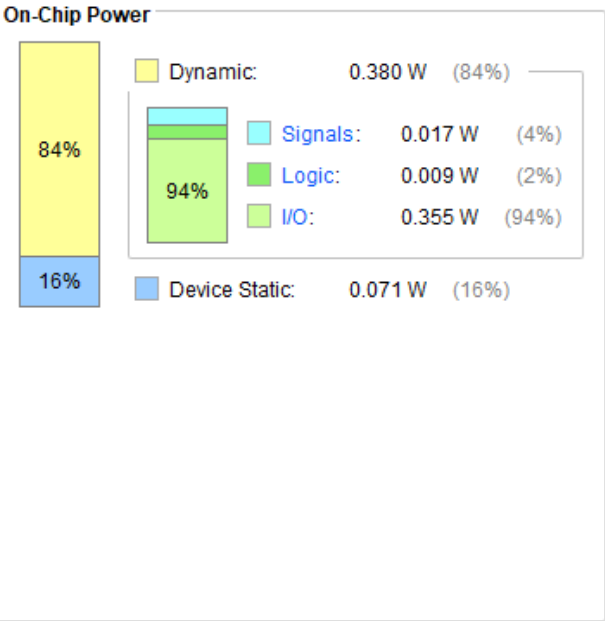
power report:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	0.451 W
Design Power Budget:	Not Specified
Process:	typical
Power Budget Margin:	N/A
Junction Temperature:	27.3°C
Thermal Margin:	57.7°C (11.5 W)
Ambient Temperature:	25.0 °C
Effective θJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Output:-



## **15) BCD to Seven Segment Display**

### **Verilog code:-**

```
module bcd_to_7seg_decoder (  
    input [3:0] bcd,  
    output reg [6:0] seg  
);
```

```
    always @* begin  
        case(bcd)  
            4'b0000: seg = 7'b1000000;  
            4'b0001: seg = 7'b1111001;  
            4'b0010: seg = 7'b0100100;  
            4'b0011: seg = 7'b0110000;  
            4'b0100: seg = 7'b0011001;  
            4'b0101: seg = 7'b0010010;  
            4'b0110: seg = 7'b0000010;  
            4'b0111: seg = 7'b1111000;  
            4'b1000: seg = 7'b0000000;  
            4'b1001: seg = 7'b0011000;  
            default: seg = 7'b1111111;  
        endcase  
    end
```

```
endmodule
```

### **Testbench:-**

```
module tb_bcd_to_7seg_decoder;  
    parameter CLK_PERIOD = 10;  
    reg [3:0] bcd;
```

```

wire [6:0] seg;

bcd_to_7seg_decoder uut (
    .bcd(bcd),
    .seg(seg)
);

initial begin
bcd = 4'b0000;

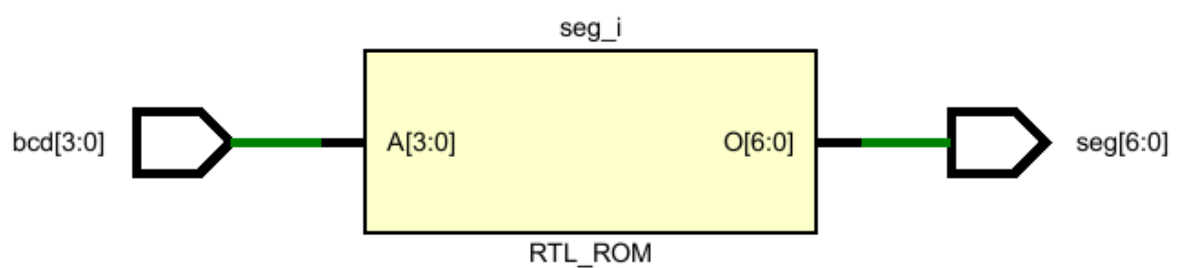
    #10 bcd = 4'b0000;
    #10 bcd = 4'b0001;
    #10 bcd = 4'b0010;
    #10 bcd = 4'b0101;
    #10 bcd = 4'b1001;
    #10 bcd = 4'b1010;
    #10 $finish;

end

endmodule

```

### **RTL schematic:-**



## Synthesis report:-

Report	Type	Options	Modified	Size
▼ Synthesis				
▼ Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/13/23, 11:18 PM	7.8 KB
synthesis_report			9/13/23, 11:18 PM	11.9 KB
▼ Implementation				
▼ impl_1				
▼ Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
▼ Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
▼ Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## power report:-

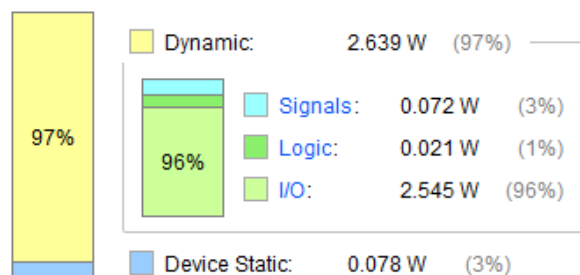
### Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

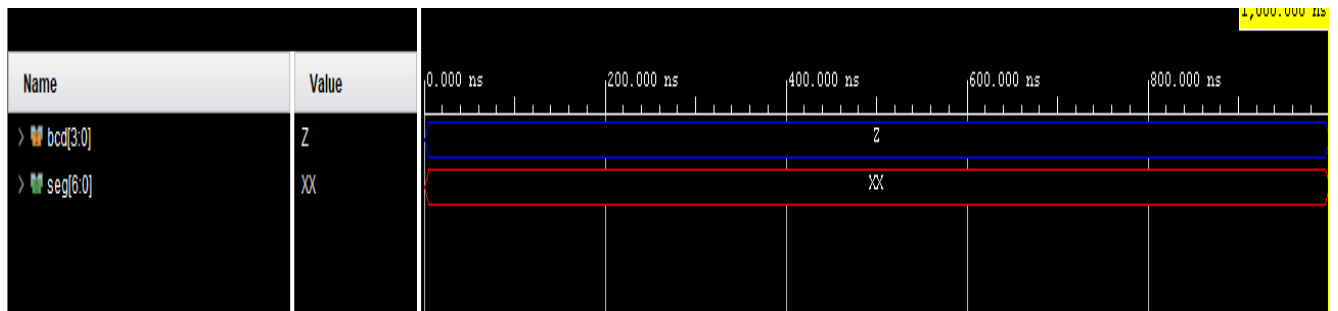
**Total On-Chip Power:** 2.716 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 38.6°C  
**Thermal Margin:** 46.4°C (9.2 W)  
**Ambient Temperature:** 25.0 °C  
**Effective  $\theta_{JA}$ :** 5.0°C/W  
**Power supplied to off-chip devices:** 0 W  
**Confidence level:** Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

### On-Chip Power



## Output:-





## **16) D Latch using 2:1 Mux**

### **Verilog code:-**

```
module d_latch_using_mux_behavioral (  
    input wire d,  
    input wire en,  
    input wire clk,  
    output reg q,  
    output reg nq  
);
```

```
    always @* begin  
        if (en) begin  
            q = d;  
            nq = ~d;  
        end  
    end  
end
```

```
endmodule
```

### **Testbench:-**

```
module tb_d_latch_using_mux_behavioral;  
    parameter CLK_PERIOD = 10;  
    reg d, en, clk;  
    wire q, nq;  
    d_latch_using_mux_behavioral uut (  
        .d(d),  
        .en(en),  
        .clk(clk),  
        .q(q),
```

```

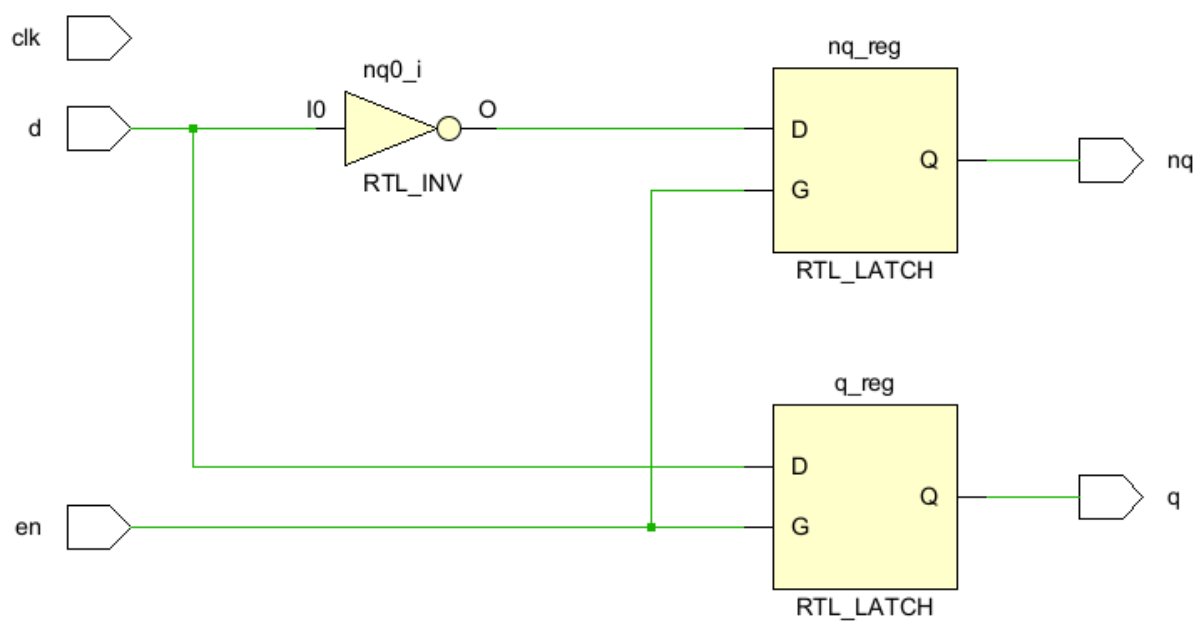
.nq(nq)
);
always #((CLK_PERIOD / 2)) clk = ~clk;
initial begin
    d = 0;
    en = 0;
    clk = 0;
    #10 d = 1;
    #10 en = 0;
    #10 en = 1;
    #10 d = 0;
    #10 en = 0;

    #10 $finish;
end

endmodule

```

### **RTL schematic:-**



## Synthesis report:-

Report	Type	Options	Modified	Size
▼ Synthesis				
▼ Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/13/23, 11:4	7.9 KB
synthesis_report			9/13/23, 11:4	12.6 KB
▼ Implementation				
▼ impl_1				
▼ Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Opt Design (opt_design)				
DRC - Opt Design	report_drc		9/13/23, 11:4	4.7 KB
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Place Design (place_design)				
IO - Place Design	report_io		9/13/23, 11:4	72.3 KB
Utilization - Place Design	report_utilization		9/13/23, 11:4	9.9 KB
Control Sets - Place Design	report_control_sets	verbose = true;	9/13/23, 11:4	3.8 KB
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Route Design (route_design)				
DRC - Route Design	report_drc		9/13/23, 11:4	4.7 KB
Methodology - Route Design	report_methodology		9/13/23, 11:4	2.4 KB
Power - Route Design	report_power		9/13/23, 11:4	8.4 KB
Route Status - Route Design	report_route_status		9/13/23, 11:4	0.6 KB
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;	9/13/23, 11:4	18.9 KB
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization		9/13/23, 11:4	10.9 KB
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;	9/13/23, 11:4	1.1 KB
implementation_log			9/13/23, 11:4	26.2 KB
▼ Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
▼ Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## power report:-

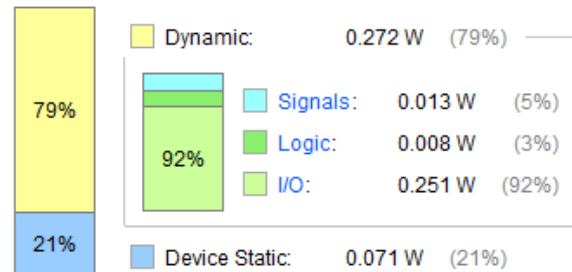
### Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

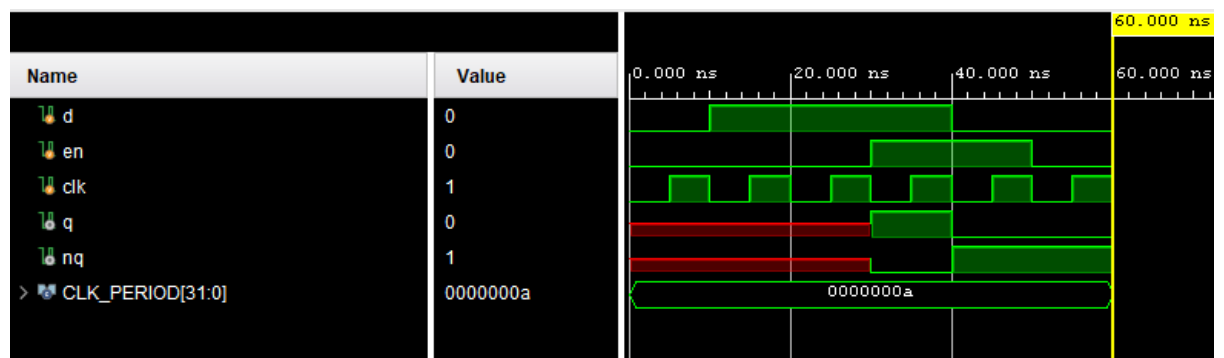
**Total On-Chip Power:** 0.343 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 26.7°C  
**Thermal Margin:** 58.3°C (11.6 W)  
**Ambient Temperature:** 25.0 °C  
**Effective  $\theta_{JA}$ :** 5.0°C/W  
**Power supplied to off-chip devices:** 0 W  
**Confidence level:** Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

### On-Chip Power



## Output:-



## **17) 8-Bit Barrel Shifter**

### **Verilog code:-**

```
module barrel_shifter_8bit (  
    input wire [7:0] data_in,  
    input wire [2:0] shift_amt,  
    input wire direction,  
    output reg [7:0] data_out  
);  
  
    wire [7:0] shifted_data;  
  
    assign shifted_data = (direction) ? (data_in >> shift_amt) : (data_in << shift_amt);  
  
    always @* begin  
        data_out = shifted_data;  
    end  
  
endmodule
```

### **Testbench:-**

```
module tb_barrel_shifter_8bit;  
    parameter CLK_PERIOD = 10;  
    reg [7:0] data_in;  
    reg [2:0] shift_amt;  
    reg direction;  
    wire [7:0] data_out;  
    barrel_shifter_8bit uut (  
        .data_in(data_in),
```

```

.shift_amt(shift_amt),
.direction(direction),
.data_out(data_out)
);

initial begin

    data_in = 8'b11001100;

    shift_amt = 3'b001;

    direction = 1;

#10 shift_amt = 3'b001;

#10 direction = 0;

    #10 shift_amt = 3'b010;

#10 shift_amt = 3'b000;

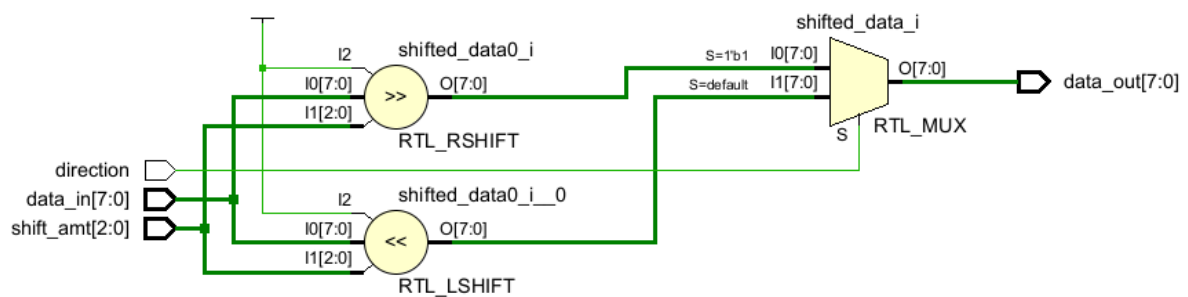
    #10 $finish;

end




























```

endmodule

### RTL schematic:-



## Synthesis report:-

Report	Type	Options	Modified	Size
▼ Synthesis				
▼ Synth Design (synth_design)				
 Utilization - Synth Design	report_utilization		9/13/23, 11:57 PM	7.9 KB
 synthesis_report			9/13/23, 11:57 PM	12.1 KB
▼ Implementation				
▼ impl_1				
▼ Design Initialization (init_design)				
 Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Opt Design (opt_design)				
 DRC - Opt Design	report_drc			
 Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Power Opt Design (power_opt_design)				
 Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Place Design (place_design)				
 IO - Place Design	report_io			
 Utilization - Place Design	report_utilization			
 Control Sets - Place Design	report_control_sets	verbose = true;		
 Incremental Reuse - Place Design	report_incremental_reuse			
 Incremental Reuse - Place Design	report_incremental_reuse			
 Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Power Opt Design (post_place_power_opt_design)				
 Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Phys Opt Design (phys_opt_design)				
 Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Route Design (route_design)				
 DRC - Route Design	report_drc			
 Methodology - Route Design	report_methodology			
 Power - Route Design	report_power			
 Route Status - Route Design	report_route_status			
 Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
 Incremental Reuse - Route Design	report_incremental_reuse			
 Clock Utilization - Route Design	report_clock_utilization			
 Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
 implementation_log				
▼ Post-Route Phys Opt Design (post_route_phys_opt_design)				
 Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
 Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
▼ Write Bitstream (write_bitstream)				
 report_webtalk				
 implementation_log				

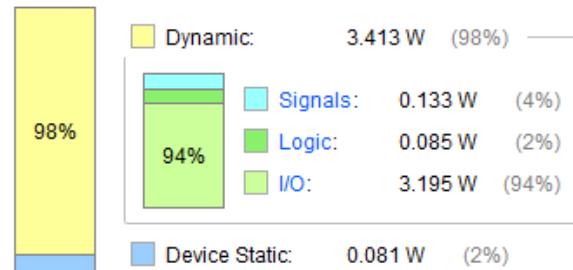
## power report:-

### Summary

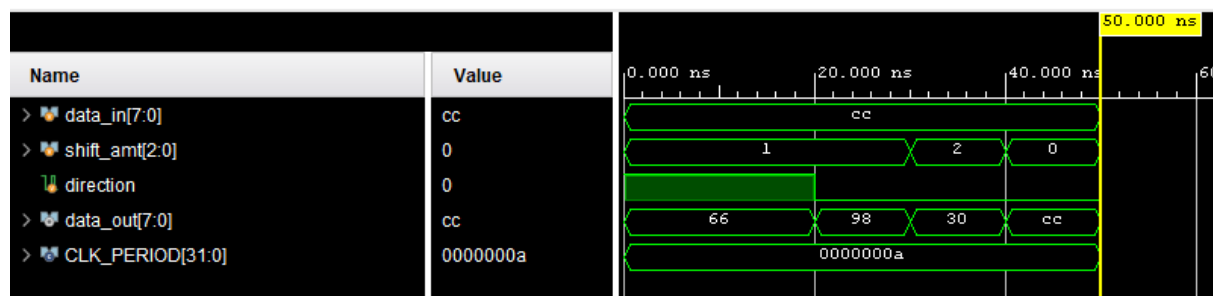
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** 3.494 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 42.5°C  
Thermal Margin: 42.5°C (8.5 W)  
Ambient Temperature: 25.0 °C  
Effective  $\theta_{JA}$ : 5.0°C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: Low  
[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

### On-Chip Power



## Output:-





## **18) 1-Bit Comparator using 4X1 Mux**

### **Verilog code:-**

```
module comparator_1bit_with_mux_behavioral (
    input wire a,
    input wire b,
    output reg gt,
    output reg eq,
    output reg lt
);

    always @* begin

        if (a > b) begin
            gt = 1;
            eq = 0;
            lt = 0;
        end else if (a == b) begin
            gt = 0;
            eq = 1;
            lt = 0;
        end else begin
            gt = 0;
            eq = 0;
            lt = 1;
        end
    end

endmodule
```

## **Testbench:-**

```
module tb_comparator_1bit_with_mux_behavioral;
```

```
    parameter CLK_PERIOD = 10;
```

```
    reg a, b;
```

```
    wire gt, eq, lt;
```

```
    comparator_1bit_with_mux_behavioral uut (
```

```
        .a(a),
```

```
        .b(b),
```

```
        .gt(gt),
```

```
        .eq(eq),
```

```
        .lt(lt)
```

```
    );
```

```
    initial begin
```

```
        a = 0;
```

```
        b = 0;
```

```
        #10 a = 1;
```

```
        #10 b = 0;
```

```
        #10 a = 1;
```

```
        #10 b = 1;
```

```
        #10 a = 0;
```

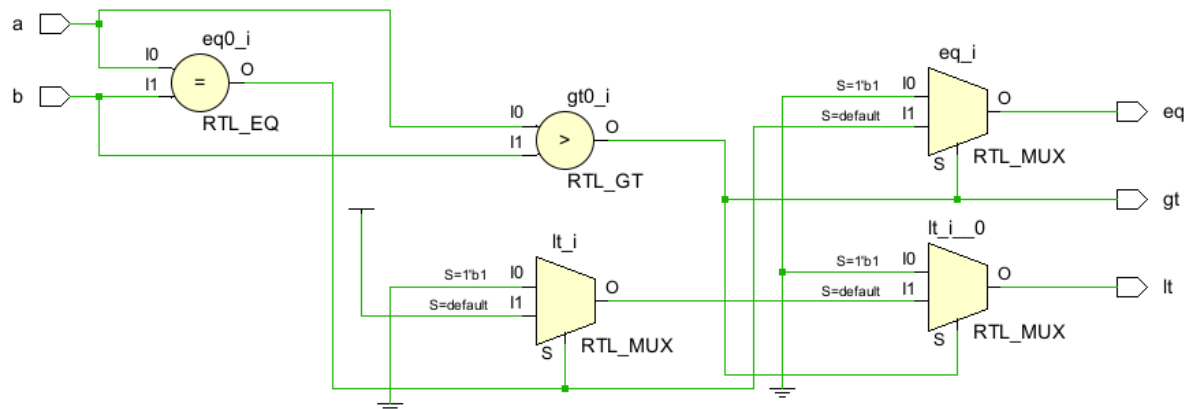
```
        #10 b = 1;
```

```
        #10 $finish;
```

```
    end
```

```
endmodule
```

### RTL schematic:-



### Synthesis report:-

Report	Type	Options	Modified	Size
▼ Synthesis				
▼ Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/14/23, 12:16 AM	7.8 KB
synthesis_report			9/14/23, 12:16 AM	12.2 KB
▼ Implementation				
▼ impl_1				
▼ Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
▼ Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
▼ Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

power report:-

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:

0.997 W

Design Power Budget:

Not Specified

Process:

typical

Power Budget Margin:

N/A

Junction Temperature:

30.0°C

Thermal Margin:

55.0°C (10.9 W)

Ambient Temperature:

25.0 °C

Effective  $\theta_{JA}$ :

5.0°C/W

Power supplied to off-chip devices:

0 W

Confidence level:

Low

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On-Chip Power

93%

7%

Dynamic: 0.925 W (93%)

94%

Signals: 0.044 W (5%)

Logic: 0.006 W (1%)

I/O: 0.875 W (94%)

Device Static: 0.072 W (7%)

Output:-

Name	Value
a	0
b	1
gt	0
eq	0
lt	1
CLK_PERIOD[31:0]	0000000a

22EL319

## **19) Logical, Algebraic, and Rotate Shift Operations**

### **Verilog code:-**

```
module logical_shift (  
    input [7:0] data_in,  
    input [2:0] shift_amt,  
    input direction,  
    output [7:0] data_out  
);
```

```
    assign data_out = (direction) ? (data_in << shift_amt) : (data_in >> shift_amt);
```

```
endmodule
```

```
module algebraic_shift (  
    input [7:0] data_in,  
    input [2:0] shift_amt,  
    input direction,  
    output [7:0] data_out  
);
```

```
    assign data_out = (direction) ? (data_in << shift_amt) : (data_in >>> shift_amt);
```

```
endmodule
```

```
module rotate_shift (  
    input [7:0] data_in,  
    input [2:0] shift_amt,  
    input direction,  
    output [7:0] data_out  
);
```

```
    assign data_out = (direction) ? (data_in << shift_amt) | (data_in >> (8 - shift_amt)) :  
    (data_in >> shift_amt) | (data_in << (8 - shift_amt));
```

```
endmodule
```

## **Testbench:-**

```
module tb_shift_operations;
```

```
    parameter CLK_PERIOD = 10;
```

```
    reg [7:0] data_in;
```

```
    reg [2:0] shift_amt;
```

```
    reg direction;
```

```
    wire [7:0] data_out;
```

```
    logical_shift u_logical_shift (
```

```
        .data_in(data_in),
```

```
        .shift_amt(shift_amt),
```

```
        .direction(direction),
```

```
        .data_out(data_out)
```

```
    );
```

```
    algebraic_shift u_algebraic_shift (
```

```
        .data_in(data_in),
```

```
        .shift_amt(shift_amt),
```

```
        .direction(direction),
```

```
        .data_out(data_out)
```

```
    );
```

```
rotate_shift u_rotate_shift (  
    .data_in(data_in),  
    .shift_amt(shift_amt),  
    .direction(direction),  
    .data_out(data_out)  
);
```

```
initial begin
```

```
    data_in = 8'b11001100;
```

```
    shift_amt = 3'b001;
```

```
    direction = 1;
```

```
#10 $display("Logical Left Shift:");
```

```
#10 shift_amt = 3'b010;
```

```
#10 $display("Logical Right Shift:");
```

```
#10 direction = 0;
```

```
#10 shift_amt = 3'b010;
```

```
#10 $display("Algebraic Left Shift:");
```

```
#10 shift_amt = 3'b010;
```

```
#10 $display("Algebraic Right Shift:");
```

```
#10 direction = 0;
```

```
#10 shift_amt = 3'b010;
```

```
#10 $display("Rotate Left:");
```

```
#10 direction = 1;
```

```
#10 shift_amt = 3'b010;
```

```
#10 $display("Rotate Right:");
```

```
#10 direction = 0;
```

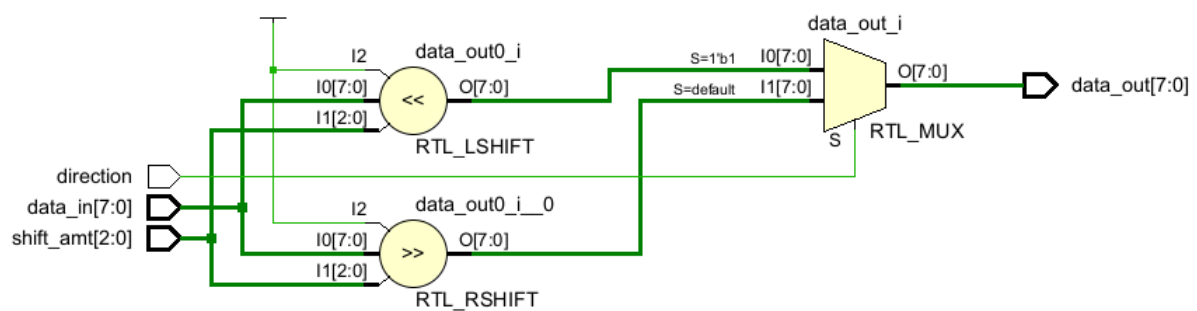
```
#10 shift_amt = 3'b010;
```

```
#10 $finish;
```

```
end
```

```
endmodule
```

## RTL schematic:-



## power report:-

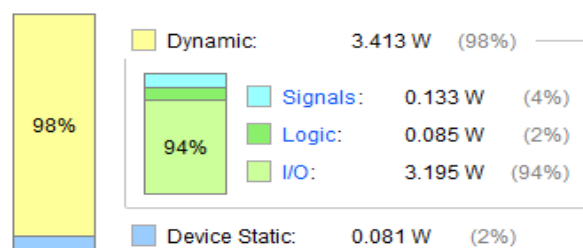
### Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** 3.494 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 42.5°C  
**Thermal Margin:** 42.5°C (8.5 W)  
**Ambient Temperature:** 25.0 °C  
**Effective  $\theta_{JA}$ :** 5.0°C/W  
**Power supplied to off-chip devices:** 0 W  
**Confidence level:** Low

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### On-Chip Power

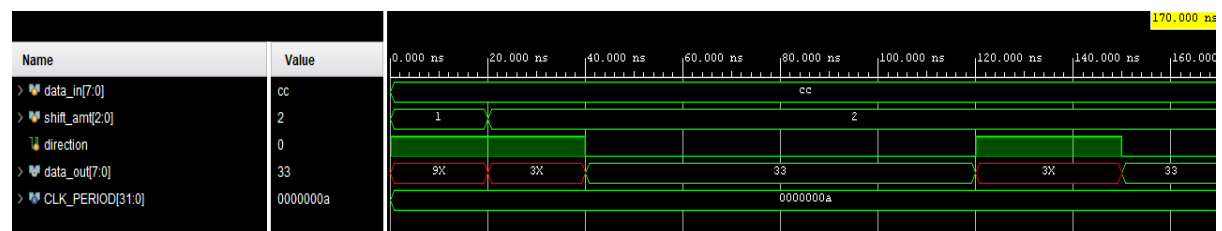




## Synthesis report:-

Report	Type	Options	Modified	Size
▼ Synthesis				
▼ Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/14/23, 12:34 AM	7.9 KB
synthesis_report			9/14/23, 12:34 AM	12.0 KB
▼ Implementation				
▼ impl_1				
▼ Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
▼ Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
▼ Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## Output:-



## **20)ALU**

### **Verilog code:-**

```
module alu_4bit (  
    input [3:0] operand_A,  
    input [3:0] operand_B,  
    input [2:0] alu_control,  
    output reg [3:0] result,  
    output reg zero_flag,  
    output reg carry_flag,  
    output reg overflow_flag  
);  
  
always @* begin  
    case (alu_control)  
        3'b000: result = operand_A + operand_B;  
        3'b001: result = operand_A - operand_B;  
        3'b010: result = operand_A & operand_B;  
        3'b011: result = operand_A | operand_B;  
        3'b100: result = operand_A ^ operand_B;  
        3'b101: result = operand_A << 1;  
        3'b110: result = operand_A >> 1;  
        3'b111: result = ~operand_A;  
        default: result = 4'b0;  
    endcase  
  
    zero_flag = (result == 4'b0);  
  
    carry_flag = (result[4] == 1);  
  
    overflow_flag = (operand_A[3] & operand_B[3] & ~result[3]) | (~operand_A[3] &  
~operand_B[3] & result[3]);  
  
end
```

```
endmodule
```

## **Testbench:-**

```
module tb_alu_4bit;
```

```
    parameter CLK_PERIOD = 10;
```

```
    reg [3:0] operand_A, operand_B;
```

```
    reg [2:0] alu_control;
```

```
    wire [3:0] result;
```

```
    wire zero_flag, carry_flag, overflow_flag;
```

```
    alu_4bit uut (
```

```
        .operand_A(operand_A),
```

```
        .operand_B(operand_B),
```

```
        .alu_control(alu_control),
```

```
        .result(result),
```

```
        .zero_flag(zero_flag),
```

```
        .carry_flag(carry_flag),
```

```
        .overflow_flag(overflow_flag)
```

```
    );
```

```
    initial begin
```

```
        operand_A = 4'b1101;
```

```
        operand_B = 4'b0101;
```

```
alu_control = 3'b000;
```

```
#10 alu_control = 3'b000;
```

```
#10 $display("Result: %b, Zero: %b, Carry: %b, Overflow: %b", result, zero_flag, carry_flag,  
overflow_flag);
```

```
#10 alu_control = 3'b001;
```

```
#10 $display("Result: %b, Zero: %b, Carry: %b, Overflow: %b", result, zero_flag, carry_flag,  
overflow_flag);
```

```
#10 alu_control = 3'b010;
```

```
#10 $display("Result: %b, Zero: %b, Carry: %b, Overflow: %b", result, zero_flag, carry_flag,  
overflow_flag);
```

```
#10 alu_control = 3'b011;
```

```
#10 $display("Result: %b, Zero: %b, Carry: %b, Overflow: %b", result, zero_flag, carry_flag,  
overflow_flag);
```

```
#10 alu_control = 3'b100;
```

```
#10 $display("Result: %b, Zero: %b, Carry: %b, Overflow: %b", result, zero_flag, carry_flag,  
overflow_flag);
```

```
#10 alu_control = 3'b101;
```

```
#10 $display("Result: %b, Zero: %b, Carry: %b, Overflow: %b", result, zero_flag, carry_flag,  
overflow_flag);
```

```
#10 alu_control = 3'b110;
```

```
#10 $display("Result: %b, Zero: %b, Carry: %b, Overflow: %b", result, zero_flag, carry_flag, overflow_flag);
```

```
#10 alu_control = 3'b111;
```

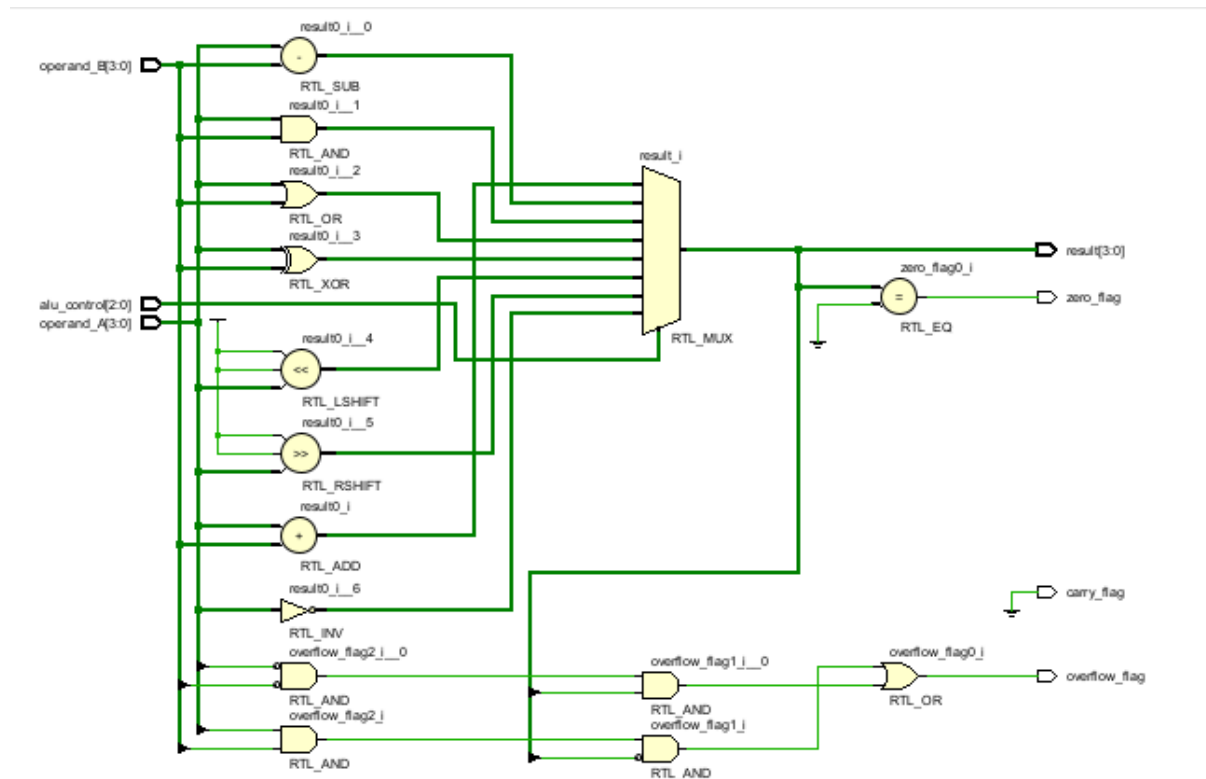
```
#10 $display("Result: %b, Zero: %b, Carry: %b, Overflow: %b", result, zero_flag, carry_flag, overflow_flag);
```

```
#10 $finish;
```

```
end
```

```
endmodule
```

## RTL schematic:-



## Synthesis report:-

Report	Type	Options	Modified	Size
▼ Synthesis				
▼ Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/14/23, 12:44 AM	7.8 KB
synthesis_report			9/14/23, 12:44 AM	12.4 KB
▼ Implementation				
▼ impl_1				
▼ Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
▼ Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
▼ Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## power report:-

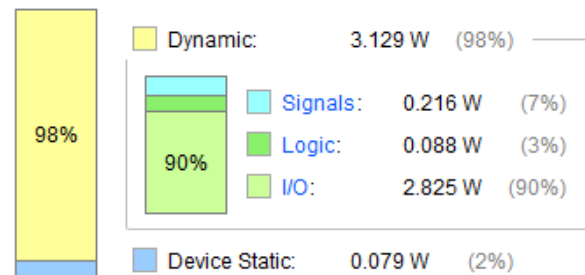
### Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

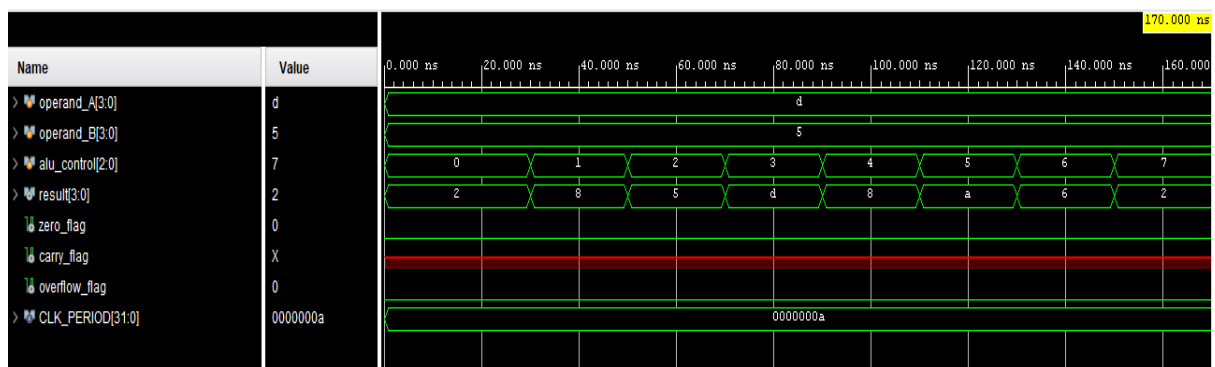
<b>Total On-Chip Power:</b>	<b>3.208 W</b>
<b>Design Power Budget:</b>	<b>Not Specified</b>
<b>Process:</b>	<b>typical</b>
<b>Power Budget Margin:</b>	<b>N/A</b>
<b>Junction Temperature:</b>	<b>41.0°C</b>
<b>Thermal Margin:</b>	<b>44.0°C (8.7 W)</b>
<b>Ambient Temperature:</b>	<b>25.0 °C</b>
<b>Effective <math>\theta_{JA}</math>:</b>	<b>5.0°C/W</b>
<b>Power supplied to off-chip devices:</b>	<b>0 W</b>
<b>Confidence level:</b>	<b>Low</b>

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### On-Chip Power



## Output:-



## **21) 4-Bit Asynchronous Down Counter**

### **Verilog code:-**

```
module down_counter_4bit (  
    input wire clk,  
    input wire rst,  
    output reg [3:0] count  
);  
  
    always @(posedge clk or posedge rst) begin  
        if (rst) begin  
            count <= 4'b0000;  
        end else begin  
            count <= count - 1;  
        end  
    end  
  
endmodule
```

### **Testbench:-**

```
module tb_down_counter_4bit;  
    parameter CLK_PERIOD = 10;  
    reg clk, rst;  
    wire [3:0] count;  
    down_counter_4bit uut (  
        .clk(clk),  
        .rst(rst),  
        .count(count)  
    );  
    always begin  
        #((CLK_PERIOD / 2));
```



```
    clk <= ~clk;
end
initial begin
    clk = 0;
    rst = 0;

    #10 rst = 0;
    #10 $display("Count: %b", count);

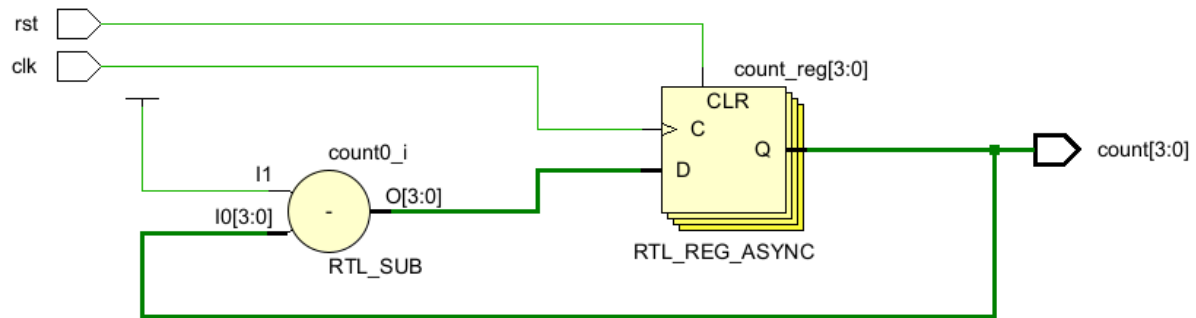
    #10 rst = 1;
    #10 $display("Count: %b", count);
    #10 rst = 0;
    #10 $display("Count: %b", count);

    #10 $display("Count: %b", count);
    #10 #20;
    #10 $display("Count: %b", count);

    #10 $finish;
end

endmodule
```

## RTL schematic:-



## Synthesis report:-

Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/14/23, 12:57 AM	7.9 KB
synthesis_report			9/14/23, 12:57 AM	12.1 KB
Implementation				
impl_1				
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## power report:-

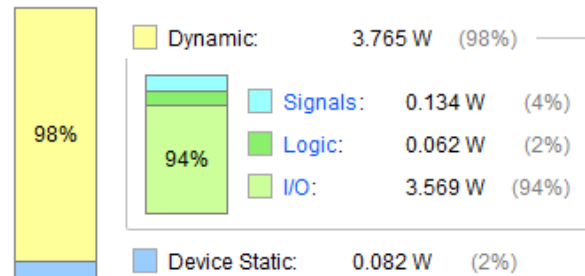
### Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

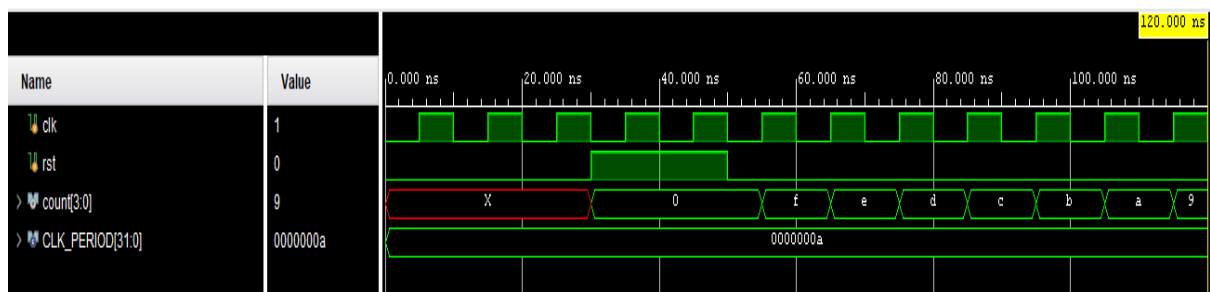
**Total On-Chip Power:** 3.847 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 44.2°C  
Thermal Margin: 40.8°C (8.1 W)  
Ambient Temperature: 25.0 °C  
Effective  $\theta_{JA}$ : 5.0°C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: Low

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### On-Chip Power



## Output:-



## **22) Mod-N UpDown Counter**

### **Verilog code:-**

```
module mod_n_updown_counter (  
    input wire clk,  
    input wire rst,  
    input wire up_down,  
    output reg [3:0] count  
);  
always @(posedge clk or posedge rst) begin  
    if (rst) begin  
        count <= 4'b0000;  
    end else begin  
        if (up_down) begin  
            if (count == 4'b1111) begin  
                count <= 4'b0000;  
            end else begin  
                count <= count + 1;  
            end  
        end else begin  
            if (count == 4'b0000) begin  
                count <= 4'b1111;  
            end else begin  
                count <= count - 1;  
            end  
        end  
    end  
end  
  
endmodule
```

## **Testbench:-**

```
module tb_mod_n_updown_counter;

parameter CLK_PERIOD = 10;

reg clk, rst, up_down;

wire [3:0] count;

mod_n_updown_counter uut (

    .clk(clk),

    .rst(rst),

    .up_down(up_down),

    .count(count)

);

always begin

    #((CLK_PERIOD / 2));

    clk <= ~clk;

end

initial begin

    clk = 0;

    rst = 0;

    up_down = 1;

    #10 rst = 0;

    #10 $display("Count: %b", count);

    #10 rst = 1;

    #10 $display("Count: %b", count);

    #10 rst = 0;

    #10 up_down = 0;

    #10 $display("Count: %b", count);

    #10 $display("Count: %b", count);

    #10 up_down = 1;

    #10 $display("Count: %b", count);
```

```
#10 #50;

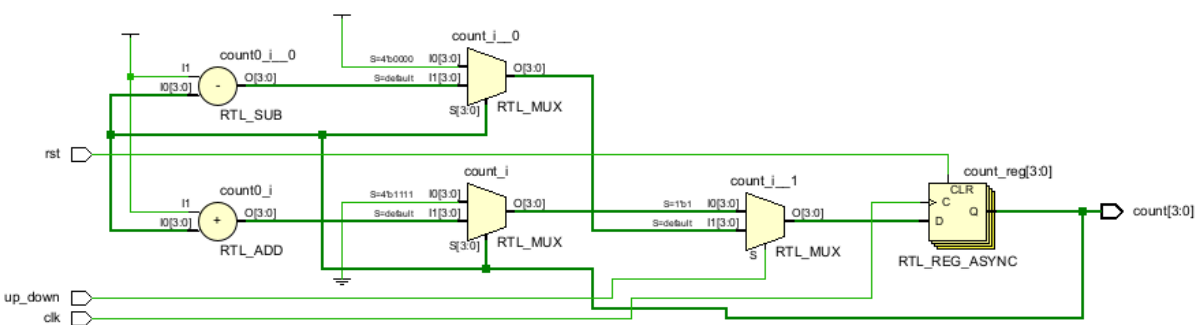
#10 $display("Count: %b", count);

#10 $finish;

end
```

```
endmodule
```

**RTL schematic:-**



**power report:-**

**Summary**

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

<b>Total On-Chip Power:</b>	<b>3.853 W</b>
<b>Design Power Budget:</b>	<b>Not Specified</b>
<b>Process:</b>	<b>typical</b>
<b>Power Budget Margin:</b>	<b>N/A</b>
<b>Junction Temperature:</b>	<b>44.3°C</b>
<b>Thermal Margin:</b>	<b>40.7°C (8.1 W)</b>
<b>Ambient Temperature:</b>	<b>25.0 °C</b>
<b>Effective θJA:</b>	<b>5.0°C/W</b>
<b>Power supplied to off-chip devices:</b>	<b>0 W</b>
<b>Confidence level:</b>	<b>Low</b>

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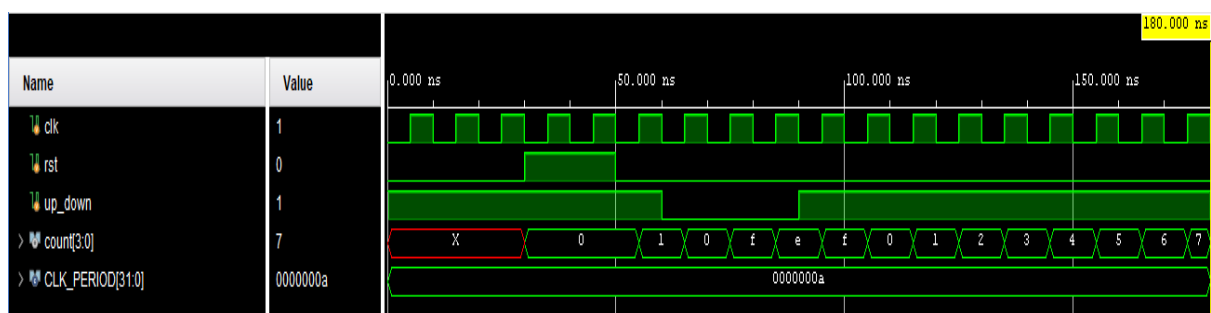
**On-Chip Power**

<b>Dynamic:</b>	<b>3.770 W</b>	<b>(98%)</b>
<b>Signals:</b>	<b>0.143 W</b>	<b>(4%)</b>
<b>Logic:</b>	<b>0.051 W</b>	<b>(1%)</b>
<b>I/O:</b>	<b>3.576 W</b>	<b>(95%)</b>
<b>Device Static:</b>	<b>0.082 W</b>	<b>(2%)</b>

## Synthesis report:-

Report	Type	Options	Modified	Size
▼ Synthesis				
▼ Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/14/23, 1:10 AM	8.0 KB
synthesis_report			9/14/23, 1:10 AM	12.2 KB
▼ Implementation				
▼ impl_1				
▼ Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
▼ Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
▼ Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## Output:-



## **23) Universal Shift Register**

### **Verilog code:-**

```
module universal_shift_register (  
    input wire clk,  
    input wire rst,  
    input wire [3:0] data_in,  
    input wire shift_en,  
    input wire left_shift,  
    input wire right_shift,  
    output reg [3:0] data_out  
);  
  
    always @(posedge clk or posedge rst) begin  
        if (rst) begin  
            data_out <= 4'b0000;  
        end else if (shift_en) begin  
            if (left_shift) begin  
                data_out <= {data_out[2:0], data_out[3]};  
            end else if (right_shift) begin  
                data_out <= {data_out[0], data_out[3:1]};  
            end  
        end else begin  
            data_out <= data_in;  
        end  
    end  
  
endmodule
```



## **Testbench:-**

```
module tb_universal_shift_register;

    parameter CLK_PERIOD = 10;

    reg clk, rst, shift_en, left_shift, right_shift;
    reg [3:0] data_in;
    wire [3:0] data_out;

    universal_shift_register uut (
        .clk(clk),
        .rst(rst),
        .data_in(data_in),
        .shift_en(shift_en),
        .left_shift(left_shift),
        .right_shift(right_shift),
        .data_out(data_out)
    );

    always begin
        #((CLK_PERIOD / 2));
        clk <= ~clk;
    end
```

initial begin

```
clk = 0;  
rst = 0;  
shift_en = 0;  
left_shift = 0;  
right_shift = 0;  
data_in = 4'b1010;
```

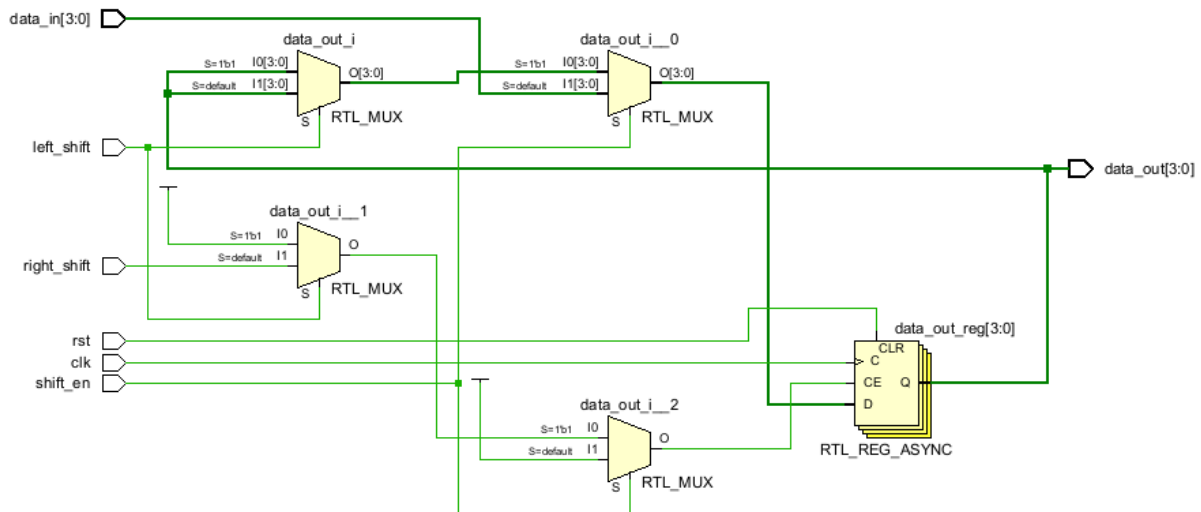
```
#10 rst = 0;  
#10 shift_en = 0;  
#10 $display("Data Out: %b", data_out);
```

```
#10 shift_en = 1;  
#10 left_shift = 1;  
#10 $display("Data Out: %b", data_out);
```

```
#10 left_shift = 0;  
#10 right_shift = 1;  
#10 $display("Data Out: %b", data_out);  
#10 shift_en = 0;  
#10 data_in = 4'b1100;  
#10 $display("Data Out: %b", data_out);  
#10 $finish;  
end
```

endmodule

## RTL schematic:-



## Synthesis report:-

Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/14/23, 1:30 AM	7.9 KB
synthesis_report			9/14/23, 1:30 AM	12.2 KB
Implementation				
impl_1				
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

## power report:-

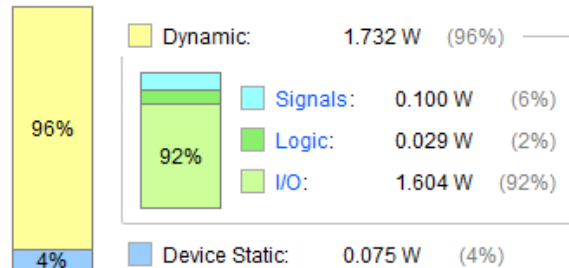
### Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

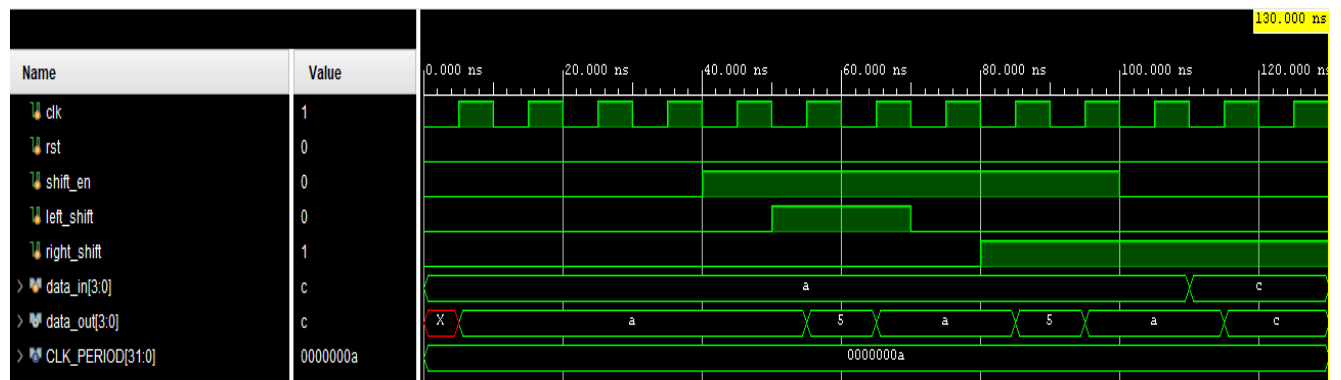
**Total On-Chip Power:** **1.807 W**  
**Design Power Budget:** **Not Specified**  
**Process:** **typical**  
**Power Budget Margin:** **N/A**  
**Junction Temperature:** **34.0°C**  
Thermal Margin: 51.0°C (10.1 W)  
Ambient Temperature: 25.0 °C  
Effective  $\theta_{JA}$ : 5.0°C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: **Low**

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

### On-Chip Power



## Output:-



## **24) CN- Flipflop (Change -No Change Flip Flop) using DFF and 2:1 Mux**

### **Verilog code:-**

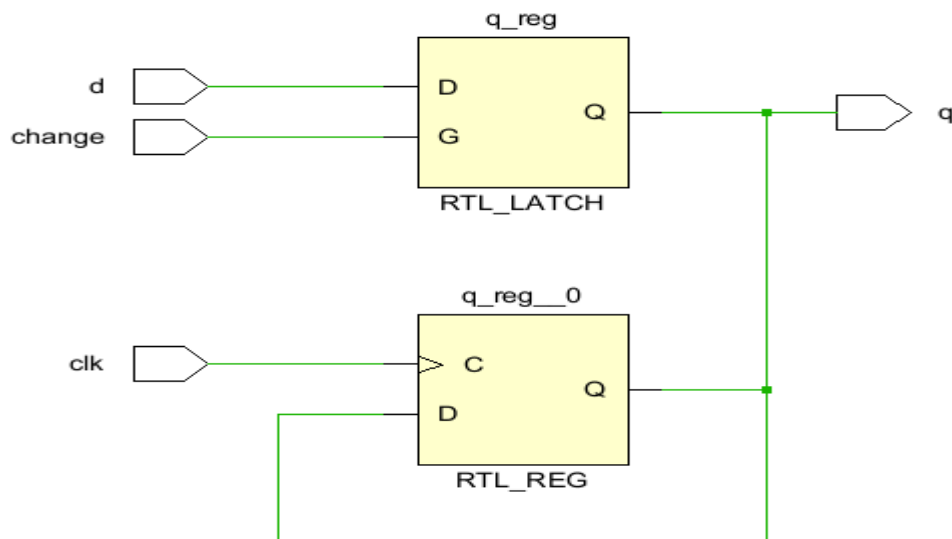
```
module cn_flipflop (  
    input wire clk,  
    input wire d,  
    input wire change,  
    output reg q  
);  
  
    wire q_bar;  
  
    always @(posedge clk) begin  
        if (change) begin  
            q <= d;  
        end  
    end  
  
    assign q_bar = ~q;  
  
    always @* begin  
        if (change) begin  
            q = d;  
        end else begin  
            q = q;  
        end  
    end  
  
endmodule
```

## **Testbench:-**

```
module tb_cn_flipflop;
parameter CLK_PERIOD = 10;
reg clk, d, change;
wire q;
cn_flipflop uut (
    .clk(clk),
    .d(d),
    .change(change),
    .q(q)
);
always begin
    #((CLK_PERIOD / 2));
    clk <= ~clk;
end
initial begin
    clk = 0;
    d = 0;
    change = 0;
    #10 d = 1;
    #10 $display("q: %b", q);
    #10 change = 1;
    #10 $display("q: %b", q);
    #10 change = 0;
    #10 $display("q: %b", q);
    #10 $finish;
end

endmodule
```

## RTL schematic:-



## Synthesis report:-

Report	Type	Options	Modified	Size
Synthesis				
Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/14/23, 1:42 AM	7.8 KB
synthesis_report			9/14/23, 1:42 AM	12.9 KB
Implementation				
impl_1				
Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

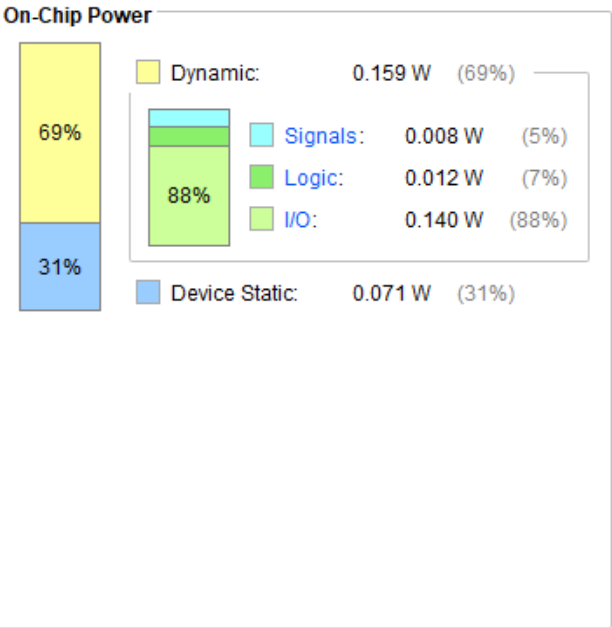
power report:-

Summary

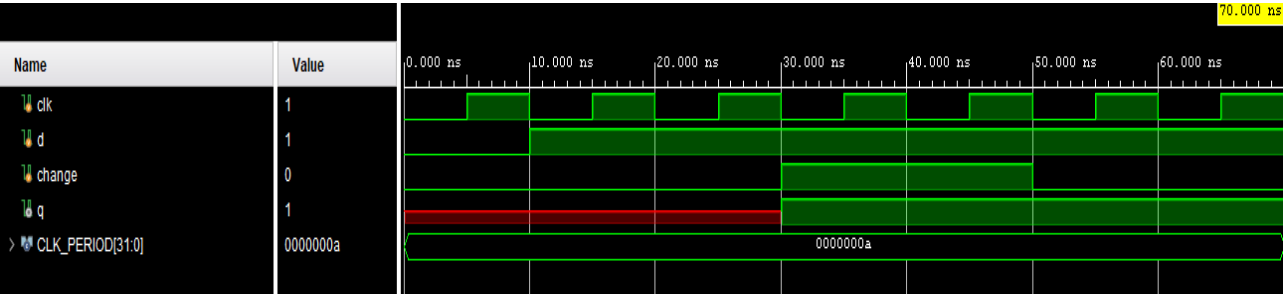
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	0.23 W
Design Power Budget:	Not Specified
Process:	typical
Power Budget Margin:	N/A
Junction Temperature:	26.1°C
Thermal Margin:	58.9°C (11.7 W)
Ambient Temperature:	25.0 °C
Effective θJA:	5.0°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity



Output:-





## **25) Frequency Divider by any Odd Number (Here I Used N=5)**

### **Verilog code:-**

```
module frequency_divider_by_5 (  
    input wire clk,  
    input wire rst,  
    output reg out  
);  
  
    reg [2:0] counter;  
  
    always @(posedge clk or posedge rst) begin  
        if (rst) begin  
            counter <= 3'b0;  
            out <= 0;  
        end else begin  
            if (counter == 3'b100) begin  
                counter <= 3'b0;  
                out <= ~out;  
            end else begin  
                counter <= counter + 1;  
            end  
        end  
    end  
  
endmodule
```

### **Testbench:-**

```
module tb_frequency_divider_by_5;
```

```

parameter CLK_PERIOD = 10;

reg clk, rst;
wire out;

frequency_divider_by_5 uut (
    .clk(clk),
    .rst(rst),
    .out(out)
);

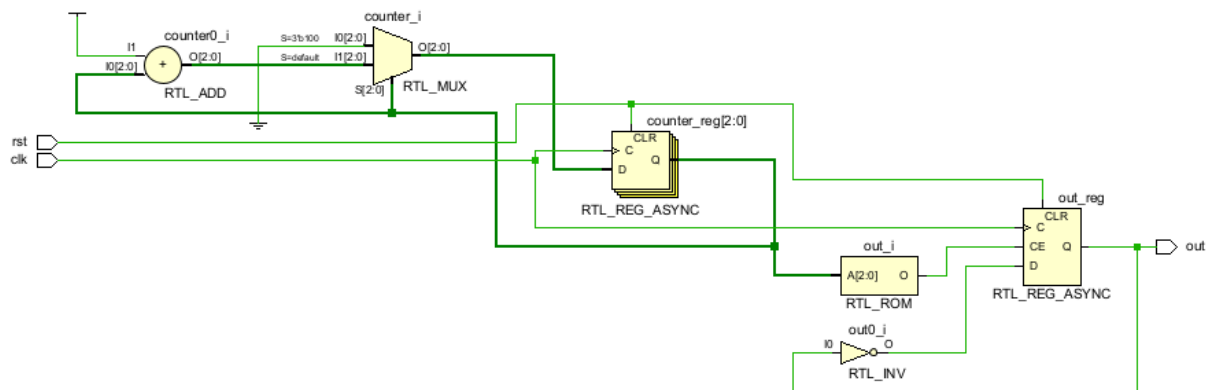
always begin
    #((CLK_PERIOD / 2));
    clk <= ~clk;
end

initial begin
    clk = 0;
    rst = 0;
    #10 $display("Output: %b", out);
    #10 rst = 1;
    #10 $display("Output: %b", out);
    #10 rst = 0;
    #10 $display("Output: %b", out);
    #10 $finish;
end

endmodule

```

## RTL schematic:-



## Synthesis report:-

Report	Type	Options	Modified	Size
▼ Synthesis				
▼ Synth Design (synth_design)				
Utilization - Synth Design	report_utilization		9/14/23, 1:57 AM	7.9 KB
synthesis_report			9/14/23, 1:57 AM	12.3 KB
▼ Implementation				
▼ impl_1				
▼ Design Initialization (init_design)				
Timing Summary - Design Initialization	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Opt Design (opt_design)				
DRC - Opt Design	report_drc			
Timing Summary - Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Power Opt Design (power_opt_design)				
Timing Summary - Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Place Design (place_design)				
IO - Place Design	report_io			
Utilization - Place Design	report_utilization			
Control Sets - Place Design	report_control_sets	verbose = true;		
Incremental Reuse - Place Design	report_incremental_reuse			
Incremental Reuse - Place Design	report_incremental_reuse			
Timing Summary - Place Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Power Opt Design (post_place_power_opt_design)				
Timing Summary - Post-Place Power Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Post-Place Phys Opt Design (phys_opt_design)				
Timing Summary - Post-Place Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
▼ Route Design (route_design)				
DRC - Route Design	report_drc			
Methodology - Route Design	report_methodology			
Power - Route Design	report_power			
Route Status - Route Design	report_route_status			
Timing Summary - Route Design	report_timing_summary	max_paths = 10; report_unconstrained = true;		
Incremental Reuse - Route Design	report_incremental_reuse			
Clock Utilization - Route Design	report_clock_utilization			
Bus Skew - Route Design	report_bus_skew	warn_on_violation = true;		
implementation_log				
▼ Post-Route Phys Opt Design (post_route_phys_opt_design)				
Timing Summary - Post-Route Phys Opt Design	report_timing_summary	max_paths = 10; report_unconstrained = true; warn_on_violation = true;		
Bus Skew - Post-Route Phys Opt Design	report_bus_skew	warn_on_violation = true;		
▼ Write Bitstream (write_bitstream)				
report_webtalk				
implementation_log				

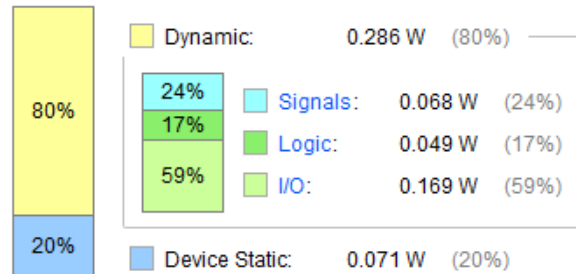
## power report:-

### Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

**Total On-Chip Power:** 0.357 W  
**Design Power Budget:** Not Specified  
**Process:** typical  
**Power Budget Margin:** N/A  
**Junction Temperature:** 26.8°C  
Thermal Margin: 58.2°C (11.6 W)  
Ambient Temperature: 25.0 °C  
Effective  $\theta_{JA}$ : 5.0°C/W  
Power supplied to off-chip devices: 0 W  
Confidence level: Low  
[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

### On-Chip Power



## Output:-

