Krishna Madhur Akella

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EDUCATION

University of Pennsylvania   Philadelphia, PA
Master of Science in Engineering (MSE) in Electrical Engineering   *Expected May 2027*
- **Concentration**: Nanotechnology & Semiconductors
- **Relevant Coursework**: Analog IC Design, Nanoscale Science & Engineering, Semiconductor Memory Devices, Nanofabrication & Nanocharacterization, MEMS & NEMS

Shiv Nadar University   Delhi NCR, India
Bachelor of Technology in Electronics and Communication Engineering   *July 2019 – July 2023*
- **Specialization**: Microelectronics

TECHNICAL SKILLS

Simulation & Modelling: Synopsys Sentaurus TCAD, Cadence Virtuoso, Spectre, Device Physics, MATLAB
Fabrication: Photolithography, Wet/Dry Etching (RIE), CVD/PVD, Spin Coating, Metrology (SEM, AFM, TEM)
Instruments: Keithley SCS-4200, VNA, Signal Analyzers, Oscilloscopes (MDO/DSO), Probe Stations
Hardware/EDA: Altium NEXUS, OrCAD, Cadence SerDes PHY, Xilinx Vivado, LTSpice, ngSpice
Programming: Verilog, C, Embedded C, Python (NumPy, Pandas), MATLAB, LaTeX

PROFESSIONAL EXPERIENCE

University of Pennsylvania (ESE Department)   Philadelphia, PA
ESE Laboratories Staff Member   *Jan 2026 – Present*
- Manage and calibrate high-precision electronic instrumentation (Keithley, Agilent) for ESE research labs.
- Provide technical support for analog component selection and circuit debugging during active lab sessions.

Silicon Laboratories   Hyderabad, India
Associate Hardware Engineer   *July 2023 - March 2025*
- Designed 21 mixed-signal evaluation boards for Silicon Labs MCUs, optimizing RF layout and Signal Integrity (SI).
- Led a team of 6 engineers to validate high-speed interfaces on 115 production-build FPGA setups.
- Achieved first-time-right (FTR) design for a USB-to-UART bridge by implementing rigorous noise reduction techniques.

Cadence Design Systems   Bangalore, India
Hardware Engineering Intern   *May 2022 - September 2022*
- Analyzed DDR SDRAM and SerDes schematics in the Memory Interface Group (MIG) using Cadence SerDes PHY.
- Performed chip layout, schematic design, and simulation on Cadence Virtuoso for 3nm technology nodes.

TECHNICAL PROJECTS

Modelling & Characterization of AlScN Devices | *Synopsys TCAD, Keithley 4200*   Aug 2025 – Present
- Conducting electrical characterization of Ferroelectric devices using **Keithley SCS-4200 Parameter Analyzer**.
- Simulating novel wide-bandgap device architectures (MOSFET, JFET, MESFET) on **SiC substrates**.
- Modelling AlScN polarization switching and hysteresis to optimize Memory Windows for Non-Volatile Memory.
- Calibrating dielectric models against experimental data to validate transport physics in Synopsys Sentaurus.

Nanofabrication of MEMS & Quantum Devices | *Singh Center for Nanotechnology*   Spring 2026
- Fabricated **MEMS Cantilever Beams** and **Comb Drive Arrays** using photolithography, DRIE, and wet etching.
- Performing device characterization utilizing **SEM, AFM, TEM, and Profilometry** to analyze etch profiles.
- Developing process flows for the fabrication of **Graphene FETs** and synthesis of **CdSe Quantum Dots**.

Wideband TIA for Optical Receivers | *Cadence Virtuoso, 45nm CMOS*   Fall 2025
- Designed 8-stage cascaded TIA achieving **519 kΩ (114 dBΩ) gain** and **311 MHz BW**, driving 600Ω load.
- Implemented "Direct Coupling" with tapered loading to eliminate area-intensive AC coupling capacitors.
- Optimized architecture to reduce power consumption to **3.5 mW** (65% below budget) while exceeding gain spec.

Device Modelling & Simulation | *Synopsys Sentaurus TCAD*   Aug 2021 – Aug 2022
- Modelled planar 2D SOI-FET and 3D 14nm FinFET, achieving 3% performance improvement over baseline.
- Simulated tunneling effects and applied advanced mobility models to validate device physics.