Krishna Madhur Akella

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Education

University of Pennsylvania — Philadelphia, PA
Master of Science in Engineering (MSE) in Electrical Engineering — *Expected May 2027*

- **Concentration**: Nanotechnology & Semiconductors
- **Additional Focus**: Mixed Signal & RFIC Design
- **Relevant Coursework**: Analog IC Design, Digital IC Design, Nanoscale Science & Engineering, Semiconductor Memory Devices, Nanofabrication & Nanocharacterization, MEMS & NEMS
- **GPA**: 3.4/4.0

Shiv Nadar University — Delhi NCR, India
Bachelor of Technology in Electronics and Communication Engineering — *July 2019 – July 2023*

- **Specialization**: Microelectronics
- **GPA**: 3.41/4.0

Professional Experience

University of Pennsylvania (ESE Department) — Philadelphia, PA
ESE Laboratories Staff Member — *Jan 2026 – Present*

- Manage and calibrate high-precision electronic instrumentation (Keithley, Agilent) for ESE research labs.
- Provide technical support for analog component selection and circuit debugging during active lab sessions.
- Maintain inventory and procure critical components for wide-bandgap and RF characterization setups.

Silicon Laboratories — Hyderabad, India
Associate Hardware Engineer — *July 2023 - March 2025*

- Designed 21 mixed-signal evaluation boards featuring 32-bit & 8-bit Silicon Labs MCUs, focusing on RF layout optimization and minimizing switching noise in high-speed digital blocks.
- Instructional Hardware at UPenn: Designed two development boards currently utilized as standard coursework platforms for ESE 5160 IoT Edge Scaling at the University of Pennsylvania.
- Led a team of 6 engineers to test and validate 115 units of production-build FPGA setups, including proFPGA motherboards and custom RF-AFE breakout boards.
- Instrumental in the first-time-right (FTR) design and validation of a USB-to-UART bridge converter board hosting Silicon Labs flagship IC, ensuring robust Signal Integrity (SI).
- Collaborated with firmware and validation teams to define board requirements and debugging interfaces, streamlining the post-silicon validation flow.
- Adhered strictly to IPC standards for PCB design, ensuring manufacturability and reliability across all evaluation hardware.

Silicon Laboratories — Hyderabad, India
Hardware Engineering Intern — *January 2023 - July 2023*

- Created schematics for a universal sensor board and aided in preliminary testing of customer-facing evaluation boards using Altium NEXUS.
- Performed rigorous component library management and layout reviews to ensure zero-defect fabrication hand-offs.

Cadence Design Systems — Bangalore, India
Hardware Engineering Intern — *May 2022 - September 2022*

- Analyzed DDR SDRAM and SerDes schematics in the Memory Interface Group (MIG) using Cadence SerDes PHY.
- Performed chip layout, schematic design, device optimization, and ran simulation techniques on Cadence Virtuoso.
- Focused on 3nm technology nodes, specifically characterizing LVTH (Low Threshold Voltage) MOSFET performance.

Technical Skills

Simulation & Modelling: Synopsys Sentaurus TCAD, Cadence Virtuoso, Spectre, Device Physics, MATLAB
Fabrication: Photolithography, Wet/Dry Etching (RIE), CVD/PVD, Spin Coating, Metrology (SEM, AFM, TEM)
Instruments: Keithley SCS-4200, VNA, Signal Analyzers, Oscilloscopes (MDO/DSO), Probe Stations
Hardware/EDA: Altium NEXUS, OrCAD, Cadence SerDes PHY, Xilinx Vivado, LTSpice, ngSpice
Programming: Verilog, C, Embedded C, Python (NumPy, Pandas), MATLAB, LaTeX
Embedded Platforms: Silicon Labs MCUs, STM32, FPGA, Raspberry Pi, Arduino, BeagleBone Black

Technical Projects

Modelling & Characterization of AlScN Ferroelectric Devices | *Synopsys TCAD* Aug 2025 – Present

- Modelling AlScN-based FE-FETs in **Synopsys Sentaurus TCAD**, replacing standard gate oxides with ferroelectric stacks to match real-life wafer configurations.
- Analyzing **Energy Band diagrams (E_c and E_v)** and polarization dynamics to tune ON-OFF voltages and scale channel lengths for cleanroom fabrication feasibility.
- Characterizing cylindrical AlScN ferroelectric memory arrays using **Keithley SCS-4200 Parameter Analyzer**.
- Extracting **PUND** pulse measurements and **DC-IV** curves across varying device dimensions to evaluate switching reliability and scalability.

Nanofabrication of MEMS & Quantum Devices | *Singh Center for Nanotechnology* Spring 2026

- Fabricated **MEMS Cantilever Beams** and **Comb Drive Arrays** using photolithography, DRIE, and wet etching.
- Performing device characterization utilizing **SEM, AFM, TEM, and Profilometry** to analyze etch profiles.
- Developing process flows for the fabrication of **Graphene Field-Effect Transistors (GFETs)** and synthesis of **CdSe Quantum Dots**.

Wideband Transimpedance Amplifier (TIA) for Optical Receivers | *Cadence Virtuoso, 45nm* Fall 2025

- Designed an 8-stage cascaded TIA achieving **519 kΩ (114 dBΩ)** gain, exceeding spec by 3.5x.
- Maintained **311 MHz bandwidth** while driving a heavy 600Ω differential load.
- Implemented a "Direct Coupling" strategy with tapered loading to eliminate area-intensive AC coupling.
- Reduced power consumption to **3.5 mW** (well below 10 mW budget) through architecture optimization.

Low-Power 16x4 SRAM Array Design | *Cadence Virtuoso, 45nm CMOS* Fall 2025

- Designed a synchronous SRAM macro achieving **249 ps (∼4GHz)** worst-case write access time.
- Engineered a robust 6T bitcell with a Cell Ratio of 1.5, eliminating read-disturb failures.
- Optimized peripheral drive strength to improve Area-Power-Delay Figure of Merit (FOM) by **46%**.
- Delivered a compact layout ($2.42\mu m^2$) consuming only 356 μW active power at 1.2V.

Device Modelling & Simulation | *Synopsys Sentaurus TCAD* Aug 2021 – Aug 2022

- Modelled planar 2D SOI-FET and 3D 14nm FinFET, achieving 3% performance improvement over baseline.
- Simulated tunneling effects and applied advanced mobility models to validate device physics.
- **Recognition**: Awarded "Research Grade: Excellent" at the Opportunities for Undergraduate Research (OUR) Conference.

Universal Sensor Board Design | *Altium NEXUS* Spring 2023

- Designed a modular 3-PCB system hosting an MCU, power management, and peripherals.
- Created schematics for 4 memory elements, 7 sensors, and 5 GPIO headers, optimizing layout for signal integrity.

Leadership & Certifications

Vice-Chairperson, IEEE Student Body Jan 2022 – Apr 2023

Secretary, Entrepreneurship Cell, SNU Sep 2019 – Mar 2022

Certifications: Introduction to Embedded System Design (NPTEL); Advances in Freeform Electronics (Yonsei Univ)

Scholarship Recipient, Oxford Royal Academy Summer School Jan 2021