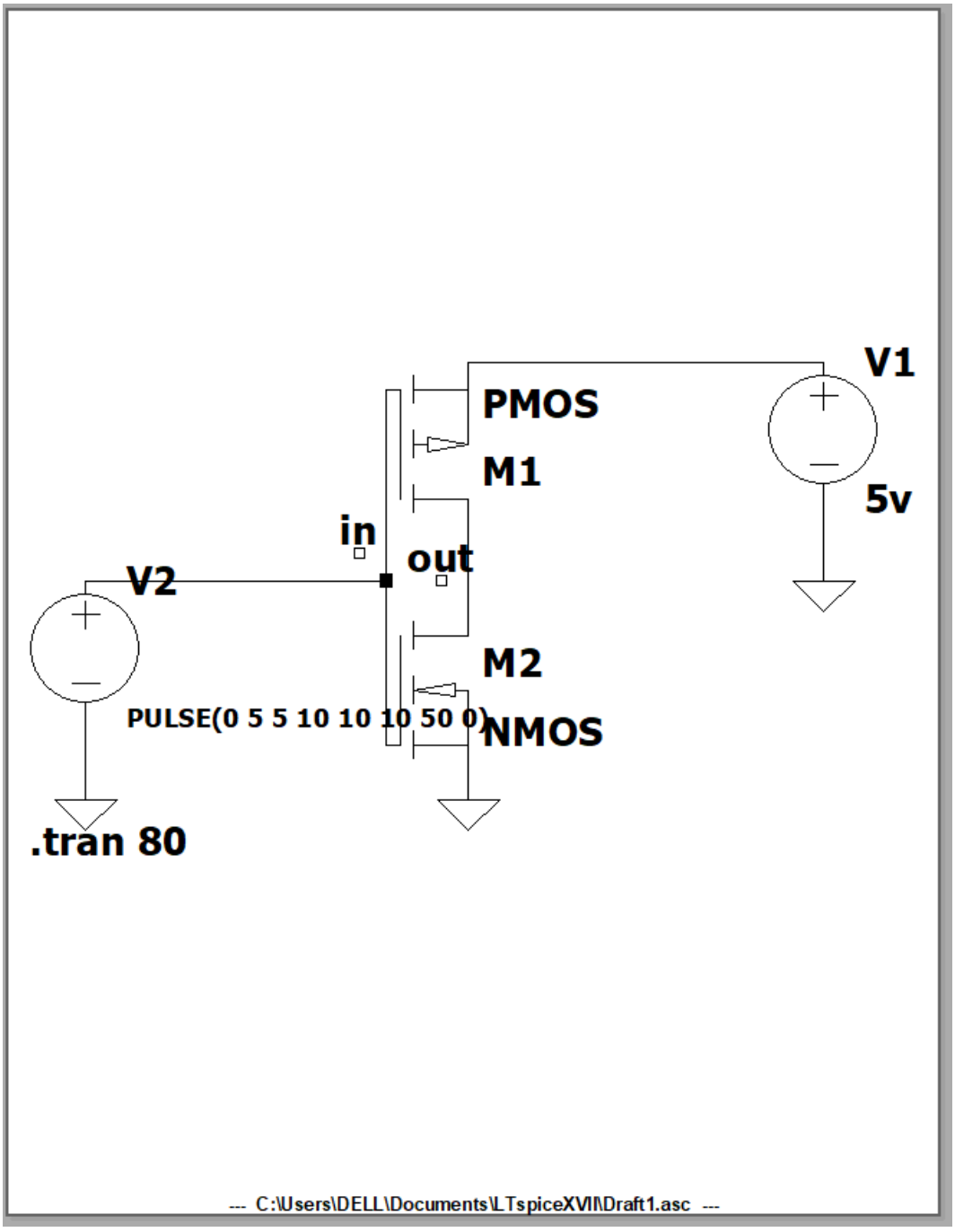
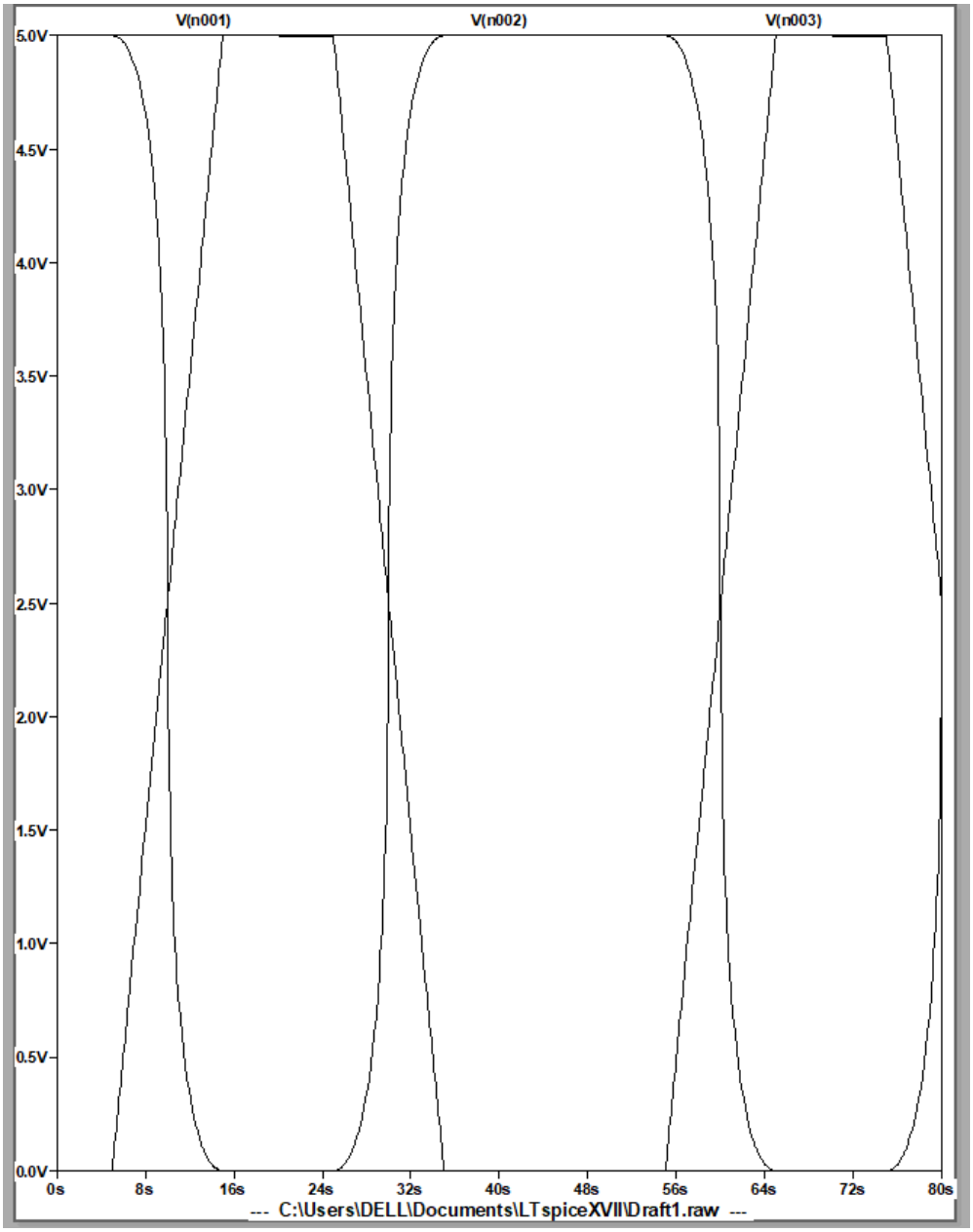
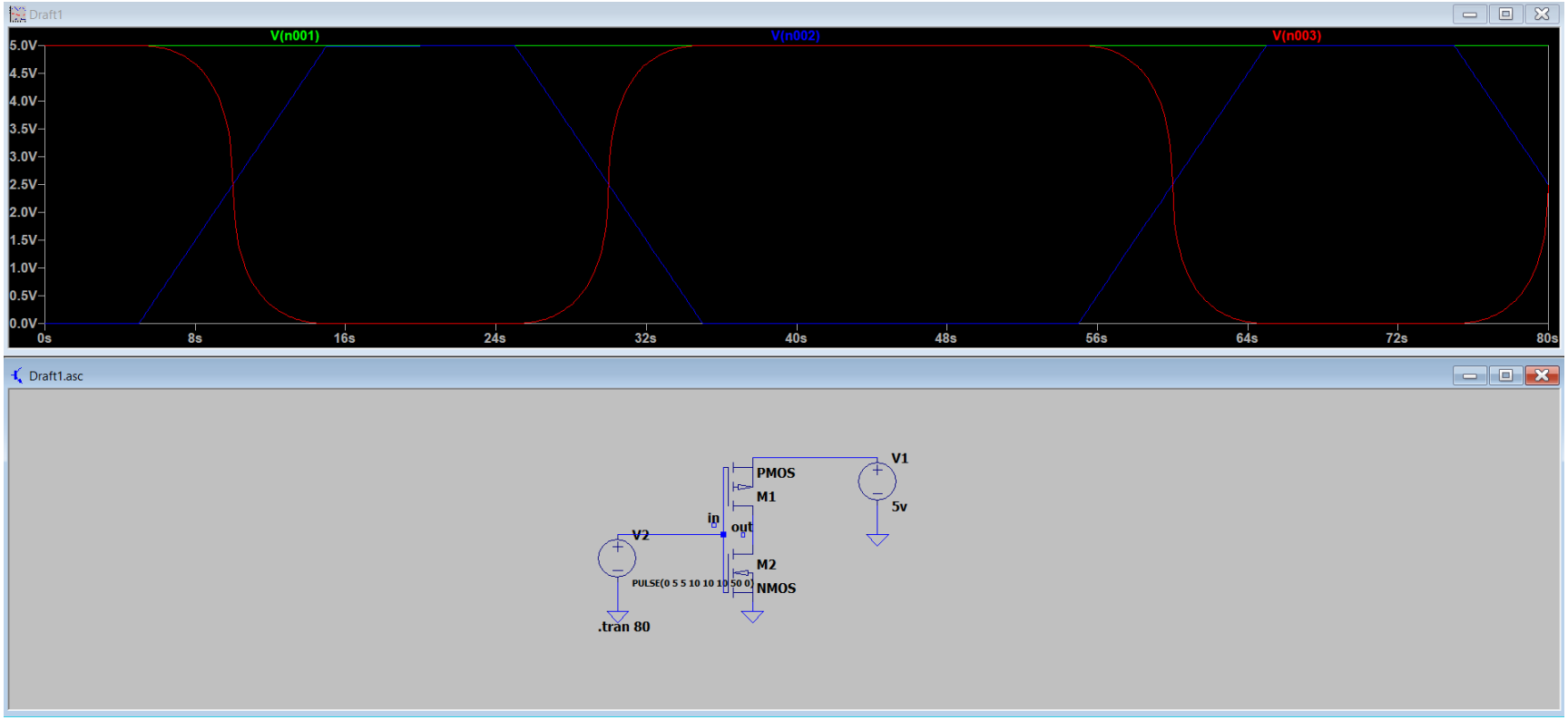
VLSI -1



Circuit Design of the CMOS Inverter circuit.



Graph Observation (in LTspice XVII)


Draft1
V(n001)
V(n002)
V(n003)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0s
8s
16s
24s
32s
40s
48s
56s
64s
72s
80s
Draft1.asc
V1
5v
PMOS
M1
in
out
V2
M2
NMOS
PULSE(0 5 5 10 10 10 50 0)
.tran 80

Lab Report 1: - CMOS Inverter

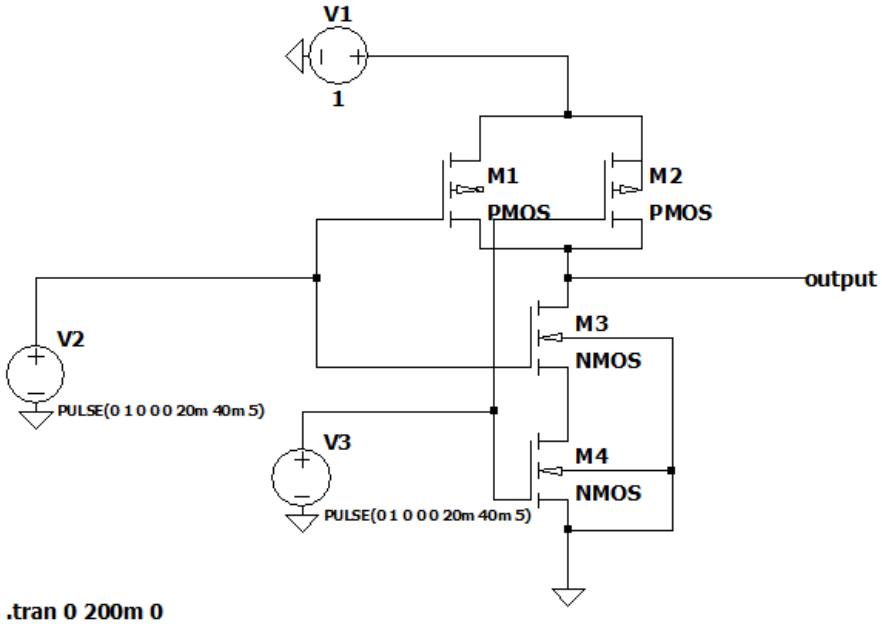
Name: - R. Hemanth Krishna Vineel

Roll no: - 118CS0017

Course : - VLSI Practice

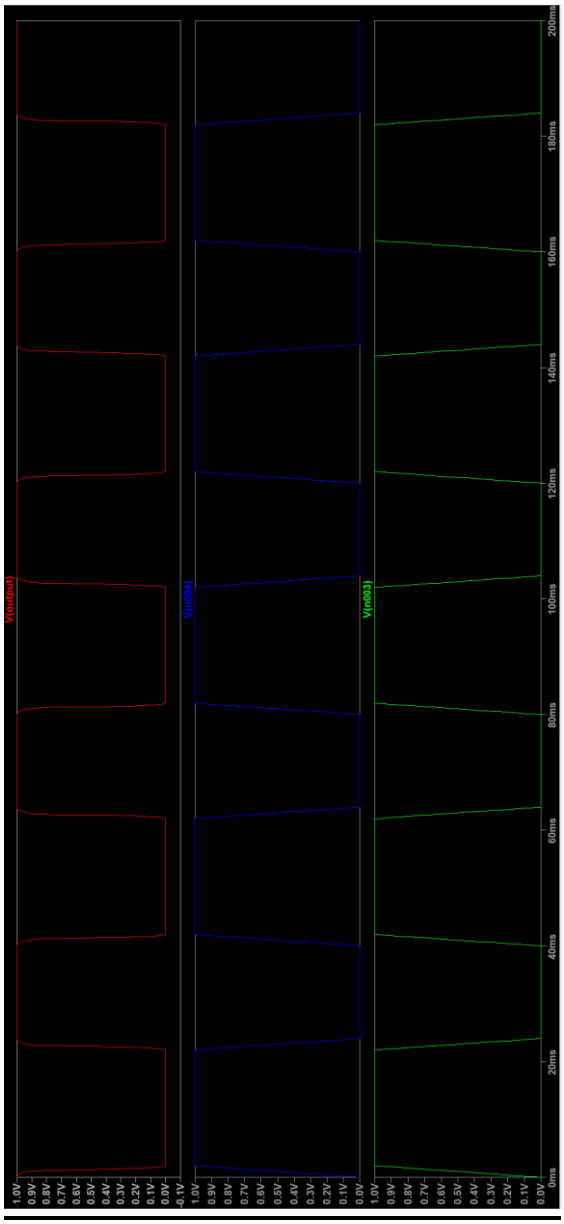
VLSI -2

A. 2 input NAND gate

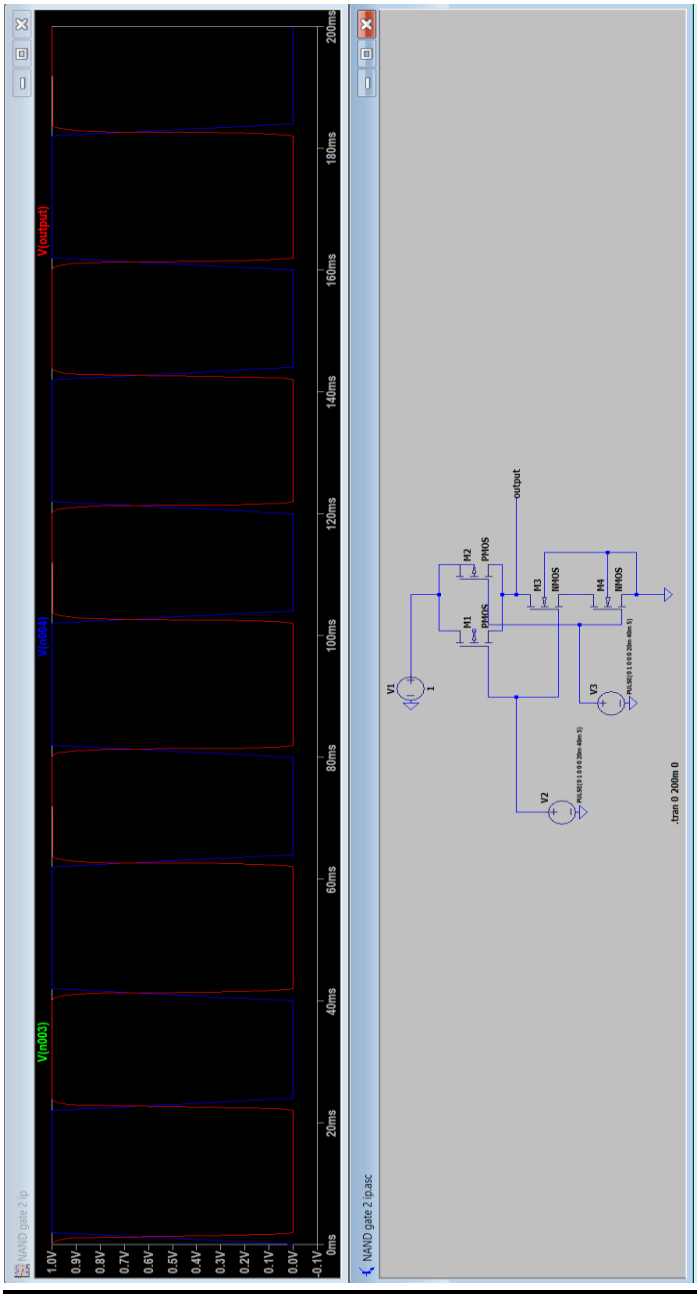


--- C:\Users\DELL\Documents\LTspiceXVII\NAND gate 2 ip.asc ---

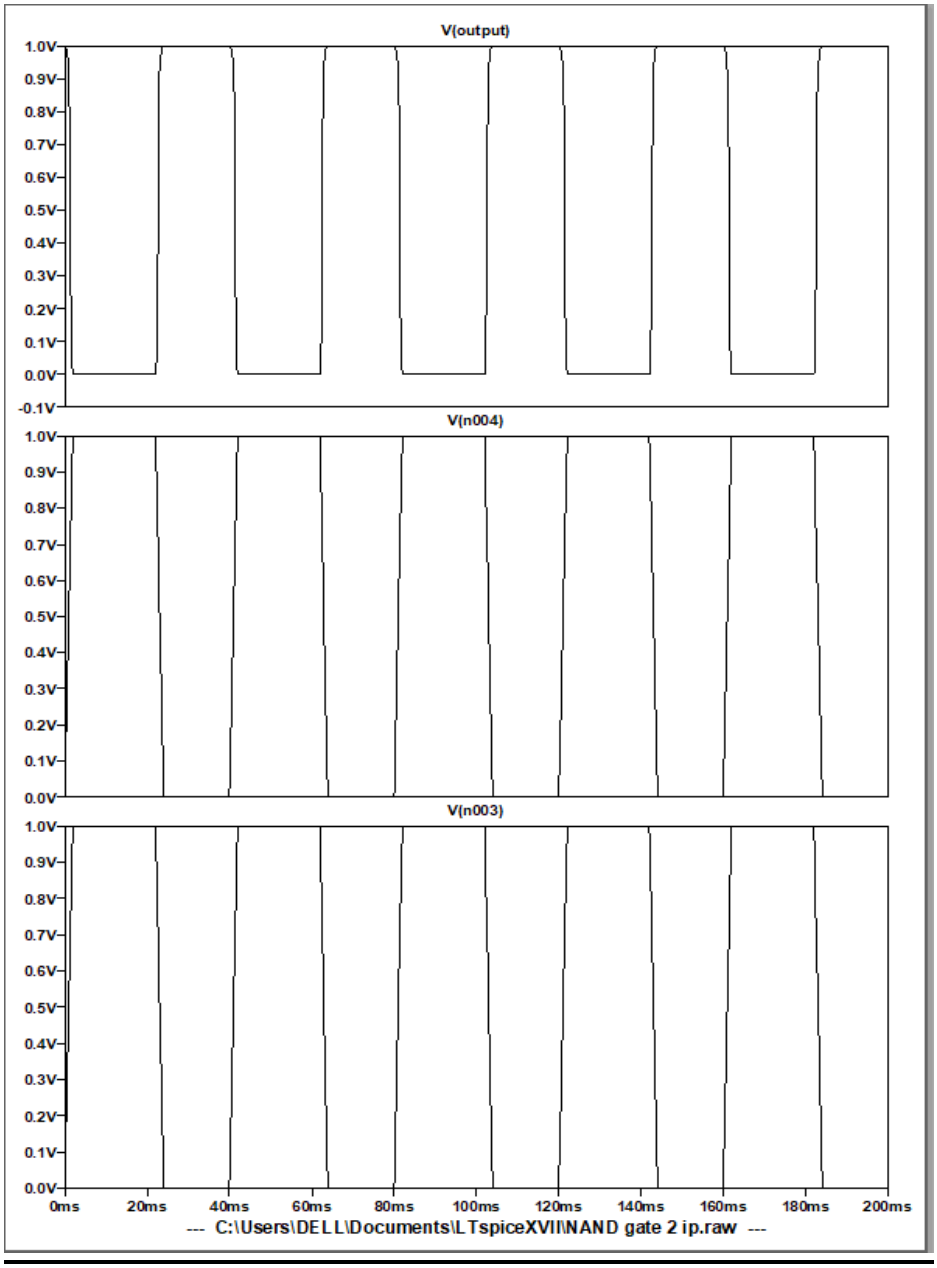
Circuit diagram of 2 input NAND gate



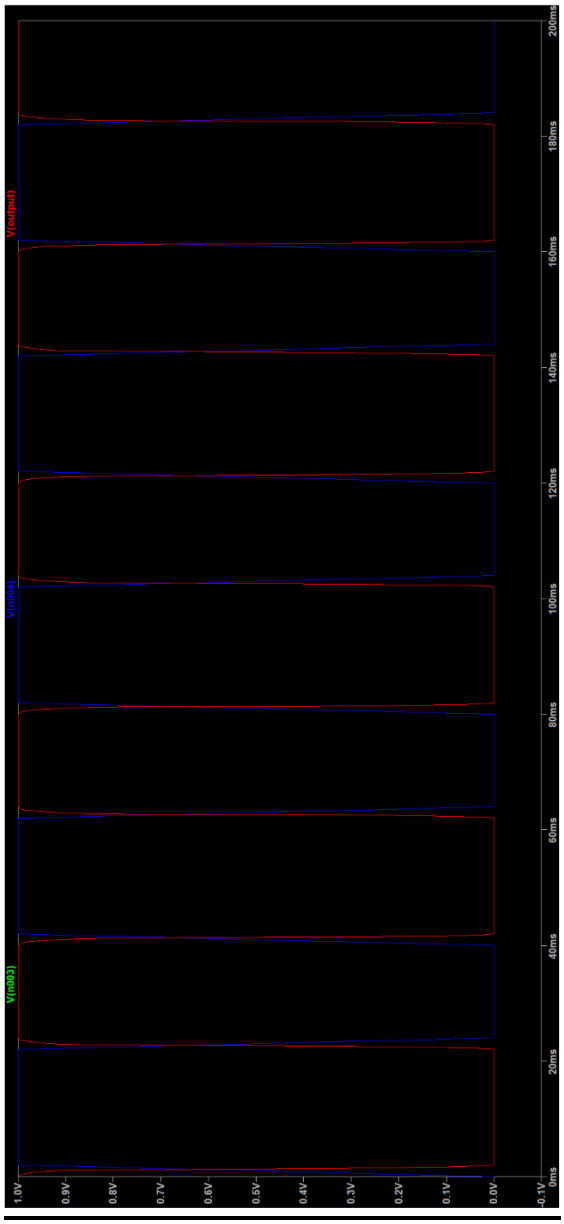
Observation graph -1



Combined image of 2 input NAND gate and it’s graph

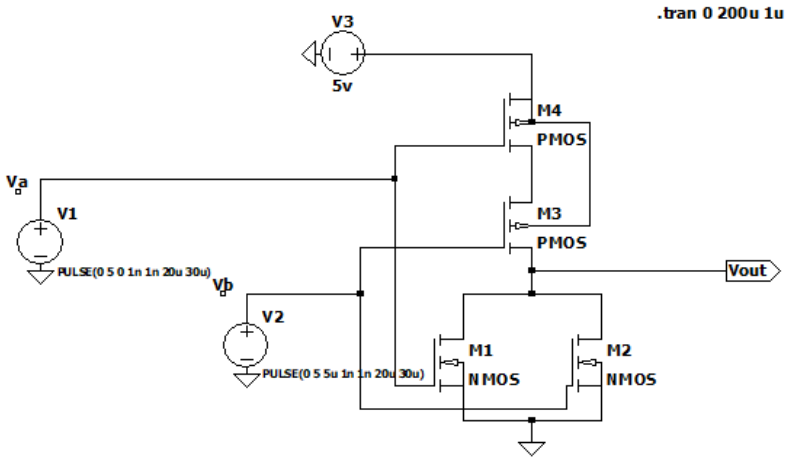


Observation graph -2



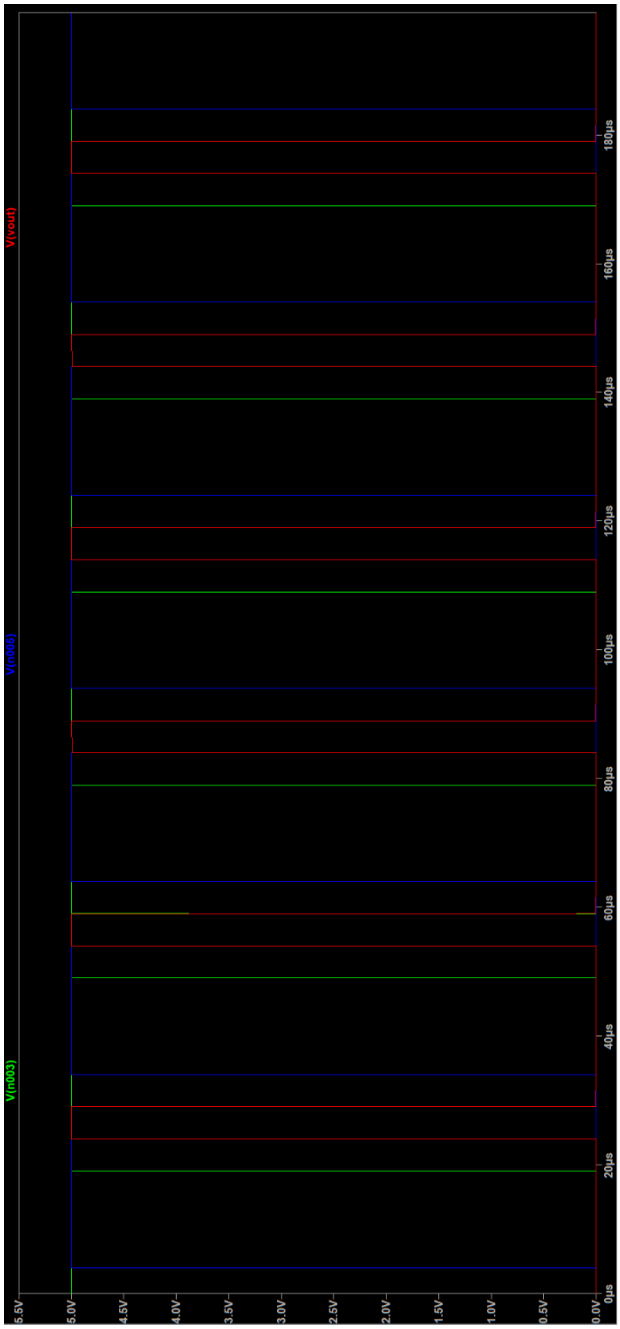
Combined graph observation

B. 2 input NOR gate

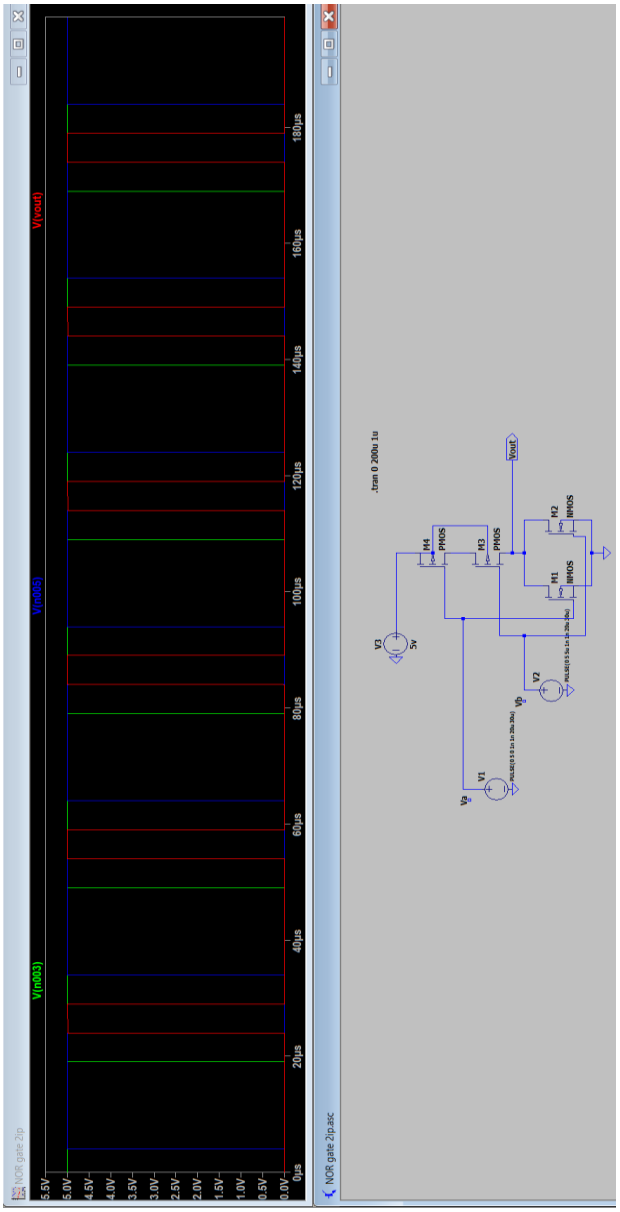


--- C:\Users\DELL\Documents\LTspiceXVII\NOR gate 2ip.asc ---

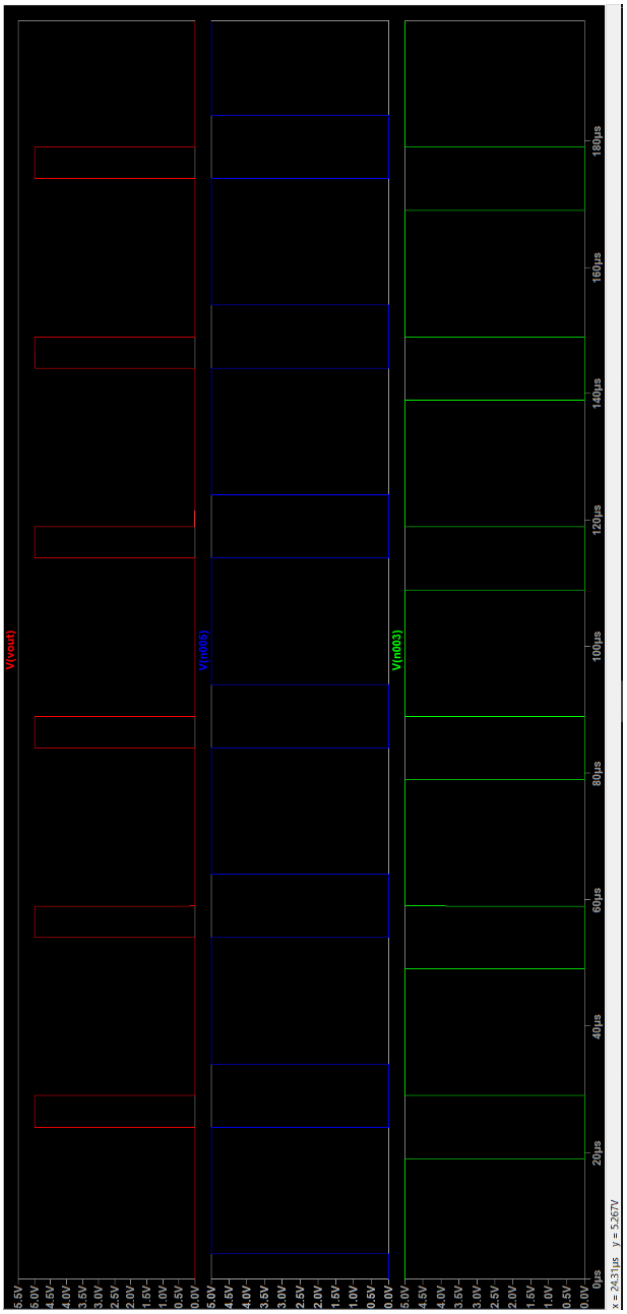
Circuit diagram of 2 input NOR gate



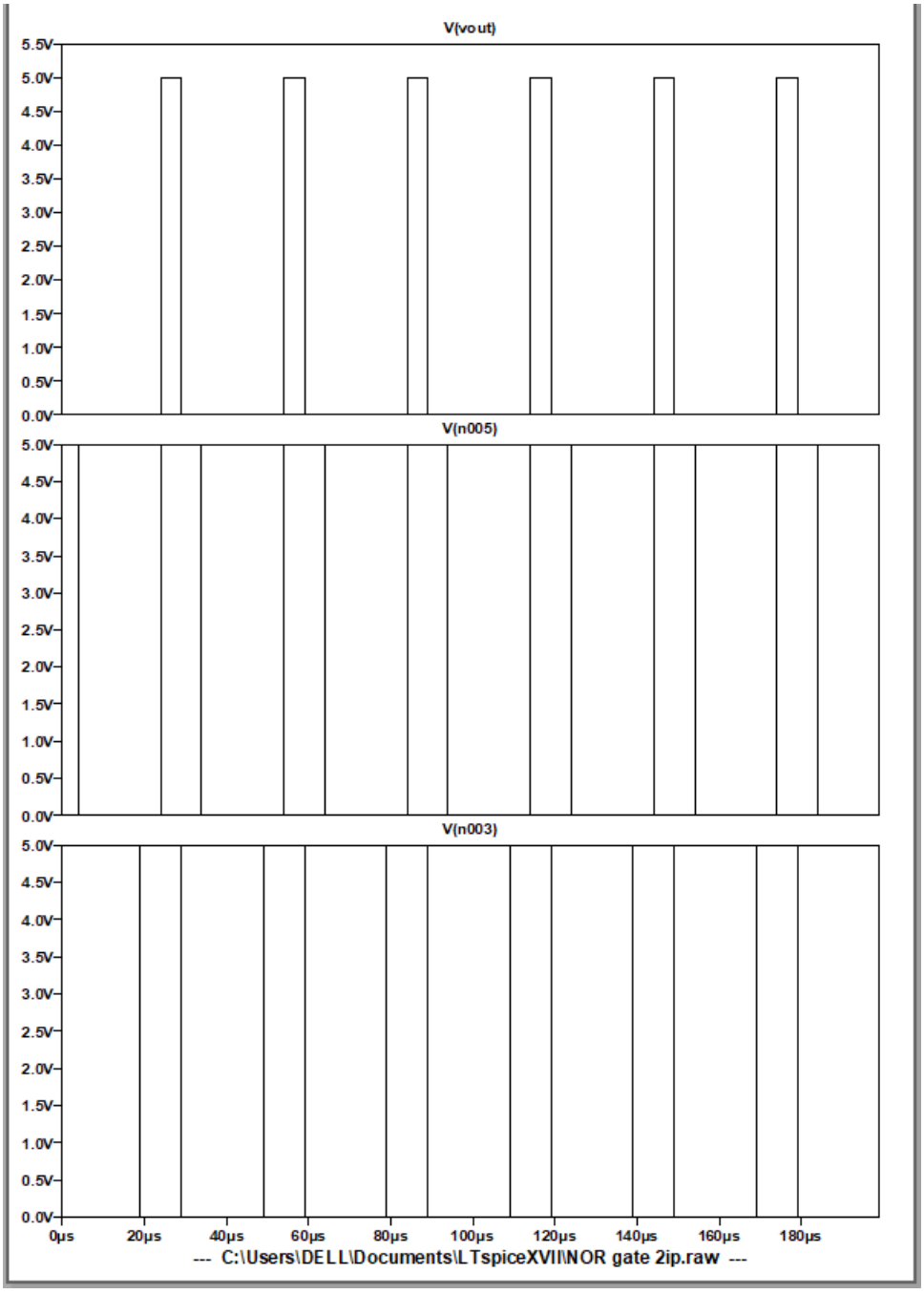
Combined graph observation



Combined image of 2 input NOR gate and it’s graph



Observation Graph 1



Observation graph -2

Lab Report 2: - 2 input NAND gate and 2 input NOR gate

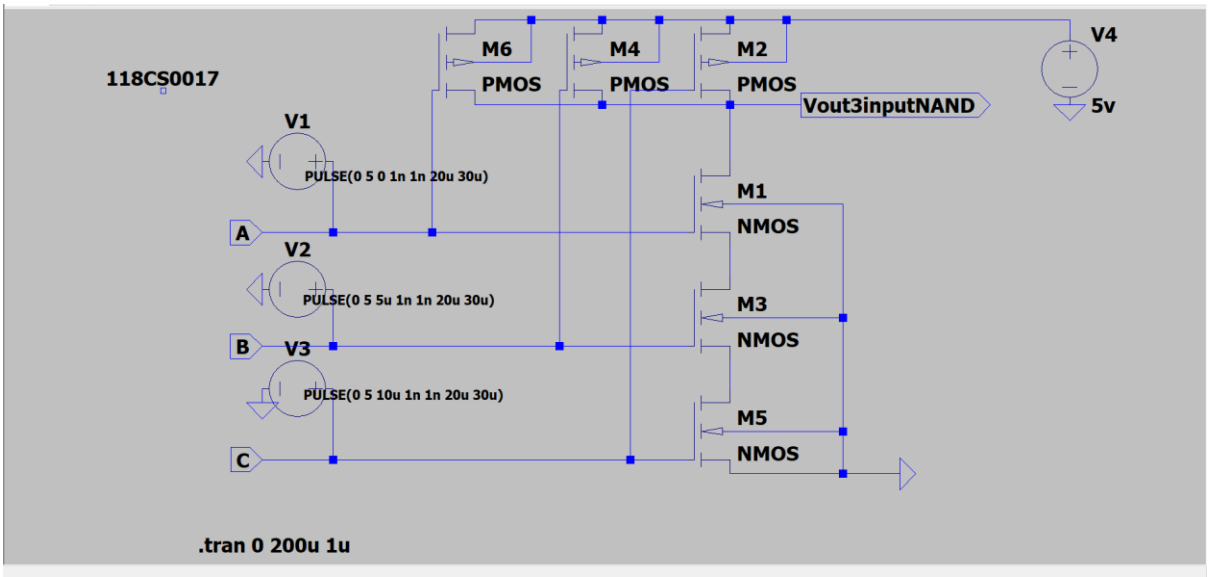
Name: - R. Hemanth Krishna Vineel

Roll no: - 118CS0017

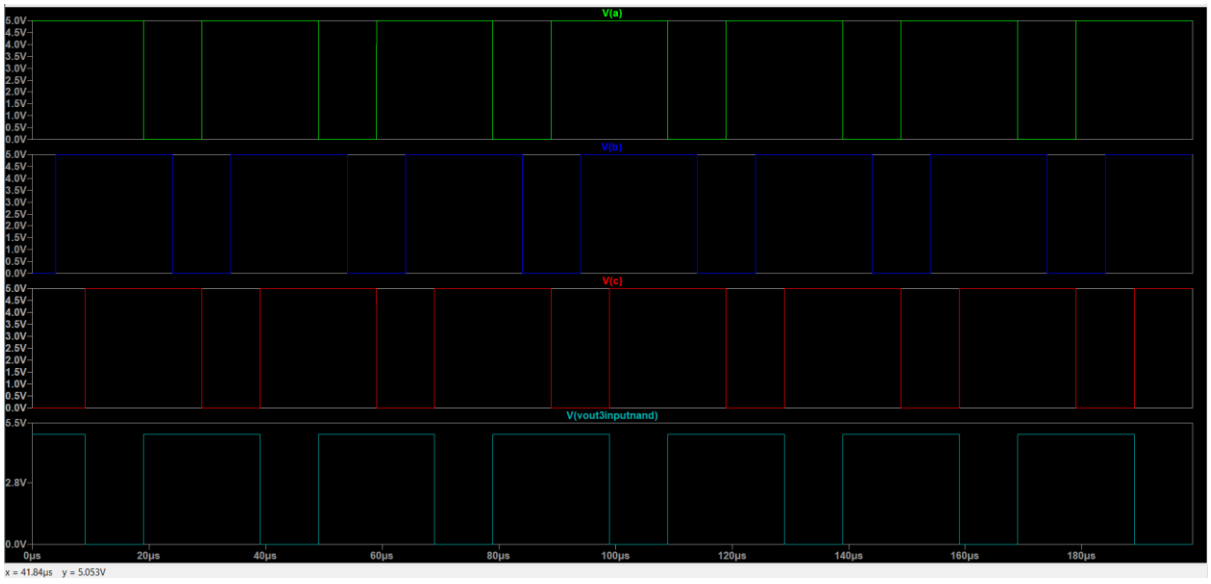
Course : - VLSI Practice

VLSI -3

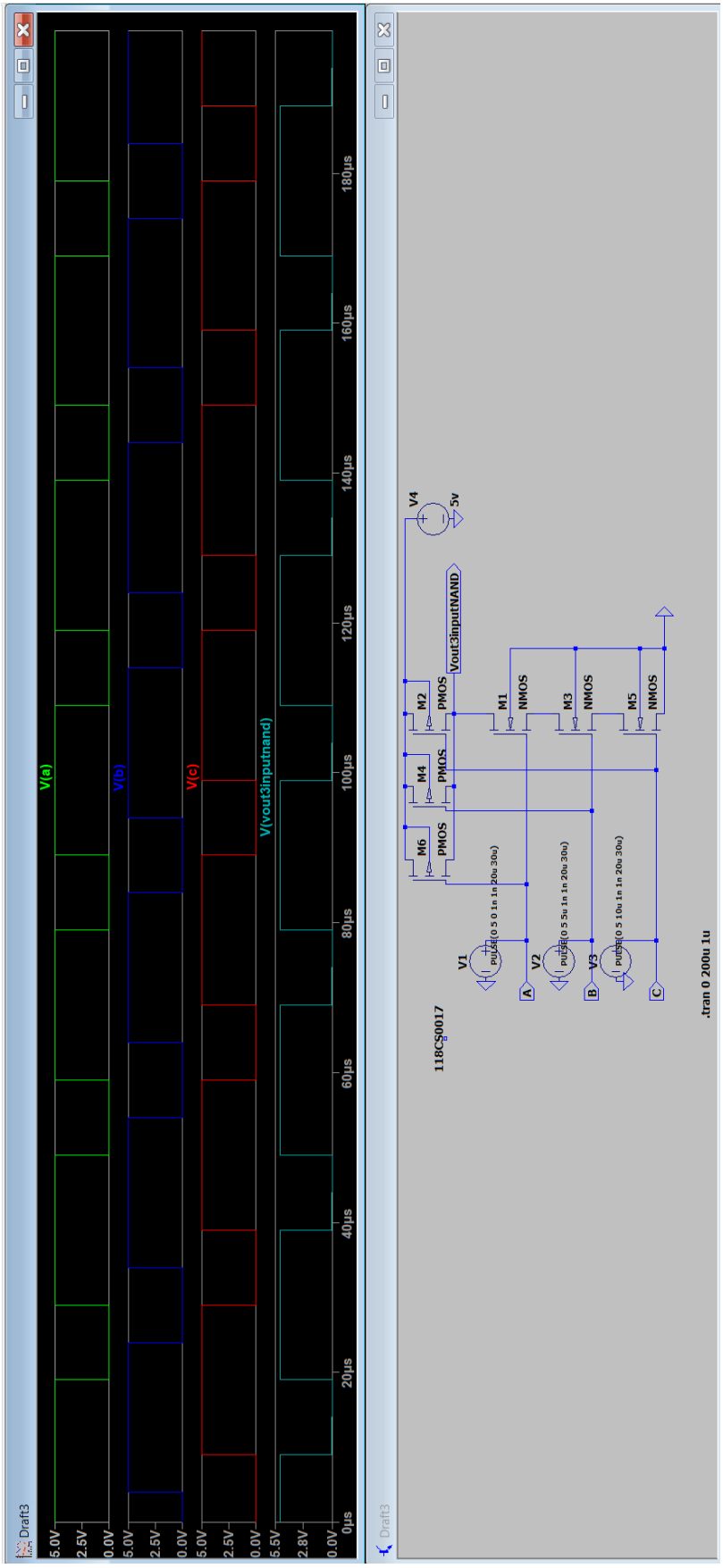
A.3 input NAND gate



Circuit diagram of 3 input NAND using CMOS

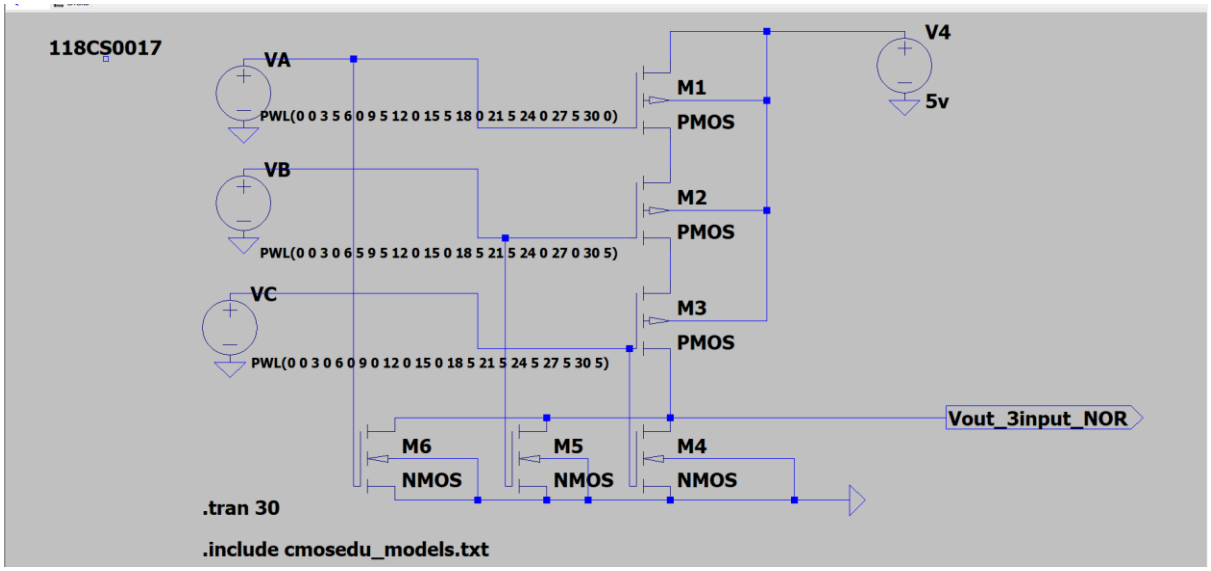


Observation Graph - 1

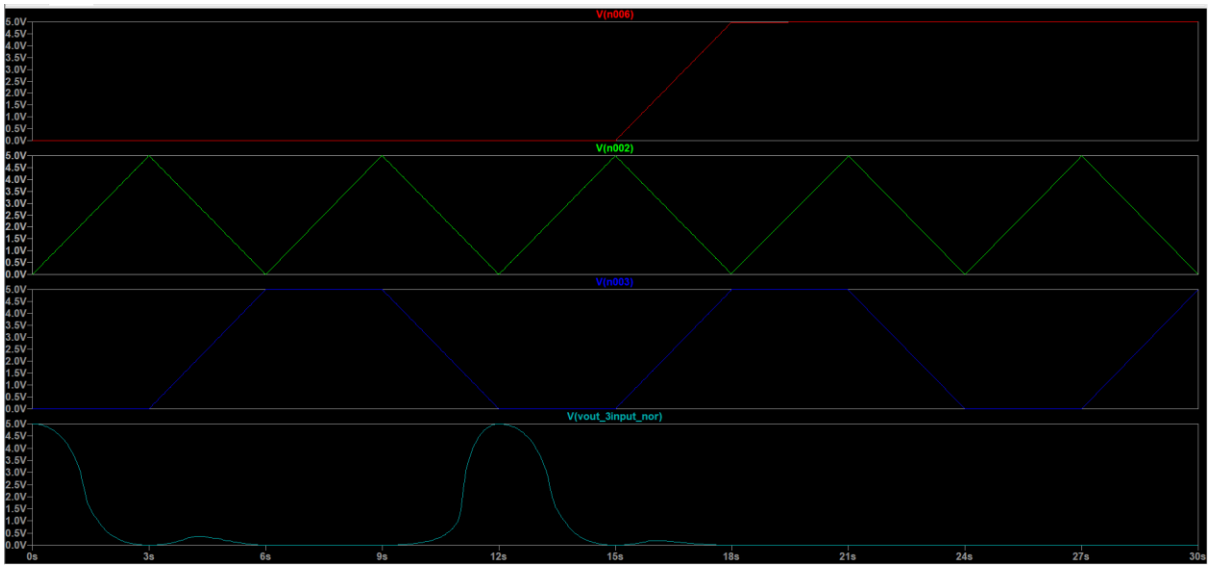


Combined picture of 3 input NAND using CMOS(Circuit and observation graph)

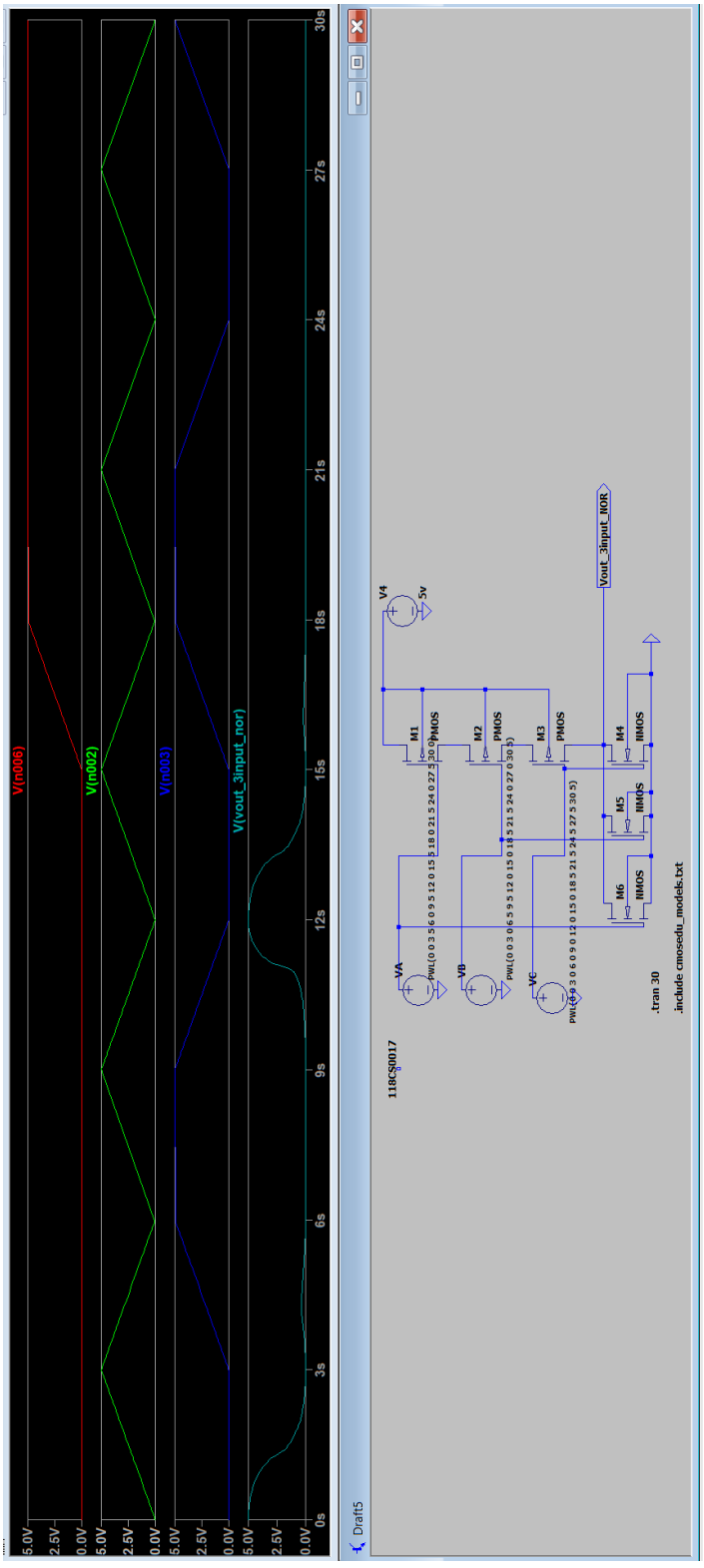
B. 3 input NOR gate



Circuit Diagram of 3 input NOR using CMOS



Observation Graph - 2



Combined picture of 3 input NOR using CMOS(Circuit and observation graph)

Lab Report 3: - 3 input NAND gate and 3 input NOR gate

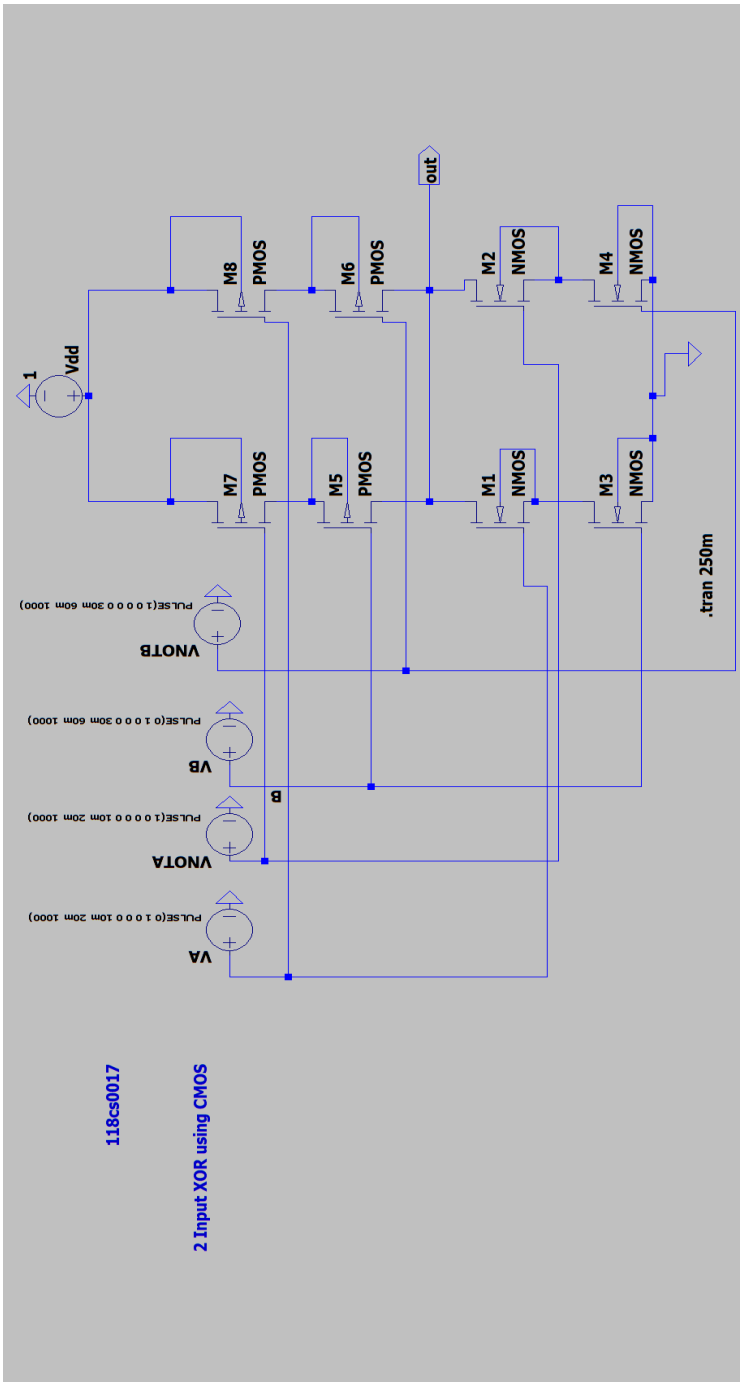
Name: - R. Hemanth Krishna Vineel

Roll no: - 118CS0017

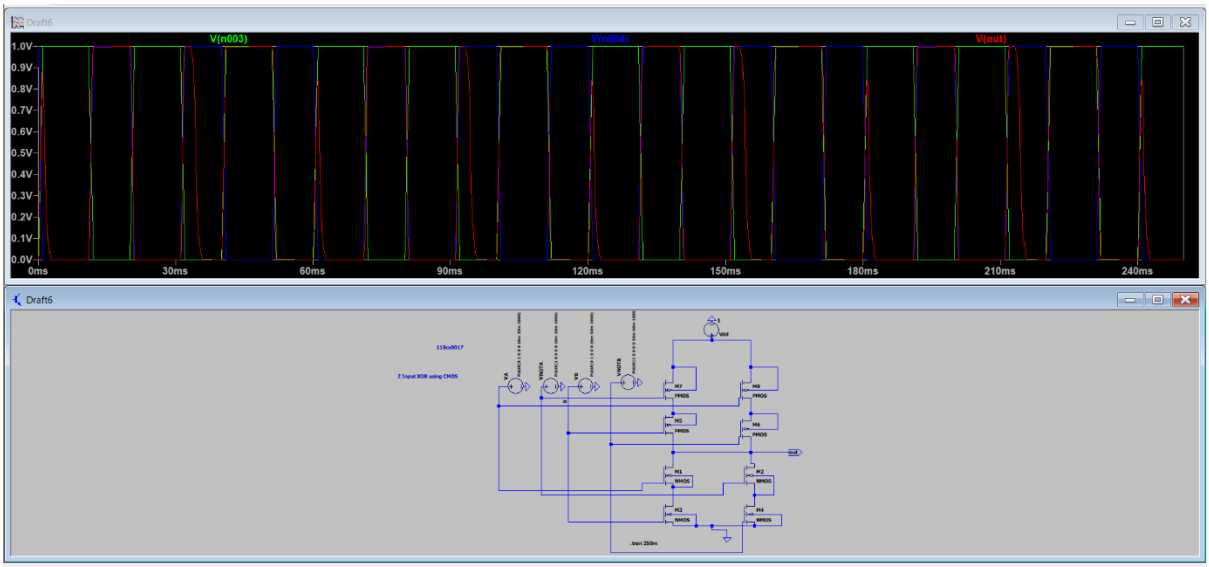
Course : - VLSI Practice

VLSI -4

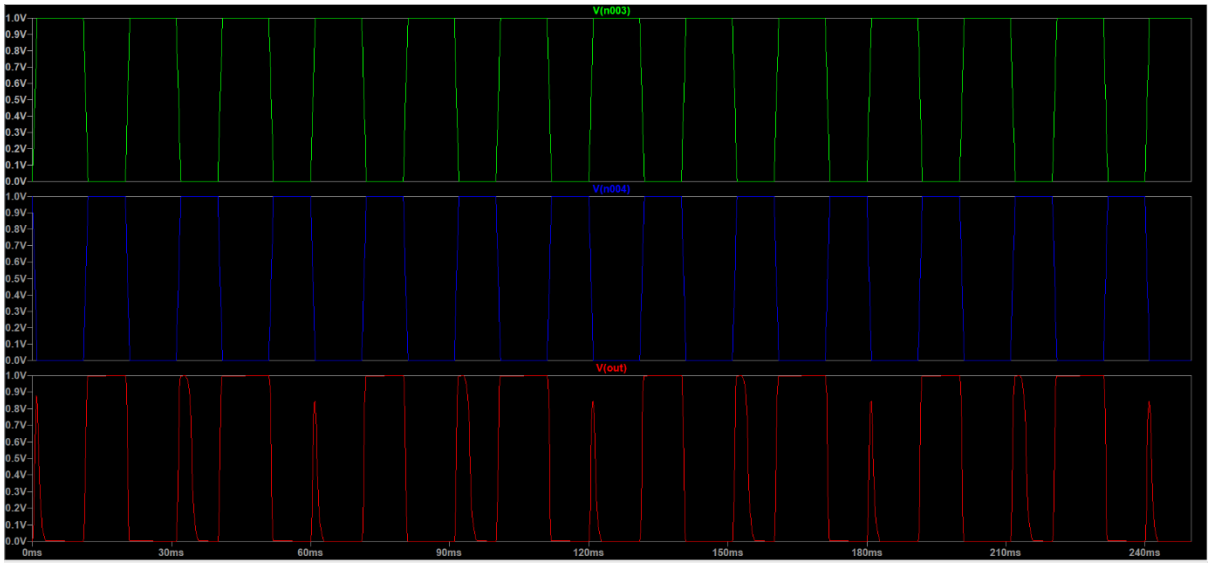
A.2 Input XOR gate using CMOS



Circuit Diagram of 2 input XOR using CMOS

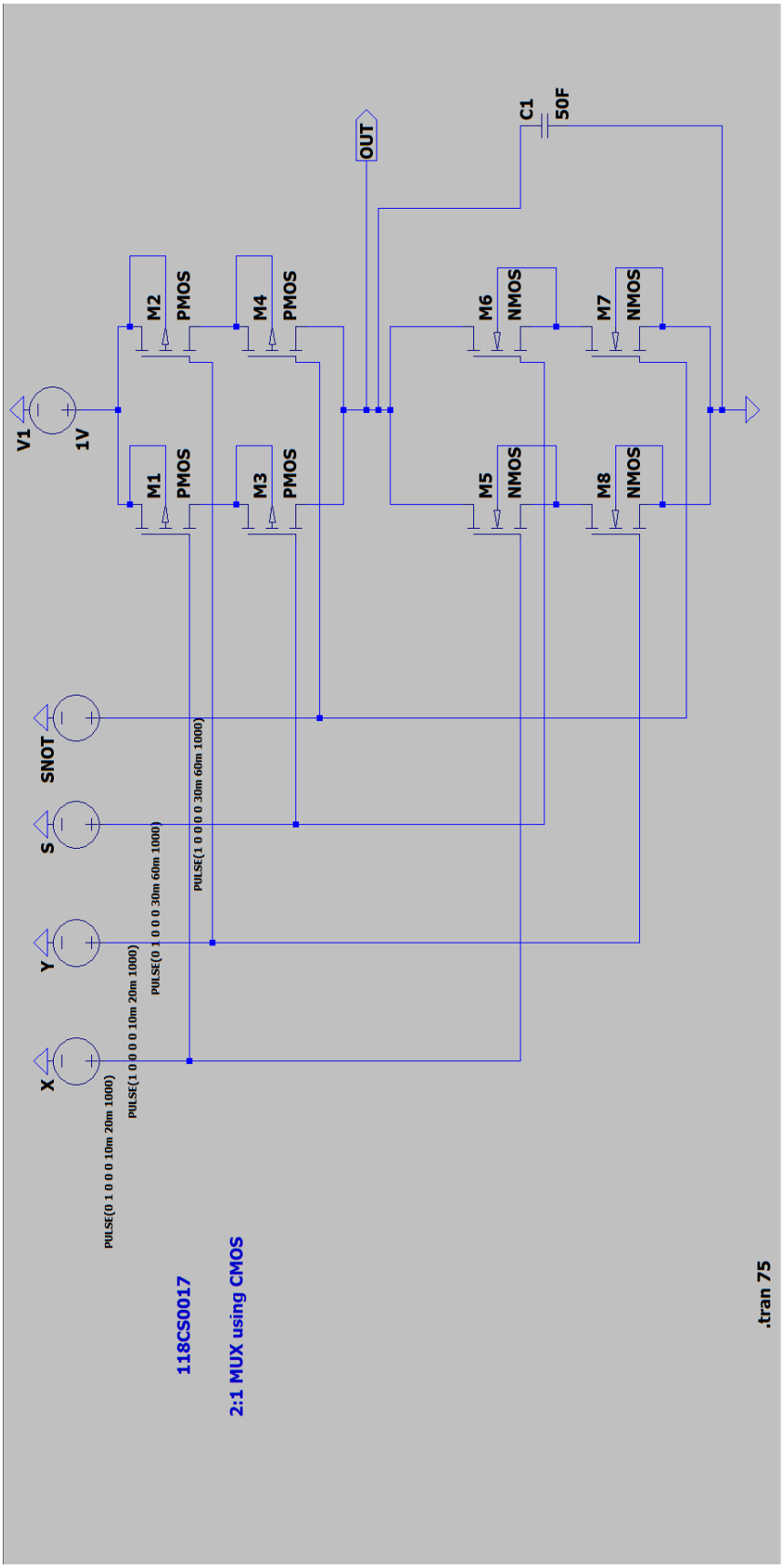


Combined image of circuit and graph

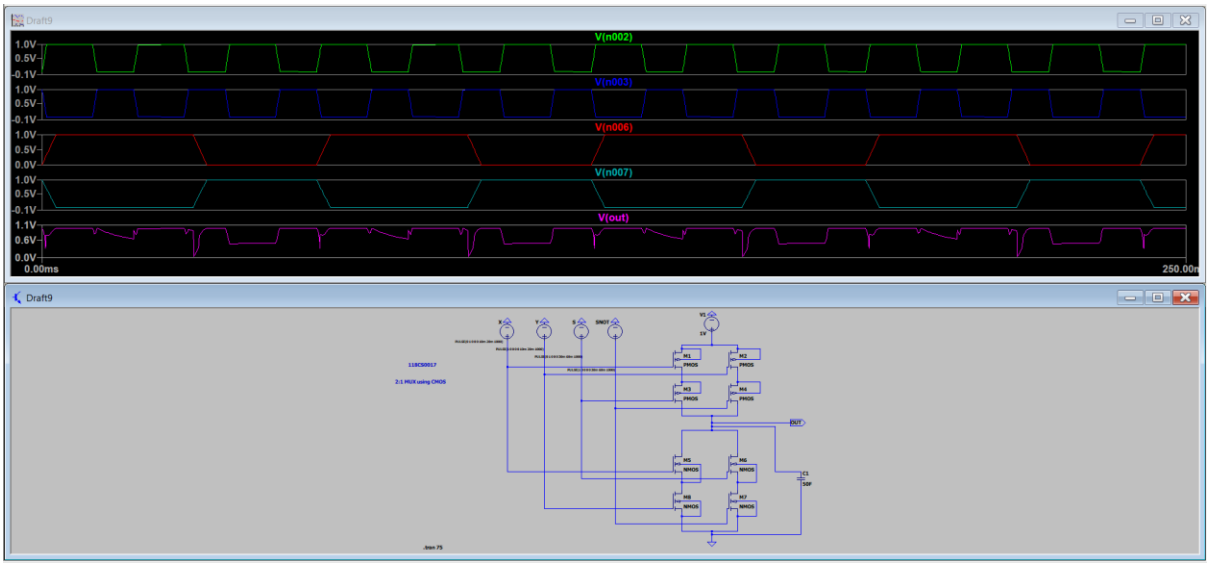


Observation Graph

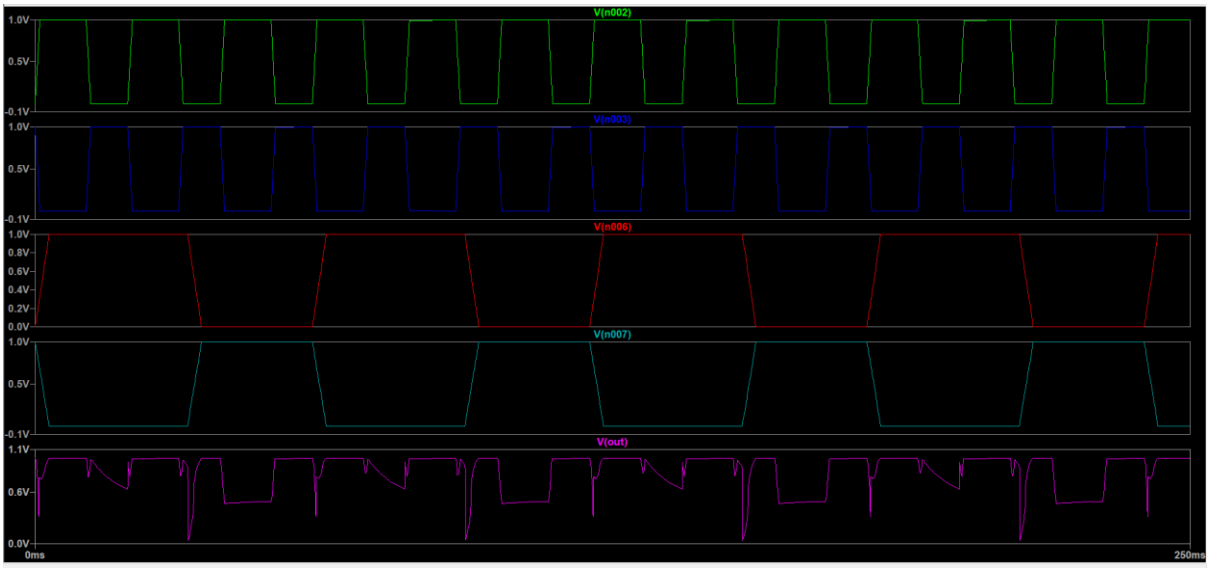
B. 2:1 MUX using CMOS



Circuit diagram of 2:1 MUX using CMOS



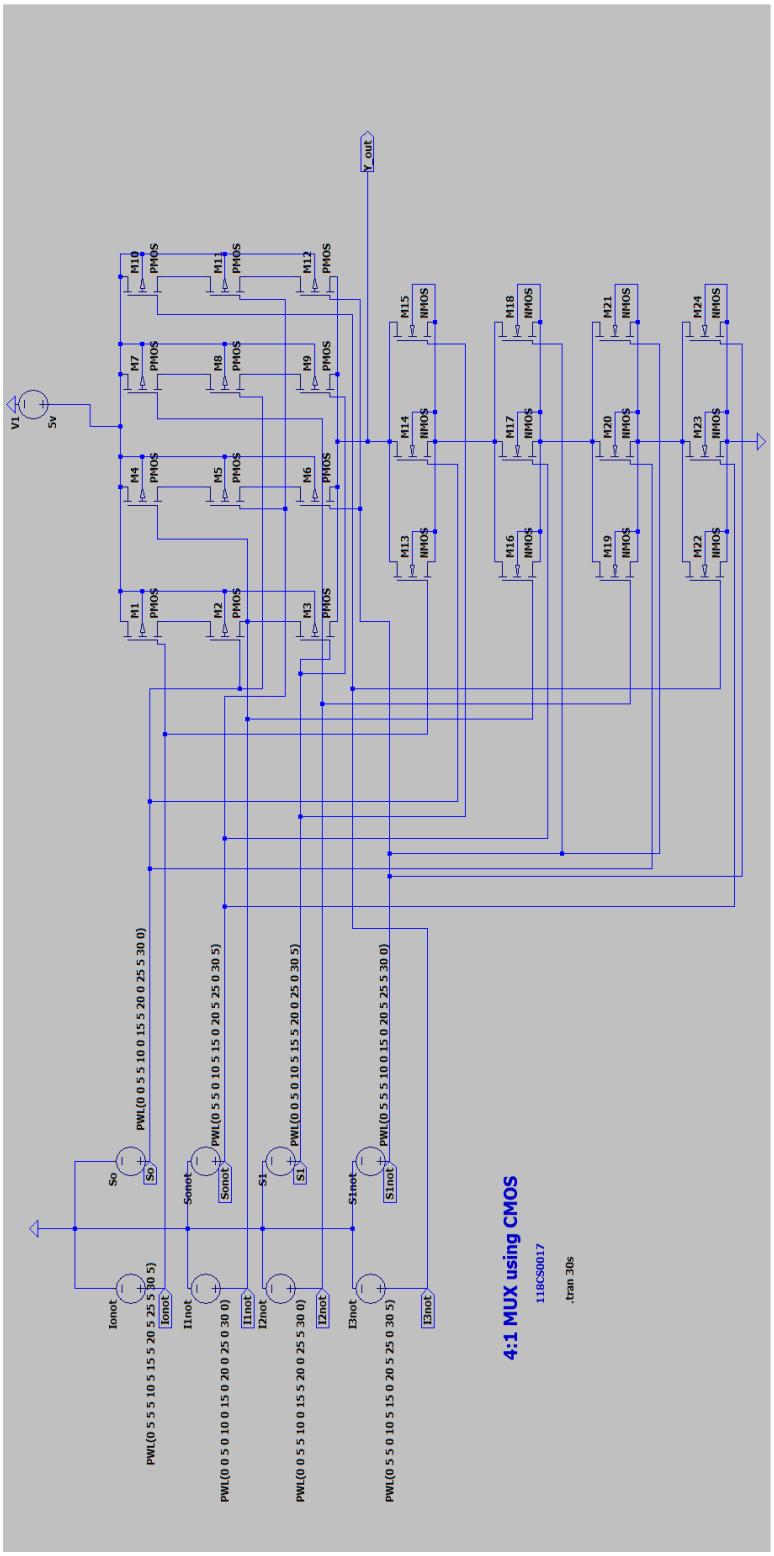
Combined image of circuit and graph



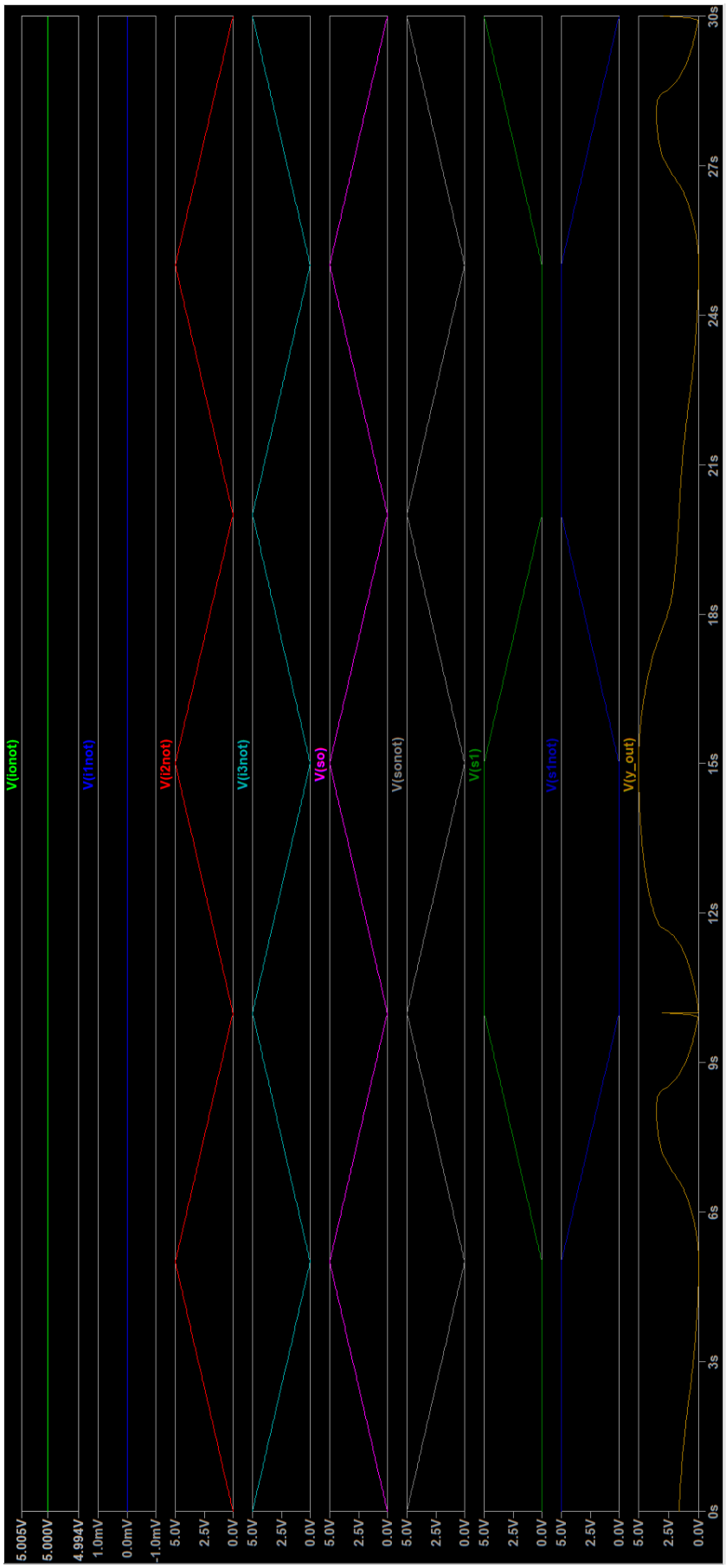
Observation Graph

VLSI LAB

a. 4:1 mux circuit design and the graph.



4:1 mux circuit design



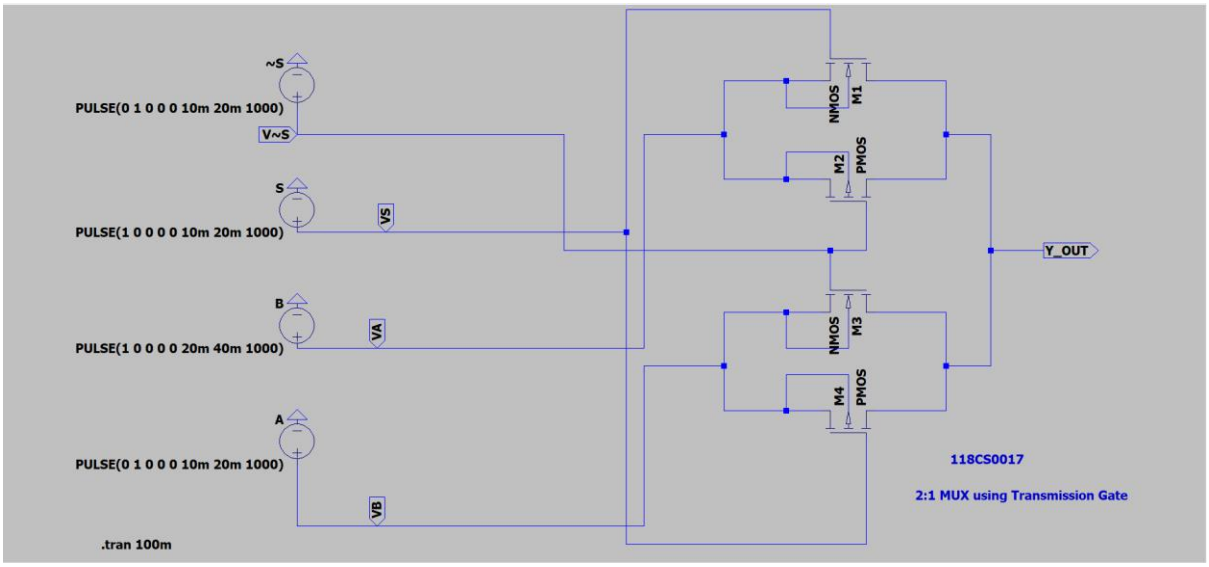
Observation graph-1

Lab report: 4:1 MUX circuit and it's design

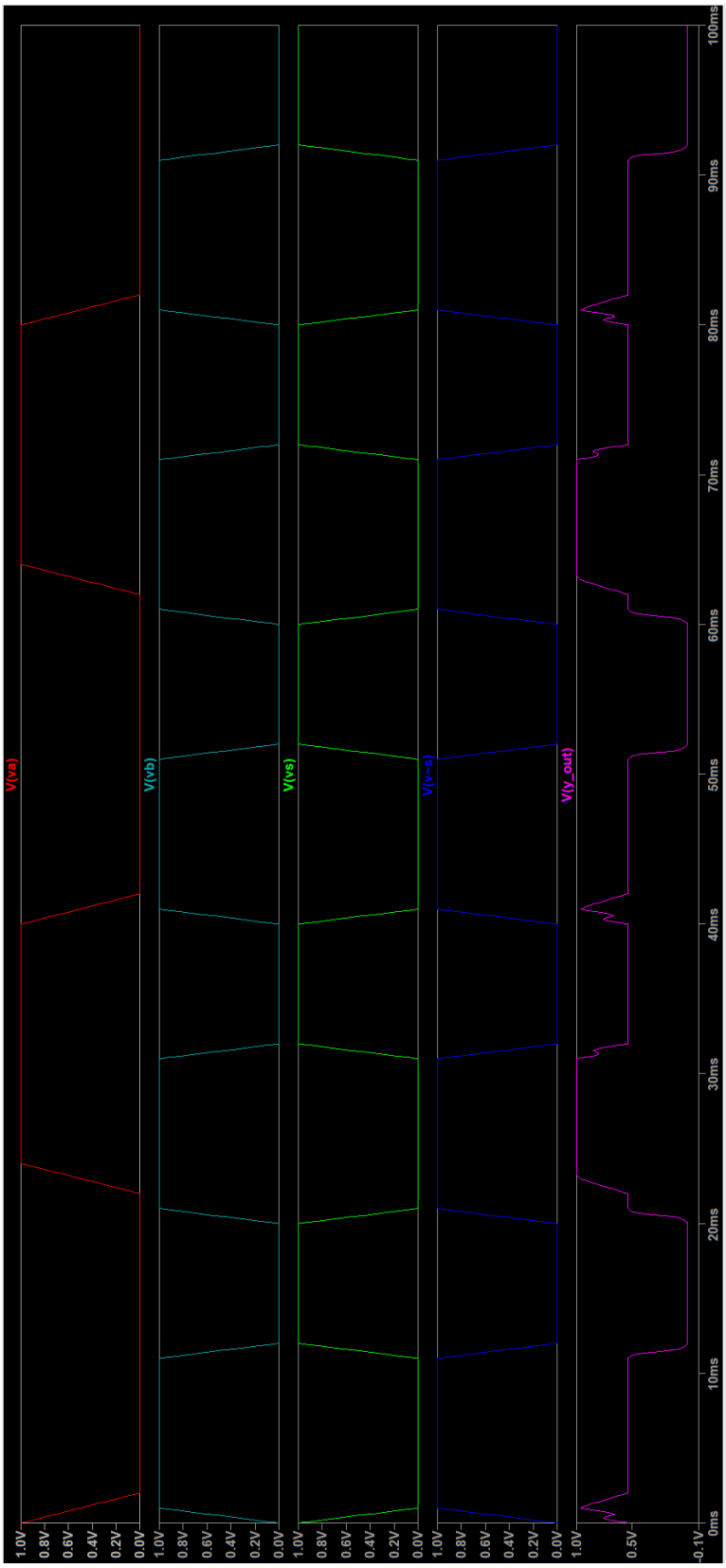
Name: R. Hemanth Krishna Vineel
Roll no: 118cs0017
Course: VLSI Lab practice

VLSI-5

a. 2:1 Mux using Transmission Gate.

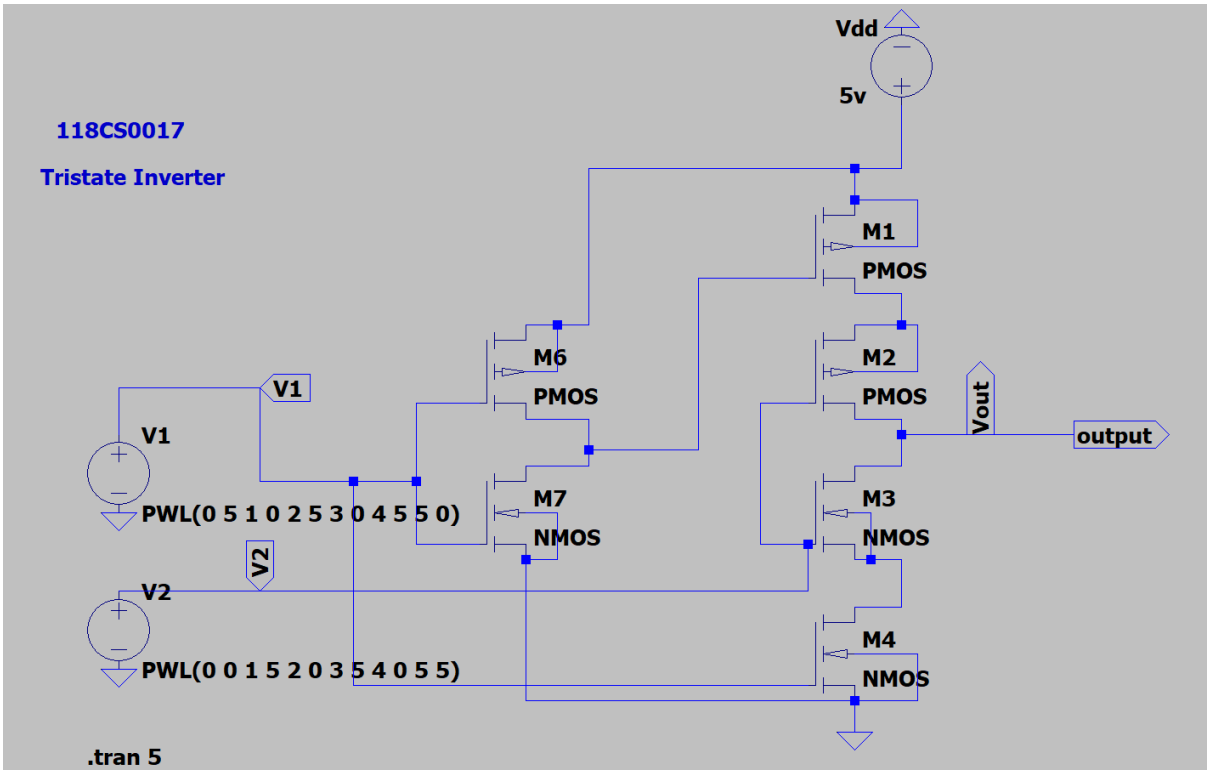


Circuit diagram of 2:1 mux using Transmission Gate

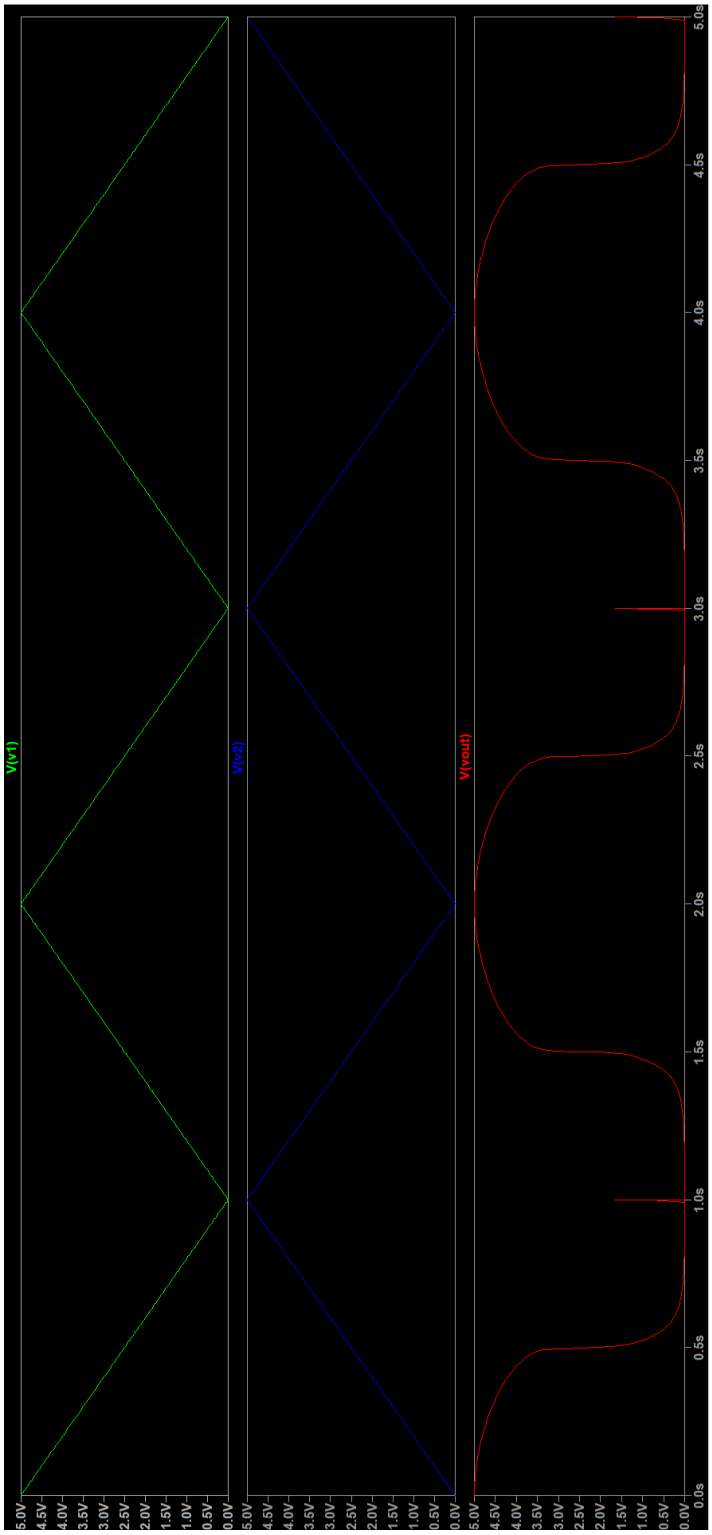


Observation Graph-1

b. Tristate Inverter



Circuit diagram of Tristate inverter



Observation Graph-2

Lab Report 5: - 2:1 mux using transmission gate and tristate inverter

Name: - R. Hemanth Krishna Vineel

Roll no: - 118CS0017

Course: - VLSI Practice