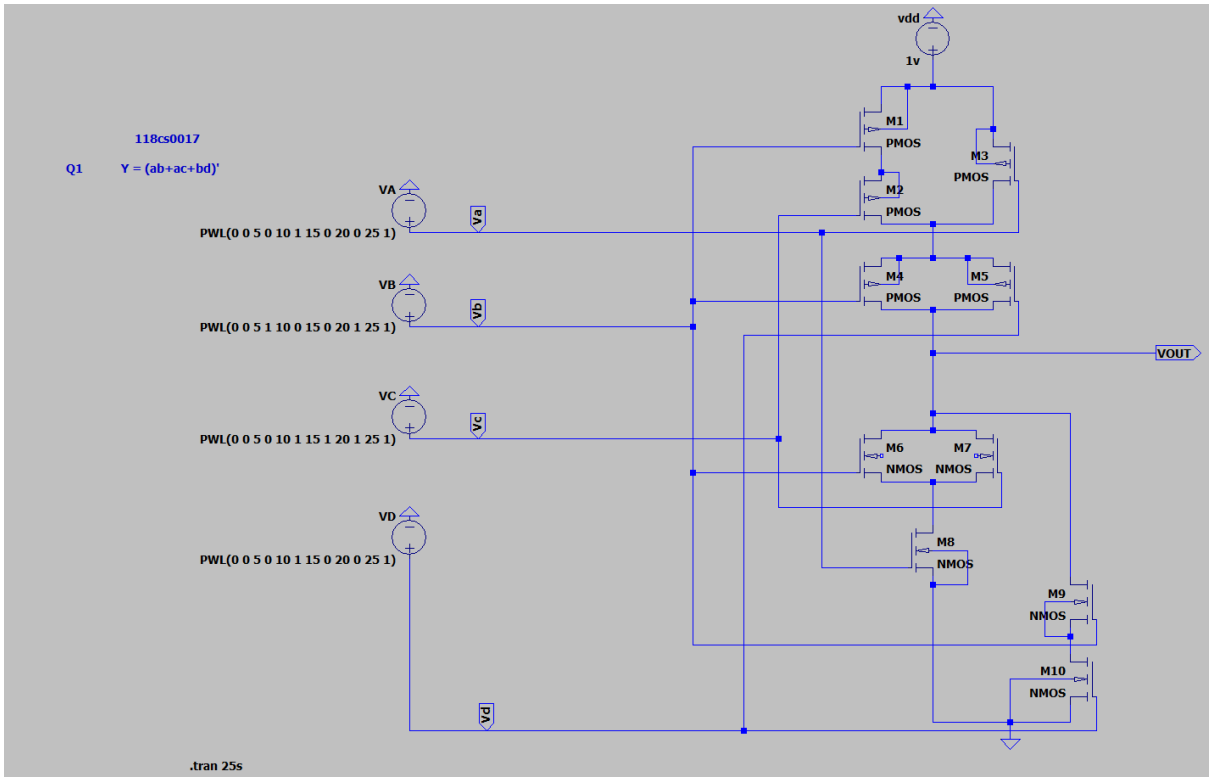
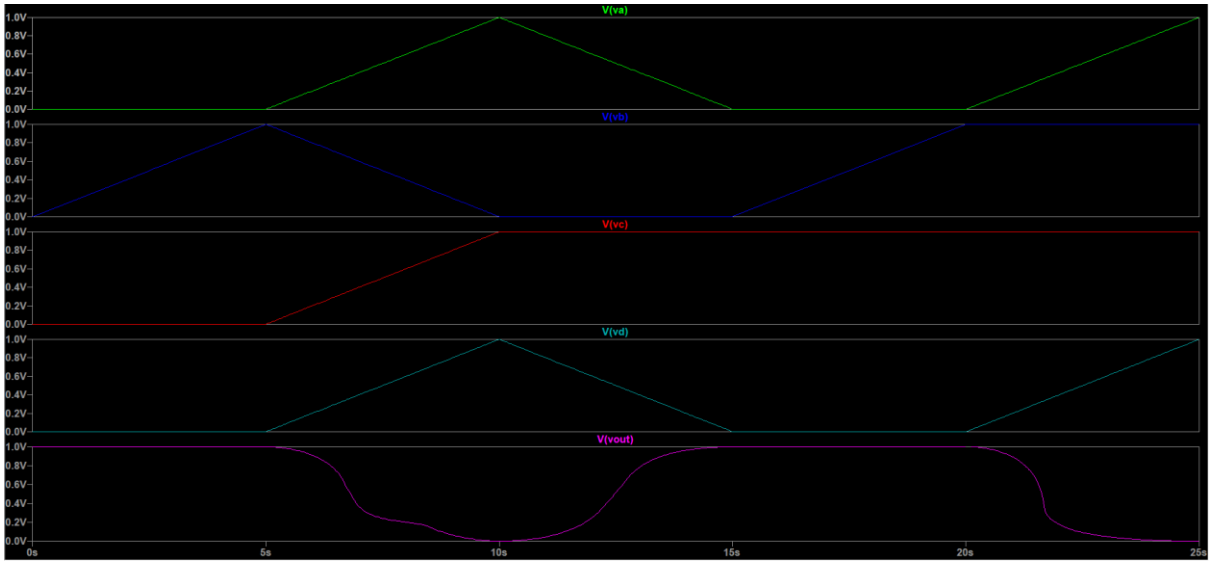
VLSI – 6

Reduce the expressions and design the circuit using MOS transistors.

Q1. **Y=** $\overline{a.b + a.c + b.d}$



Circuit diagram of Q1



Observation graph – 1

Q1. $Y = (ab + ac + bd)'$

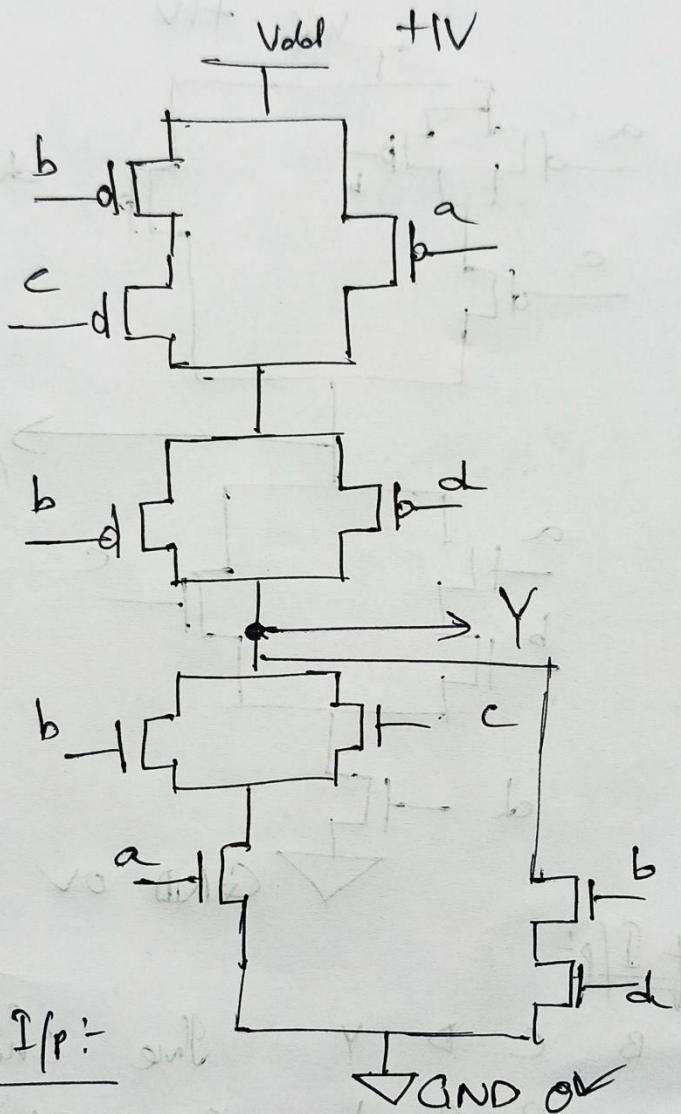
$Y' = a(b+c) + bd$

118CS0017

R.H.K Vineel

VLSI

Lab-6

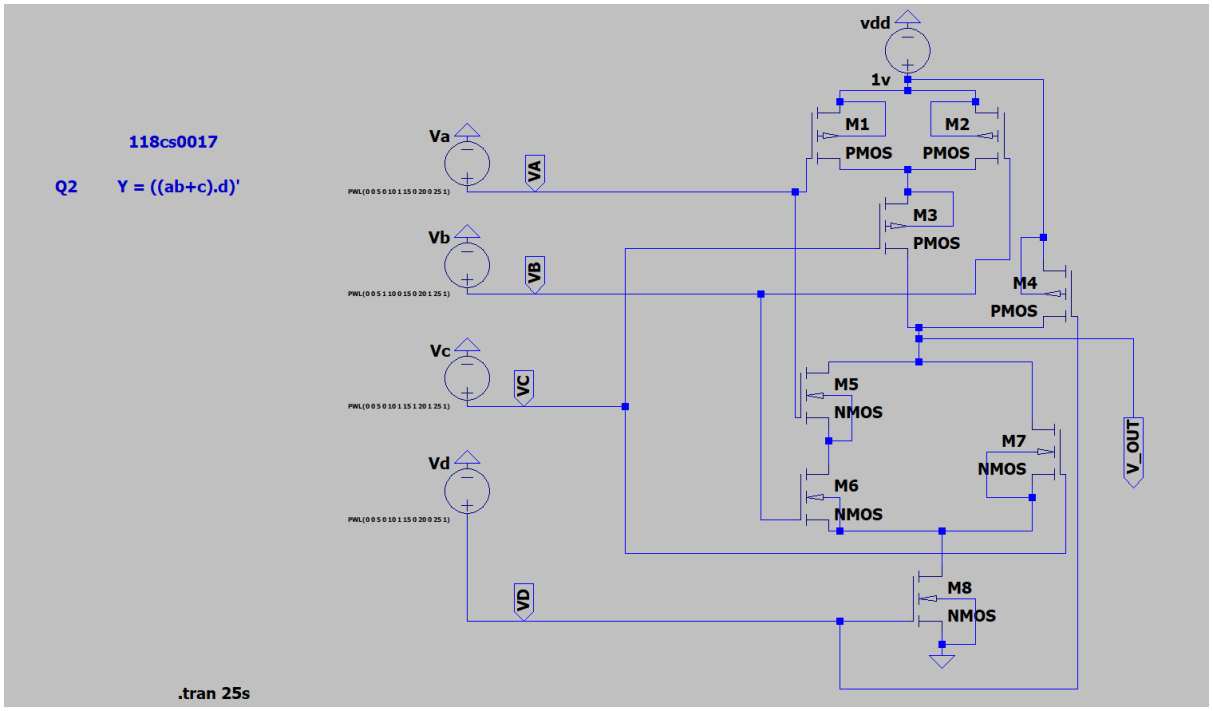


My Set of I/p :-

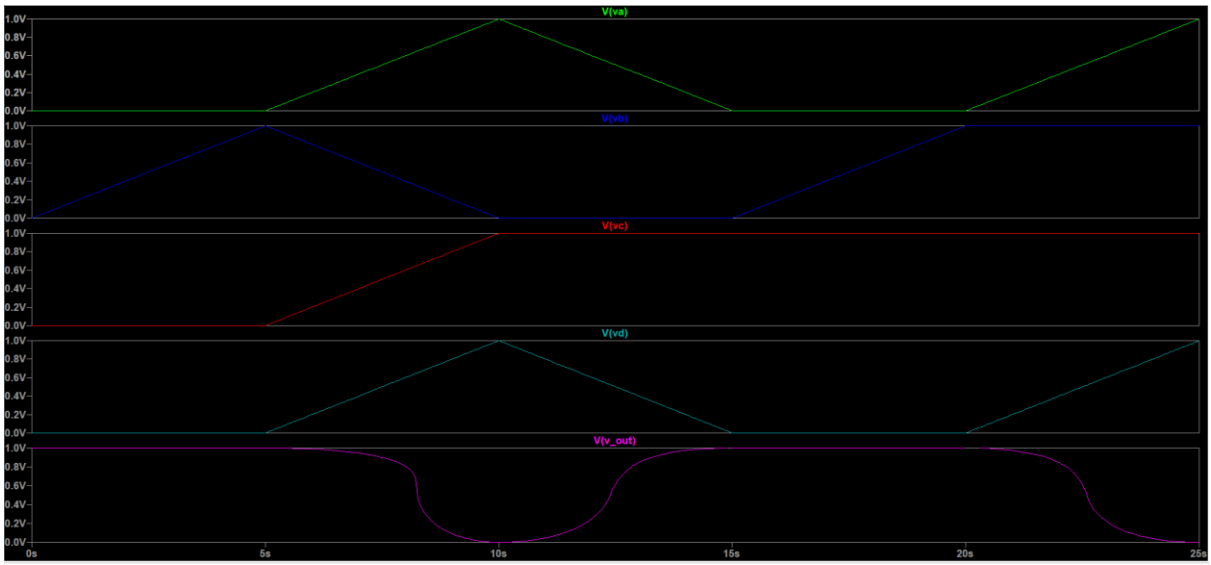
A	B	C	D	Y
0	0	0	0	1
0	1	0	0	1
1	0	1	1	0
0	0	1	0	1
0	1	1	0	1
1	1	1	1	0

I've chosen 5 Sets of I/p & the O/p is right. (for ref use Graph)

Q2. $Y = \overline{(ab + c).d}$



Circuit diagram of Q2



Observation graph -2

Q2. $Y = ((a \cdot b + c) \cdot d)'$

$Y' = (ab+c) \cdot (d)$

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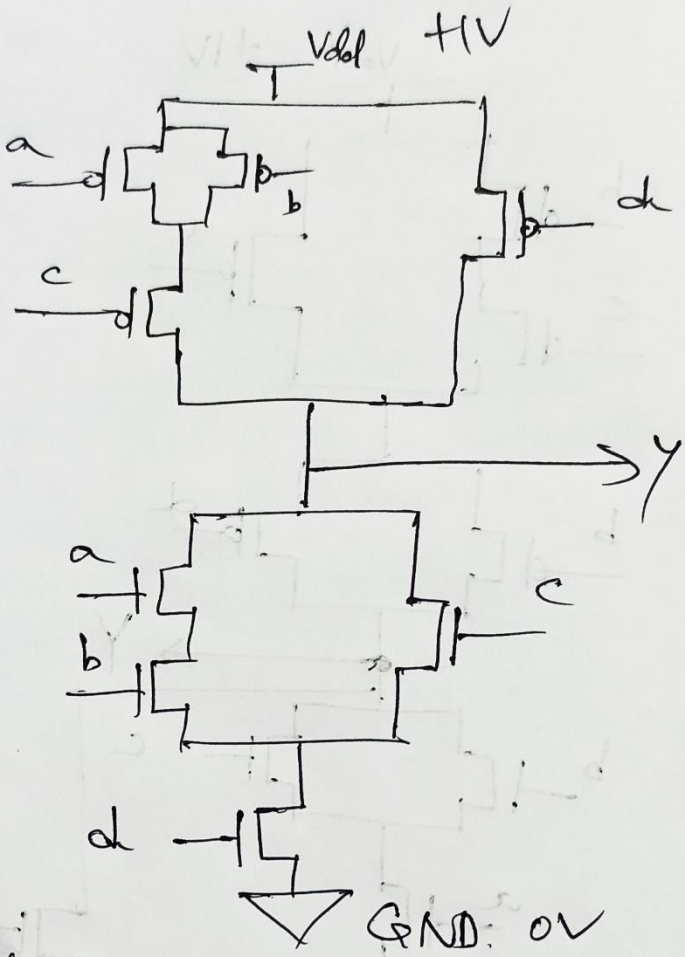


My Set of I/P:-

A	B	C	D	Y
0	0	0	0	1
0	1	0	0	1
1	0	1	1	0
0	0	1	0	1
0	1	1	0	1
1	1	1	1	0

I've choosen 5 sets of I/P & the O/P right.
(for ref use graph).

Lab Report 6: - Reduce the expressions and design the circuit using MOS transistors.

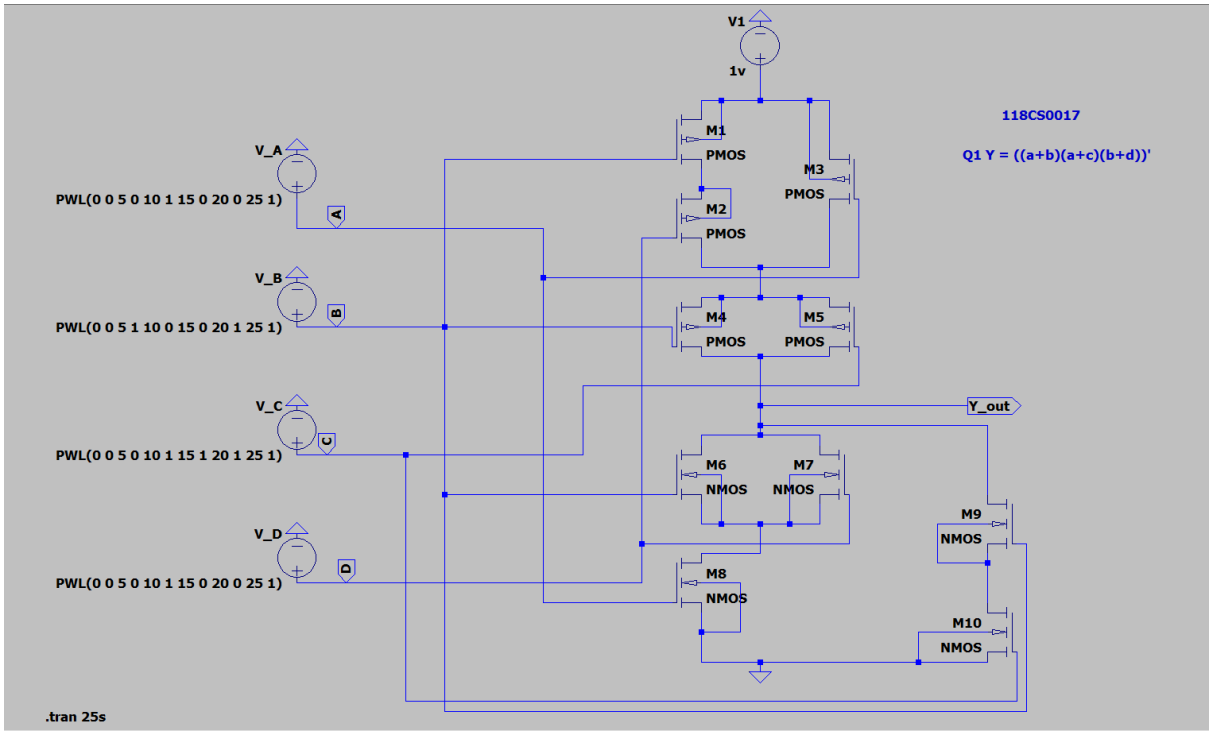
Name: - R. Hemanth Krishna Vineel

Roll no: - 118CS0017

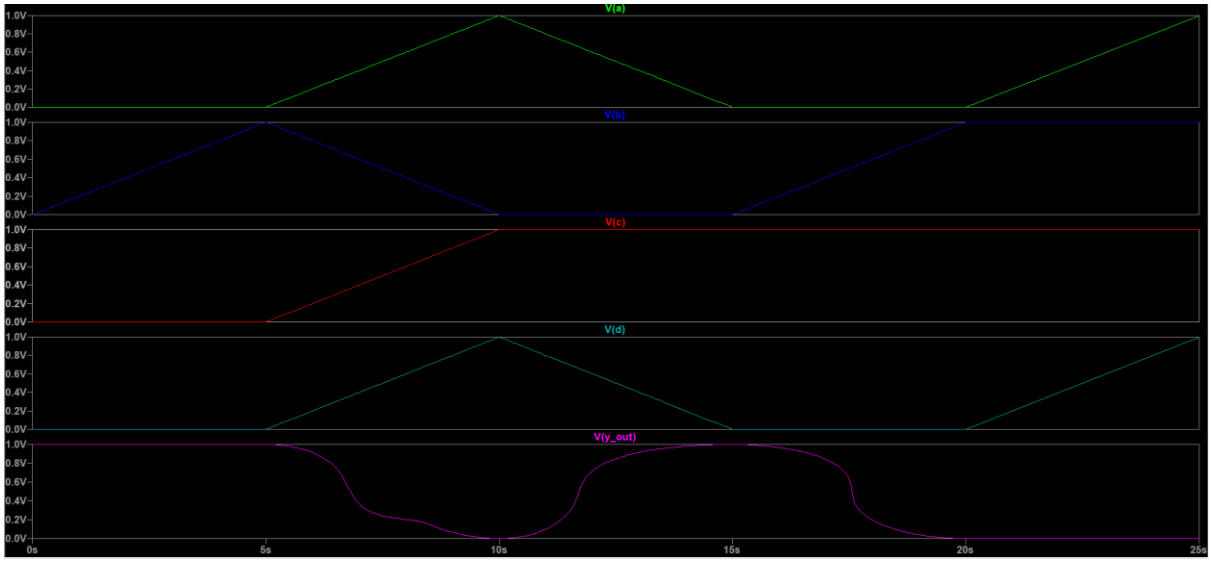
Course: - VLSI Practice

VLSI – 7

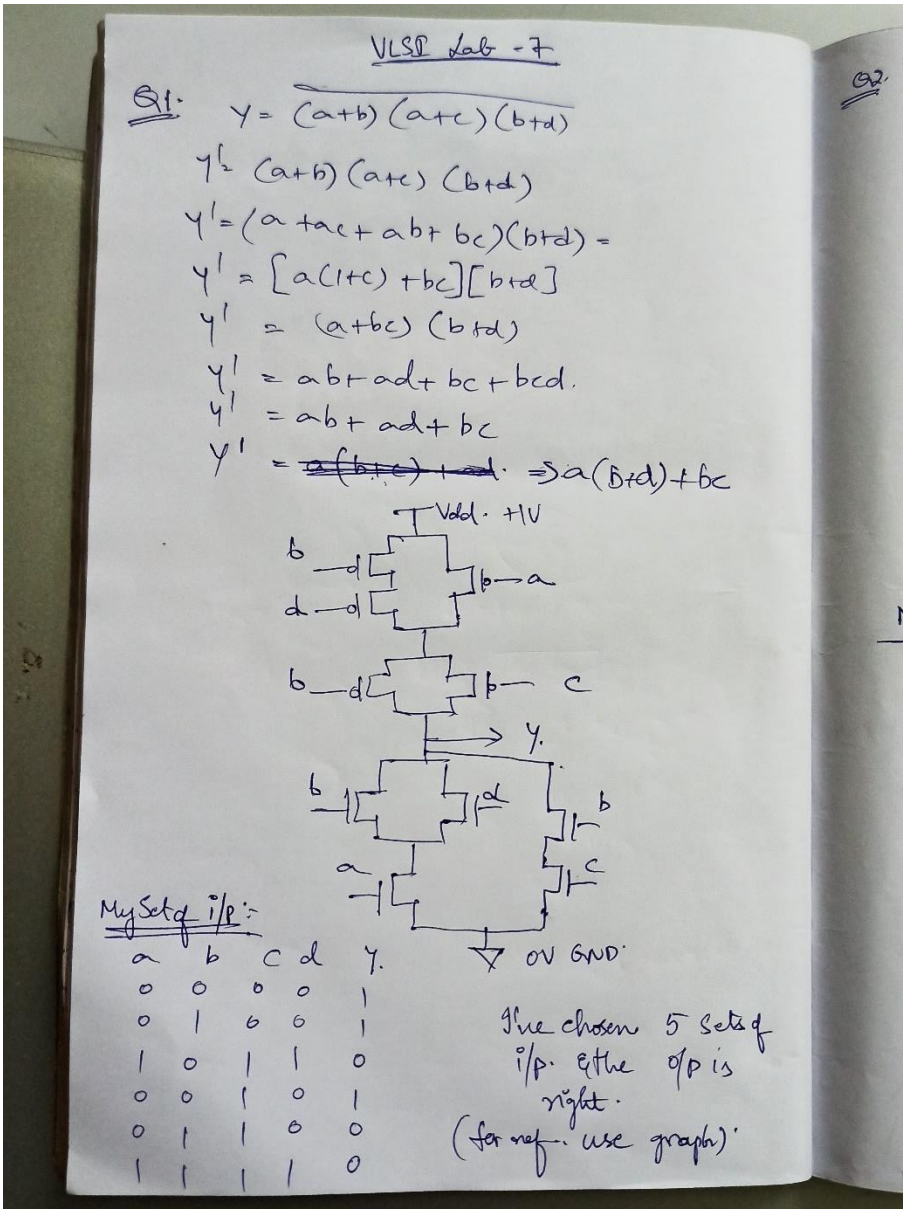
Q1. Y = ((a+b)(a+c)(b+d))’



Circuit of Q1. Using CMOS

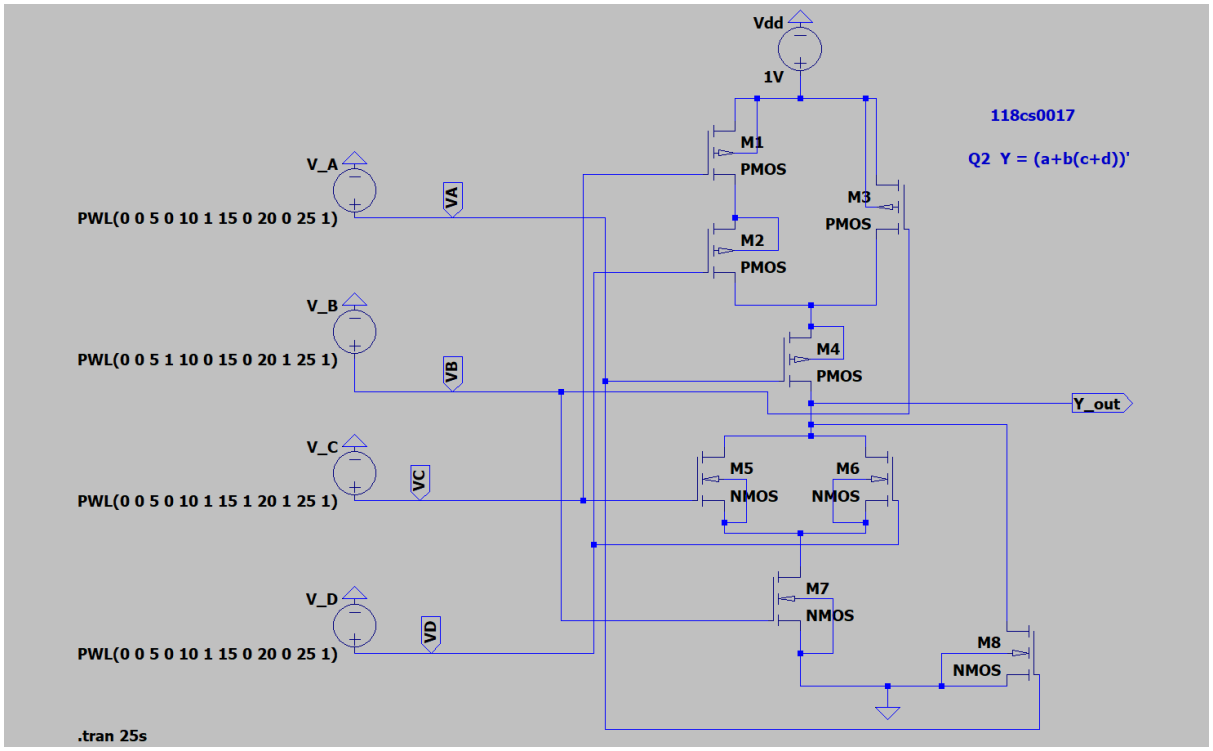


Observation Graph-1

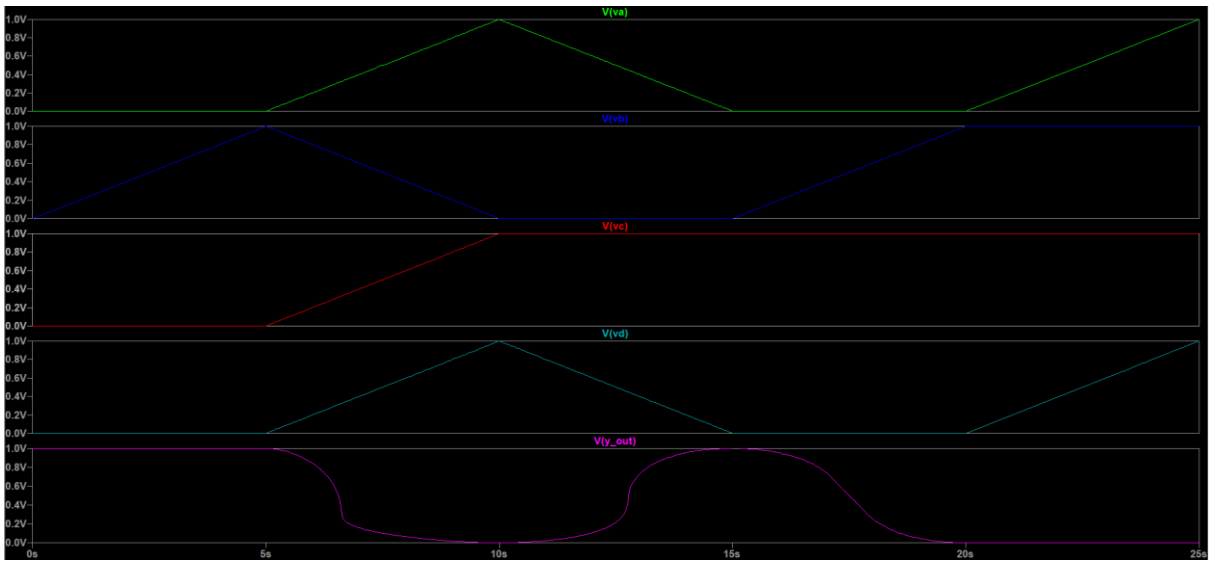


Simplification

Q2. Y = (a+b(c+d))’



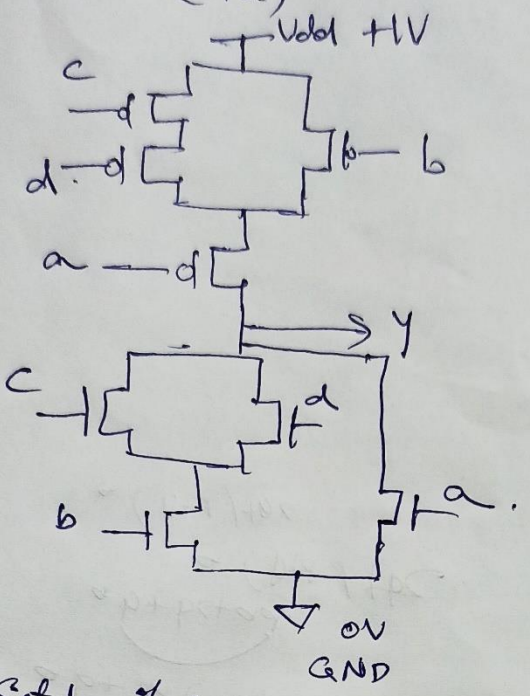
Circuit design of Q2 using CMOS



Observation Graph – 2

Q2. $Y = \overline{a + b(c+d)}$

$Y' = a + b(c+d)$



My Set of i/p's:

a	b	c	d	Y
0	0	0	0	1
0	1	0	0	1
1	0	(	1	0
0	0	1	0	1
0	1	1	0	0
1	1	1	1	0

The chosen 5 Sets of i/p's & the o/p is right (for ref. use graph)

Explanation

Lab Report 7: - Reduce the following Boolean expressions

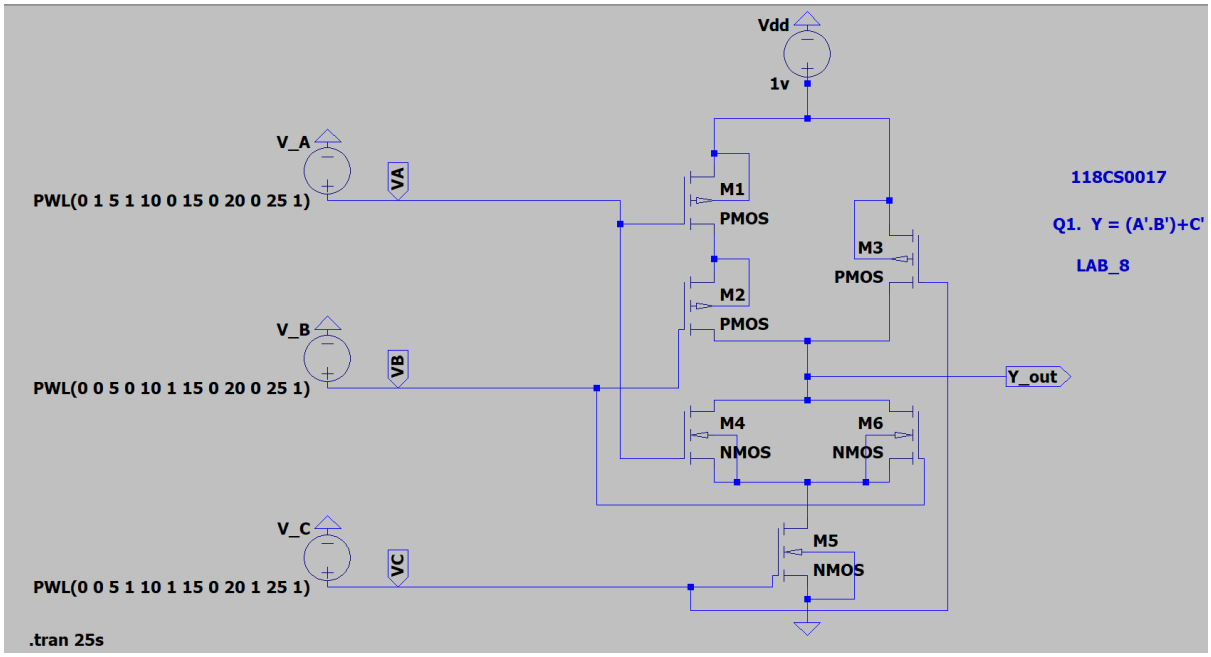
Name: - R. Hemanth Krishna Vineel

Roll no: - 118CS0017

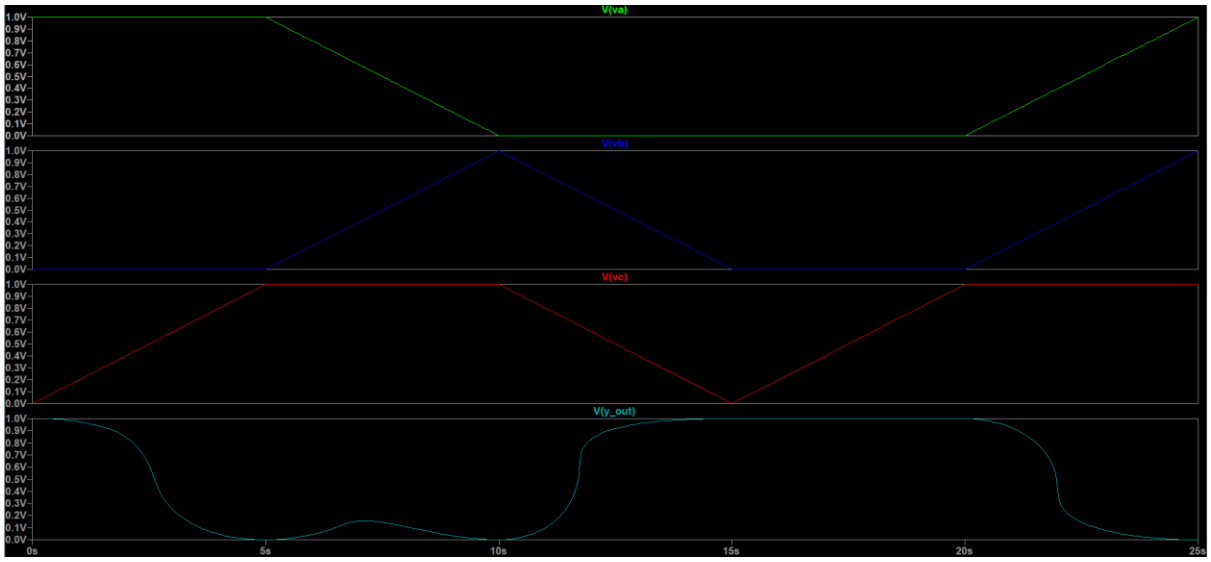
Course : - VLSI Practice

VLSI – 8

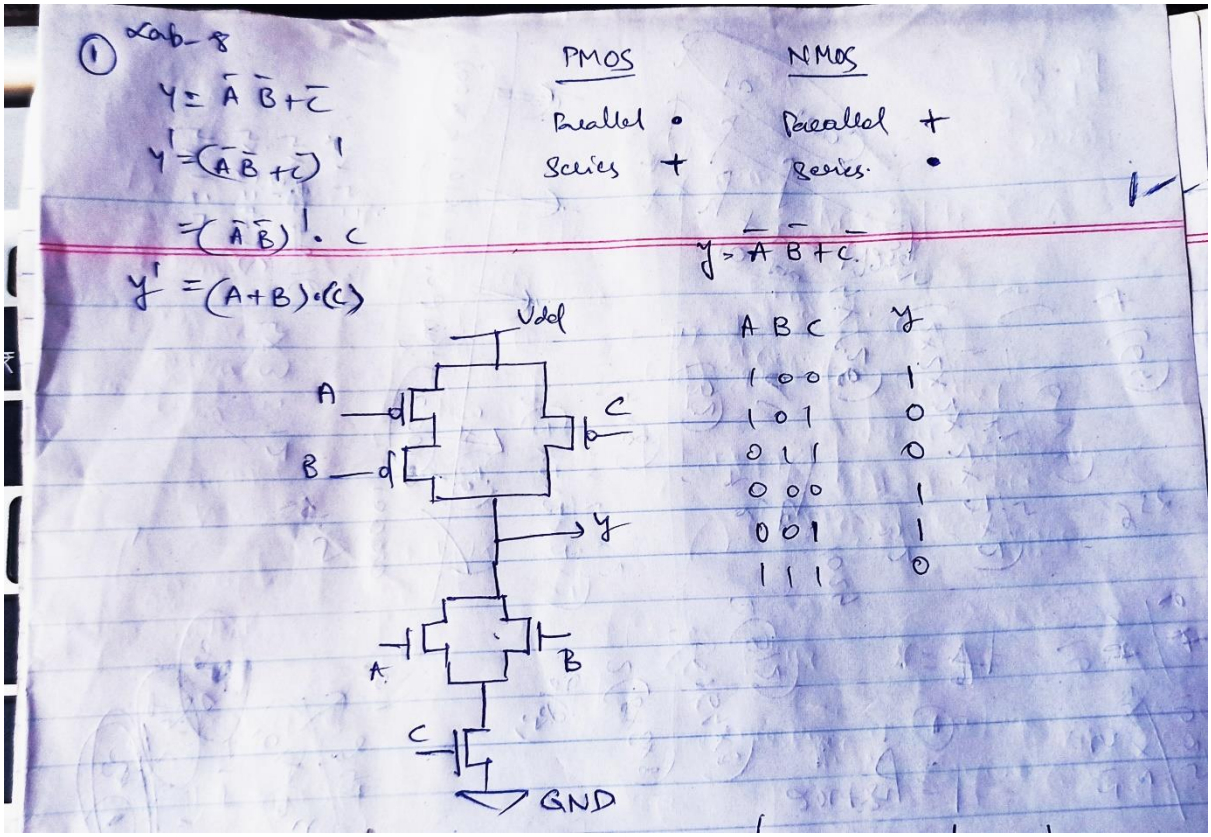
Q1. Y = A'.B' + C'



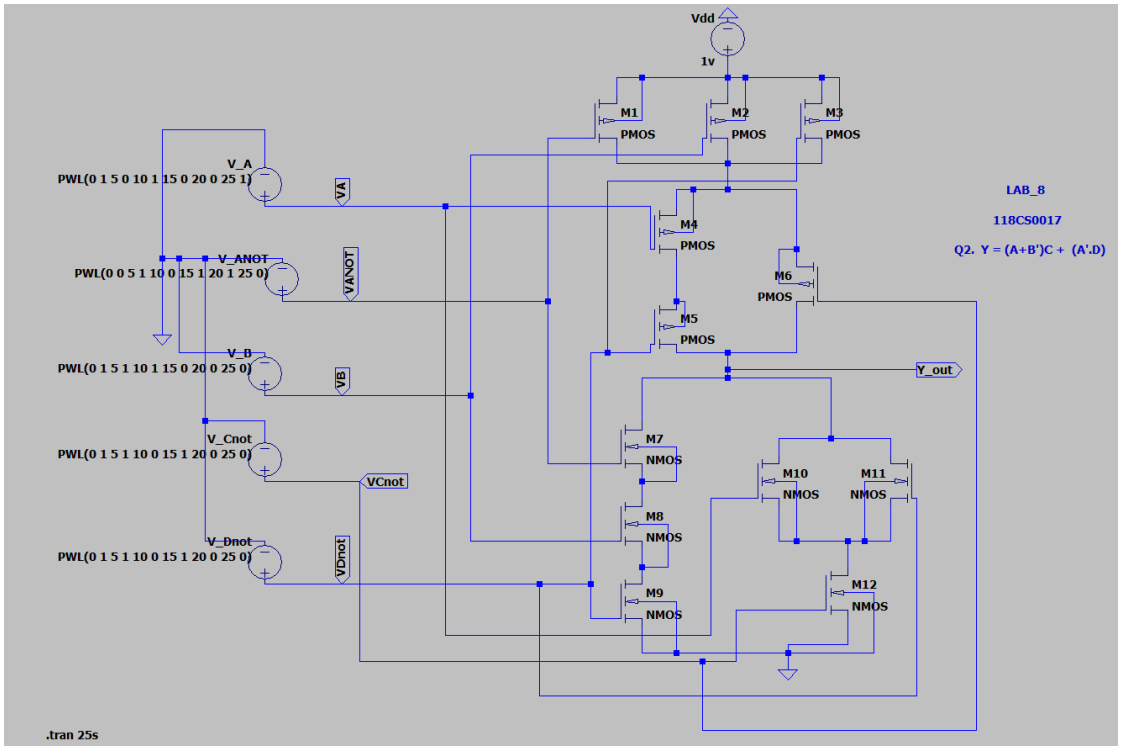
Circuit Diagram



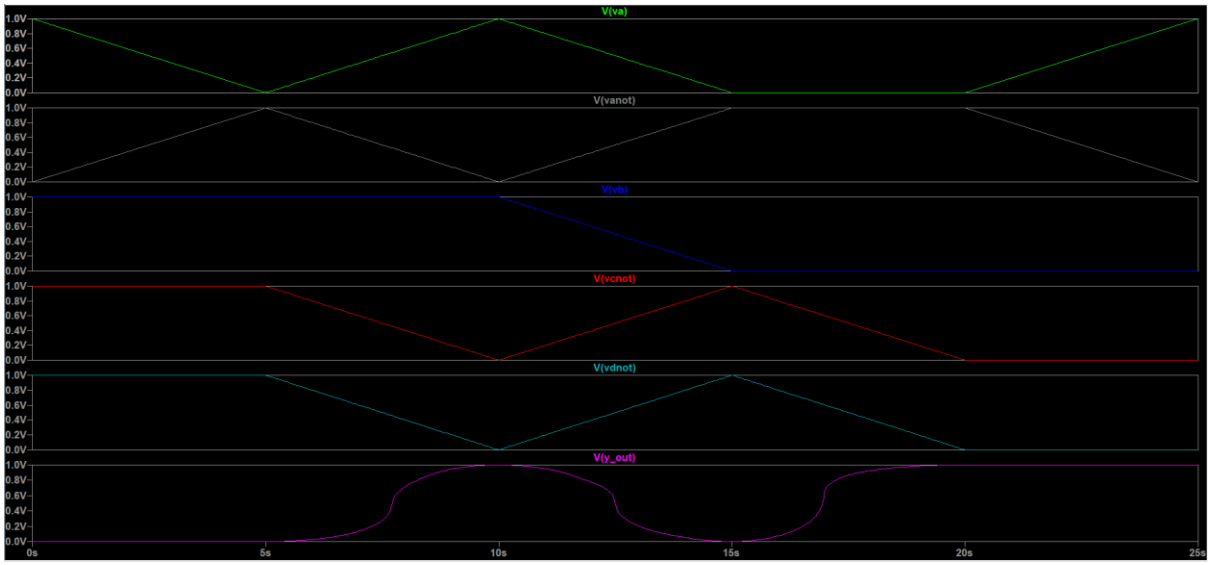
Observation Graph



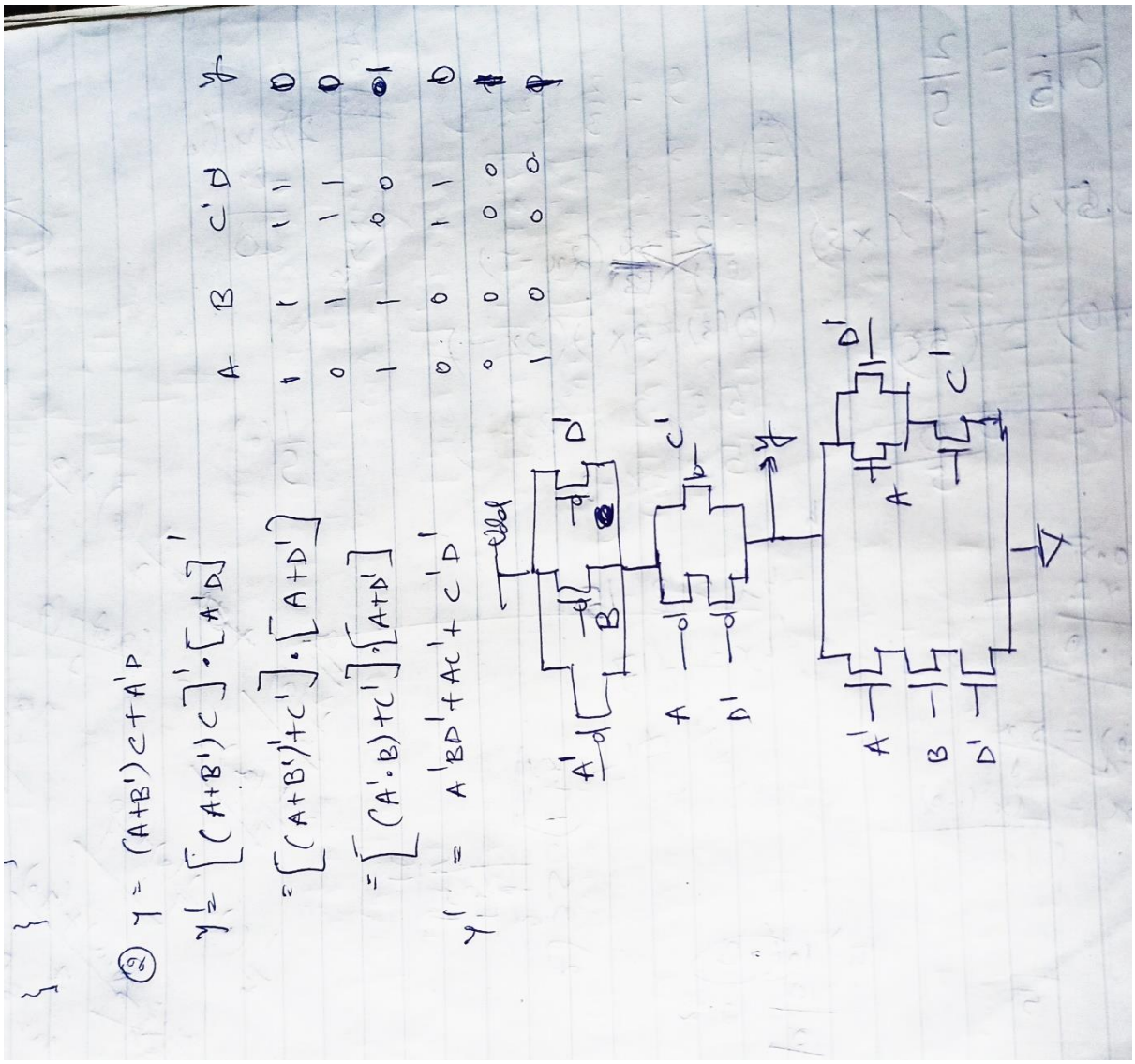
Q2. Y = (A + B').C + A'.D



Circuit Diagram



Observation graph



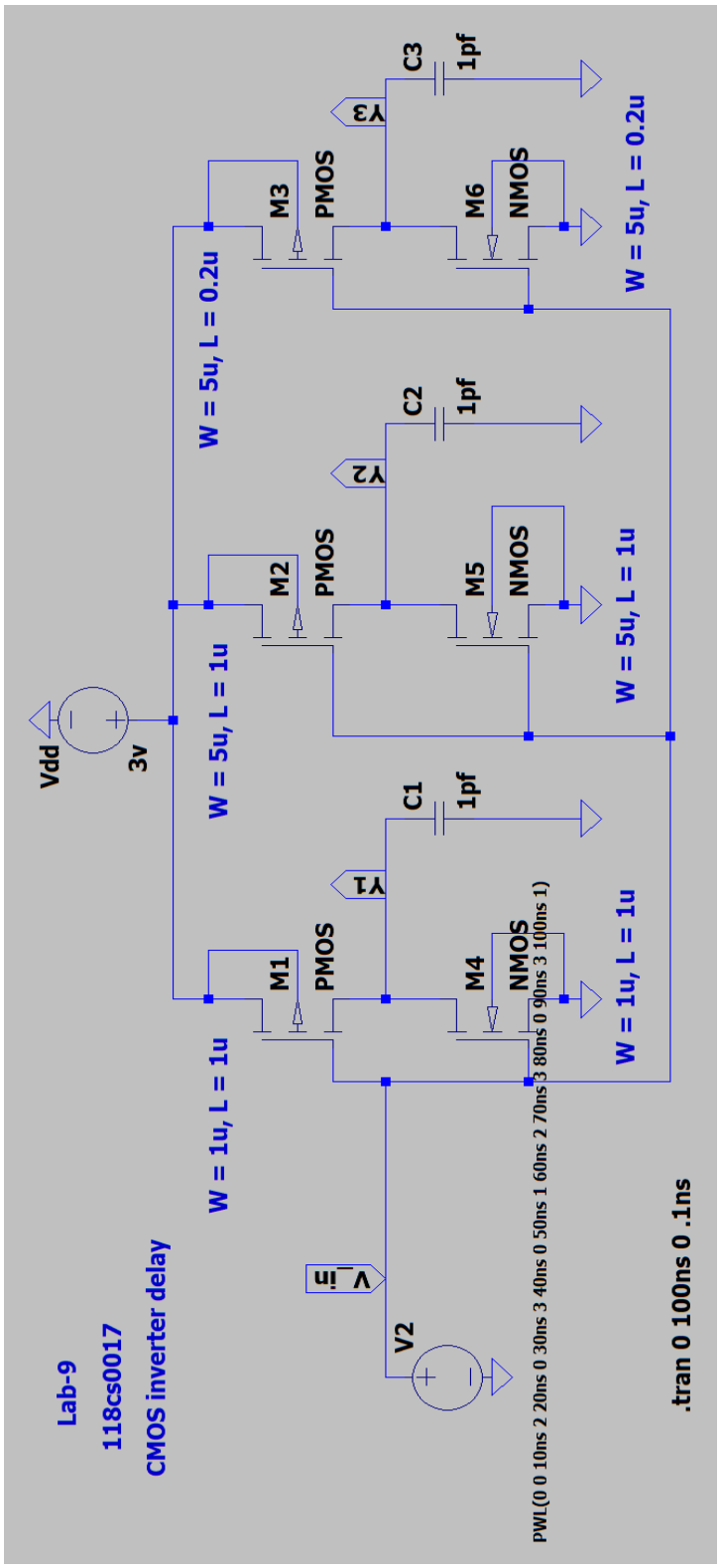
Lab Report 8: - Reduce the following Boolean expressions

Name: R. H. Krishna Vineel

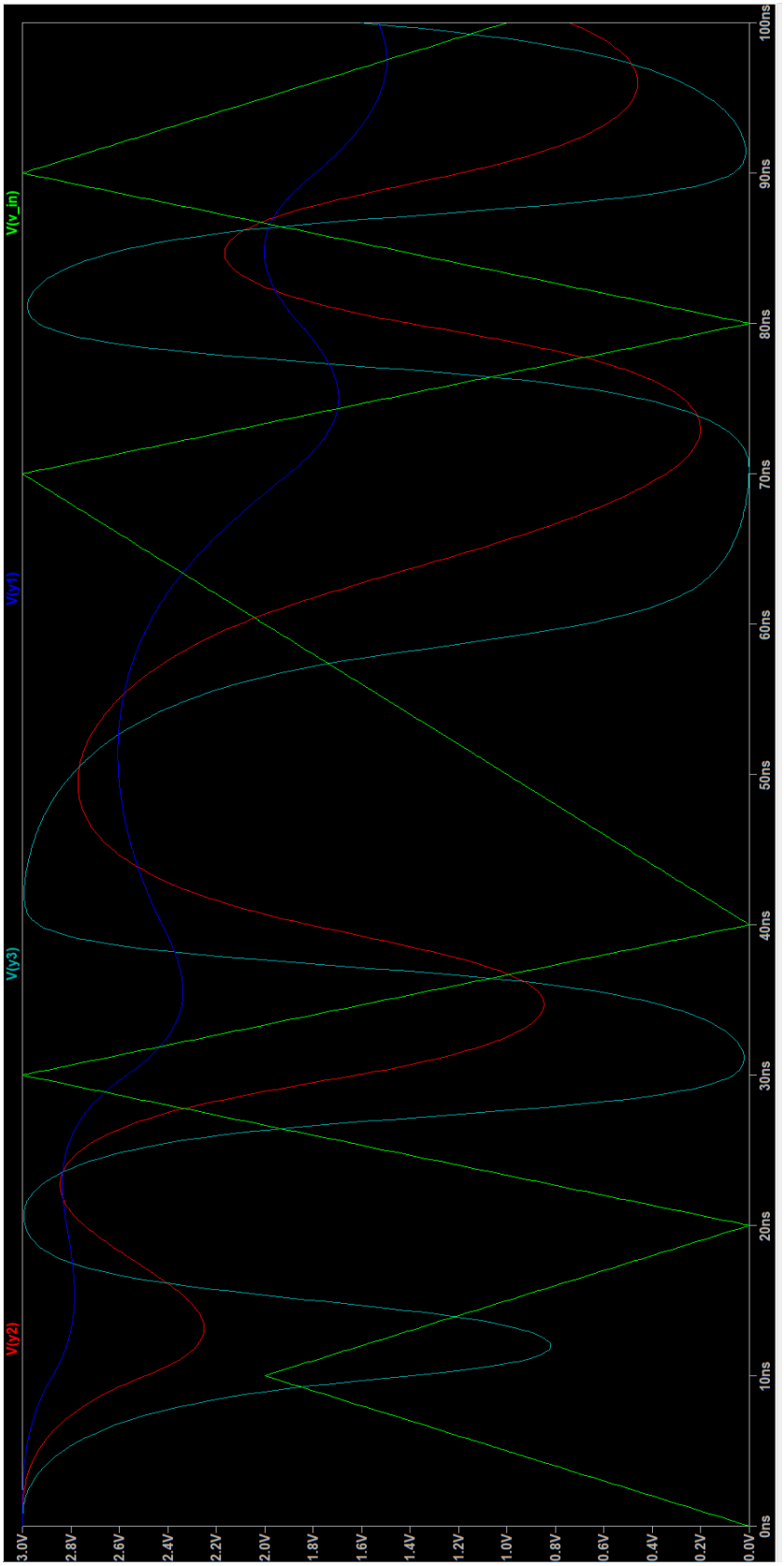
Roll: 118CS0017

VLSI – 9

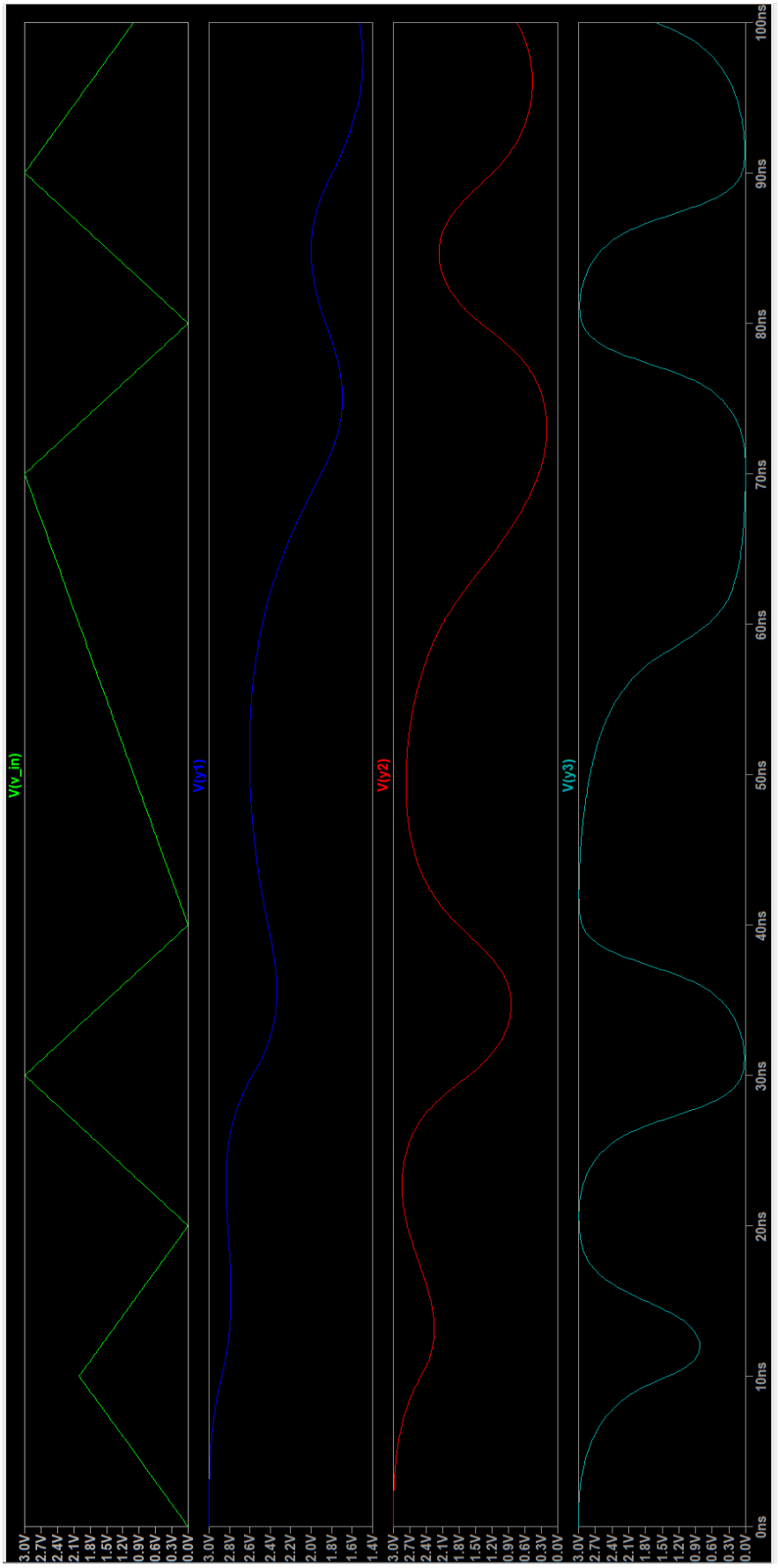
Q1.



Circuit Diagram



Observation Graph-1



Observation Graph-2

Lab Report 9: - CMOS Inverter Delay

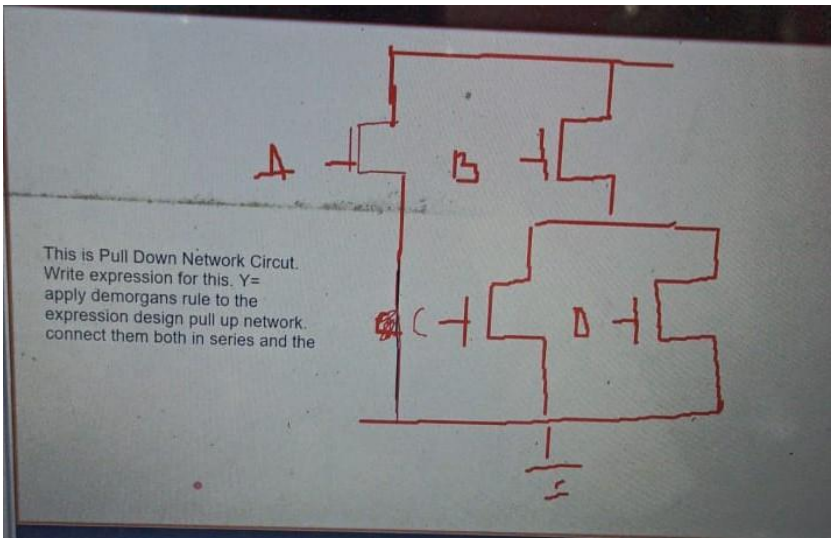
Name: - R. Hemanth Krishna Vineel

Roll no: - 118CS0017

Course: - VLSI Practice

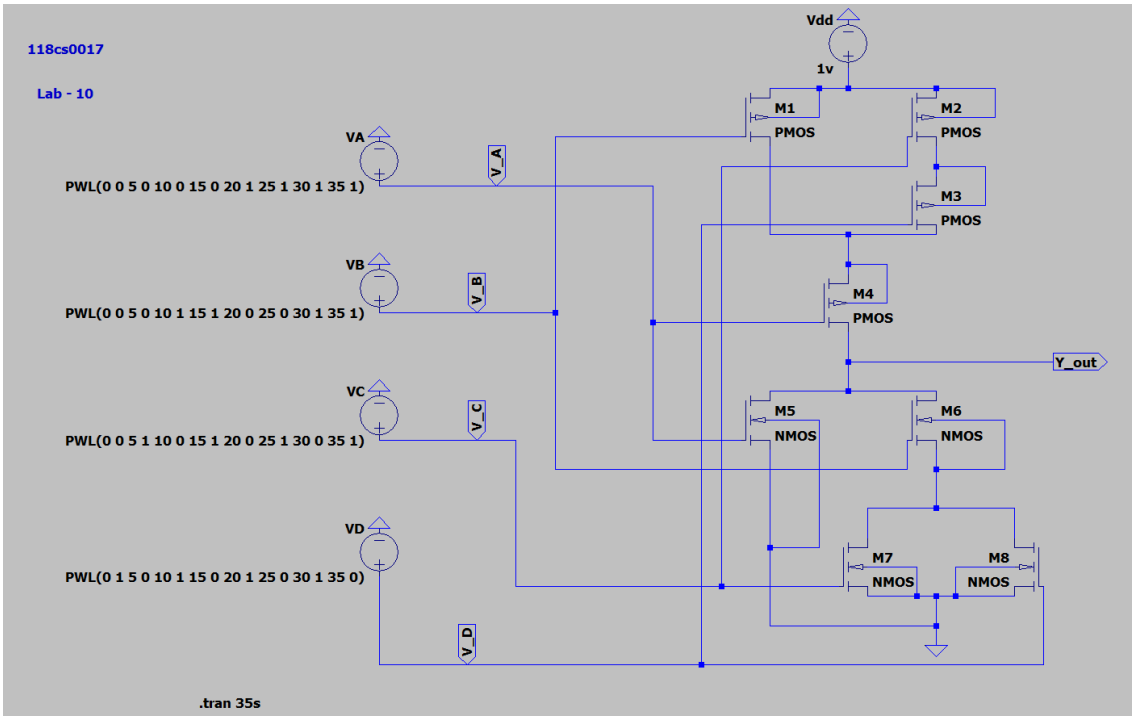
VLSI -10

Q1. Given a PDN, draw a the PUN using the De Morgan Law and write the expression Y.

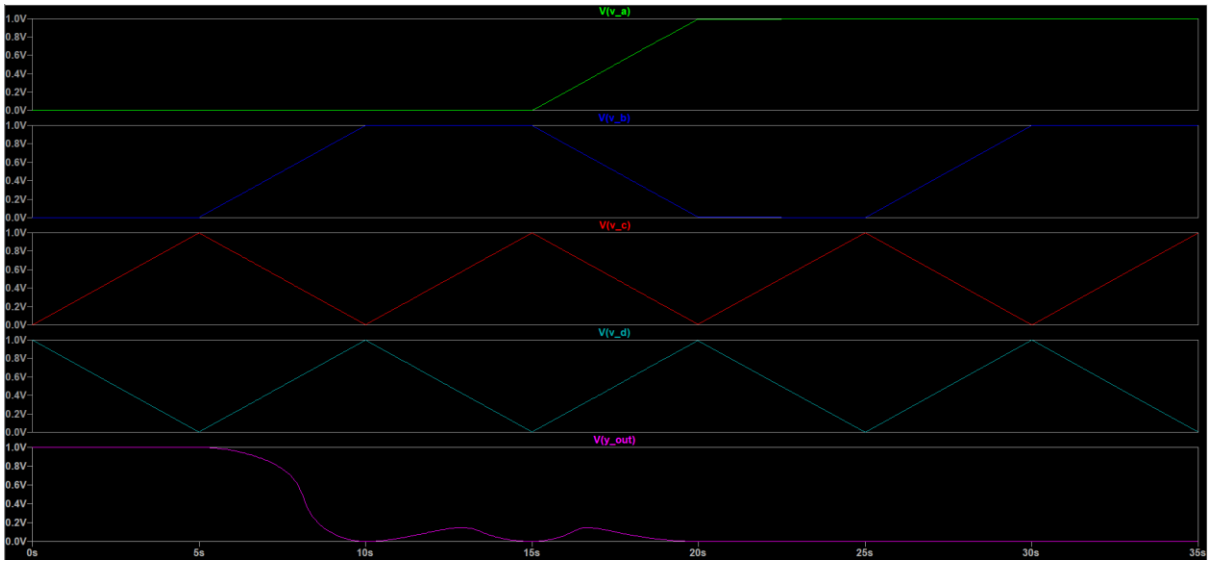


Given is Y' = (A+B(C+D))

(Y')' = Y = A'.[B'+C'.D']

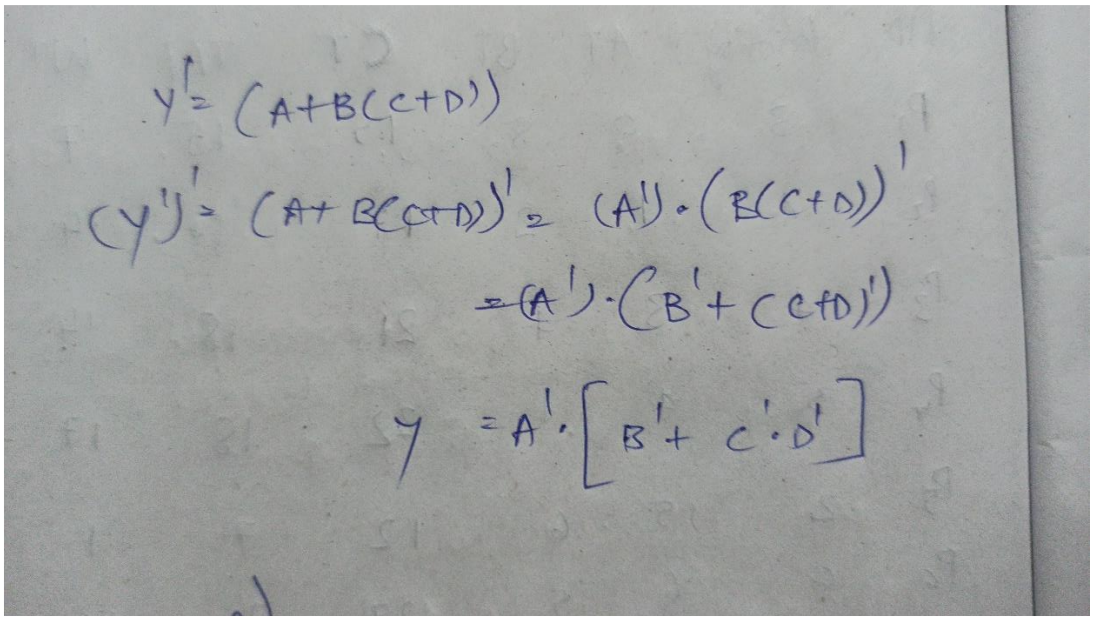


Circuit diagram

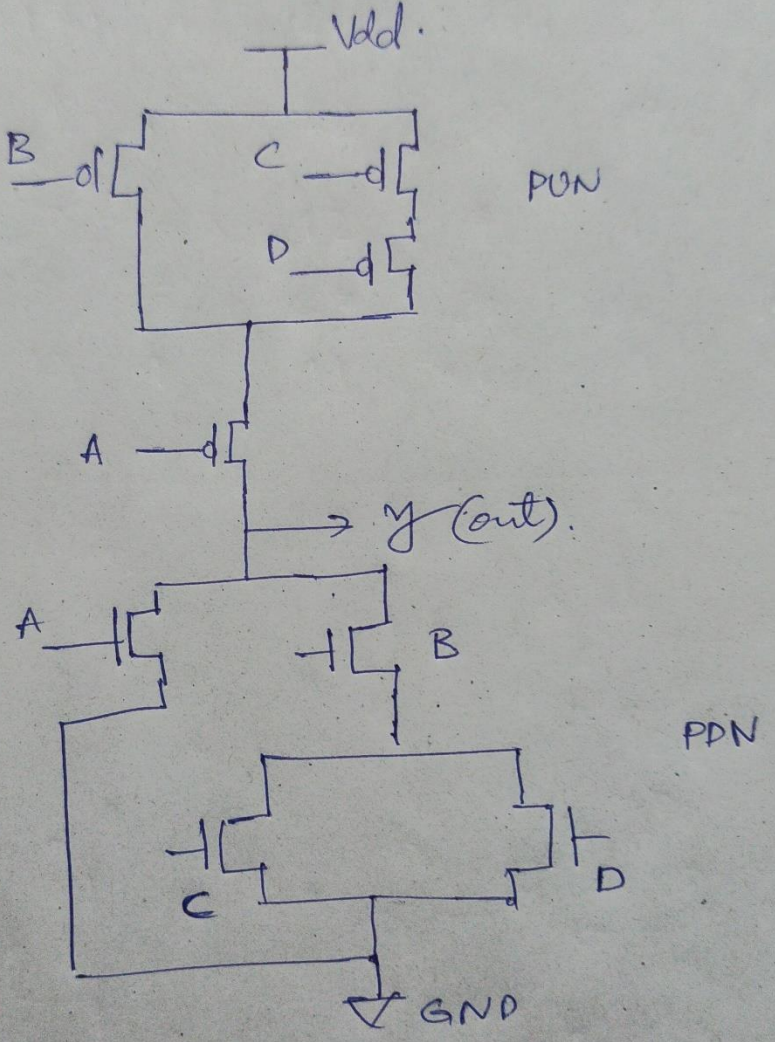


Observation Graph

Manual work:



Lab - 10



Lab Report 10: - Identify the Boolean Expression

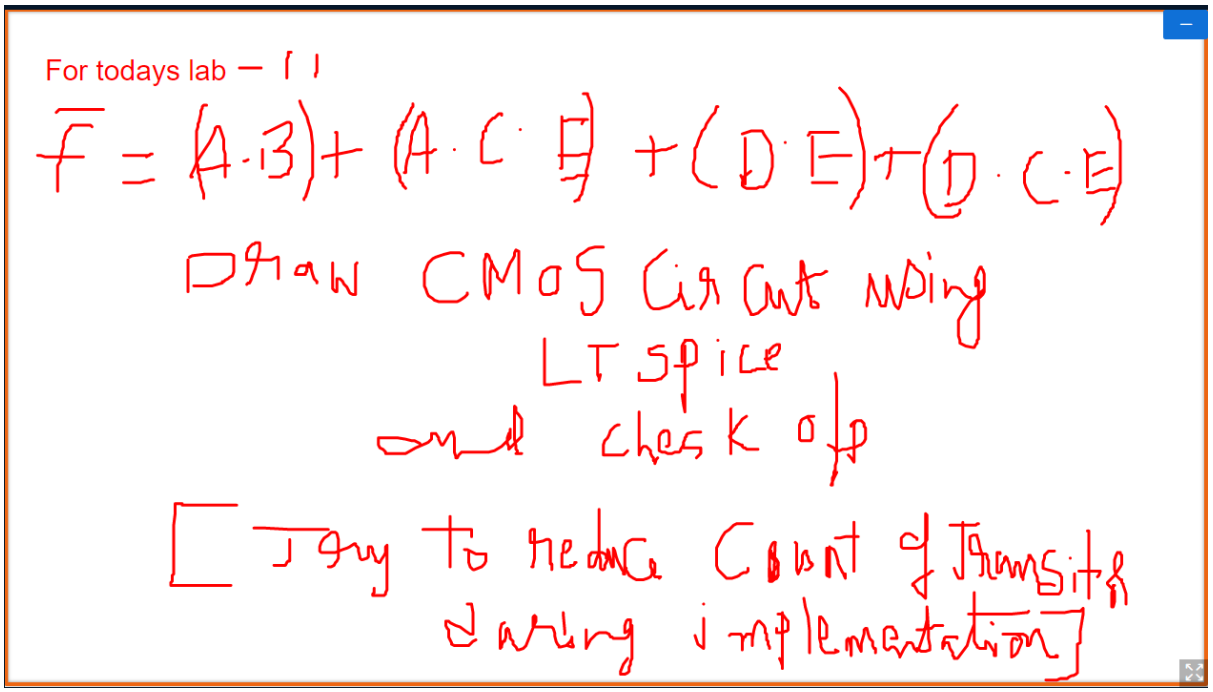
Name: - R. Hemanth Krishna Vineel

Roll no: - 118CS0017

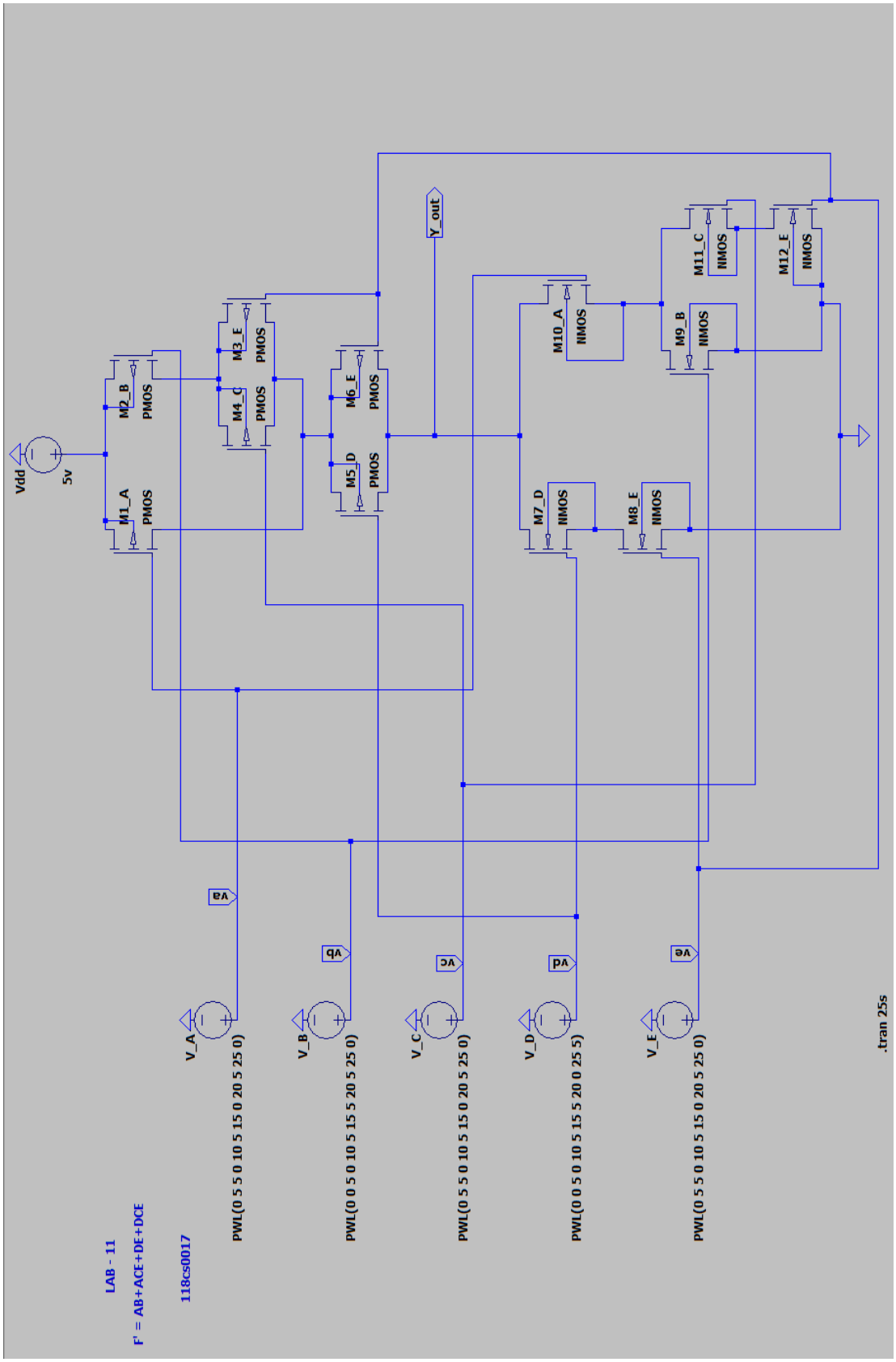
Course : - VLSI Practice

VLSI – 11

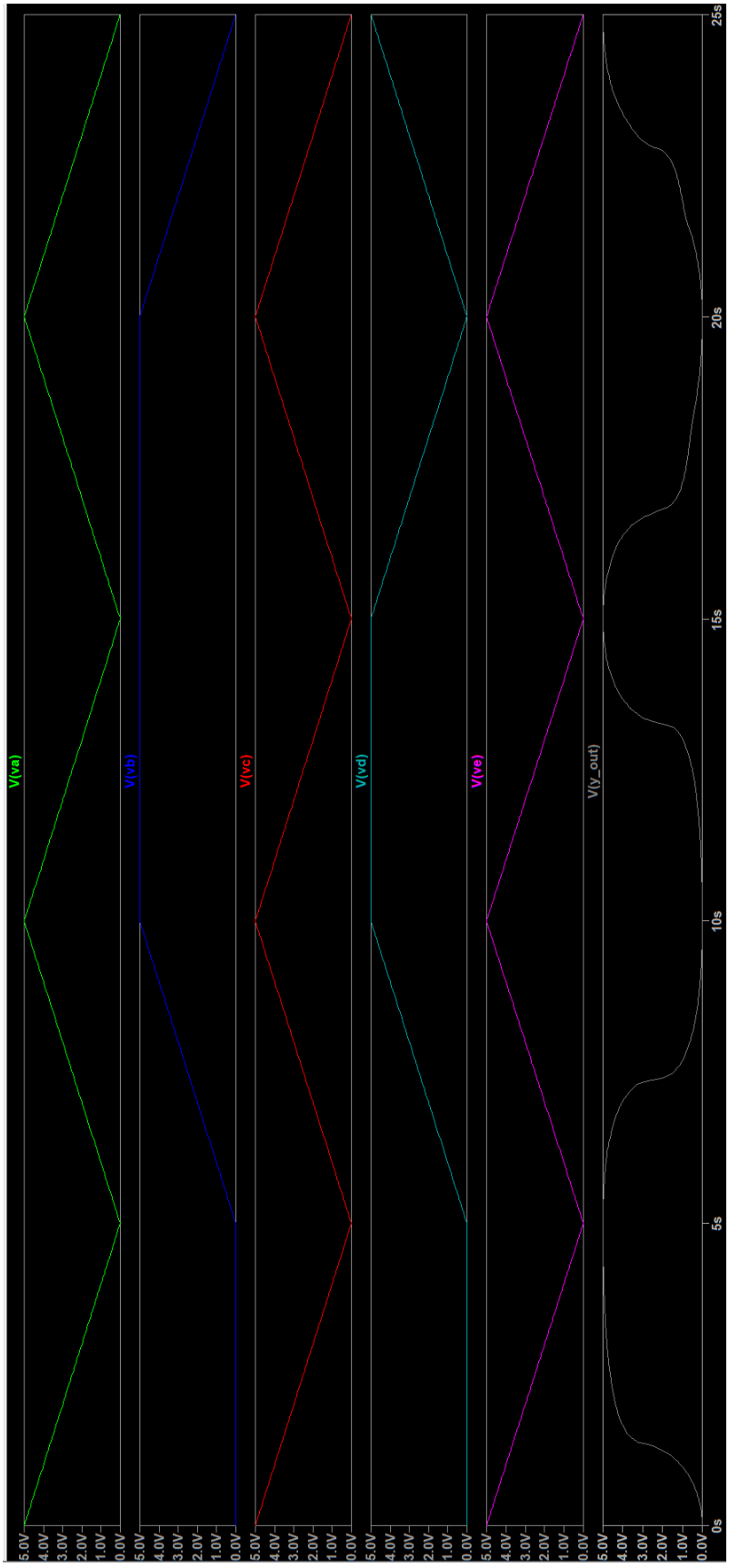
Question:



Answer:

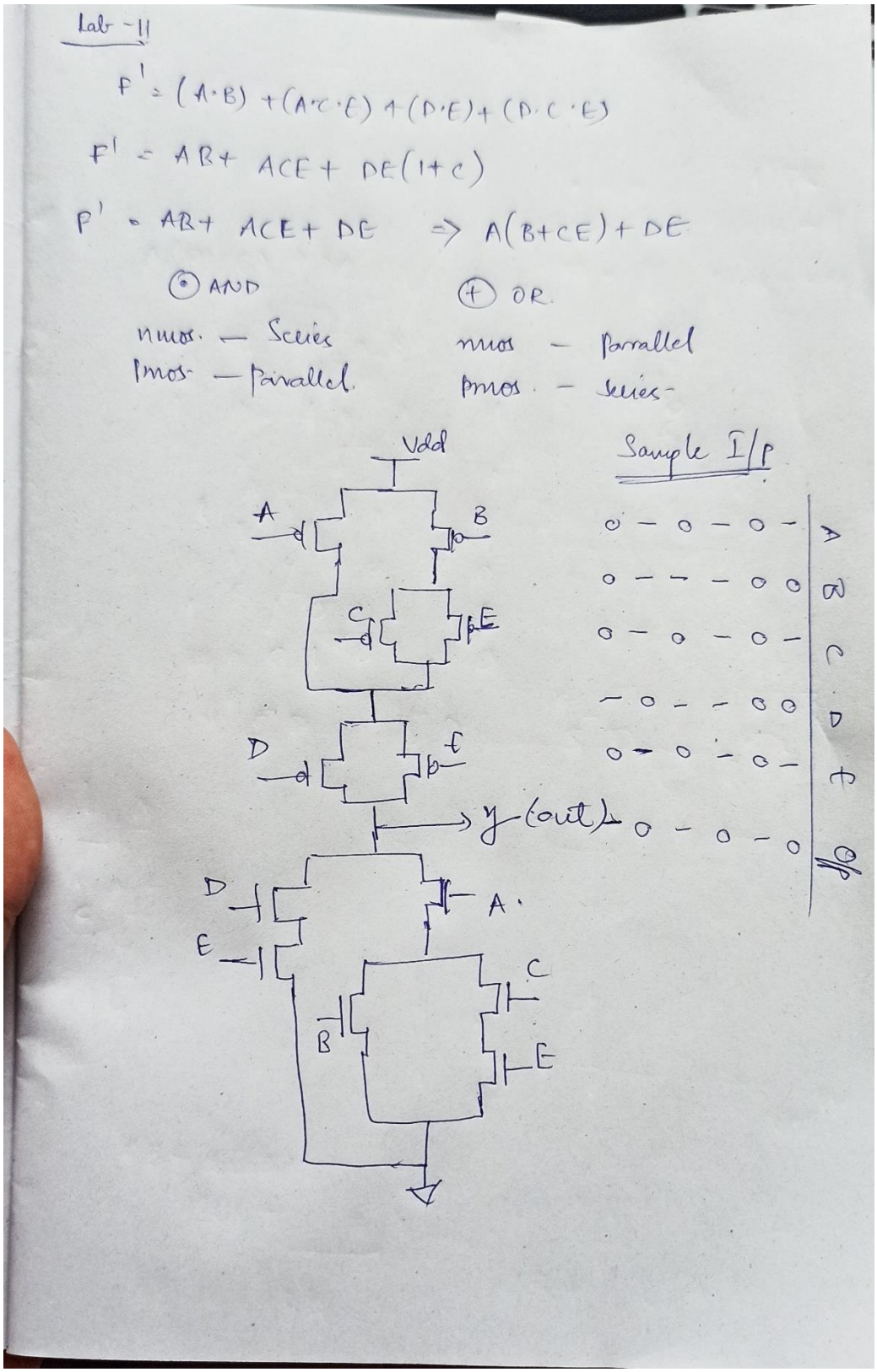


Circuit Diagram



Observation Graph

Manually Written Script:



Truth table: -

A	B	C	D	E	F_output
1	1	1	1	1	FALSE
1	1	1	1	0	FALSE
1	1	1	0	1	FALSE
1	1	1	0	0	FALSE
1	1	0	1	1	FALSE
1	1	0	1	0	FALSE
1	1	0	0	1	FALSE
1	1	0	0	0	FALSE
1	0	1	1	1	FALSE
1	0	1	1	0	TRUE
1	0	1	0	1	FALSE
1	0	1	0	0	TRUE
1	0	0	1	1	FALSE
1	0	0	1	0	TRUE
1	0	0	0	1	TRUE
1	0	0	0	0	TRUE
0	1	1	1	1	FALSE
0	1	1	1	0	TRUE
0	1	1	0	1	TRUE
0	1	1	0	0	TRUE
0	1	0	1	1	FALSE
0	1	0	1	0	TRUE
0	1	0	0	1	TRUE
0	1	0	0	0	TRUE
0	0	1	1	1	FALSE
0	0	1	1	0	TRUE
0	0	1	0	1	TRUE
0	0	1	0	0	TRUE
0	0	0	1	1	FALSE
0	0	0	1	0	TRUE
0	0	0	0	1	TRUE
0	0	0	0	0	TRUE

Lab Report 11: - Draw the Pull-Up Network and Pull-Down Network for given Boolean Expression & check the output with a truth table.

Name: - R. Hemanth Krishna Vineel

Roll no: - 118CS0017

Course: - VLSI Practice