COMPUTER ORGANIZATION AND ARCHITECTURE
COA LAB ASSIGNMENT – 4
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Plot of IPC vs Configurations:

I have calculated the values of IPC using the benchmarks of Rodinia CUDA gpgpusim for the following configurations:

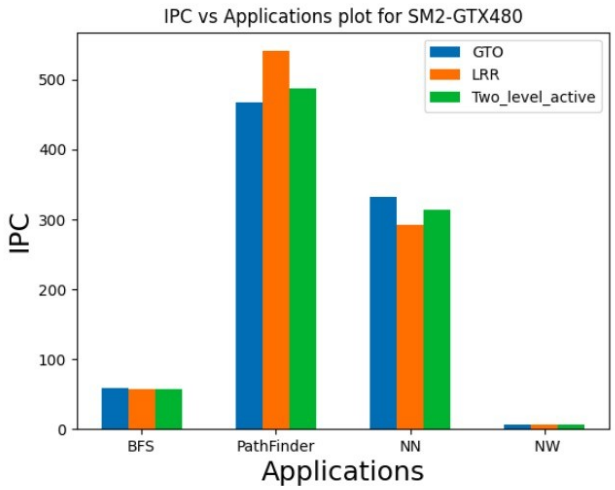
- SM2_GTX480
- SM3_KEPLER_TITAN
- SM6_TitanX
- SM7_QV100
- SM7_TITANV
- SM75_RTX2060

I have calculated the IPC for the following Warp Schedulers:

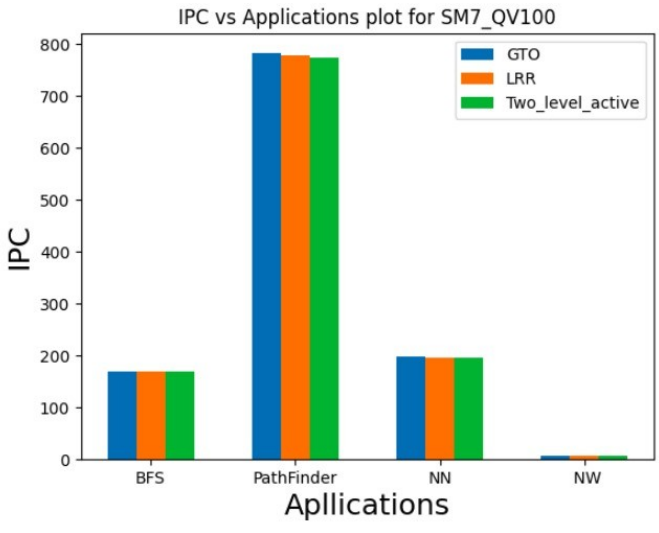
- GTO - Greedy-then-oldest
- LRR - Loose Round Robin
- TL - Two Level

PLOT:

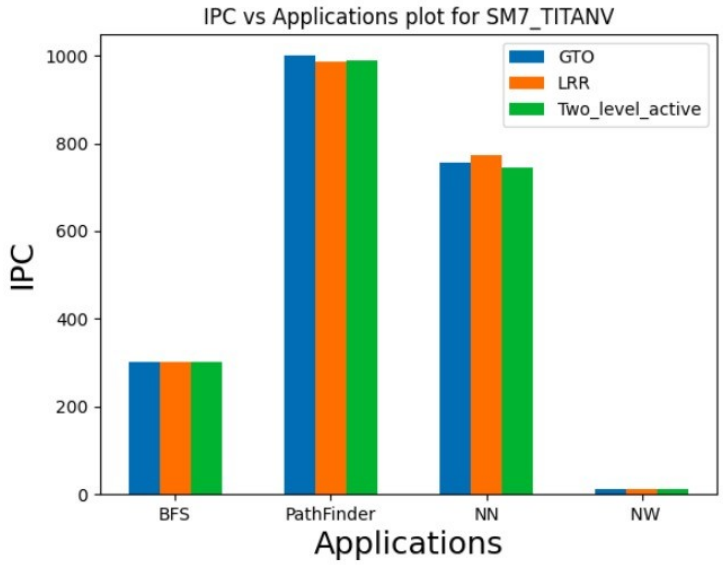
SM2-GTX480:



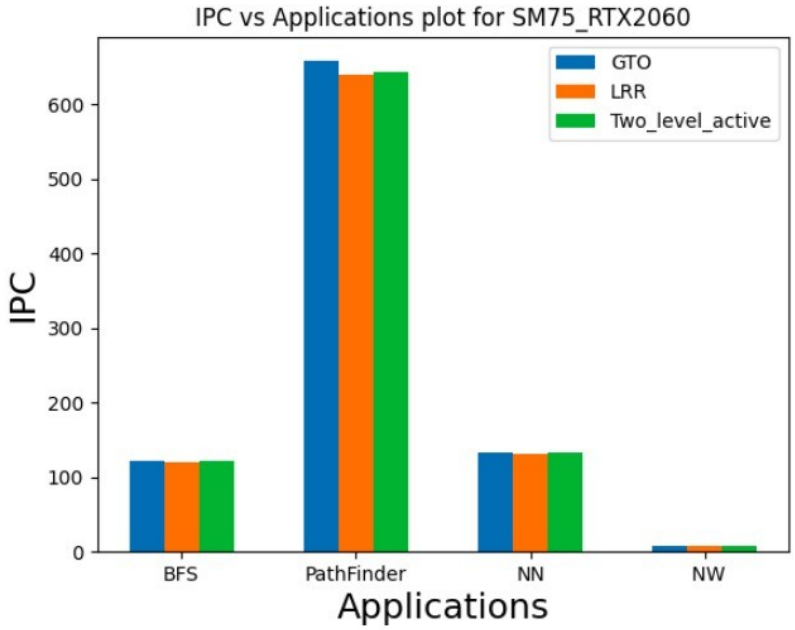
SM7-QV100:



SM7-TITANV:

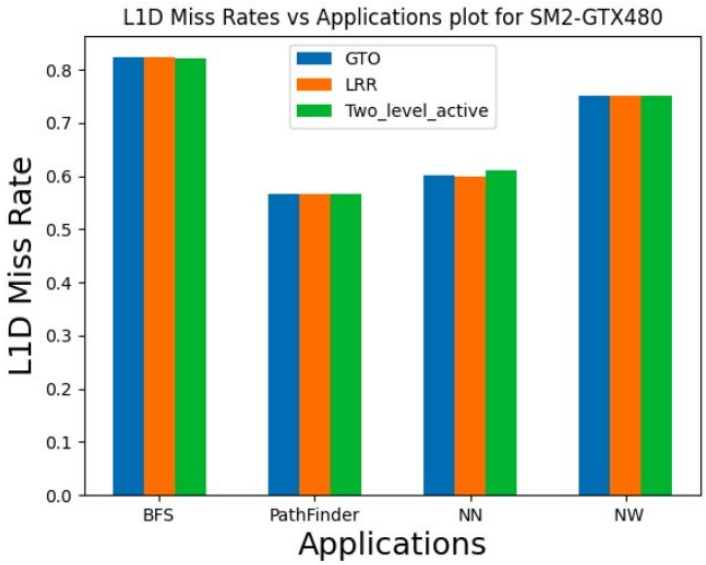


SM75-RTX2060:

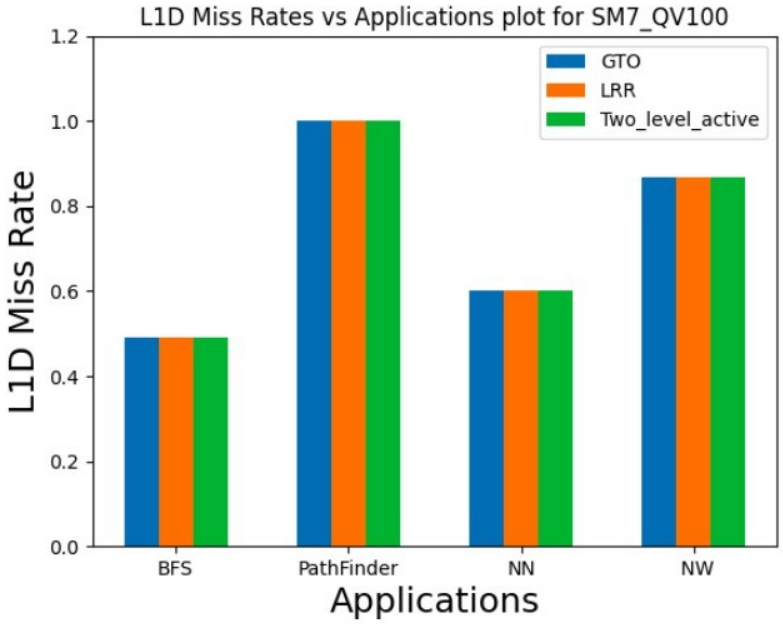


Q2: Plot of L1D Miss Rates:

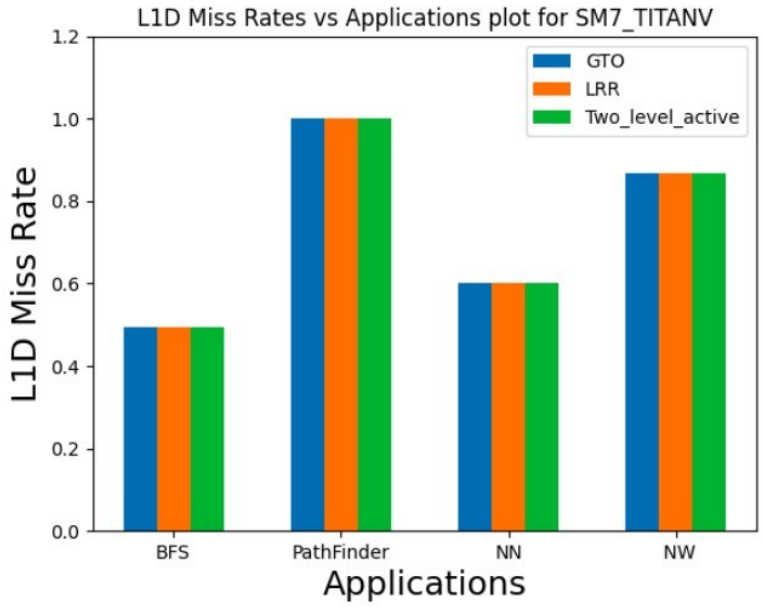
SM2-GTX480:



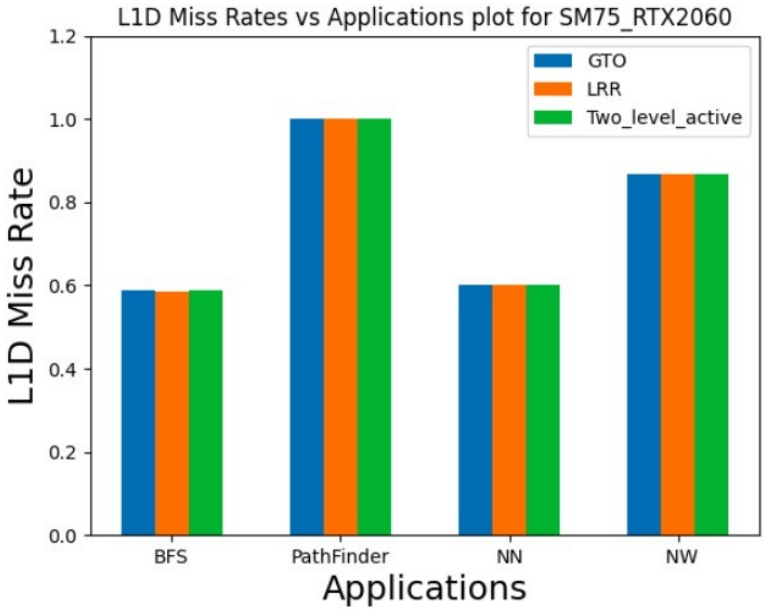
SM7-QV100:



SM7-TITANV:

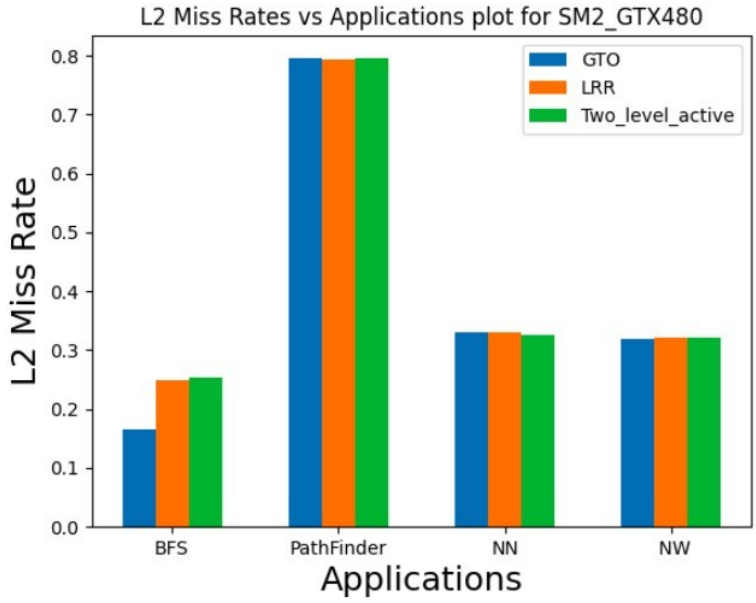


SM75-RTX2060:



Q2 – b: L2 Miss Rates PLOT:

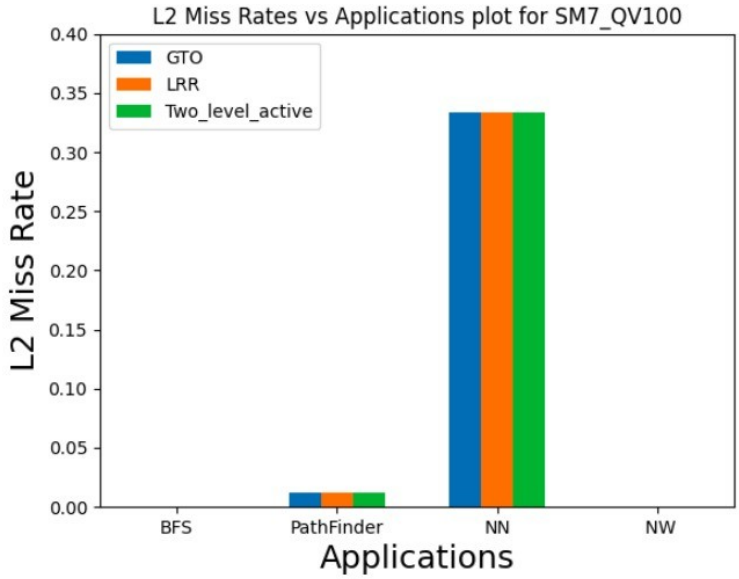
SM2-GTX480:



Supporting data

			SM2_GTX480					
			IPS	CPS	IPC	RUN_TIME	L1D MR	L2 MR
BFS	GTO		140474	2397	58.60408844	219	0.8225	0.1651
	LRR		212164	3712	57.15625	145	0.823	0.2493
	TWO_LEVEL_ACTIVE		146494	2549	57.47116516	210	0.8209	0.2537
PathFinder	GTO		1031370	2205	467.7414966	61	0.5671	0.7951
	LRR		1398080	2584	541.0526316	45	0.567	0.7946
	TWO_LEVEL_ACTIVE		911791	1870	487.5887701	69	0.567	0.7956
NN	GTO		600526	1811	331.5991165	2	0.6009	0.3304
	LRR		600526	2059	291.6590578	2	0.6	0.3309
	TWO_LEVEL_ACTIVE		600526	1911	314.2469911	2		0.3255
NW	GTO		58284	9428	6.182011031	107	0.7509	0.3192
	LRR		62364	10083	6.185063969	100	0.7509	0.3207
	TWO_LEVEL_ACTIVE		43009	6966	6.174131496	145	0.7509	0.3205

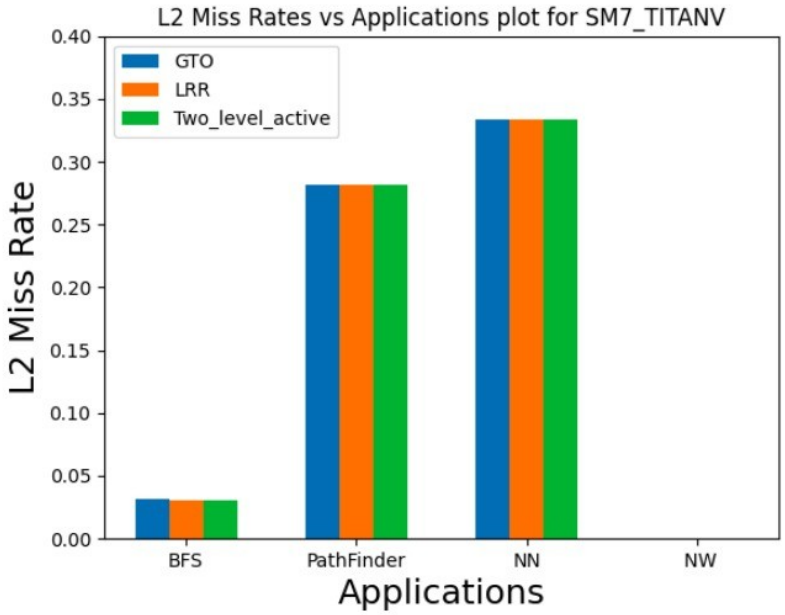
SM7-QV100:



Supporting data

SM7_QV100					
IPS	CPS	IPC	RUN_TIME	L1 MR	L2 MR
136123	803	169.5180573	226	0.4894	0
175793	1039	169.1944177	175	0.4881	0
112688	666	169.2012012	273	0.4895	0
547074	699	782.6523605	115	1	0.0123
796374	1024	777.7089844	79	1	0.0123
452615	585	773.7008547	139	1	0.0123
300263	1513	198.4553866	4	0.6	0.3334
300263	1524	197.0229659	4	0.6	0.3334
200175	1017	196.8289086	6	0.6	0.3334
18024	2502	7.20383693	346	0.8661	0
19013	2639	7.204622963	328	0.8661	0
13074	1817	7.195376995	477	0.8661	0

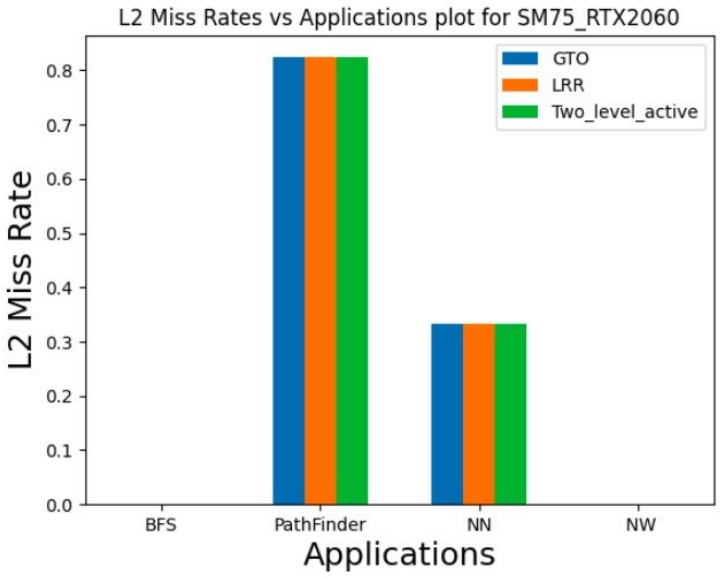
SM7-TITANV:



Supporting data

SM7_TITANV					
IPS	CPS	IPC	RUN_TIME	L1 MR	L2 MR
133755	444	301.25	230	0.4931	0.0317
221322	735	301.1183673	139	0.4936	0.0301
116972	388	301.4742268	263	0.493	0.031
367915	368	999.7690217	171	1	0.282
911791	924	986.7867965	69	1	0.282
487702	493	989.2535497	129	1	0.282
400350	529	756.805293	3	0.6	0.3334
400350	518	772.8764479	3	0.6	0.3334
300263	403	745.0694789	4	0.6	0.3334
30721	2720	11.29448529	203	0.8661	0
32146	2846	11.29515109	194	0.8661	0
21140	1876	11.26865672	295	0.8661	0

SM75-RTX2060:



Supporting data

SM75_RTX2060					
IPS	CPS	IPC	RUN_TIME	L1 MR	L2 MR
201070	1650	121.8606061	153	0.5869	0
287512	2388	120.39866	107	0.5865	0
184214	1506	122.3200531	167	0.5875	0
786420	1196	657.541806	80	1	0.824
1143883	1791	638.6839754	55	1	0.824
706894	1100	642.6309091	89	1	0.824
400350	3003	133.3166833	3	0.6	0.3334
400350	3074	130.2374756	3	0.6	0.3334
300263	2252	133.3317052	4	0.6	0.3334
43308	6089	7.112497947	144	0.8661	0
44866	6308	7.112555485	139	0.8661	0
31338	4393	7.133621671	199	0.8661	0

Q3 – L1D Cache size increase from 32KB to 8MB
DATA for 32KB

		SM2_GTX480	
		L1D MR	L2 MR
BFS	GTO	0.8225	0.1651
NN	GTO	0.6009	0.3304
NW	GTO	0.7509	0.3192

DATA for 8MB

		SM2_GTX480	
		L1D MR	L2 MR
BFS	GTO	0.3257	0.4795
NN	GTO	0.6	0.3309
NW	GTO	0.7481	0.3214

Changes observed in L1D miss rate when cache size is increased by 256 times

Miss rate = Number of misses / Number of accesses

Decrease in L1D miss rate
On increasing the size of L1D Cache, We can observe that L1D miss rate has decreased. This is because with increase in size, we can store greater amount of memory in the L1D cache and hence there are less number of misses.

Increase in L2 miss rate
Increasing the size of L1D Cache definitely has an impact on L2 Cache miss rate. But whether it is increases or decrease depends on various factors. Here as we can see, the L2 Cache miss rate has increased. Both L2 misses and acceses decreases. This could be because the decrease in number of L2 accesses with increasing in the size of L1D is dominant.

Q4 – Power Consumption of different applications
DATA for 32KB

		Power	Total Average Power
BFS	RFP	7.15	62.6126
	DRAMP	0.0948	
	L1P	3.8962	
	L2P	0.923	
NN	RFP	9.312	79.2563
	DRAMP	0.0579366	
	L1P	5.1959	
	L2P	10.0307	

DATA for 8MB

		Power	Total Average Power
BFS	RFP	7.15057	94.2833
	DRAMP	0.094	
	L1P	3.895	
	L2P	0.923	
NN	RFP	9.31267	79.2728
	DRAMP	0.0579366	
	L1P	5.1959	
	L2P	10.0307	

- Here we can observe that the percentage of power consumption of each component in the total power is decreasing by increasing the size of L1D.
- Increase in size of L1D cache helps in caching more data which in turn decreases the latency and hence decreasing the power consumption.