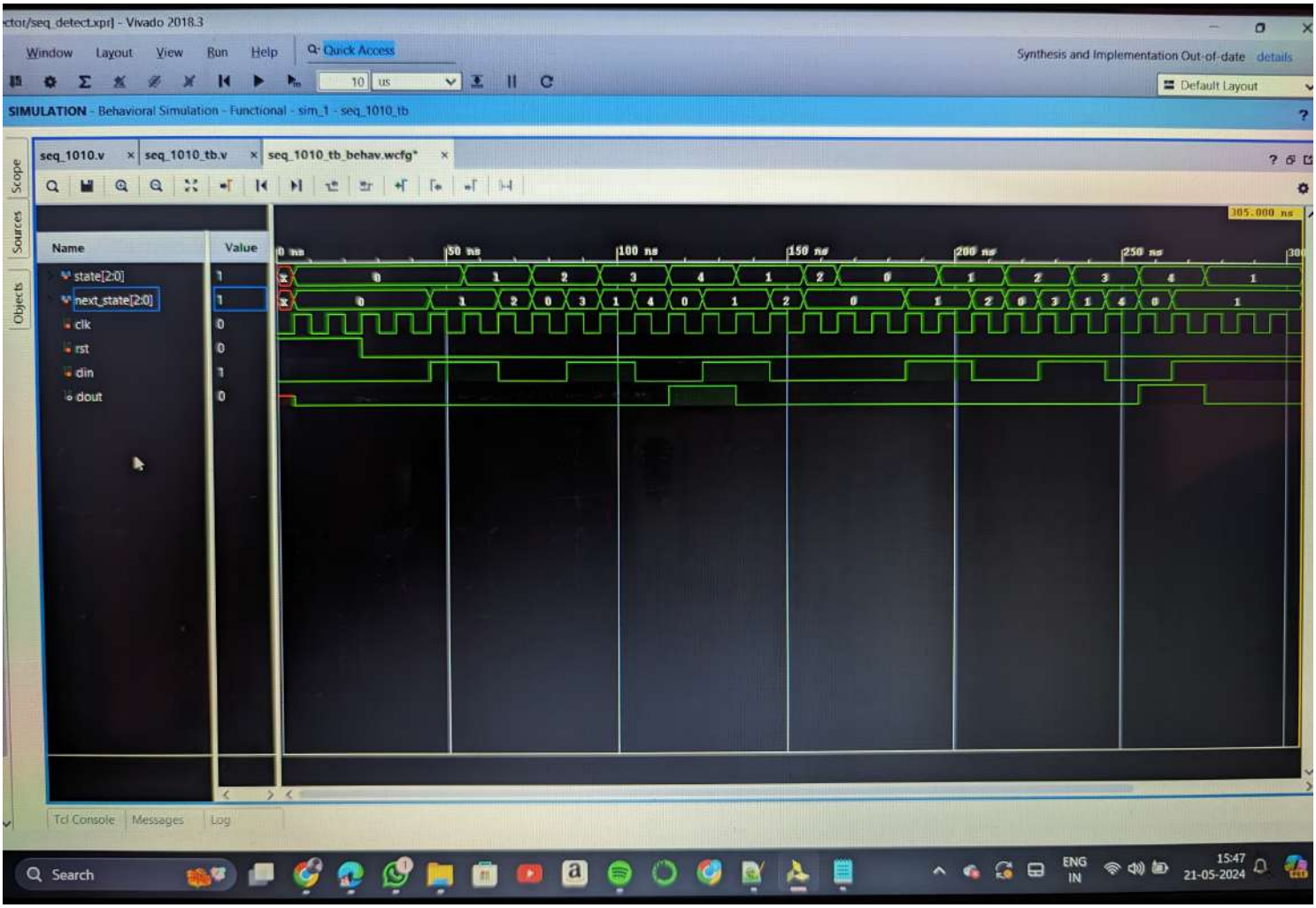
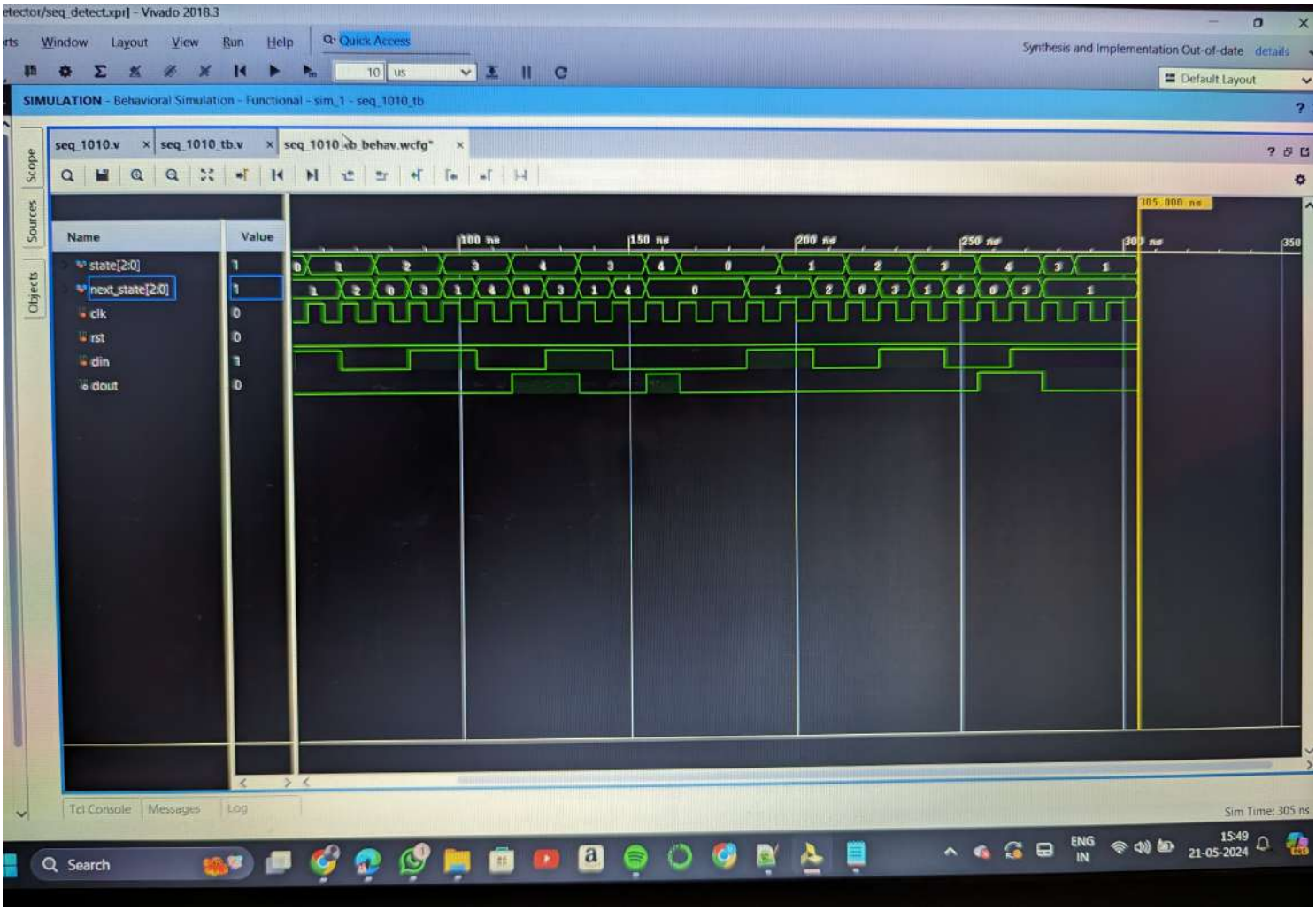
```
`timescale 1ns / 1ps

module seq_1010(
    //global signals
    input i_clock,
    input i_reset,

    // Btn
    input i_btn,
    //LED
    output o_led
) ;

//local parameters
localparam [2:0]  s0 = 0, s1 = 1, s2 = 2, s3 = 3, s4 = 4;

//Internal Regs or wire declarations
reg [2:0] state, next_state;

//Reset condition
always@(posedge i_clock) begin

    if(i_reset)
        state <= 3'b000;
    else
        state <= next_state;

end

always@(*) begin

    //Store the state
    next_state = state;

    //state machine
    case(state)

        s0: next_state <= i_btn ? s1 : s0;
        s1: next_state <= i_btn ? s1 : s2;
        s2: next_state <= i_btn ? s3 : s0;
        s3: next_state <= i_btn ? s1 : s4;
        s4: next_state <= i_btn ? s1 : s0;      //Non overlapping
       //s4: next_state <= i_btn ? s3 : s0;    //overlapping

   endcase

end

assign o_led =(state == s4) ? 1 : 0;

endmodule

```

```
`timescale 1ns / 1ps



module seq_1010_tb;
//Internal Regs/wires
reg     clk, rst, din;
wire    dout         ;

always
    #5 clk = ~clk;


initial begin

    clk = 0;
    rst = 1;
    din = 0;

    #25 rst  = 0;
    #20 din = 1;
    #20 din = 0;
    #20 din = 1;
    #20 din = 0;
    #20 din = 1;
    #20 din = 0;
    #20 din = 0;
    #20 din = 1;
    #20 din = 0;
    #20 din = 1;
    #20 din = 0;
    #20 din = 1;

    #40 $stop;
end

//initial begin

//    $dumpfile("dump.vcd")
//    $dumpvars(0);
//end

//Instantiation
seq_1010 uut(
.i_clock(clk),
.i_reset(rst),
.i_btn(din),
.o_led(dout)
);
endmodule

```


ctor/seq_detect.xpr] - Vivado 2018.3
Window
Layout
View
Run
Help
Quick Access
Synthesis and Implementation Out-of-date details
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - seq_1010_tb
seq_1010.v
seq_1010_tb.v
seq_1010_tb_behav.wcfg*
Name
Value
state[2:0]
next_state[2:0]
clk
rst
din
dout
305.000 ns
Tcl Console
Messages
Log
Search
ENG
IN
15:47
21-05-2024


etector/seq_detect.xpr] - Vivado 2018.3
Window
Layout
View
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Quick Access
Synthesis and Implementation Out-of-date
Default Layout
SIMULATION - Behavioral Simulation - Functional - sim_1 - seq_1010_tb
seq_1010.v
seq_1010_tb.v
seq_1010_tb_behav.wcfg*
Scope
Sources
Objects
Name
Value
state[2:0]
next_state[2:0]
clk
rst
din
dout
100 ns
150 ns
200 ns
250 ns
Tcl Console
Messages
Log
Sim Time: 305 ns
Search
ENG
IN
15:49
21-05-2024