MIT World Peace University

Digital Electronics and Computer Architecture
Second Year B. Tech, Semester 3

Design and Implementation of Combinational Logic Design using MUX/Decoder ICs.

Practical Report

Prepared By

Krishnaraj Thadesar
Cyber Security and Forensics
Batch A2, PA 34

October 10, 2022

Contents

1 Problem Statement

Design and Implement Combinational Logic Design using MUX/Decoder ICs.

1. To Verify the Truth table of multiplexers using IC74153
2. Design and Implement two variable Functions (SOP and POS) and half adder using IC74LS153
3. Verify its Truth Table.
4. Design and implement an 8:1 Multiplexer using two 4:1 Multiplexers for a given function using IC 74LS153.
$$Y = f(A,B,C) = \sum m(0,2,4,7)$$
5. Design and implement 8:1 Multiplexer using One 4:1 Multiplexer, applying reduction method for given function using IC 74LS153
$$Y = f(A,B,C) = \sum m(0,2,4,7)$$

2 ICs Used

1. IC7404 (NOR Gate)
2. IC7432 (OR Gate)
3. IC74LS153 (Dual 4: 1 Multiplexer IC)

3 Platform Used

Digital Trainer Kit

4 Theory

4.1 What is a Multiplexer

- Multiplexer (MUX) is a network device that allows one or more analog or digital input signals to travel together over the same communications transmission link. The purpose of multiplexing is to combine and transmit signals over a single shared medium in order to optimize efficiency and decrease the total cost of communication.
- Essentially, a MUX functions as a multiple-input, single-output switch that allows multiple analog and digital input signals and to be routed through a single output line. At the receiving end, another device called a demultiplexer recovers the original individual signals.
- Multiplexers are capable of handling both analog and digital applications. In analog applications, multiplexers are made up of relays and transistor switches, whereas in digital applications, the multiplexers are built from standard logic gates. When the multiplexer is used for digital applications, it is called a digital multiplexer

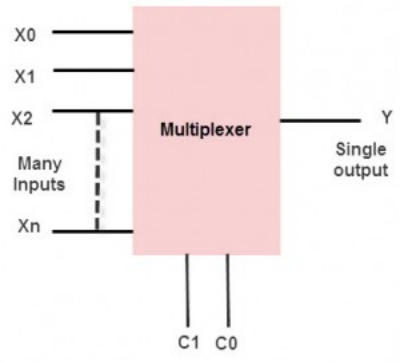

Figure 1: Multiplexer Representation

4.1.1 Types

1. 2-1 multiplexer (1 select line)
2. 4-1 multiplexer (2 select lines)
3. 8-1 multiplexer(3 select lines)
4. 16-1 multiplexer (4 select lines)

4.2 Advantages of a Multiplexer

1. In multiplexer, the usage of a number of wires can be decreased
2. It reduces the cost as well as the complexity of the circuit
3. The implementation of a number of combination circuits can be possible by using a multiplexer
4. Mux doesn't require K-maps and simplification
5. The multiplexer can make the transmission circuit less complex and economical
6. The multiplexer ability can be extended to switch audio signals, video signals, etc.
7. The digital system reliability can be improved using a MUX as it decreases the number of exterior wired connections.
8. MUX is used to implement several combinational circuits
9. The logic design can be simplified through MUX

4.3 Applications of a Multiplexer

Multiplexers are used in various applications wherein multiple-data need to be transmitted by using a single line.

1. Communication Systems
   A communication system has both a communication network and a transmission system. By using a multiplexer, the efficiency of the communication system can be increased by allowing the transmission of data, such as audio and video data from different channels through single lines or cables.

2. Computer Memory
   Multiplexers are used in computer memory to maintain a huge amount of memory in the computers, and also to reduce the number of copper lines required to connect the memory to other parts of the computer.
3. Telephone networks:
   In telephone networks, multiple audio signals are integrated on a single line of transmission with the help of a multiplexer.
4. Transmission From the computer system of a Sattelite
   The multiplexer is used to transmit the data signals from the computer system of a spacecraft or a satellite to the ground system by using a GSM satellite.

4.4 Involved Truth Tables

4.4.1 OR Gate

A	B	Q
0	*0*	*0*
0	*1*	*1*
1	*0*	*1*
1	*1*	*1*

4.4.2 NOT Gate

A	Q
0	1
1	0

4.4.3 Truth Table of Half Adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

4.4.4 Truth Table of a Full Adder

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

4.4.5 Function Table of the IC74LS153

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Figure 2: Function Table for IC 74LS153

4.5 Symbols in the Pin Diagram of IC74LS153

Pin	Symbol	Description
1	1E	enable input 1
2	S1	common data select input
3	1I3	data input from source 1
4	1I2	data input from source 1
5	1I1	data input from source 1
6	1I0	data input from source 1
7	1Y	multiplexer output from source 1
8	GND	ground
9	2Y	multiplexer output from source 2
10	2I0	data input from source 2
11	2I1	data input from source 2
12	2I2	data input from source 2
13	2I3	data input from source 2
14	S0	common data select input
15	2E	enable input 2
16	Vcc	supply voltage

4.5.1 Given SOP Function for 4 : 1 Implementation

$$Y = f(A,B,C) = \sum m(0,2)$$

Inputs	A	B	Y
I0	0	0	1
I1	0	1	0
I2	1	0	1
I3	1	1	0

4.5.2 Given POS Function for 4 : 1 Implementation

$$Y = f(A,B,C) = \Pi M(1,2)$$

Inputs	B	A	Y
I0	0	0	1
I1	0	1	0
I2	1	0	0
I3	1	1	1

4.6 Given SOP Function for 8 : 1 Implementation

$$Y = f(A,B,C) = \sum m(0,2,4,7)$$

Decimal	C	B	A	Output
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	1

5 Pin Diagrams of ICs Used

5.1 Pin Diagram of IC74LS153

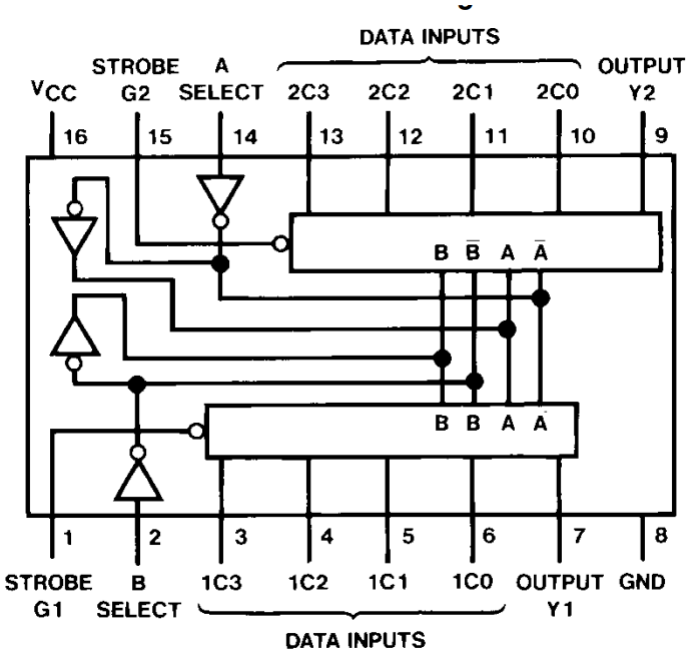

Figure 3: Pin Diagram for IC 74LS153

5.2 Pin Diagram of IC7432

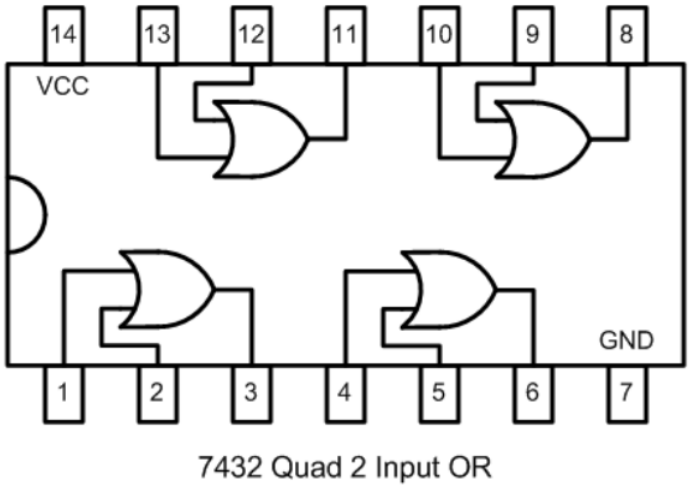

Figure 4: Pin Diagram for IC 7432

5.3 Pin Diagram of IC7404

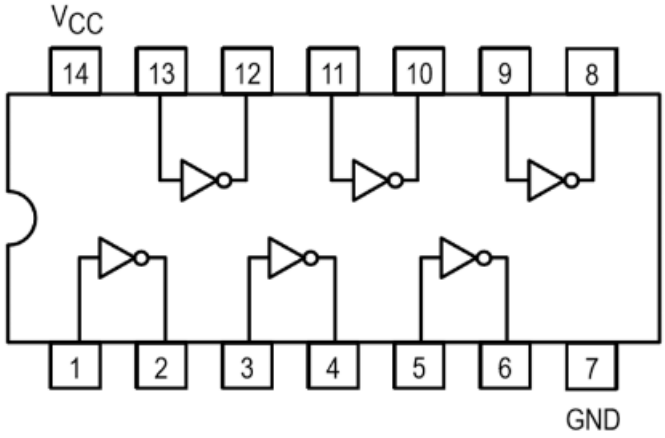

Figure 5: Pin Diagram for IC 7404

6 Design and Implementation

6.1 Logical Design for Verification of Truth Table of IC74LS153

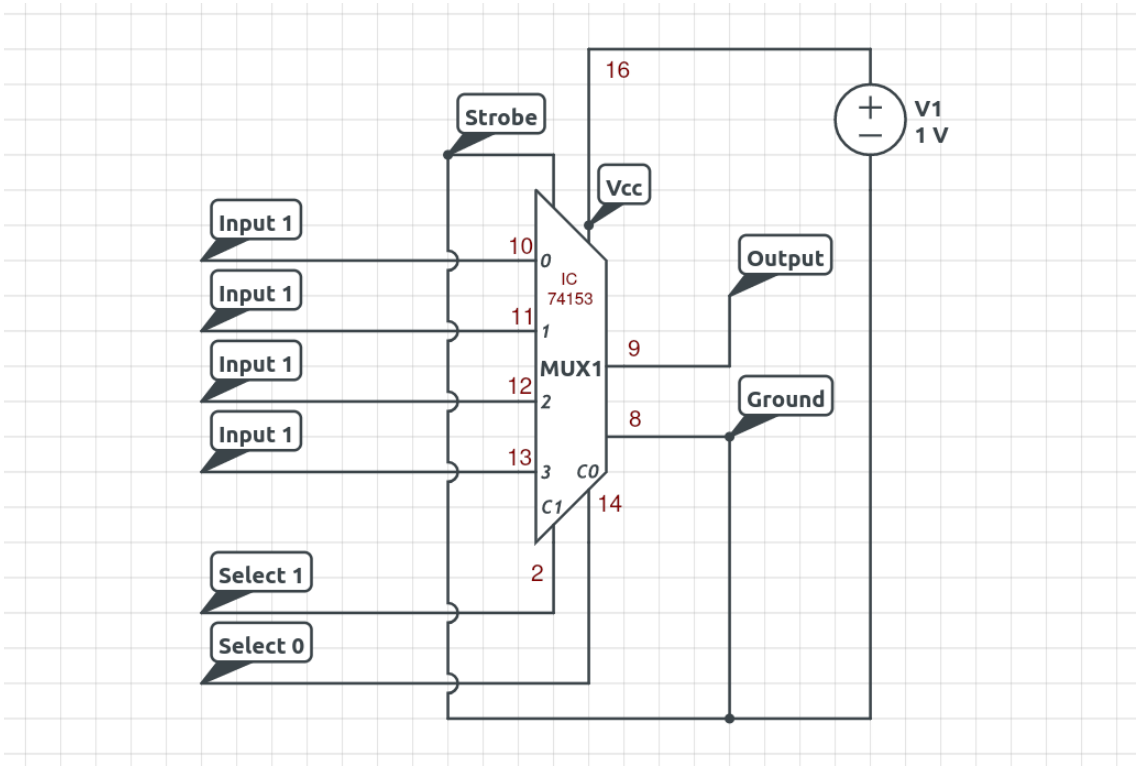

Figure 6: Truth Table for IC 74153

6.2 Logical Design of SOP on 4: 1 Multiplexer using IC74LS153

$$Y = f(A,B,C) = \sum m(0,2)$$

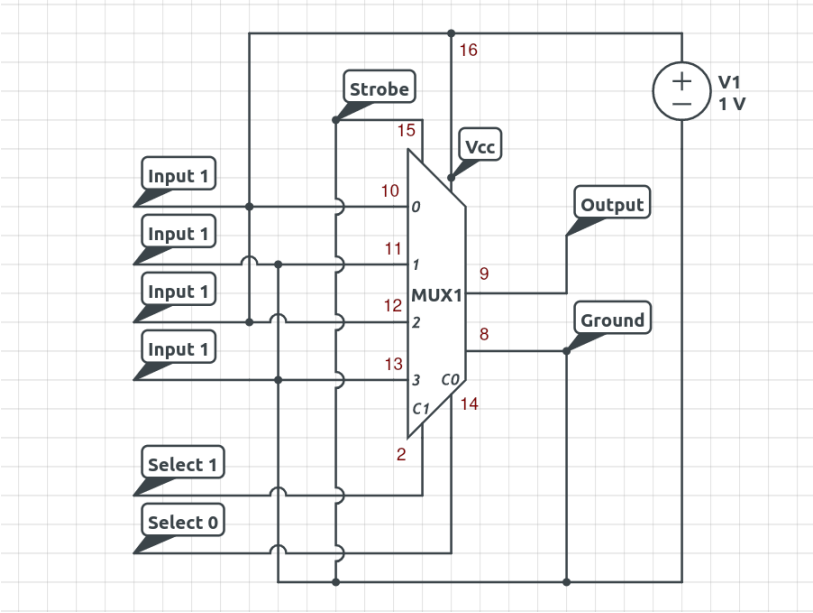

Figure 7: Diagram for Implementation of SOP

6.3 Logical Design of POS on 4: 1 Multiplexer using IC74LS153

$$Y = f(A,B,C) = \Pi M(1,2)$$

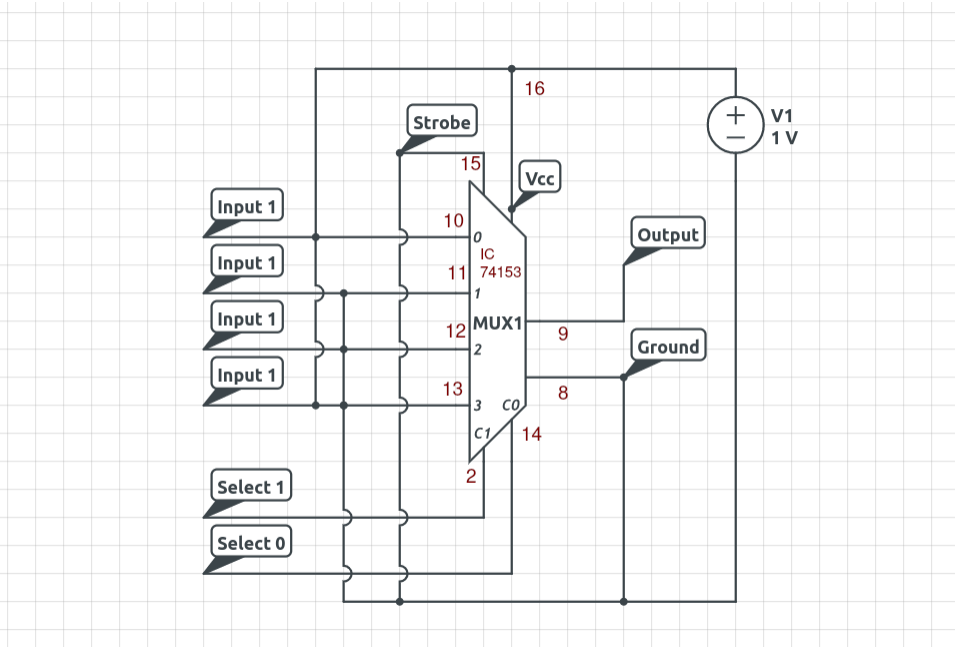

Figure 8: Diagram for Implementation of POS

6.4 Logical Design of Half Adder using IC74LS153

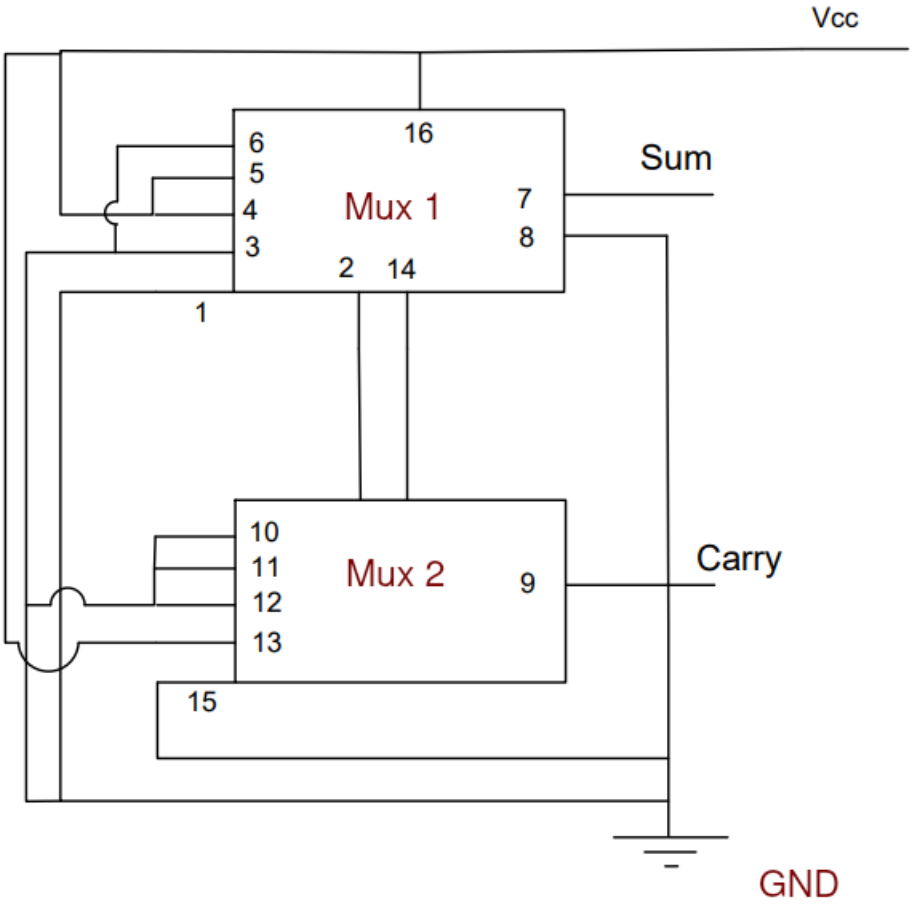

Figure 9: Half Adder Implementation using 2 4:1 Mux

6.5 Logical Design of Full Adder using IC74LS153

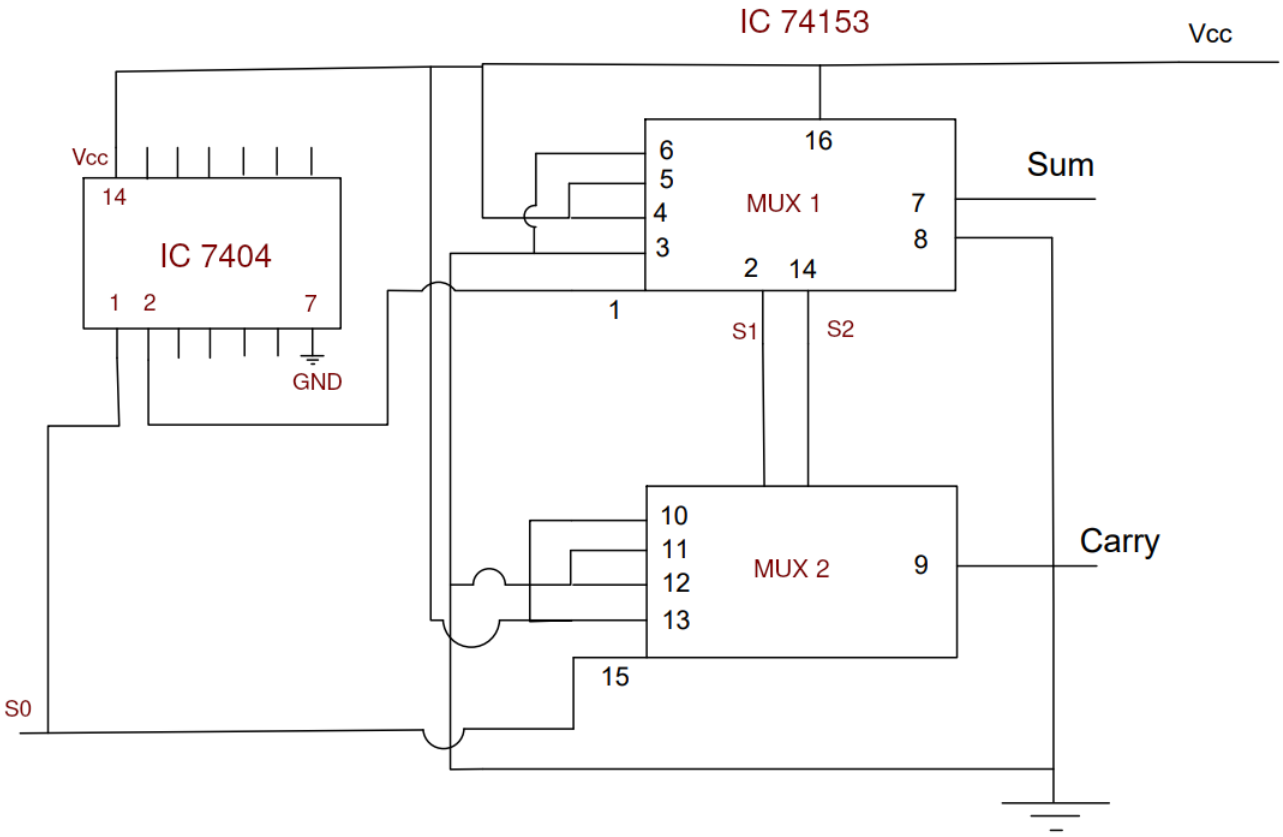

Figure 10: Full Adder Implementation using 2 4:1 Mux

6.6 Logical Design for Implementing 8 : 1 Multiplexer using 2 4: 1 Multiplexers in IC74LS153 for Given SOP Function

$$Y = f(A,B,C) = \sum m(0,2,4,7)$$

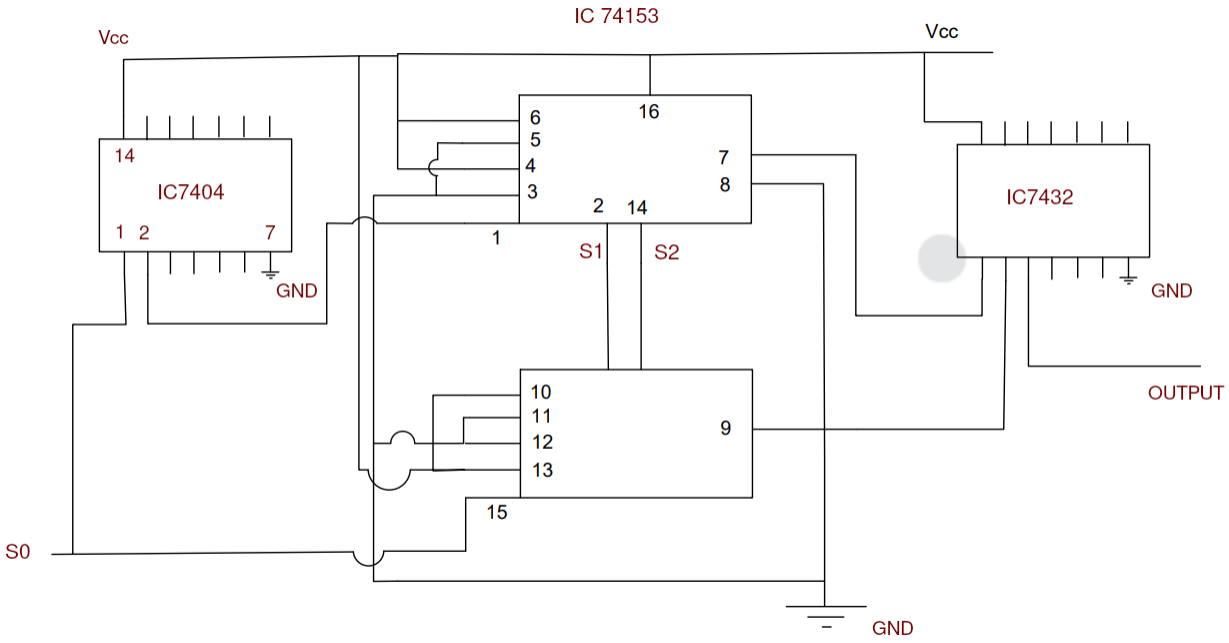

Figure 11: Given SOP Function Implementation 2 4:1 Mux

6.7 Logical Design for Implementing 8 : 1 Multiplexer using only 1 4: 1 Multiplexers in IC74LS153 for Given SOP Function using Reduction Method

$$Y = f(A,B,C) = \sum m(0,2,4,7)$$

Reduction Method

A \ $I_0I_1I_2I_3$	00	01	11	10
0	1	0	1	0
1	1	0	0	1

$$I_0 = V_{cc} \tag{1}$$
$$I_1 = GND \tag{2}$$
$$I_2 = \overline{A} \tag{3}$$
$$I_3 = A \tag{4}$$

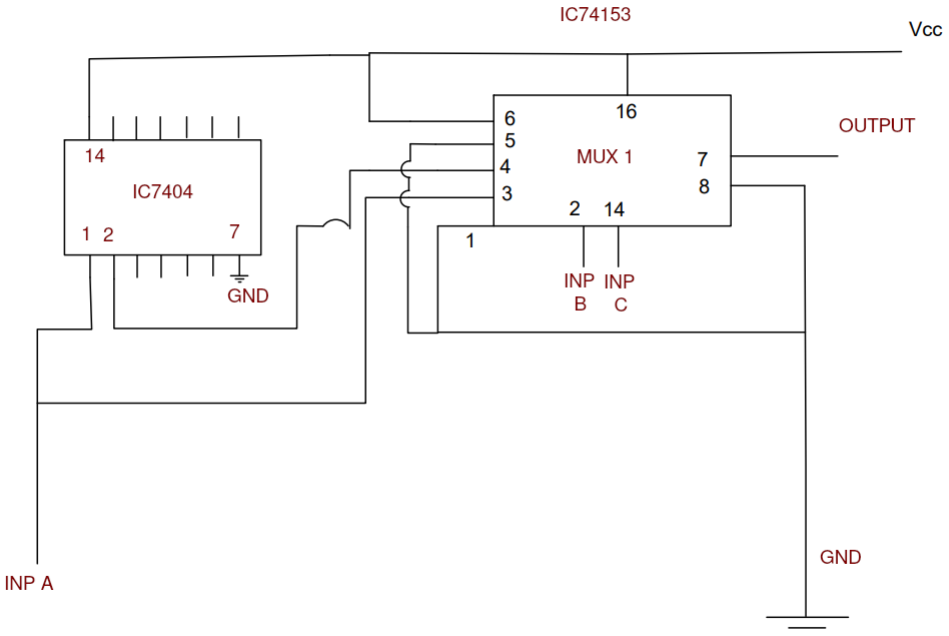

Figure 12: Given SOP Function Implementation 1 4:1 Mux

7 Procedure

1. Design Combinational logic circuit as per given problem statement.
2. Connect the IC 74153 and other basic logic gate ICs as per diagram.
3. Give Vcc supply and ground connection to each IC.
4. Give various combinations to select lines.
5. Observe the output and verify the truth table.
6. Switch off the power supply of the trainer kit.

8 Conclusion

We have learnt the application, usage and implementation of Multiplexers. SOP and POS Implementations on MUX were also understood. The Functionalities of Half Adder and Full adder were learnt in detail, and we also learnt how to apply basic logic gates in a different circuit according to its requirements.

9 FAQs

1. **What is the use of Strobe in a Multiplexer?** Strobe is the enable pin in MUX. It is the pin that enables the functioning of the MUX. Depending on it being Active Low or Active High, If we pass deactivating signal to strobe, none of the inputs are selected in the MUX. Each mux has a Strobe.

2. **Design and Implement a Full Adder using a Multiplexer** Implementation, Diagram and Truth Table are given above.