MIT World Peace University

Digital Electronics and Computer Architecture
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3 bit Synchronous UP Counter using JK-Flip flop

Practical Report
Assignment 5

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Contents

1 Objectives

1. To understand the operation of Synchronous counter
2. To design and implement 3-Bit Synchronous UP counter using JK- Flip flop

2 Problem Statement

Design and Implement 3 bit Synchronous UP Counter using JK- Flip flop

3 ICs Used

1. IC7408 (AND Gate)
2. IC7476 (Dual Master Slave JK Flip Flop)

4 Platform Used

Digital Trainer Kit

5 Theory

5.1 Definition of Synchronous counter

Synchrounous generally refers to something which is cordinated with others based on time. Synchronous signals occur at same clock rate and all the clocks follow the same reference clock.

In previous tutorial of Asynchronous Counter, we have seen that the output of that counter is directly connected to the input of next subsequent counter and making a chain system, and due to this chain system propagation delay appears during counting stage and create counting delays. In synchronous counter, the clock input across all the flip-flops use the same source and create the same clock signal at the same time. So, a counter which is using the same clock signal from the same source at the same time is called Synchronous counter.

5.2 Advantages of Synchronous counter

1. It's easier to design than the Asynchronous counter.
2. It acts simultaneously.
3. No propagation delay associated with it.
4. Count sequence is controlled using logic gates, error chances are lower.
5. Faster operation than the Asynchronous counter.

5.3 Application of Synchronous counter

1. Machine Motion control
2. Motor RPM counter
3. Rotary Shaft Encoders
4. Digital clock or pulse generators.
5. Digital Watch and Alarm systems.

5.4 Involved Truth Tables

5.4.1 AND Gate

A	B	Q
0	*0*	*0*
0	*1*	*1*
1	*0*	*1*
1	*1*	*1*

5.4.2 Truth table of 3 Bit synchrounous down counter.

5.4.3 Function Table of the IC7476

Function Tables:

Inputs					Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H †	H †
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

† This configuration is nonstable; that is, it will not persist when wither preset or clear returns to its inactive (high) level.

Figure 1: Function Table for IC 7476

5.5 JK Flip Flop Truth table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	0
1	0	X	1
1	1	X	0

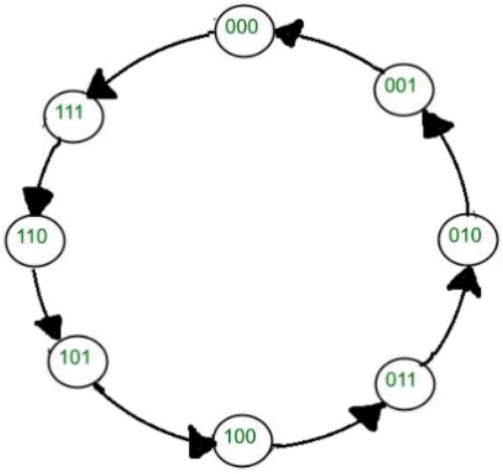
5.6 JK Flip Flop Excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	0
1	0	X	1
1	1	X	0

5.7 JK Flip Flop Characteristic table

J	K	Q_n	Q_{n+1}	State
0	0	0	0	Q_n (Hold)
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	1	Toggel
1	1	1	0	

5.8 State diagram of 3 Bit Synchronous Down Counter



6 Pin Diagrams of ICs Used

6.1 Pin Diagram of IC7476

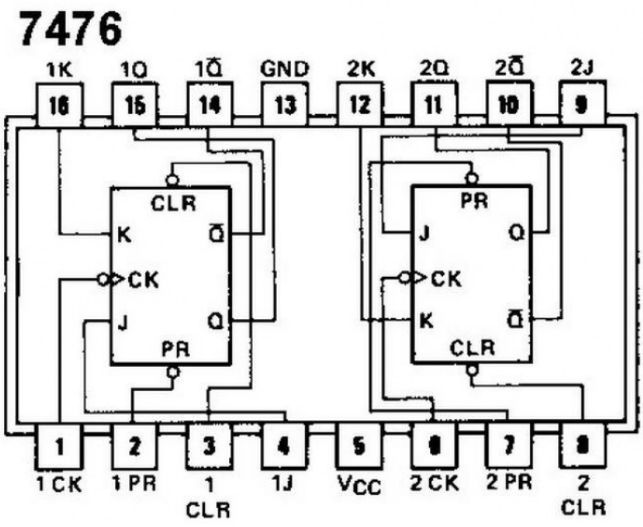


Figure 2: Pin Diagram for IC 7476

6.2 Pin Diagram of IC7408

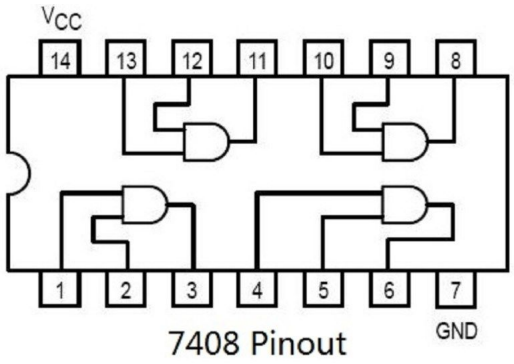


Figure 3: Pin Diagram for IC 7408

7 Design and Implementation

7.1 Circuit diagram of a 3-bit asynchronous counter: (3 Bit Asynchronous - DOWN Counter / Modulus 8)

Logic Diagram for 3-bit Down Counter:

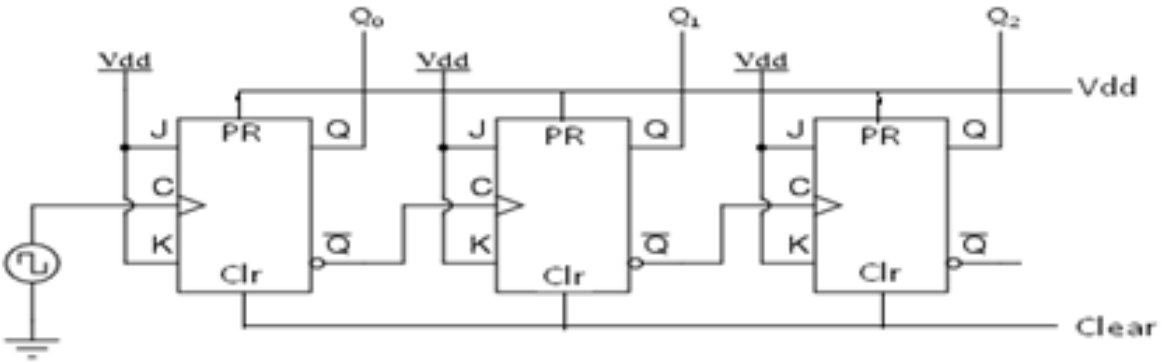


Figure 4: Circuit diagram of a 3-bit synchronous counter - Down

8 Procedure

1. Design Sequential circuit logic circuit as per given problem statement.
2. Connect the IC 74LS76 and other basic logic gate ICs as per diagram.
3. Give VCC supply and ground connection to each IC.
4. Give clock to first JK FF.

5. Observe the output and verify the truth table.

6. Switch off the power supply of trainer kit.

9 Conclusion

Thus, we have learnt a fundamental application and working of the IC 7476, and verified the truth table of its dual Master Slave JK Flip Flops. The Logic of Flip Flops was understood in detail, and implemented on the Digital Trainer Kit. Synchronous counters were also implemented with MOD 8. Their results were observed, noted and understood.

10 FAQs

1. Why a synchronous counter operate at a higher frequency than a ripple counter?

   Synchronous counters can operate at a higher frequency than a ripple counter because the dual flip flops in the counter operate at the same time, therefore reducing the time by a huge margin, and subsequently increasing the frequency.

2. A 5-bit synchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp(total)) is ?

   Each bit has propagation delay = 12ns. So, 5 bits = 12ns * 5 = 60ns. Since a counter is constructed using flip-flops, therefore, the propagation delay in the counter occurs only due to the flip-flops. Each bit has propagation delay = 15ns.