

# Design Of Vedic IEEE 754 Floating Point Multiplier

Soumya Havaldar, K S Gurumurthy

**Abstract -** Floating point number can co-occurredly develop a prominent range of numbers and a high level of precision. Multiplication of floating point numbers found extensive use in wider range of technological and commercial calculations. It is needed to implement faster multipliers involving limited area and consuming reduced power. An IEEE-754 format established multiplier applying Vedic Urdhva - Tiriyagbhyam mathematics will be cultivated to cover both single precision and double precision format floating point numbers in the paper. This paper proposes a floating point multiplier which manages overflow, underflow and rounding. The proposed and conventional floating point multipliers based on Vedic mathematics would be coded in Verilog, Synthesized and Simulated using ISE Simulator. Xilinx Virtex VI FPGA will be used for Hardware realization and Verification. It is proposed to compare resource utilization and timing performance of the proposed multiplier with that of existing as of now.

**Keywords -** Floating point number, IEEE 754 format, Vedic mathematics, Urdhva-Triyakbhyam sutra, Verilog.

## I. INTRODUCTION

Floating point numbers represent real numbers in binary format. Since computer memory is limited, you cannot store numbers with precision up to infinity, no matter whether you use binary fractions or decimal ones, at some point you have to truncate the number. Representing a number in floating point format has more boldness and efficiency when compared to fixed-point representations. Fixed-point quantities are represented in two's complement format which is complicated as compared to biasing the exponent part in floating point multiplication. These are the few issues which motivated me to carry out this as my final year project and same is introduced in the paper.

The floating point numbers can be expressed using the IEEE-754 standard which defines a set of floating point data formats, single precision consisting of 32 bits and double precision consisting of 64 bits. Xilinx Virtex VI platform FPGA usage for the implementation of Floating Point numbers rather than microprocessor based configurations will be the leading choice due to high speed operation, parallel processing, re-programmability. This paper describes the Design of Single and Double Precision Floating Point Multiplier based on Vedic mathematics. Proposed Multiplier will be modeled using Verilog. The design is Synthesized and Simulated using ISE Simulator. Xilinx Virtex VI FPGA will be used for Hardware implementation of the multiplier algorithms.

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## II. LITERATURE REVIEW

Paldurai. K and Dr. K. Hariharan [1] designed a FPGA Implementation of Delay Optimized Single Precision Floating point multiplier which shows an improvement in multiplication speed by 21.7% when compared to conventional multiplier. Irene Padma B. T et al [2] proposed a Pipelined Floating point multiplier based on Vedic Multiplication technique where the LUTs used are less in number which implies reduced hardware requirement, thereby reducing the power consumption. Sai Siva Teja et al [3] designed a FPGA implementation of low-area floating point multiplier using Vedic Nikhilam Sutra, here the area has been reduced because of the less usage of CLBs and flip flops. Priyanka Koneru et al [4] proposed Asynchronous single precision floating point multiplier using verilog HDL, here the mantissa part of floating point format is done using booth algorithm and vedic multiplier where they showed that the Vedic Multiplier was surpassing in terms of path delay and area. I. V. Vaibhav et al [5] designed a VHDL implementation of floating point multiplier using vedic mathematics, to obtain the improvement in power efficiency the urdhva triyagbhyam is implemented and they found that the components can be decreased which in turn reduces the complexity of the hardware circuit. Ms Meenu S Ravi et al [6] proposed an analysis and study of different multipliers to design floating point MAC units for digital signal processing applications; they showed here that the floating point multiplier can be run at the frequency 80 MHz when implemented on FPGA.

## III. ARCHITECTURE OF THE SYSTEM

**A. Floating Point Number -** Floating point number mean the decimal point can be shifted to right or left of the fixed number, hence the name floating point. The floating point representation gives greater precision and reinforces a much expandable range of values compared to the fixed point representation.

**B. Floating Point Representation -** The IEEE-754 standard format can be represented in binary pattern as well as in a decimal format. In this paper the multiplication of two binary floating point numbers is done. A Single Precision Floating Point Multiplier and a Double Precision Floating Point Multiplier in IEEE-754 standard binary format is shown in the fig 1 and fig 2. The Single Precision Floating Point Multiplier consists of 32 bits in which the sign bit is represented by 1 bit, the exponent bit is represented by 8 bits, and the mantissa bit is of 23 bits. The Double Precision Floating Point Multiplier consists of 64 bits in which the sign bit is represented by MSB bit, the exponent bit is represented by 11bits, and the mantissa bits are of 52 bits.

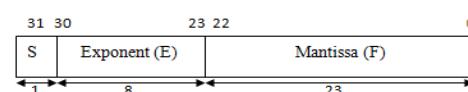


Fig.1: IEEE-754 Single Precision Floating Point Pattern

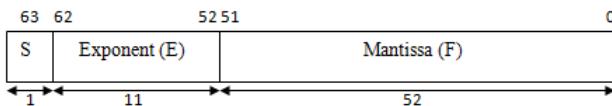


Fig.2: IEEE-754 Double Precision Floating Point Pattern

**C. Vedic Mathematics -** Vedic mathematics was reorganized from the ancient Indian scriptures (Vedas) by Swami Bharati Krishna Tirthaji Maharaja (1884-1960) after his eight years of research on Vedas, he came up with sixteen sutras and 13 sub-sutras. Out of these sutras Urdhva Tiryagbhyam is used in the paper. This sutra is simple in understanding, simple in design, less steps are involved in calculating and uses less hardware compared to other sutras of Vedas. A demonstration of two decimal number multiplication using Urdhva Tiryagbhyam sutra is shown in fig 3.

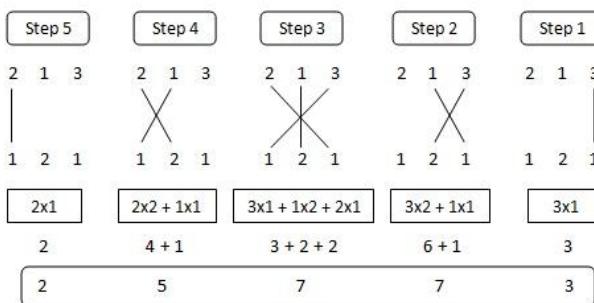


Fig.3: Illustration of Urdhva Tiryagbhyam Sutra

The  $3 \times 3$  multiplication is done for the two numbers, where the solution is obtained in a single line calculation. Thus, by using Urdhva Tiryagbhyam Sutra for binary multiplication, the steps involved in reaching the final product will be less, therefore the execution time of the multiplier decreases and also operates in a higher speed.

#### IV. DESIGN METHOD FOR SINGLE AND DOUBLE PRECISION FLOATING POINT MULTIPLIER

**A.** In this paper a Single and double precision floating point multiplier which can handle over flow, under flow and rounding of the result are designed. Fig 4 shows the multiplier structure that includes the addition of exponents, multiplication of mantissa, and sign calculation. This structure remains same for all precision floating point multipliers according to the standard IEEE 754, except the biasing value, number of bits in an exponent part and mantissa part will be as shown in the floating point bit pattern in fig 1 and 2.

#### B. Floating Point Multiplication Algorithm

Multiplication of two floating point binary digits represented in IEEE 754 format is interpreted as:

$$V = (-1)^{\text{Sign}} * 2^{\text{exponent} - \text{bias}} * 1.\text{fraction}$$

Let me consider one example to multiply two floating point numbers so that it will be easy to understand the steps involved:

Let two floating point numbers be,

$$X1 = 0 10000101 11110100100000000000000000000000$$

$$X2 = 0 10000010 10010100000000000000000000000000$$

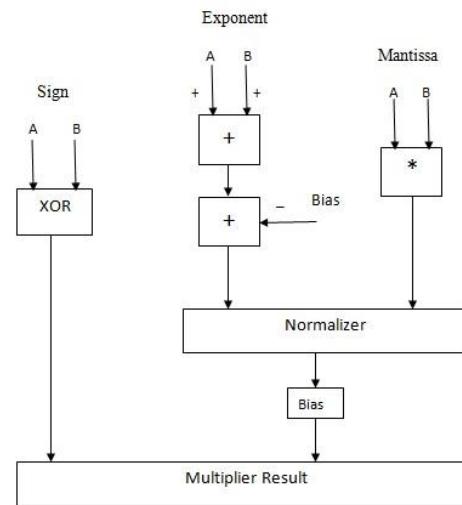


Fig.4: Floating Point Multiplier Structure

#### Step 1: 24 bit Mantissa multiplication

$$\begin{aligned} M &= X1 * X2 = 1.111101001000... * 1.100101000... \\ &= 10.1111001010010000... \\ &= 1.01111001010010000... * 2^1 \text{ (normalizing)} \\ E\_M &= 1+127 = 128_{10} = 1000\ 0000_2 \end{aligned}$$

#### Step 2: 8 bit Exponent Addition

$$\begin{aligned} E &= E\_X1 + E\_X2 + E\_M - 127 \text{ (biasing)} \\ &= 133 + 130 + 128 - 127 \\ &= 137_{10} = 10001001_2 \end{aligned}$$

#### Step 3: Sign bit

$$S1 \text{ XOR } S2 = 0 \text{ XOR } 0 = 0$$

#### Step 4: Final Floating point Multiplier Result

$$V = 0 10001001 0111100101001000000000000000$$

Hence seeing the example we can summarize the steps involved in an IEEE 754 Single precision floating point multiplier as follows:

#### 1. Multiplying the significant

$$M_{\text{out}} = (1.\text{Mantissa A} * 1.\text{Mantissa B})$$

Take the bit Mantissa part, add 1 at the MSB and now it has 53 bits. Multiply these two Mantissa's using Vedic Multiplier and get the result.

#### 2. Addition of Exponents

$$E_{\text{out}} = (\text{Exponent A} + \text{Exponent B} - \text{Bias})$$

Here three 11 bit numbers are added in order to calculate the exponent by using Ripple Carry Adder.

#### 3. Sign bit Calculation

$$S = \text{Sign A XOR Sign B}$$

If S is 0 it indicates the given value is positive, and if S is 1 it indicates the value as a negative number.

#### 4. Normalization

It gives the normalized 52 bits and biased exponent, after checking the leading 1 on the 108 bit mantissa output.

#### 5. Round up the result to fit in the available bits. And check for bits underflow/overflow occurrence.

## V. PROPOSED VEDIC MULTIPLIER

Proposed design uses Urdhva - Tiryagbhyam Vedic Multiplication technique for the implementation of the Mantissa part of IEEE 754 Floating Point Multiplier. Here 3x3 blocks is used as the key block. For a 3 bit product the partial multiplications and their additions of product are accessed parallel in Urdhva - Tiryagbhyam as shown in fig 5.

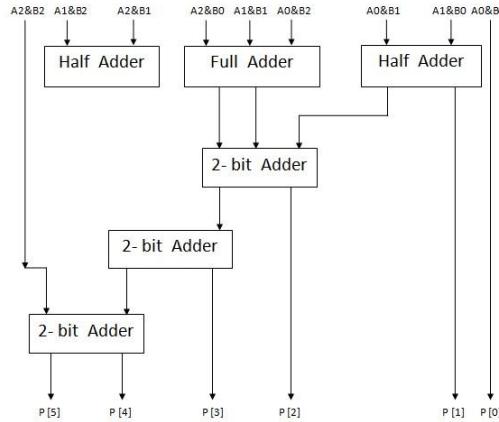


Fig.5: Hardware implementation of 3x3 block

The Vedic multiplier architecture for mantissa part for the proposed single and double precision, 24x24 and 53x53 are shown in Fig.6 and Fig.7. Firstly the basic block of 3x3 bit multiplier is designed with two half adders, one full adder and three 2-bit adders as shown in fig 4, then 6x6 block multiplier is designed using 3x3 block, then a 12x12 block multiplier is designed using 6x6 block, and from these 12x12 block the required VM are designed which uses Ripple carry adder for the final output of the Vedic Multipliers.

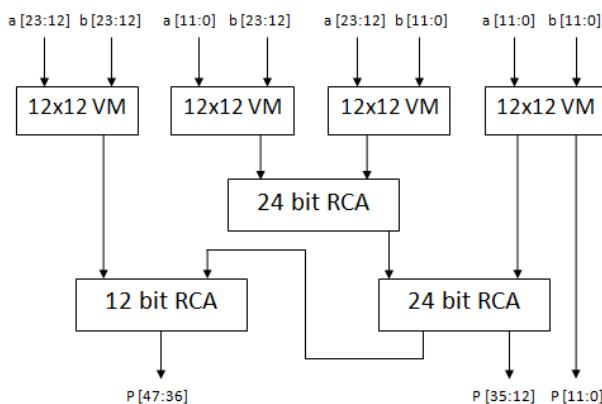


Fig.6: Proposed Single Precision 24x24 Vedic Multiplier

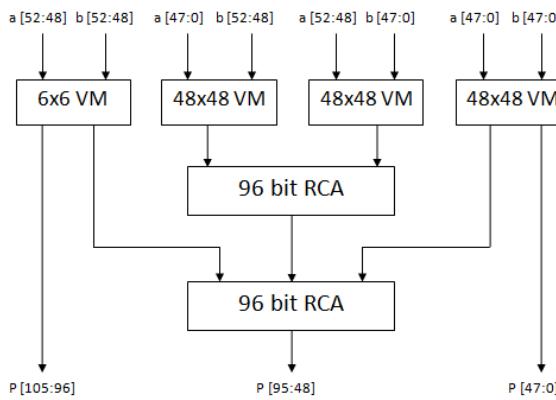


Fig.7: Proposed Double Precision 53x53 Vedic Multiplier

## VI. DESIGN OF EXPONENT AND SIGN BITS

The Exponent parts of two numbers to be multiplied are added using Ripple Carry Adders as shown in fig 8.

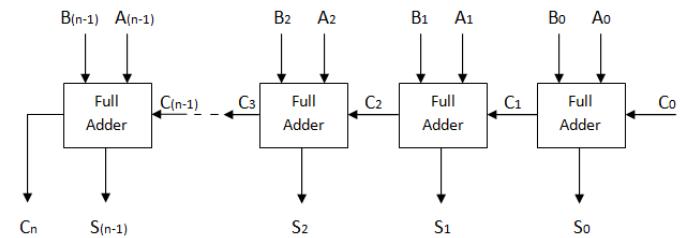


Fig.8: Ripple Carry Adder

The MSB bits of two numbers which are multiplied will be XORed to obtain Sign bit which represents whether the product is positive or negative.

## VII. SIMULATION RESULTS

The design is developed using Verilog HDL and Synthesized in Xilinx ISE 14.6 platform. The Block diagram, RTL schematic and the Simulation results of IEEE 754 single and double precision floating point multipliers are shown in Fig.9, Fig.10, Fig.11, Fig.12, Fig.13 and Fig.14.

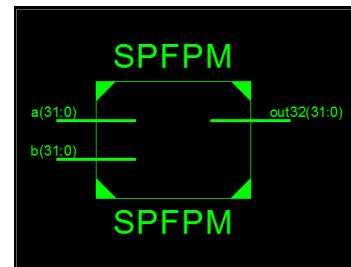


Fig.9: Block diagram of IEEE 754 Vedic Single precision floating point multiplier

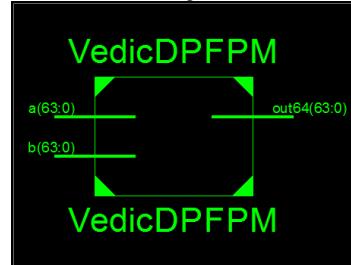


Fig.10: Block diagram of IEEE 754 Vedic Double precision floating point multiplier

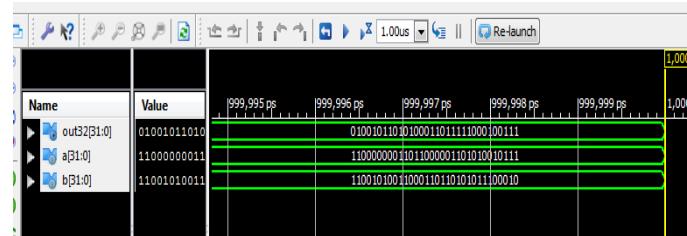


Fig.13: Simulation result of IEEE 754 Vedic Single Precision Floating point multiplier

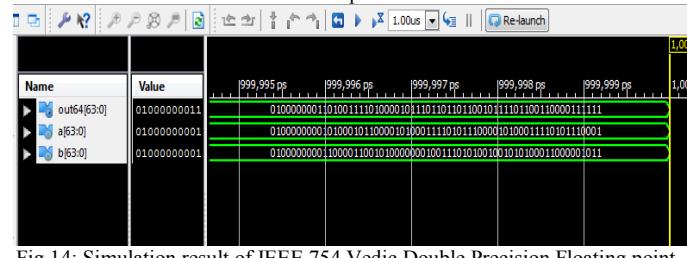


Fig.14: Simulation result of IEEE 754 Vedic Double Precision Floating point multiplier

Also, Fig.15 and Fig.16 shows the Simulation results of the 24x24 and 53x53 blocks Mantissa part of the IEEE 754 Single precision and Double precision floating point number Urdhva – Tiryagbhyam Vedic multiplier.

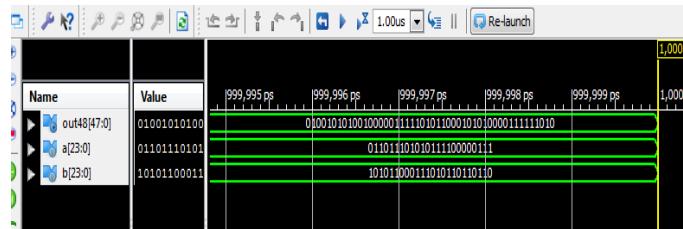


Fig.15: Simulation result of 24x24 Vedic Multiplier

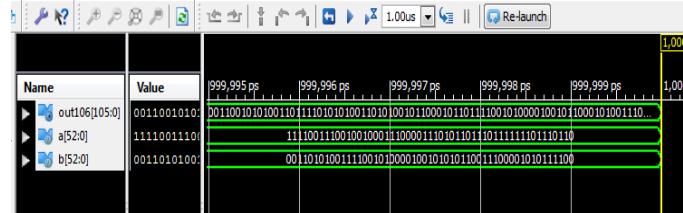


Fig.16: Simulation result of 53x53 Vedic Multiplier

The Device Utilization Summary and Timing Details of IEEE 754 Single and Double precision floating multiplier on Virtex VI FPGA are shown in Table 1.a, Table 1.b, and Table 2 respectively.

Table 1.a: Device Utilization Summary for SP

Logic utilization	Previous design	Used
No. of Slice LUTs	1018 / 2400 (42%)	705 / 465600 (1%)
No. of bonded IOBs	96 / 102 (94%)	96 / 240 (40%)

Table 1.b: Device Utilization Summary for DP

Logic utilization	Used	Available	Utilization
No. of slices LUTs	5153	204000	2%
No. of bonded IOBs	192	600	32%

Table 2: Timing Constraints

Delay	Previous design	Proposed design
SP FPM	49.497 ns	21.823 ns
DP FPM	-	45.169 ns

### VIII. SCOPE FOR FUTURE WORK

The different Vedic sutras can be used to develop a mantissa part. Also the design can be extended to the next format of 128 bits for designing floating point multiplier.

### IX. CONCLUSION

The paper proposes a floating point multiplier that supports the IEEE 754 Single and Double Precision Floating Point standard. The design concludes that use of Urdhva Tiryagbhyam Vedic Multiplier gives the complete multiplication calculation in one line, hence occupies less space which implies reduction in area. Also hardware components used are less and Operating speed is high due to crosswise and vertical calculation hence reduces complexity.

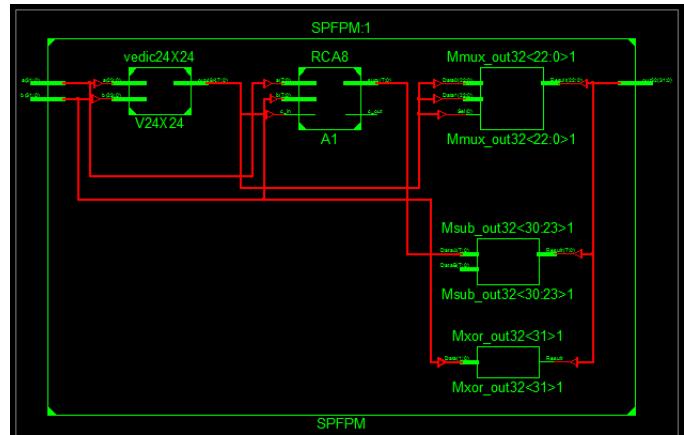


Fig.11: RTL schematic of IEEE 754 Vedic Single Precision Floating point multiplier

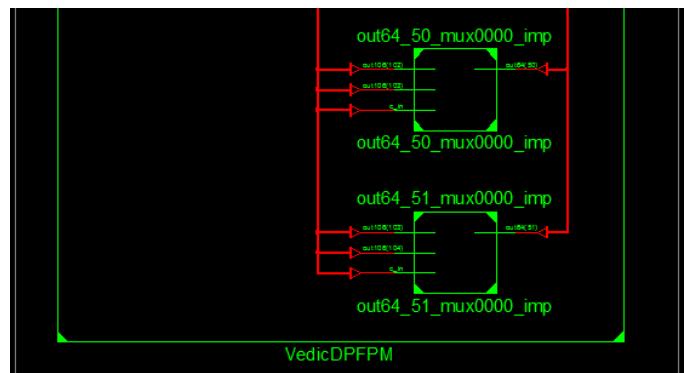
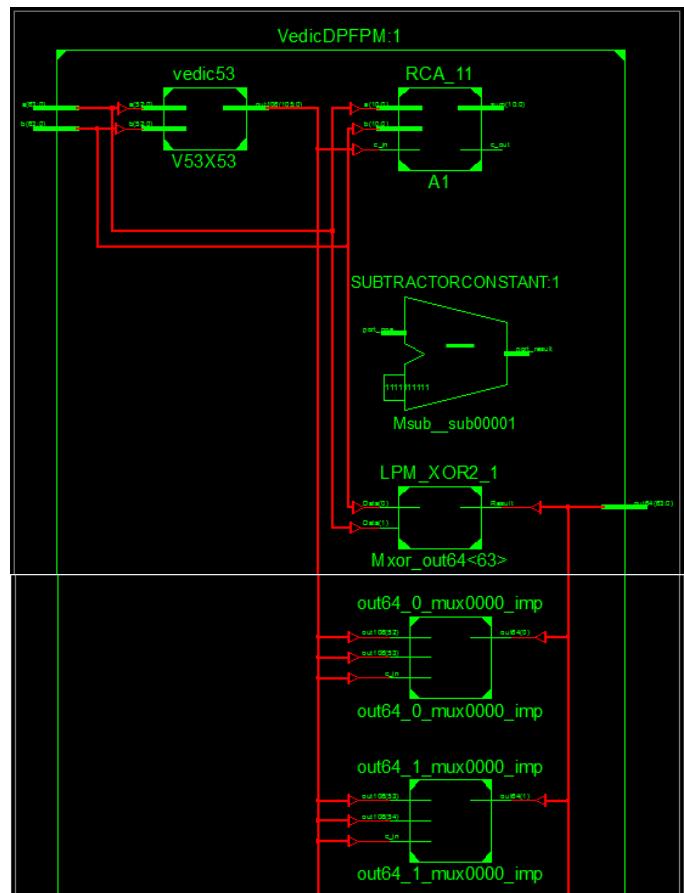


Fig.11: RTL schematic of IEEE 754 Vedic Double Precision Floating point multiplier

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