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PSoC 4100S Plus

PSoC 4 Registers Technical Reference Manual (TRM)

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Revision History **1901**

Register Mapping

The Register Mapping section discusses the registers and lists all the registers in mapping tables, in address order. For architecture details, see PSoC 4100S and 4100S Plus: PSoC 4 Architecture Technical Reference Manual (TRM).

Register General Conventions

The register conventions specific to this section and the Register Reference chapter are listed in this table.

Convention	Example	Description
‘x’ in a register name	ACBxxCR1	Multiple instances/address ranges of the same register
R	R : 00	Read register or bit(s)
W	W : 00	Write register or bit(s)
WOC	WOC:0	Write one to clear
WZC	WZC:0	Write zero to clear
RC	RC:0	Read to clear
WC	WC:0	Write to clear
NA	NA:000	Reserved
U	R:U	Undefined
00	RW : 00	Reset value is 0x00
XX	RW : XX	Register is not reset

Acronyms

This table lists the acronyms used in this document

Table 3-1. Acronyms

Symbol	Unit of Measure
ABUS	analog output bus
AC	alternating current
ADC	analog-to-digital converter
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
API	application programming interface
APOR	analog power-on reset
BC	broadcast clock
BOM	bill of materials
BR	bit rate
BRA	bus request acknowledge
BRQ	bus request
CAN	controller area network
CI	carry in
CMP	compare
CO	carry out

Table 3-1. Acronyms

Symbol	Unit of Measure
CPU	central processing unit
CRC	cyclic redundancy check
CSD	CapSense sigma delta
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
DI	digital or data input
DMA	direct memory access
DNL	differential nonlinearity
DO	digital or data output
DSI	digital signal interface
DSM	deep-sleep mode
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read only memory
EMIF	external memory interface
FB	feedback
FIFO	first in first out
FSR	full scale range
GPIO	general purpose I/O
HCI	host-controller interface
HFCLK	high-frequency clock
I^2C	inter-integrated circuit
IDE	integrated development environment
ILO	internal low-speed oscillator
IMO	internal main oscillator
INL	integral nonlinearity
I/O	input/output
IOR	I/O read
IOW	I/O write
IRES	initial power on reset
IRA	interrupt request acknowledge
IRQ	interrupt request
ISR	interrupt service routine
IVR	interrupt vector read
L2CAP	logical link control and adaptation protocol
LRb	last received bit
LRB	last received byte
LSb	least significant bit
LSB	least significant byte
LUT	lookup table
MISO	master-in-slave-out
MMIO	memory mapped input/output
MOSI	master-out-slave-in
MSb	most significant bit

Table 3-1. Acronyms

Symbol	Unit of Measure
MSB	most significant byte
PC	program counter
PCH	program counter high
PCL	program counter low
PD	power down
PGA	programmable gain amplifier
PM	power management
PMA	PSoC memory arbiter
POR	power-on reset
PPOR	precision power-on reset
PRS	pseudo random sequence
PSoC®	Programmable System-on-Chip
PSRR	power supply rejection ratio
PSSDC	power system sleep duty cycle
PWM	pulse width modulator
RAM	random-access memory
RETI	return from interrupt
RF	radio frequency
ROM	read only memory
RW	read/write
SAR	successive approximation register
SC	switched capacitor
SCB	serial communication block
SIE	serial interface engine
SIO	special I/O
SE0	single-ended zero
SNR	signal-to-noise ratio
SOF	start of frame
SOI	start of instruction
SP	stack pointer
SPD	sequential phase detector
SPI	serial peripheral interconnect
SPIM	serial peripheral interconnect master
SPIS	serial peripheral interconnect slave
SRAM	static random-access memory
SROM	supervisory read only memory
SSADC	single slope ADC
SSC	supervisory system call
SYSCLK	system clock
SWD	single wire debug
TC	terminal count
TD	transaction descriptors
UART	universal asynchronous receiver/transmitter
UDB	universal digital block

Table 3-1. Acronyms

Symbol	Unit of Measure
USB	universal serial bus
USBIO	USB I/O
WCO	watch crystal oscillator
WDT	watchdog timer
WDR	watchdog reset
XRES	external reset
XRES_N	external reset, active low

1 Controller Area Network Registers

This section discusses the Controller Area Network (CAN) registers. It lists all the registers in mapping tables, in address order.

1.1 Register Details

Register Name	Address
CAN_INT_STATUS	0x402E0000
CAN_INT_EBL	0x402E0004
CAN_BUFFER_STATUS	0x402E0008
CAN_ERROR_STATUS	0x402E000C
CAN_COMMAND	0x402E0010
CAN_CONFIG	0x402E0014
CAN_ECR	0x402E0018
CAN_CNTL	0x402E0400
CAN_TTCAN_COUNTER	0x402E0404
CAN_TTCAN_COMPARE	0x402E0408
CAN_TTCAN_CAPTURE	0x402E040C
CAN_TTCAN_TIMING	0x402E0410
CAN_INTR_CAN	0x402E0414
CAN_INTR_CAN_SET	0x402E0418
CAN_INTR_CAN_MASK	0x402E041C
CAN_INTR_CAN_MASKED	0x402E0420

1.1.1 CAN_INT_STATUS

Interrupt Status

Address: 0x402E0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	None	
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	None	
Name	FORM_ERR	ACK_ERR	STUFF_ERR	BIT_ERR	OVR_LOAD	ARB_LOSS	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	SST_FAIL-URE	STUCK_AT_0	RTR_MSG	RX_MSG	TX_MSG	RX_MS-G_LOSS	BUS_OFF	CRC_ERR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	SST_FAILURE	Single shot transmission failure 0: Normal operation 1: A buffer set for single shot transmission experienced an arbitration loss or a bus error during transmission The sst_failure interrupt is set as well when the CAN controller is being stopped while an SST message is in the transmit buffer. user should transmit or remove respective SST messages before stopping the IP, to avoid triggering SST_FAILURE after writing COMMAND.RUN=0. Default Value: 0
14	STUCK_AT_0	Stuck at dominant error 0: Normal Operation 1: Indicates if the rx input remains stuack at 0 (dominant level) for more than 16 consecutive bit times. The "stuck at 0" condition is checked, only when COMMAND.RUN is set Default Value: 0

(continued)

13	RTR_MSG	RTR auto-reply message sent 0: Normal operation 1: Indicates that a RTR auto-reply message was sent Default Value: 0
12	RX_MSG	Indicates that a message was received 0: Normal operation 1: A new message was successfully received and stored in a receive buffer which has its RxIntEBL flag asserted. Default Value: 0
11	TX_MSG	Indicates that a message was sent 0: Normal operation 1: A message was successfully sent from a transmit buffer which has its TxIntEbl flag asserted. Default Value: 0
10	RX_MSG_LOSS	when a new message arrives, but the RxMessage flag MSG_AV is set and LINK_FLAG is not set, RX_MSG_LOSS is set, and the new message is discarded. Default Value: 0
9	BUS_OFF	The CAN has reached the bus off state Default Value: 0
8	CRC_ERR	A CAN CRC error was detected Default Value: 0
7	FORM_ERR	A CAN message format error was detected please ignore this interrupt, when ERROR_STATUS.ERROR_STATE=2'B1x Default Value: 0
6	ACK_ERR	An CAN message acknowledge error was detected Default Value: 0
5	STUFF_ERR	A bit stuffing error was detected Default Value: 0
4	BIT_ERR	A bit error was detected Default Value: 0
3	OVR_LOAD	An overload frame was received, or reactive overload frame condition is detected (ISO-11898-1 section 10.11) Default Value: 0
2	ARB_LOSS	The arbitration was lost while sending a message Default Value: 0

1.1.2 CAN_INT_EBL

Interrupt Enable

Address: 0x402E0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	None	RW
HW Access	R	R	R	R	R	R	None	R
Name	FORM_ER-R_ENBL	ACK_ER-R_ENBL	STUFF_ER-R_ENBL	BIT_ER-R_ENBL	OVR_-LOAD_EN-BL	AR-B_LOSS_ENBL	None	GLOBAL_INT_ENBL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SST_FAIL-URE_ENBL	STUCK_AT_0_ENBL	RTR_MS-G_ENBL	RX_MS-G_ENBl	TX_MS-G_ENBL	RX_MS-G_LOSS	BUS_OFF_ENBL	CRC_ER-R_ENBL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	SST_FAILURE_ENBL	See description in INT_STATUS Default Value: 0
14	STUCK_AT_0_ENBL	See description in INT_STATUS Default Value: 0
13	RTR_MSG_ENBL	See description in INT_STATUS Default Value: 0
12	RX_MSG_ENBl	See description in INT_STATUS Default Value: 0
11	TX_MSG_ENBL	See description in INT_STATUS Default Value: 0
10	RX_MSG_LOSS	See description in INT_STATUS Default Value: 0
9	BUS_OFF_ENBL	See description in INT_STATUS Default Value: 0

(continued)

8	CRC_ERR_ENBL	See description in INT_STATUS Default Value: 0
7	FORM_ERR_ENBL	See description in INT_STATUS Default Value: 0
6	ACK_ERR_ENBL	See description in INT_STATUS Default Value: 0
5	STUFF_ERR_ENBL	See description in INT_STATUS Default Value: 0
4	BIT_ERR_ENBL	See description in INT_STATUS Default Value: 0
3	OVR_LOAD_ENBL	See description in INT_STATUS Default Value: 0
2	ARB_LOSS_ENBL	See description in INT_STATUS Default Value: 0
0	GLOBAL_INT_ENBL	global interrupt enable flag 0: All interrupts are disabled 1: Enabled interrupt sources are available Default Value: 0

1.1.3 CAN_BUFFER_STATUS

RxMessage and TxMessage Buffer Status

Address: 0x402E0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	RX7_MS-G_AV	RX6_MS-G_AV	RX5_MS-G_AV	RX4_MS-G_AV	RX3_MS-G_AV	RX2_MS-G_AV	RX1_MS-G_AV	RX0_MS-G_AV

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	RX15_MS-G_AV	RX14_MS-G_AV	RX13_MS-G_AV	RX12_MS-G_AV	RX11_MS-G_AV	RX10_MS-G_AV	RX9_MS-G_AV	RX8_MS-G_AV

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	TX-7_REQ_PEND	TX-6_REQ_PEND	TX-5_REQ_PEND	TX-4_REQ_PEND	TX-3_REQ_PEND	TX-2_REQ_PEND	TX-1_REQ_PEND	TX-0_REQ_PEND

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	TX7_REQ_PEND	TxMessage Buffer Status Default Value: 0
22	TX6_REQ_PEND	TxMessage Buffer Status Default Value: 0
21	TX5_REQ_PEND	TxMessage Buffer Status Default Value: 0
20	TX4_REQ_PEND	TxMessage Buffer Status Default Value: 0
19	TX3_REQ_PEND	TxMessage Buffer Status Default Value: 0
18	TX2_REQ_PEND	TxMessage Buffer Status Default Value: 0

(continued)

17	TX1_REQ_PEND	TxMessage Buffer Status Default Value: 0
16	TX0_REQ_PEND	TxMessage Buffer Status Default Value: 0
15	RX15_MSG_AV	RxMessage Buffer Status Default Value: 0
14	RX14_MSG_AV	RxMessage Buffer Status Default Value: 0
13	RX13_MSG_AV	RxMessage Buffer Status Default Value: 0
12	RX12_MSG_AV	RxMessage Buffer Status Default Value: 0
11	RX11_MSG_AV	RxMessage Buffer Status Default Value: 0
10	RX10_MSG_AV	RxMessage Buffer Status Default Value: 0
9	RX9_MSG_AV	RxMessage Buffer Status Default Value: 0
8	RX8_MSG_AV	RxMessage Buffer Status Default Value: 0
7	RX7_MSG_AV	RxMessage Buffer Status Default Value: 0
6	RX6_MSG_AV	RxMessage Buffer Status Default Value: 0
5	RX5_MSG_AV	RxMessage Buffer Status Default Value: 0
4	RX4_MSG_AV	RxMessage Buffer Status Default Value: 0
3	RX3_MSG_AV	RxMessage Buffer Status Default Value: 0
2	RX2_MSG_AV	RxMessage Buffer Status Default Value: 0
1	RX1_MSG_AV	RxMessage Buffer Status Default Value: 0
0	RX0_MSG_AV	RxMessage Buffer Status Default Value: 0

1.1.4 CAN_ERROR_STATUS

CAN Error Status

Address: 0x402E000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TX_ERR_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RX_ERR_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R	R	R	
HW Access	None				RW	RW	RW	
Name	None [23:20]				RXGTE96	TXGTE96	ERROR_STATE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	RXGTE96	The Rx error counter is greater or equal 96 Default Value: 0
18	TXGTE96	The Tx error counter is greater or equal 96 Default Value: 0
17 : 16	ERROR_STATE	The error state of the CAN node: "00": error active (normal operation) "01": error passive "1x": bus off Default Value: 0
15 : 8	RX_ERR_CNT	The receive error counter according to the CAN 2.0 specification. When in bus-off state, this counter is used to count 128 groups of 11 recessive bits. it is fixed at 255 Default Value: 0

(continued)

7 : 0	TX_ERR_CNT	The transmitter error counter according to the CAN standard. When it is greater than 255, it is fixed at 255 Default Value: 0

1.1.5 CAN_COMMAND

CAN Command Register

Address: 0x402E0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				SRAM_TEST	LOOP-BACK_TEST	LISTEN	RUN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	IP_REV_NUMBER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	R				R			
Name	IP_MAJOR_VERSION [31:28]				IP_MINOR_VERSION [27:24]			

Bits	Name	Description
31 : 28	IP_MAJOR_VERSION	IP Major Version Number Default Value: 3
27 : 24	IP_MINOR_VERSION	IP Minor Version Number Default Value: 0
23 : 16	IP_REV_NUMBER	IP Revision Number Default Value: 0
3	SRAM_TEST	SRAM test mode "0": Normal operation "1": Enable SRAM test mode it can be set, only when the IP is stopped (COMMAND.RUN=0, and really finished transition from run mode), this mode will not be used, so it should never be set. Default Value: 0

(continued)

2	LOOPBACK_TEST	TEST_MODE[2]. With TEST_MODE[2:1], 00: normal operation 01: Listen-only mode, The output is held at "R" level. The CANmodule-III is only listening. 10: external loopback mode 11: internal loopback mode Default Value: 0
1	LISTEN	TEST_MODE[1] Default Value: 0
0	RUN	Run/Stop mode: "0": Sets the CAN controller into stop mode. Stop mode can be granted only in "bus idle" field Returns "0" when stopped. "1": Sets the CAN controller into run mode. Returns "1" when running. Default Value: 0

1.1.6 CAN_CONFIG

CAN Configuration

Address: 0x402E0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW	RW		RW	RW
HW Access	R			R	R		R	R
Name	CFG_TSEG2 [7:5]			AUTO_RE-START	CFG_SJW [3:2]		SAM-PLING_-MODE	EDGE_-MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW	RW			
HW Access	None	R	R	R	R			
Name	None	ECR_-MODE	SWAP_EN-DIAN	CFG_ARBI-TER	CFG_TSEG1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CFG_BITRATE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	CFG_BITRATE [30:24]						

Bits	Name	Description
30 : 16	CFG_BITRATE	Prescaler for generating the time quantum which defines the TQ: 0: One time quantum equals 1 clock cycle 1: One time quantum equals 2 clock cycles ... 32767: One time quantum equals 32768 clock cycles Default Value: 0
14	ECR_MODE	Error Capture mode 0: Free running: The ECR register shows the current bit position within the CAN frame 1: Capture mode: The ecr register shows the bit position and type of the last captured CAN error. Default Value: 0

(continued)

13	SWAP_ENDIAN	Swap Endian - the byte position of the CAN receive and transmit data fields can be modified to match the endian setting of the processor or the used CAN protocol 0: CAN data byte position is not swapped (big endian) 1: CAN data byte position is swapped (little endian) Default Value: 0
12	CFG_ARBITER	Transmit buffer arbiter 0: Round robin arbitration 1: Fixed priority arbitration Default Value: 0
11 : 8	CFG_TSEG1	Time segment 1 Length of the first time segment: tseg1 = cfg_tseg1 + 1 Time segment 1 includes the propagation time. cfg_tseg1=0 and cfg_tseg1=1 are not allowed. Default Value: 0
7 : 5	CFG_TSEG2	Time segment 2 Length of the second time segment: tseg2 = cfg_tseg2 + 1 cfg_tseg2=0 is not allowed; cfg_tseg2=1 is only allowed in direct sampling mode. Default Value: 0
4	AUTO_RESTART	0: After bus-off, the CAN core must be restarted by setting COMMAND.RUN register. This is the recommended setting. 1: After bus-off, the CAN core is restarting automatically after 128 groups of 11 recessive bits Default Value: 0
3 : 2	CFG_SJW	Synchronization jump width - 1 sjw = tseg1 and sjw = tseg2 Default Value: 0
1	SAMPLING_MODE	CAN bus bit sampling 0: One sampling point is used in the receiver path 1: 3 sampling points with majority decision are used Default Value: 0
0	EDGE_MODE	CAN bus synchronization logic 0: Edge from R to D is used for synchronization 1: Both edges are used Note, only R to D edge shall be used for synchronization per ISO-11898-1 spec, so this bit should always be set 0 (by default) Default Value: 0

1.1.7 CAN_ECR

Error Capture Register

Address: 0x402E0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R	R	R			RW
HW Access	RW		RW	RW	RW			RW
Name	BIT [7:6]		TX_MODE	RX_MODE	ERROR_TYPE [3:1]			ECR_STA-TUS

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	Field [15:12]				BIT [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							Field

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16 : 12	Field	Field - 0x00 : Stopped 0x01 : Synchronize 0x05 : Interframe 0x06 : Bus Idle 0x07 : Start of Frame 0x08 : Arbitration 0x09 : Control 0x0A : Data 0x0B : CRC 0x0C : ACK 0x0D : End of frame 0x10 : Error flag 0x11 : Error echo 0x12 : Error delimiter 0x18 : Overload flag 0x19 : Overload echo 0x1A : Overload delimiter Others : N/A Default Value: 0

(continued)

11 : 6	BIT	Bit number inside of Field Default Value: 0
5	TX_MODE	TX Mode - 0: No status 1: CAN Controller is transmitter Default Value: 0
4	RX_MODE	RX Mode - 0: No status 1: CAN Controller is receiver Default Value: 0
3 : 1	ERROR_TYPE	Error type - 000 : Arbitration loss 001 : Bit Error 010 : Bit Stuffing Error 011 : Acknowledge Error 100 : Form Error 101 : CRC Error Others : N/A Default Value: 0
0	ECR_STATUS	ECR STATUS - 0: ECR register captured an error, or it is in free running mode 1: ECR register is armed Default Value: 0

1.1.8 CAN_CNTL

Control

Address: 0x402E0400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TT_EN-ABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	IP_ENABLE	None [30:24]						

Bits	Name	Description
31	IP_ENABLE	IP Enable/Disable 0=IP is disabled/reset 1=IP is enabled/running Default Value: 0
0	TT_ENABLE	TTCAN enable/disable 0=TTCAN is disabled; Interrupt_can is sourced from 3PIP. INT_EBL.GLOBAL_INT_ENBL & (INT_EBL[i] & INT_STATUS[i]) 1=TTCAN is enabled; Interrupt_can is sourced from INTR_CAN_MASKED. Default Value: 0

1.1.9 CAN_TTCAN_COUNTER

TTCAN Level1 16-Bit local time counter

Address: 0x402E0404

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	LOCAL_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	LOCAL_TIME [31:24]							

Bits	Name	Description
31 : 16	LOCAL_TIME	Bit time counter in TTCAN level 1 Default Value: 0

1.1.10 CAN_TTCAN_COMPARE

TTCAN Level1 compare configuration

Address: 0x402E0408

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TIME_MARK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TIME_MARK [31:24]							

Bits	Name	Description
31 : 16	TIME_MARK	compare target, when TTCAN_COUNTER.LOCAL_TIME counts to TT_COMPARE, INTR_CAN.TT_COMPARE will be set Default Value: 65535

1.1.11 CAN_TTCAN_CAPTURE

TTCAN Level1 capture configuration

Address: 0x402E040C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SYNC_MARK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SYNC_MARK [31:24]							

Bits	Name	Description
31 : 16	SYNC_MARK	copy TTCAN_COUNTER.LOCAL_TIME to TTCAN_CAPTURE.SYNC_MARK, when SOF detected. when new event triggers, new LOCAL_TIME value will overwrite previous SYNC_MARK value Default Value: 0

1.1.12 CAN_TTCAN_TIMING

TTCAN Level1 timing configuration, duplicate of CONFIG fields

Address: 0x402E0410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			None			RW	None
HW Access	R			None			R	None
Name	CFG_TSEG2 [7:5]			None [4:2]			SAM-PLING_-MODE	None

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				CFG_TSEG1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CFG_BITRATE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	CFG_BITRATE [30:24]						

Bits	Name	Description
30 : 16	CFG_BITRATE	Prescaler for generating the time quantum which defines the TQ: 0: One time quantum equals 1 clock cycle 1: One time quantum equals 2 clock cycles ... 32767: One time quantum equals 32768 clock cycles Default Value: 0
11 : 8	CFG_TSEG1	Time segment 1 Length of the first time segment: tseg1 = cfg_tseg1 + 1 Time segment 1 includes the propagation time. cfg_tseg1=0 and cfg_tseg1=1 are not allowed. Default Value: 0

(continued)

7 : 5	CFG_TSEG2	Time segment 2 Length of the second time segment: tseg2 = cfg_tseg2 + 1 cfg_tseg2=0 is not allowed; cfg_tseg2=1 is only allowed in direct sampling mode. Default Value: 0
1	SAMPLING_MODE	CAN bus bit sampling 0: One sampling point is used in the receiver path 1: 3 sampling points with majority decision are used Default Value: 0

1.1.13 CAN_INTR_CAN

CAN Interrupt Cause (TTCAN + INT_STATUS Or)

Address: 0x402E0414

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [7:3]					TT_CAP-TURE	TT_COM-PARE	INT_STA-TUS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	TT_CAPTURE	Triggers when LOCAL_TIME is saved to TT_CAPTURE, on SOF detection Default Value: 0
1	TT_COMPARE	Triggers when LOCAL_TIME is equal to TT_COMPARE Default Value: 0
0	INT_STATUS	Triggers when any enabled (INT_EBL) interrupt are set in INT_STATUS Default Value: 0

1.1.14 CAN_INTR_CAN_SET

CAN Interrupt Set (TTCAN + INT_STATUS Or)

Address: 0x402E0418

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					TT_CAP-TURE	TT_COM-PARE	INT_STA-TUS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	TT_CAPTURE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	TT_COMPARE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	INT_STATUS	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

1.1.15 CAN_INTR_CAN_MASK

CAN Interrupt Mask (TTCAN + INT_STATUS Or)

Address: 0x402E041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					TT_CAP-TURE	TT_COM-PARE	INT_STA-TUS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	TT_CAPTURE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	TT_COMPARE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	INT_STATUS	Mask bit for corresponding bit in interrupt request register. Default Value: 0

1.1.16 CAN_INTR_CAN_MASKED

Can Interrupt Masked (TTCAN + INT_STATUS Or)

Address: 0x402E0420

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					TT_CAP-TURE	TT_COM-PARE	INT_STA-TUS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	TT_CAPTURE	Logical and of corresponding request and mask bits. Default Value: 0
1	TT_COMPARE	Logical and of corresponding request and mask bits. Default Value: 0
0	INT_STATUS	Logical and of corresponding request and mask bits. Default Value: 0

2 CAN Receive Registers

This section discusses the CAN Receive Registers (CAN_RX) registers. It lists all the registers in mapping tables, in address order.

2.1 Register Details

Register Name	Address
CAN_CAN_RX0_CONTROL	0x402E00A0
CAN_CAN_RX0_ID	0x402E00A4
CAN_CAN_RX0_DATA_HIGH	0x402E00A8
CAN_CAN_RX0_DATA_LOW	0x402E00AC
CAN_CAN_RX0_AMR	0x402E00B0
CAN_CAN_RX0_ACR	0x402E00B4
CAN_CAN_RX0_AMR_DATA	0x402E00B8
CAN_CAN_RX0_ACR_DATA	0x402E00BC
CAN_CAN_RX1_CONTROL	0x402E00C0
CAN_CAN_RX1_ID	0x402E00C4
CAN_CAN_RX1_DATA_HIGH	0x402E00C8
CAN_CAN_RX1_DATA_LOW	0x402E00CC
CAN_CAN_RX1_AMR	0x402E00D0
CAN_CAN_RX1_ACR	0x402E00D4
CAN_CAN_RX1_AMR_DATA	0x402E00D8
CAN_CAN_RX1_ACR_DATA	0x402E00DC
CAN_CAN_RX2_CONTROL	0x402E00E0
CAN_CAN_RX2_ID	0x402E00E4
CAN_CAN_RX2_DATA_HIGH	0x402E00E8
CAN_CAN_RX2_DATA_LOW	0x402E00EC
CAN_CAN_RX2_AMR	0x402E00F0
CAN_CAN_RX2_ACR	0x402E00F4
CAN_CAN_RX2_AMR_DATA	0x402E00F8
CAN_CAN_RX2_ACR_DATA	0x402E00FC
CAN_CAN_RX3_CONTROL	0x402E0100
CAN_CAN_RX3_ID	0x402E0104
CAN_CAN_RX3_DATA_HIGH	0x402E0108

Register Name	Address
CAN_CAN_RX3_DATA_LOW	0x402E010C
CAN_CAN_RX3_AMR	0x402E0110
CAN_CAN_RX3_ACR	0x402E0114
CAN_CAN_RX3_AMR_DATA	0x402E0118
CAN_CAN_RX3_ACR_DATA	0x402E011C
CAN_CAN_RX4_CONTROL	0x402E0120
CAN_CAN_RX4_ID	0x402E0124
CAN_CAN_RX4_DATA_HIGH	0x402E0128
CAN_CAN_RX4_DATA_LOW	0x402E012C
CAN_CAN_RX4_AMR	0x402E0130
CAN_CAN_RX4_ACR	0x402E0134
CAN_CAN_RX4_AMR_DATA	0x402E0138
CAN_CAN_RX4_ACR_DATA	0x402E013C
CAN_CAN_RX5_CONTROL	0x402E0140
CAN_CAN_RX5_ID	0x402E0144
CAN_CAN_RX5_DATA_HIGH	0x402E0148
CAN_CAN_RX5_DATA_LOW	0x402E014C
CAN_CAN_RX5_AMR	0x402E0150
CAN_CAN_RX5_ACR	0x402E0154
CAN_CAN_RX5_AMR_DATA	0x402E0158
CAN_CAN_RX5_ACR_DATA	0x402E015C
CAN_CAN_RX6_CONTROL	0x402E0160
CAN_CAN_RX6_ID	0x402E0164
CAN_CAN_RX6_DATA_HIGH	0x402E0168
CAN_CAN_RX6_DATA_LOW	0x402E016C
CAN_CAN_RX6_AMR	0x402E0170
CAN_CAN_RX6_ACR	0x402E0174
CAN_CAN_RX6_AMR_DATA	0x402E0178
CAN_CAN_RX6_ACR_DATA	0x402E017C
CAN_CAN_RX7_CONTROL	0x402E0180
CAN_CAN_RX7_ID	0x402E0184
CAN_CAN_RX7_DATA_HIGH	0x402E0188
CAN_CAN_RX7_DATA_LOW	0x402E018C
CAN_CAN_RX7_AMR	0x402E0190
CAN_CAN_RX7_ACR	0x402E0194
CAN_CAN_RX7_AMR_DATA	0x402E0198
CAN_CAN_RX7_ACR_DATA	0x402E019C
CAN_CAN_RX8_CONTROL	0x402E01A0
CAN_CAN_RX8_ID	0x402E01A4
CAN_CAN_RX8_DATA_HIGH	0x402E01A8
CAN_CAN_RX8_DATA_LOW	0x402E01AC
CAN_CAN_RX8_AMR	0x402E01B0

Register Name	Address
CAN_CAN_RX8_ACR	0x402E01B4
CAN_CAN_RX8_AMR_DATA	0x402E01B8
CAN_CAN_RX8_ACR_DATA	0x402E01BC
CAN_CAN_RX9_CONTROL	0x402E01C0
CAN_CAN_RX9_ID	0x402E01C4
CAN_CAN_RX9_DATA_HIGH	0x402E01C8
CAN_CAN_RX9_DATA_LOW	0x402E01CC
CAN_CAN_RX9_AMR	0x402E01D0
CAN_CAN_RX9_ACR	0x402E01D4
CAN_CAN_RX9_AMR_DATA	0x402E01D8
CAN_CAN_RX9_ACR_DATA	0x402E01DC
CAN_CAN_RX10_CONTROL	0x402E01E0
CAN_CAN_RX10_ID	0x402E01E4
CAN_CAN_RX10_DATA_HIGH	0x402E01E8
CAN_CAN_RX10_DATA_LOW	0x402E01EC
CAN_CAN_RX10_AMR	0x402E01F0
CAN_CAN_RX10_ACR	0x402E01F4
CAN_CAN_RX10_AMR_DATA	0x402E01F8
CAN_CAN_RX10_ACR_DATA	0x402E01FC
CAN_CAN_RX11_CONTROL	0x402E0200
CAN_CAN_RX11_ID	0x402E0204
CAN_CAN_RX11_DATA_HIGH	0x402E0208
CAN_CAN_RX11_DATA_LOW	0x402E020C
CAN_CAN_RX11_AMR	0x402E0210
CAN_CAN_RX11_ACR	0x402E0214
CAN_CAN_RX11_AMR_DATA	0x402E0218
CAN_CAN_RX11_ACR_DATA	0x402E021C
CAN_CAN_RX12_CONTROL	0x402E0220
CAN_CAN_RX12_ID	0x402E0224
CAN_CAN_RX12_DATA_HIGH	0x402E0228
CAN_CAN_RX12_DATA_LOW	0x402E022C
CAN_CAN_RX12_AMR	0x402E0230
CAN_CAN_RX12_ACR	0x402E0234
CAN_CAN_RX12_AMR_DATA	0x402E0238
CAN_CAN_RX12_ACR_DATA	0x402E023C
CAN_CAN_RX13_CONTROL	0x402E0240
CAN_CAN_RX13_ID	0x402E0244
CAN_CAN_RX13_DATA_HIGH	0x402E0248
CAN_CAN_RX13_DATA_LOW	0x402E024C
CAN_CAN_RX13_AMR	0x402E0250
CAN_CAN_RX13_ACR	0x402E0254
CAN_CAN_RX13_AMR_DATA	0x402E0258

Register Name	Address
CAN_CAN_RX13_ACR_DATA	0x402E025C
CAN_CAN_RX14_CONTROL	0x402E0260
CAN_CAN_RX14_ID	0x402E0264
CAN_CAN_RX14_DATA_HIGH	0x402E0268
CAN_CAN_RX14_DATA_LOW	0x402E026C
CAN_CAN_RX14_AMR	0x402E0270
CAN_CAN_RX14_ACR	0x402E0274
CAN_CAN_RX14_AMR_DATA	0x402E0278
CAN_CAN_RX14_ACR_DATA	0x402E027C
CAN_CAN_RX15_CONTROL	0x402E0280
CAN_CAN_RX15_ID	0x402E0284
CAN_CAN_RX15_DATA_HIGH	0x402E0288
CAN_CAN_RX15_DATA_LOW	0x402E028C
CAN_CAN_RX15_AMR	0x402E0290
CAN_CAN_RX15_ACR	0x402E0294
CAN_CAN_RX15_AMR_DATA	0x402E0298
CAN_CAN_RX15_ACR_DATA	0x402E029C

2.1.1 CAN_CAN_RX0_CONTROL

RxMessage Buffer control/command

Address: 0x402E00A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.2 CAN_CAN_RX0_ID

Identifier

Address: 0x402E00A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.3 CAN_CAN_RX0_DATA_HIGH

RxMessage Data high

Address: 0x402E00A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.4 CAN_CAN_RX0_DATA_LOW

RxMessage Data low

Address: 0x402E00AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.5 CAN_CAN_RX0_AMR

Acceptance Mask Register

Address: 0x402E00B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.6 CAN_CAN_RX0_ACR

Acceptance Code Register

Address: 0x402E00B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.7 CAN_CAN_RX0_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E00B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.8 CAN_CAN_RX0_ACR_DATA

Acceptance Code Register Data

Address: 0x402E00BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.9 CAN_CAN_RX1_CONTROL

RxMessage Buffer control/command

Address: 0x402E00C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.10 CAN_CAN_RX1_ID

Identifier

Address: 0x402E00C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.11 CAN_CAN_RX1_DATA_HIGH

RxMessage Data high

Address: 0x402E00C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.12 CAN_CAN_RX1_DATA_LOW

RxMessage Data low

Address: 0x402E00CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.13 CAN_CAN_RX1_AMR

Acceptance Mask Register

Address: 0x402E00D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.14 CAN_CAN_RX1_ACR

Acceptance Code Register

Address: 0x402E00D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.15 CAN_CAN_RX1_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E00D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.16 CAN_CAN_RX1_ACR_DATA

Acceptance Code Register Data

Address: 0x402E00DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.17 CAN_CAN_RX2_CONTROL

RxMessage Buffer control/command

Address: 0x402E00E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.18 CAN_CAN_RX2_ID

Identifier

Address: 0x402E00E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.19 CAN_CAN_RX2_DATA_HIGH

RxMessage Data high

Address: 0x402E00E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.20 CAN_CAN_RX2_DATA_LOW

RxMessage Data low

Address: 0x402E00EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.21 CAN_CAN_RX2_AMR

Acceptance Mask Register

Address: 0x402E00F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.22 CAN_CAN_RX2_ACR

Acceptance Code Register

Address: 0x402E00F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.23 CAN_CAN_RX2_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E00F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.24 CAN_CAN_RX2_ACR_DATA

Acceptance Code Register Data

Address: 0x402E00FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.25 CAN_CAN_RX3_CONTROL

RxMessage Buffer control/command

Address: 0x402E0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.26 CAN_CAN_RX3_ID

Identifier

Address: 0x402E0104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.27 CAN_CAN_RX3_DATA_HIGH

RxMessage Data high

Address: 0x402E0108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.28 CAN_CAN_RX3_DATA_LOW

RxMessage Data low

Address: 0x402E010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.29 CAN_CAN_RX3_AMR

Acceptance Mask Register

Address: 0x402E0110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.30 CAN_CAN_RX3_ACR

Acceptance Code Register

Address: 0x402E0114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.31 CAN_CAN_RX3_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E0118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.32 CAN_CAN_RX3_ACR_DATA

Acceptance Code Register Data

Address: 0x402E011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.33 CAN_CAN_RX4_CONTROL

RxMessage Buffer control/command

Address: 0x402E0120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.34 CAN_CAN_RX4_ID

Identifier

Address: 0x402E0124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.35 CAN_CAN_RX4_DATA_HIGH

RxMessage Data high

Address: 0x402E0128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.36 CAN_CAN_RX4_DATA_LOW

RxMessage Data low

Address: 0x402E012C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.37 CAN_CAN_RX4_AMR

Acceptance Mask Register

Address: 0x402E0130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.38 CAN_CAN_RX4_ACR

Acceptance Code Register

Address: 0x402E0134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.39 CAN_CAN_RX4_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E0138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.40 CAN_CAN_RX4_ACR_DATA

Acceptance Code Register Data

Address: 0x402E013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.41 CAN_CAN_RX5_CONTROL

RxMessage Buffer control/command

Address: 0x402E0140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.42 CAN_CAN_RX5_ID

Identifier

Address: 0x402E0144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.43 CAN_CAN_RX5_DATA_HIGH

RxMessage Data high

Address: 0x402E0148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.44 CAN_CAN_RX5_DATA_LOW

RxMessage Data low

Address: 0x402E014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.45 CAN_CAN_RX5_AMR

Acceptance Mask Register

Address: 0x402E0150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.46 CAN_CAN_RX5_ACR

Acceptance Code Register

Address: 0x402E0154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.47 CAN_CAN_RX5_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E0158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.48 CAN_CAN_RX5_ACR_DATA

Acceptance Code Register Data

Address: 0x402E015C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.49 CAN_CAN_RX6_CONTROL

RxMessage Buffer control/command

Address: 0x402E0160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.50 CAN_CAN_RX6_ID

Identifier

Address: 0x402E0164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.51 CAN_CAN_RX6_DATA_HIGH

RxMessage Data high

Address: 0x402E0168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.52 CAN_CAN_RX6_DATA_LOW

RxMessage Data low

Address: 0x402E016C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.53 CAN_CAN_RX6_AMR

Acceptance Mask Register

Address: 0x402E0170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.54 CAN_CAN_RX6_ACR

Acceptance Code Register

Address: 0x402E0174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.55 CAN_CAN_RX6_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E0178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.56 CAN_CAN_RX6_ACR_DATA

Acceptance Code Register Data

Address: 0x402E017C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.57 CAN_CAN_RX7_CONTROL

RxMessage Buffer control/command

Address: 0x402E0180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.58 CAN_CAN_RX7_ID

Identifier

Address: 0x402E0184

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.59 CAN_CAN_RX7_DATA_HIGH

RxMessage Data high

Address: 0x402E0188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.60 CAN_CAN_RX7_DATA_LOW

RxMessage Data low

Address: 0x402E018C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.61 CAN_CAN_RX7_AMR

Acceptance Mask Register

Address: 0x402E0190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.62 CAN_CAN_RX7_ACR

Acceptance Code Register

Address: 0x402E0194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.63 CAN_CAN_RX7_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E0198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.64 CAN_CAN_RX7_ACR_DATA

Acceptance Code Register Data

Address: 0x402E019C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.65 CAN_CAN_RX8_CONTROL

RxMessage Buffer control/command

Address: 0x402E01A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.66 CAN_CAN_RX8_ID

Identifier

Address: 0x402E01A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.67 CAN_CAN_RX8_DATA_HIGH

RxMessage Data high

Address: 0x402E01A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.68 CAN_CAN_RX8_DATA_LOW

RxMessage Data low

Address: 0x402E01AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.69 CAN_CAN_RX8_AMR

Acceptance Mask Register

Address: 0x402E01B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.70 CAN_CAN_RX8_ACR

Acceptance Code Register

Address: 0x402E01B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.71 CAN_CAN_RX8_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E01B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.72 CAN_CAN_RX8_ACR_DATA

Acceptance Code Register Data

Address: 0x402E01BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.73 CAN_CAN_RX9_CONTROL

RxMessage Buffer control/command

Address: 0x402E01C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.74 CAN_CAN_RX9_ID

Identifier

Address: 0x402E01C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.75 CAN_CAN_RX9_DATA_HIGH

RxMessage Data high

Address: 0x402E01C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.76 CAN_CAN_RX9_DATA_LOW

RxMessage Data low

Address: 0x402E01CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.77 CAN_CAN_RX9_AMR

Acceptance Mask Register

Address: 0x402E01D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.78 CAN_CAN_RX9_ACR

Acceptance Code Register

Address: 0x402E01D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.79 CAN_CAN_RX9_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E01D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.80 CAN_CAN_RX9_ACR_DATA

Acceptance Code Register Data

Address: 0x402E01DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.81 CAN_CAN_RX10_CONTROL

RxMessage Buffer control/command

Address: 0x402E01E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.82 CAN_CAN_RX10_ID

Identifier

Address: 0x402E01E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.83 CAN_CAN_RX10_DATA_HIGH

RxMessage Data high

Address: 0x402E01E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.84 CAN_CAN_RX10_DATA_LOW

RxMessage Data low

Address: 0x402E01EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.85 CAN_CAN_RX10_AMR

Acceptance Mask Register

Address: 0x402E01F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.86 CAN_CAN_RX10_ACR

Acceptance Code Register

Address: 0x402E01F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.87 CAN_CAN_RX10_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E01F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.88 CAN_CAN_RX10_ACR_DATA

Acceptance Code Register Data

Address: 0x402E01FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.89 CAN_CAN_RX11_CONTROL

RxMessage Buffer control/command

Address: 0x402E0200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.90 CAN_CAN_RX11_ID

Identifier

Address: 0x402E0204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.91 CAN_CAN_RX11_DATA_HIGH

RxMessage Data high

Address: 0x402E0208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.92 CAN_CAN_RX11_DATA_LOW

RxMessage Data low

Address: 0x402E020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.93 CAN_CAN_RX11_AMR

Acceptance Mask Register

Address: 0x402E0210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.94 CAN_CAN_RX11_ACR

Acceptance Code Register

Address: 0x402E0214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.95 CAN_CAN_RX11_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E0218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.96 CAN_CAN_RX11_ACR_DATA

Acceptance Code Register Data

Address: 0x402E021C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.97 CAN_CAN_RX12_CONTROL

RxMessage Buffer control/command

Address: 0x402E0220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.98 CAN_CAN_RX12_ID

Identifier

Address: 0x402E0224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.99 CAN_CAN_RX12_DATA_HIGH

RxMessage Data high

Address: 0x402E0228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.100 CAN_CAN_RX12_DATA_LOW

RxMessage Data low

Address: 0x402E022C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.101 CAN_CAN_RX12_AMR

Acceptance Mask Register

Address: 0x402E0230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.102 CAN_CAN_RX12_ACR

Acceptance Code Register

Address: 0x402E0234

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.103 CAN_CAN_RX12_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E0238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.104 CAN_CAN_RX12_ACR_DATA

Acceptance Code Register Data

Address: 0x402E023C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.105 CAN_CAN_RX13_CONTROL

RxMessage Buffer control/command

Address: 0x402E0240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.106 CAN_CAN_RX13_ID

Identifier

Address: 0x402E0244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.107 CAN_CAN_RX13_DATA_HIGH

RxMessage Data high

Address: 0x402E0248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.108 CAN_CAN_RX13_DATA_LOW

RxMessage Data low

Address: 0x402E024C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.109 CAN_CAN_RX13_AMR

Acceptance Mask Register

Address: 0x402E0250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.110 CAN_CAN_RX13_ACR

Acceptance Code Register

Address: 0x402E0254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.111 CAN_CAN_RX13_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E0258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.112 CAN_CAN_RX13_ACR_DATA

Acceptance Code Register Data

Address: 0x402E025C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.113 CAN_CAN_RX14_CONTROL

RxMessage Buffer control/command

Address: 0x402E0260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.114 CAN_CAN_RX14_ID

Identifier

Address: 0x402E0264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.115 CAN_CAN_RX14_DATA_HIGH

RxMessage Data high

Address: 0x402E0268

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.116 CAN_CAN_RX14_DATA_LOW

RxMessage Data low

Address: 0x402E026C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.117 CAN_CAN_RX14_AMR

Acceptance Mask Register

Address: 0x402E0270

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.118 CAN_CAN_RX14_ACR

Acceptance Code Register

Address: 0x402E0274

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.119 CAN_CAN_RX14_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E0278

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.120 CAN_CAN_RX14_ACR_DATA

Acceptance Code Register Data

Address: 0x402E027C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

2.1.121 CAN_CAN_RX15_CONTROL

RxMessage Buffer control/command

Address: 0x402E0280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	R	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	WPNL	LINK_FLAG	RX_INT_E-BL	RTR_RE-PLY	BUFFER_E N	RTR_ABOR T	RTR_RE-PLY_PEND	MS-G_AV_R-TRSENT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR_MSG	IDE_FMT	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying the bits[21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR_MSG	Remote Bit '1': This is an RTR message '0': This is a regular message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be set to 0 (data frame type) by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined

(continued)

20	IDE_FMT	Extended Identifier Bit '1': This is an extended format message '0': This is a standard format message depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
19 : 16	DLC	DLC, Data Length Code 0: Message has 0 data bytes, data[63:0] is notvalid 1: Message has 1 data byte, data[63:56] is valid .. 8: Message has 8 data bytes, data[63:0] is valid 9-15: Message has 8 data bytes depending on RTR_REPLY setting, 0, this field will be updated by received data/remote frame 1, this field should be aligned offline and set by user in advance, will not be updated by received data/remote frame, and will be sent out in responsive data frame Default Value: Undefined
7	WPNL	WPNL, Write Protectiontion for bit [6:3]. '0': Bits [6:3] are write protected, '1': Bits [6:3] are modified by writes. This WPNL bit must always be set in the same write that is modifying bits [6:3], as this bit state is not preserved. This bit is always zero for readback. Default Value: 0
6	LINK_FLAG	Link Flag 0: This buffer is not linked to the next 1: This buffer is linked with next buffer Default Value: 0
5	RX_INT_EBL	RxIntEbl, Receive Interrupt Enable 0: Interrupt generation is disabled '1: Interrupt generation is enabled Default Value: 0
4	RTR_REPLY	automatic message reply upon receipt of an RTR message 0: Automatic RTR message handling disabled 1: Automatic RTR message handling enabled when this bit is set, only RTR message can be received, by setting AMR.RTR=0, AMR.RTR=1. Otherwise, the RTR reply message content will corrupted by received non-RTR message. Default Value: 0
3	BUFFER_EN	Buffer Enable 0: Buffer is disabled 1: Buffer is enabled Default Value: 0

(continued)

2	RTR_ABORT	RTR Abort Request '0': Idle '1': Requests removal of a pending RTR message reply. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time. Default Value: 0
1	RTR_REPLY_PEND	RTReply_pending status '0': No RTR reply request pending '1': RTR reply request pending Default Value: 0
0	MSG_AV_RTRSENT	Msg Available/RTR Sent If RTReply flag is set, this bit shows if an RTR auto-reply message has been sent, otherwise it indicates if the buffer contains a valid message. Read: '0': Idle '1': New message available (RTRreply=0), RTR auto-reply message sent (RTRreply=1). Write: '0': Idle '1': Acknowledges receipt of new message or transmission of RTR auto-reply message. Default Value: 0

2.1.122 CAN_CAN_RX15_ID

Identifier

Address: 0x402E0284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	RxMessage: Identifier Default Value: Undefined

2.1.123 CAN_CAN_RX15_DATA_HIGH

RxMessage Data high

Address: 0x402E0288

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] Default Value: Undefined

2.1.124 CAN_CAN_RX15_DATA_LOW

RxMessage Data low

Address: 0x402E028C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

2.1.125 CAN_CAN_RX15_AMR

Acceptance Mask Register

Address: 0x402E0290

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier it cannot be used to match both 11bit and 29bit identifiers, in case of 11bit identifiers, lower 18bits should be all ones (dont care) Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.126 CAN_CAN_RX15_ACR

Acceptance Code Register

Address: 0x402E0294

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	None
HW Access	RW					RW	RW	None
Name	ID [7:3]					IDE	RTR	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Identifier Default Value: Undefined
2	IDE	Default Value: Undefined
1	RTR	Default Value: Undefined

2.1.127 CAN_CAN_RX15_AMR_DATA

Acceptance Mask Register Data

Address: 0x402E0298

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48], when DUT is NOT configured to receive only DATA frame, this register should be configured with all ones (dont care) Default Value: Undefined

2.1.128 CAN_CAN_RX15_ACR_DATA

Acceptance Code Register Data

Address: 0x402E029C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATAL	Data[63:48] Default Value: Undefined

3 CAN Transmit Registers

This section discusses the CAN Transmit Registers (CAN_TX) registers. It lists all the registers in mapping tables, in address order.

3.1 Register Details

Register Name	Address
CAN_CAN_TX0_CONTROL	0x402E0020
CAN_CAN_TX0_ID	0x402E0024
CAN_CAN_TX0_DATA_HIGH	0x402E0028
CAN_CAN_TX0_DATA_LOW	0x402E002C
CAN_CAN_TX1_CONTROL	0x402E0030
CAN_CAN_TX1_ID	0x402E0034
CAN_CAN_TX1_DATA_HIGH	0x402E0038
CAN_CAN_TX1_DATA_LOW	0x402E003C
CAN_CAN_TX2_CONTROL	0x402E0040
CAN_CAN_TX2_ID	0x402E0044
CAN_CAN_TX2_DATA_HIGH	0x402E0048
CAN_CAN_TX2_DATA_LOW	0x402E004C
CAN_CAN_TX3_CONTROL	0x402E0050
CAN_CAN_TX3_ID	0x402E0054
CAN_CAN_TX3_DATA_HIGH	0x402E0058
CAN_CAN_TX3_DATA_LOW	0x402E005C
CAN_CAN_TX4_CONTROL	0x402E0060
CAN_CAN_TX4_ID	0x402E0064
CAN_CAN_TX4_DATA_HIGH	0x402E0068
CAN_CAN_TX4_DATA_LOW	0x402E006C
CAN_CAN_TX5_CONTROL	0x402E0070
CAN_CAN_TX5_ID	0x402E0074
CAN_CAN_TX5_DATA_HIGH	0x402E0078
CAN_CAN_TX5_DATA_LOW	0x402E007C
CAN_CAN_TX6_CONTROL	0x402E0080
CAN_CAN_TX6_ID	0x402E0084
CAN_CAN_TX6_DATA_HIGH	0x402E0088

Register Name	Address
CAN_CAN_TX6_DATA_LOW	0x402E008C
CAN_CAN_TX7_CONTROL	0x402E0090
CAN_CAN_TX7_ID	0x402E0094
CAN_CAN_TX7_DATA_HIGH	0x402E0098
CAN_CAN_TX7_DATA_LOW	0x402E009C

3.1.1 CAN_CAN_TX0_CONTROL

TxMessage Buffer control/command

Address: 0x402E0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_E-BL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying bits [21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

(continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPNL: Write protection for bit [2]. '0': Bit [2] is write protected, '1': Bit [2] is modified by writes The WPNL bit must always be set in the same write that is modifying bit [2] as this bit state is not preserved. This WPNL bit is always zero for readback. Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable 0: Interrupt disabled 1: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle 1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time when there is a pending TX message (read out TxReq=1 and TxAbort=0), Writing TxReq=1 and TxAbort=1 has no effect. for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

3.1.2 CAN_CAN_TX0_ID

TxMessage Buffer Identifier

Address: 0x402E0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

3.1.3 CAN_CAN_TX0_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

3.1.4 CAN_CAN_TX0_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.5 CAN_CAN_TX1_CONTROL

TxMessage Buffer control/command

Address: 0x402E0030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_E-BL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying bits [21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

(continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPNL: Write protection for bit [2]. '0': Bit [2] is write protected, '1': Bit [2] is modified by writes The WPNL bit must always be set in the same write that is modifying bit [2] as this bit state is not preserved. This WPNL bit is always zero for readback. Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable 0: Interrupt disabled 1: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle 1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time when there is a pending TX message (read out TxReq=1 and TxAbort=0), Writing TxReq=1 and TxAbort=1 has no effect. for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

3.1.6 CAN_CAN_TX1_ID

TxMessage Buffer Identifier

Address: 0x402E0034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

3.1.7 CAN_CAN_TX1_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

3.1.8 CAN_CAN_TX1_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.9 CAN_CAN_TX2_CONTROL

TxMessage Buffer control/command

Address: 0x402E0040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_E-BL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying bits [21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

(continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPNL: Write protection for bit [2]. '0': Bit [2] is write protected, '1': Bit [2] is modified by writes The WPNL bit must always be set in the same write that is modifying bit [2] as this bit state is not preserved. This WPNL bit is always zero for readback. Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable 0: Interrupt disabled 1: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle 1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time when there is a pending TX message (read out TxReq=1 and TxAbort=0), Writing TxReq=1 and TxAbort=1 has no effect. for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

3.1.10 CAN_CAN_TX2_ID

TxMessage Buffer Identifier

Address: 0x402E0044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

3.1.11 CAN_CAN_TX2_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

3.1.12 CAN_CAN_TX2_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.13 CAN_CAN_TX3_CONTROL

TxMessage Buffer control/command

Address: 0x402E0050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_E-BL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying bits [21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

(continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPNL: Write protection for bit [2]. '0': Bit [2] is write protected, '1': Bit [2] is modified by writes The WPNL bit must always be set in the same write that is modifying bit [2] as this bit state is not preserved. This WPNL bit is always zero for readback. Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable 0: Interrupt disabled 1: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle 1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time when there is a pending TX message (read out TxReq=1 and TxAbort=0), Writing TxReq=1 and TxAbort=1 has no effect. for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

3.1.14 CAN_CAN_TX3_ID

TxMessage Buffer Identifier

Address: 0x402E0054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

3.1.15 CAN_CAN_TX3_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

3.1.16 CAN_CAN_TX3_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E005C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.17 CAN_CAN_TX4_CONTROL

TxMessage Buffer control/command

Address: 0x402E0060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_E-BL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying bits [21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

(continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPNL: Write protection for bit [2]. '0': Bit [2] is write protected, '1': Bit [2] is modified by writes The WPNL bit must always be set in the same write that is modifying bit [2] as this bit state is not preserved. This WPNL bit is always zero for readback. Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable 0: Interrupt disabled 1: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle 1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time when there is a pending TX message (read out TxReq=1 and TxAbort=0), Writing TxReq=1 and TxAbort=1 has no effect. for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

3.1.18 CAN_CAN_TX4_ID

TxMessage Buffer Identifier

Address: 0x402E0064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

3.1.19 CAN_CAN_TX4_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

3.1.20 CAN_CAN_TX4_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E006C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.21 CAN_CAN_TX5_CONTROL

TxMessage Buffer control/command

Address: 0x402E0070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_E-BL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying bits [21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

(continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPNL: Write protection for bit [2]. '0': Bit [2] is write protected, '1': Bit [2] is modified by writes The WPNL bit must always be set in the same write that is modifying bit [2] as this bit state is not preserved. This WPNL bit is always zero for readback. Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable 0: Interrupt disabled 1: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle 1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time when there is a pending TX message (read out TxReq=1 and TxAbort=0), Writing TxReq=1 and TxAbort=1 has no effect. for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

3.1.22 CAN_CAN_TX5_ID

TxMessage Buffer Identifier

Address: 0x402E0074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

3.1.23 CAN_CAN_TX5_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

3.1.24 CAN_CAN_TX5_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E007C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.25 CAN_CAN_TX6_CONTROL

TxMessage Buffer control/command

Address: 0x402E0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_E-BL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying bits [21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

(continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPNL: Write protection for bit [2]. '0': Bit [2] is write protected, '1': Bit [2] is modified by writes The WPNL bit must always be set in the same write that is modifying bit [2] as this bit state is not preserved. This WPNL bit is always zero for readback. Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable 0: Interrupt disabled 1: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle 1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time when there is a pending TX message (read out TxReq=1 and TxAbort=0), Writing TxReq=1 and TxAbort=1 has no effect. for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

3.1.26 CAN_CAN_TX6_ID

TxMessage Buffer Identifier

Address: 0x402E0084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

3.1.27 CAN_CAN_TX6_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

3.1.28 CAN_CAN_TX6_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

3.1.29 CAN_CAN_TX7_CONTROL

TxMessage Buffer control/command

Address: 0x402E0090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				WPNL	TX_INT_E-BL	TX_ABORT	TX_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW	RW	RW			
HW Access	RW	None	RW	RW	RW			
Name	WPNH	None	RTR	IDE	DLC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	WPNH	WPNH, Write Protection for bits[21:16]. '0': Bit [21:16] are write protected, '1': Bit [21:16] are modified by writes. The WPNH bit must always be set in the same write that is modifying bits [21:16] as this bit state is not preserved. The readback value of this bit is undefined. Default Value: Undefined
21	RTR	Remote Bit '0': This is a standard message '1': This is an RTR message Default Value: Undefined
20	IDE	Extended Identifier Bit '0': This is a standard format message '1': This is an extended format message Default Value: Undefined

(continued)

19 : 16	DLC	DLC, Data Length Code Invalid values are transmitted as they are, but the number of data bytes is limited to eight. 0: Message has 0 data byte, data[63:0] is not used 1: Message has 1 data byte, data[63:56] is used ... 8: Message has 8 data bytes, data[63:0] is used 9-15: Message has 8 data bytes Default Value: Undefined
3	WPNL	WPNL: Write protection for bit [2]. '0': Bit [2] is write protected, '1': Bit [2] is modified by writes The WPNL bit must always be set in the same write that is modifying bit [2] as this bit state is not preserved. This WPNL bit is always zero for readback. Default Value: 0
2	TX_INT_EBL	Tx Interrupt Enable 0: Interrupt disabled 1: Interrupt enabled, successful message transmission sets the TxMsg Default Value: 0
1	TX_ABORT	Transmit Abort Request '0': idle 1': Requests removal of a pending message. The message is removed the next time an arbitration loss happens or a CAN error is detected. The flag is cleared when the message was removed or when the message won arbitration. The TxReq flag is released at the same time when there is a pending TX message (read out TxReq=1 and TxAbort=0), Writing TxReq=1 and TxAbort=1 has no effect. for SST message,when the message is aborted, the TxReq fag is cleared, but the TxAbort fag remains asserted. Default Value: 0
0	TX_REQ	TxReq, Transmit Request Write: '0': idle '1': Message Transmit Request5 Read: '0': TxReq completed '1': TxReq pending Default Value: 0

3.1.30 CAN_CAN_TX7_ID

TxMessage Buffer Identifier

Address: 0x402E0094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	ID [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ID [31:24]							

Bits	Name	Description
31 : 3	ID	Message identifier Default Value: Undefined

3.1.31 CAN_CAN_TX7_DATA_HIGH

TxMessage Buffer Data high

Address: 0x402E0098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[63:32] when CONFIG.SWAP_ENDIAN=0(Big Endian, by default), the sequence of DATA transmission is, {DATA_HIGH[31:0], DATA_LOW[31:0]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted when CONFIG.SWAP_ENDIAN=1(Little Endian), the sequence of DATA transmission is, {DATA_HIGH[7:0], [15:8], [23:16], [31:24], DATA_LOW[7:0], [15:8], [23:16], [31:24]} if only byte is defined in CONTROL.DLC, DATA_HIGH[7:0] will be transmitted Default Value: Undefined

3.1.32 CAN_CAN_TX7_DATA_LOW

TxMessageBuffer Data low

Address: 0x402E009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data[31:0] Default Value: Undefined

4 Cortex M0+ Registers

This section discusses the Cortex M0+ (CM0+) registers. It lists all the registers in mapping tables, in address order.

4.1 Register Details

Register Name	Address
CM0P_DWT_PID4	0xE0001FD0
CM0P_DWT_PID0	0xE0001FE0
CM0P_DWT_PID1	0xE0001FE4
CM0P_DWT_PID2	0xE0001FE8
CM0P_DWT_PID3	0xE0001FEC
CM0P_DWT_CID0	0xE0001FF0
CM0P_DWT_CID1	0xE0001FF4
CM0P_DWT_CID2	0xE0001FF8
CM0P_DWT_CID3	0xE0001FFC
CM0P_BP_PID4	0xE0002FD0
CM0P_BP_PID0	0xE0002FE0
CM0P_BP_PID1	0xE0002FE4
CM0P_BP_PID2	0xE0002FE8
CM0P_BP_PID3	0xE0002FEC
CM0P_BP_CID0	0xE0002FF0
CM0P_BP_CID1	0xE0002FF4
CM0P_BP_CID2	0xE0002FF8
CM0P_BP_CID3	0xE0002FFC
CM0P_SYST_CSR	0xE000E010
CM0P_SYST_RVR	0xE000E014
CM0P_SYST_CVR	0xE000E018
CM0P_SYST_CALIB	0xE000E01C
CM0P_ISER	0xE000E100
CM0P_ICER	0xE000E180
CM0P_ISPR	0xE000E200
CM0P_ICPR	0xE000E280
CM0P_IPR0	0xE000E400

Register Name	Address
CM0P_IPR1	0xE000E404
CM0P_IPR2	0xE000E408
CM0P_IPR3	0xE000E40C
CM0P_IPR4	0xE000E410
CM0P_IPR5	0xE000E414
CM0P_IPR6	0xE000E418
CM0P_IPR7	0xE000E41C
CM0P_CPUID	0xE000ED00
CM0P_ICSR	0xE000ED04
CM0P_AIRCR	0xE000ED0C
CM0P_SCR	0xE000ED10
CM0P_CCR	0xE000ED14
CM0P_SHPR2	0xE000ED1C
CM0P_SHPR3	0xE000ED20
CM0P_SHCSR	0xE000ED24
CM0P_SCS_PID4	0xE000EFD0
CM0P_SCS_PID0	0xE000EFE0
CM0P_SCS_PID1	0xE000EFE4
CM0P_SCS_PID2	0xE000EFE8
CM0P_SCS_PID3	0xE000EFEC
CM0P_SCS_CID0	0xE000EFF0
CM0P_SCS_CID1	0xE000EFF4
CM0P_SCS_CID2	0xE000EFF8
CM0P_SCS_CID3	0xE000EFFC
CM0P_ROM_SCS	0xE00FF000
CM0P_ROM_DWT	0xE00FF004
CM0P_ROM_BPU	0xE00FF008
CM0P_ROM_END	0xE00FF00C
CM0P_ROM_CSMT	0xE00FFFCC
CM0P_ROM_PID4	0xE00FFFD0
CM0P_ROM_PID0	0xE00FFFE0
CM0P_ROM_PID1	0xE00FFFE4
CM0P_ROM_PID2	0xE00FFFE8
CM0P_ROM_PID3	0xE00FFFEC
CM0P_ROM_CID0	0xE00FFFF0
CM0P_ROM_CID1	0xE00FFFF4
CM0P_ROM_CID2	0xE00FFFF8
CM0P_ROM_CID3	0xE00FFFFC

4.1.1 CM0P_DWT_PID4

Watchpoint Unit CoreSight ROM Table Peripheral ID #4

Address: 0xE0001FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

4.1.2 CM0P_DWT_PID0

Watchpoint Unit CoreSight ROM Table Peripheral ID #0

Address: 0xE0001FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 10

4.1.3 CM0P_DWT_PID1

Watchpoint Unit CoreSight ROM Table Peripheral ID #1

Address: 0xE0001FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

4.1.4 CM0P_DWT_PID2

Watchpoint Unit CoreSight ROM Table Peripheral ID #2

Address: 0xE0001FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

4.1.5 CM0P_DWT_PID3

Watchpoint Unit CoreSight ROM Table Peripheral ID #3

Address: 0xE0001FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

4.1.6 CM0P_DWT_CID0

Watchpoint Unit CoreSight ROM Table Component ID #0

Address: 0xE0001FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

4.1.7 CM0P_DWT_CID1

Watchpoint Unit CoreSight ROM Table Component ID #1

Address: 0xE0001FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

4.1.8 CM0P_DWT_CID2

Watchpoint Unit CoreSight ROM Table Component ID #2

Address: 0xE0001FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

4.1.9 CM0P_DWT_CID3

Watchpoint Unit CoreSight ROM Table Component ID #3

Address: 0xE0001FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

4.1.10 CM0P_BP_PID4

Breakpoint Unit CoreSight ROM Table Peripheral ID #4

Address: 0xE0002FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

4.1.11 CM0P_BP_PID0

Breakpoint Unit CoreSight ROM Table Peripheral ID #0

Address: 0xE0002FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 11

4.1.12 CM0P_BP_PID1

Breakpoint Unit CoreSight ROM Table Peripheral ID #1

Address: 0xE0002FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

4.1.13 CM0P_BP_PID2

Breakpoint Unit CoreSight ROM Table Peripheral ID #2

Address: 0xE0002FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

4.1.14 CM0P_BP_PID3

Breakpoint Unit CoreSight ROM Table Peripheral ID #3

Address: 0xE0002FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

4.1.15 CM0P_BP_CID0

Breakpoint Unit CoreSight ROM Table Component ID #0

Address: 0xE0002FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

4.1.16 CM0P_BP_CID1

Breakpoint Unit CoreSight ROM Table Component ID #1

Address: 0xE0002FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

4.1.17 CM0P_BP_CID2

Breakpoint Unit CoreSight ROM Table Component ID #2

Address: 0xE0002FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

4.1.18 CM0P_BP_CID3

Breakpoint Unit CoreSight ROM Table Component ID #3

Address: 0xE0002FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

4.1.19 CM0P_SYST_CSR

SysTick Control & Status

Address: 0xE000E010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CLK-SOURCE	TICKINT	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							COUNT-FLAG

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	COUNTFLAG	Indicates whether the counter has counted to "0" since the last read of this register: '0': counter has not counted to "0". '1': counter has counted to "0". COUNTFLAG is set to '1' by a count transition from "1" to "0". COUNTFLAG is cleared to '0' by a read of this register, and by any write to the SYST_CVR register. Default Value: 0

(continued)

2	CLKSOURCE	Indicates the SysTick counter clock source: '0': SysTick uses the low frequency clock "clk_lf". For this mode to function, "clk_lf" should be less than half the frequency of "clk_sys". Note that "clk_lf" is generated by a low accuracy ILO (Internal Low power Oscillator), with a target frequency of 32.768 kHz (frequency can be as low as 15 KHz and as high as 60 kHz). '1': SysTick uses the system/processor clock "clk_sys". In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided. in SF, TSG6M products, this functionality is not provided. For these products, this field should be set to '1', such that SysTick uses the system clock "clk_sys". Default Value: 0
1	TICKINT	Indicates whether counting to "0" causes the status of the SysTick exception to change to pending: '0': count to "0" does not affect the SysTick exception status. '1': count to "0" changes the SysTick exception status to pending. Changing the value of the counter to "0" by writing zero to the SYST_CVR register to "0" never changes the status of the SysTick exception. Default Value: 0
0	ENABLE	Indicates the enabled status of the SysTick counter: '0': counter is disabled. '1': counter is operating. Default Value: 0

4.1.20 CM0P_SYST_RVR

SysTick Reload Value

Address: 0xE000E014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RELOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RELOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RELOAD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	RELOAD	The value to load into the SYST_CVR register when the counter reaches 0. Default Value: X

4.1.21 CM0P_SYST_CVR

SysTick Current Value

Address: 0xE000E018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CURRENT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CURRENT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CURRENT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	CURRENT	Current counter value. This is the value of the counter at the time it is sampled. Default Value: X

4.1.22 CM0P_SYST_CALIB

SysTick Calibration Value

Address: 0xE000E01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	None	RW	None					
Name	NOREF	SKEW	None [29:24]					

Bits	Name	Description
31	NOREF	Indicates whether a implementation defined reference clock is provided: '0': the reference clock is provided. '1': the reference clock is not provided. When this bit is '1', the SYST_CSR.CLKSOURCEis forced to '1' and cannot be cleared to '0'. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is '0'. In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is '1'. Default Value: 0
30	SKEW	Indicates whether the 10ms calibration value is exact: '0': 10ms calibration value is exact. '1': 10ms calibration value is inexact, because of the clock frequency. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is '1' (due to the low accuracy ILO). In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is '0'. Default Value: X

(continued)

23 : 0	TENMS	Optionally, holds a reload value to be used for 10ms (100Hz) timing, subject to system clock skew errors. If this field is "0", the calibration value is not known. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is 0x00:00147. In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is 0x00:0000. Default Value: X

4.1.23 CM0P_ISER

Interrupt Set-Enable Register

Address: 0xE000E100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	SETENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	SETENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	SETENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	SETENA [31:24]							

Bits	Name	Description
31 : 0	SETENA	Enables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

4.1.24 CM0P_ICER

Interrupt Clear Enable Register

Address: 0xE000E180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CLRENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CLRENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CLRENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CLRENA [31:24]							

Bits	Name	Description
31 : 0	CLRENA	Disables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

4.1.25 CM0P_ISPR

Interrupt Set-Pending Register

Address: 0xE000E200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	SETPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	SETPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	SETPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	SETPEND [31:24]							

Bits	Name	Description
31 : 0	SETPEND	Changes the state of one or more interrupts to pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

4.1.26 CM0P_ICPR

Interrupt Clear-Pending Register

Address: 0xE000E280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [31:24]							

Bits	Name	Description
31 : 0	CLRPEND	Changes the state of one or more interrupts to not pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

4.1.27 CM0P_IPR0

Interrupt Priority Registers

Address: 0xE000E400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

4.1.28 CM0P_IPR1

Interrupt Priority Registers

Address: 0xE000E404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

4.1.29 CM0P_IPR2

Interrupt Priority Registers

Address: 0xE000E408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

4.1.30 CM0P_IPR3

Interrupt Priority Registers

Address: 0xE000E40C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

4.1.31 CM0P_IPR4

Interrupt Priority Registers

Address: 0xE000E410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

4.1.32 CM0P_IPR5

Interrupt Priority Registers

Address: 0xE000E414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

4.1.33 CM0P_IPR6

Interrupt Priority Registers

Address: 0xE000E418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

4.1.34 CM0P_IPR7

Interrupt Priority Registers

Address: 0xE000E41C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

4.1.35 CM0P_CPUID

CPUID Register

Address: 0xE000ED00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	None				None			
Name	PARTNO [7:4]				REVISION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	PARTNO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	None				None			
Name	VARIANT [23:20]				CONSTANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	IMPLEMENTER [31:24]							

Bits	Name	Description
31 : 24	IMPLEMENTER	Implementer code for ARM. Default Value: 65
23 : 20	VARIANT	Implementation defined. In ARM implementations this is the major revision number n in the rn part of the rnpn revision status, Product revision status on page xii. Default Value: 0
19 : 16	CONSTANT	Indicates the architecture, ARMv6-M Default Value: 12
15 : 4	PARTNO	Indicates part number, Cortex-M0+ Default Value: 3168
3 : 0	REVISION	Indicates revision. In ARM implementations this is the minor revision number n in the pn part of the rnpn revision status, see Product revision status on page xii. For release r0p1. Default Value: 1

4.1.36 CM0P_ICSR

Interrupt Control State Register

Address: 0xE000ED04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VECTACTIVE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			R
HW Access	RW				None			RW
Name	VECTPENDING [15:12]				None [11:9]			VECTAC-TIVE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	None	R				
HW Access	RW	RW	None	RW				
Name	ISRPRE-EMPT	ISRPEND-ING	None	VECTPENDING [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None		RW1S	RW1C	RW1S	RW1C	None
HW Access	RW	None		RW	R	RW	R	None
Name	NMIPEND-SET	None [30:29]		PENDS-VSET	PENDSV-CLR	PENDST-SETb	PENDST-CLR	None

Bits	Name	Description
31	NMIPENDSET	Activates an NMI exception or reads back the current state. Because NMI is the highest priority exception, it activates as soon as it is registered. Default Value: 0
28	PENDSVSET	Sets a pending PendSV interrupt or reads back the current state. Use this normally to request a context switch. Writing PENDSVSET and PENDSVCLR to '1' concurrently is UNPREDICT-ABLE. Default Value: 0
27	PENDSVCLR	Clears a pending PendSV interrupt. Default Value: 0
26	PENDSTSETb	Sets a pending SysTick or reads back the current state. Writing PENDSTSET and PENDSTCLR to '1' concurrently is UNPREDICTABLE. Default Value: 0
25	PENDSTCLR	Clears a pending SysTick, whether set here or by the timer hardware. Default Value: 0

(continued)

23	ISRPREEMPT	Indicates whether a pending exception will be serviced on exit from debug halt state. Default Value: 0
22	ISRPENDING	Indicates if an external configurable, NVIC generated, interrupt is pending. Default Value: 0
20 : 12	VECTPENDING	The exception number for the highest priority pending exception. 0= No pending exceptions. The pending state includes the effect of memory-mapped enable and mask registers. It does not include the PRIMASK special-purpose register qualifier. Default Value: 0
8 : 0	VECTACTIVE	The exception number for the current executing exception. 0= Thread mode. This is the same value as IPSR[8:0] Default Value: 0

4.1.37 CM0P_AIRCR

Application Interrupt and Reset Control Register

Address: 0xE000ED0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1C	None
HW Access	None					R	R	None
Name	None [7:3]					SYSRESE-TREQ	VECTCL-RACTIVE	None

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	None	None						
Name	ENDIAN-NESS	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VECTKEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VECTKEY [31:24]							

Bits	Name	Description
31 : 16	VECTKEY	Vector Key. The value 0x05FA must be written to this register, otherwise the register write is UN-PREDICTABLE. Readback value is UNKNOWN. Default Value: X
15	ENDIANNESS	Indicates the memory system data endianness: 0 little endian 1 big endian. See Endian support on page A3-44 for more information. Default Value: 0
2	SYSRESETREQ	System Reset Request. Writing 1 to this bit asserts a signal to request a reset by the external system. This will cause a full system reset of the CPU and all other components in the device. See Reset management on page B1-240 for more information. Default Value: 0
1	VECTCLRACTIVE	Clears all active state information for fixed and configurable exceptions. The effect of writing a 1 to this bit if the processor is not halted in Debug state is UNPREDICTABLE. Default Value: 0

4.1.38 CM0P_SCR

System Control Register

Address: 0xE000ED10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	None
HW Access	None			R	None	R	R	None
Name	None [7:5]			SEVON-PEND	None	SLEEP-DEEP	SLEEPON-EXIT	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	SEVONPEND	Determines whether an interrupt transition from inactive state to pending state is a wakeup event: 0: transitions from inactive to pending are not wakeup events. 1: transitions from inactive to pending are wakeup events. See WFE on page A6-197 for more information. Default Value: 0
2	SLEEPDEEP	An implementation can use this bit to select DeepSleep/Hibernate power modes upon execution of WFI/WFE: 0: Select Sleep mode 1: Select DeepSleep/Hibernate (depends on PWR_CONTROL.HIBERNATE) Default Value: 0
1	SLEEPONEXIT	Determines whether, on an exit from an ISR that returns to the base level of execution priority, the processor enters a sleep state: 0 do not enter sleep state. 1 enter sleep state. See Power management on page B1-240 for more information. Default Value: 0

4.1.39 CM0P_CCR

Configuration and Control Register

Address: 0xE000ED14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	None		
HW Access	None				None	None		
Name	None [7:4]				UN-ALIGN_TRP	None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	None
HW Access	None						None	None
Name	None [15:10]						STKALIGN	None

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	STKALIGN	1: On exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return. Default Value: 1
3	UNALIGN_TRP	1: unaligned word and halfword accesses generate a HardFault exception. Default Value: 1

4.1.40 CM0P_SHPR2

System Handler Priority Register 2

Address: 0xE000ED1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_11 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_11	Priority of system handler 11, SVCall Default Value: 0

4.1.41 CM0P_SHPR3

System Handler Priority Register 3

Address: 0xE000ED20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_14 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_15 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_15	Priority of system handler 15, SysTick Default Value: 0
23 : 22	PRI_14	Priority of system handler 14, PendSV Default Value: 0

4.1.42 CM0P_SHCSR

System Handler Control and State Register

Address: 0xE000ED24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None						
HW Access	RW	None						
Name	SVCALL-PENDED	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	SVCALLPENDED	0 SVCall is not pending. 1 SVCall is pending. This bit reflects the pending state on a read, and updates the pending state, to the value written, on a write. (Pending state bits are set to 1 when an exception occurs, and are cleared to 0 when an exception becomes active.) Default Value: 0

4.1.43 CM0P_SCS_PID4

System Control Space ROM Table Peripheral ID #4

Address: 0xE000EFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

4.1.44 CM0P_SCS_PID0

System Control Space ROM Table Peripheral ID #0

Address: 0xE000EFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 8

4.1.45 CM0P_SCS_PID1

System Control Space ROM Table Peripheral ID #1

Address: 0xE000EFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

4.1.46 CM0P_SCS_PID2

System Control Space ROM Table Peripheral ID #2

Address: 0xE000EFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

4.1.47 CM0P_SCS_PID3

System Control Space ROM Table Peripheral ID #3

Address: 0xE000EFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

4.1.48 CM0P_SCS_CID0

System Control Space ROM Table Component ID #0

Address: 0xE000EFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

4.1.49 CM0P_SCS_CID1

System Control Space ROM Table Component ID #1

Address: 0xE000EFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

4.1.50 CM0P_SCS_CID2

System Control Space ROM Table Component ID #2

Address: 0xE000EFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

4.1.51 CM0P_SCS_CID3

System Control Space ROM Table Component ID #3

Address: 0xE000EFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

4.1.52 CM0P_ROM_SCS

CM0+ CoreSight ROM Table Peripheral #0

Address: 0xE00FF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to SCS ROM Table Default Value: 4293980163

4.1.53 CM0P_ROM_DWT

CM0+ CoreSight ROM Table Peripheral #1

Address: 0xE00FF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to DWT ROM Table Default Value: 4293926915

4.1.54 CM0P_ROM_BPU

CM0+ CoreSight ROM Table Peripheral #2

Address: 0xE00FF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to BPU ROM Table Default Value: 4293931011

4.1.55 CM0P_ROM_END

CM0+ CoreSight ROM Table End Marker

Address: 0xE00FF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	End marker in peripheral list Default Value: 0

4.1.56 CM0P_ROM_CSMT

CM0+ CoreSight ROM Table Memory Type

Address: 0xE00FFFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Memory Type Default Value: 1

4.1.57 CM0P_ROM_PID4

CM0+ CoreSight ROM Table Peripheral ID #4

Address: 0xE00FFFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

4.1.58 CM0P_ROM_PID0

CM0+ CoreSight ROM Table Peripheral ID #0

Address: 0xE00FFFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 192

4.1.59 CM0P_ROM_PID1

CM0+ CoreSight ROM Table Peripheral ID #1

Address: 0xE00FFFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 180

4.1.60 CM0P_ROM_PID2

CM0+ CoreSight ROM Table Peripheral ID #2

Address: 0xE00FFFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

4.1.61 CM0P_ROM_PID3

CM0+ CoreSight ROM Table Peripheral ID #3

Address: 0xE00FFFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

4.1.62 CM0P_ROM_CID0

CM0+ CoreSight ROM Table Component ID #0

Address: 0xE00FFFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

4.1.63 CM0P_ROM_CID1

CM0+ CoreSight ROM Table Component ID #1

Address: 0xE00FFFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 16

4.1.64 CM0P_ROM_CID2

CM0+ CoreSight ROM Table Component ID #2

Address: 0xE00FFFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

4.1.65 CM0P_ROM_CID3

CM0+ CoreSight ROM Table Component ID #3

Address: 0xE00FFFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

5 Timer, Counter, PWM Counter Registers

This section discusses the Timer, Counter, PWM Counter (TCPWM_CNT) registers. It lists all the registers in mapping tables, in address order.

5.1 Register Details

Register Name	Address
TCPWM_CNT0_CTRL	0x40200100
TCPWM_CNT0_STATUS	0x40200104
TCPWM_CNT0_COUNTER	0x40200108
TCPWM_CNT0_CC	0x4020010C
TCPWM_CNT0_CC_BUFF	0x40200110
TCPWM_CNT0_PERIOD	0x40200114
TCPWM_CNT0_PERIOD_BUFF	0x40200118
TCPWM_CNT0_TR_CTRL0	0x40200120
TCPWM_CNT0_TR_CTRL1	0x40200124
TCPWM_CNT0_TR_CTRL2	0x40200128
TCPWM_CNT0_INTR	0x40200130
TCPWM_CNT0_INTR_SET	0x40200134
TCPWM_CNT0_INTR_MASK	0x40200138
TCPWM_CNT0_INTR_MASKED	0x4020013C
TCPWM_CNT1_CTRL	0x40200140
TCPWM_CNT1_STATUS	0x40200144
TCPWM_CNT1_COUNTER	0x40200148
TCPWM_CNT1_CC	0x4020014C
TCPWM_CNT1_CC_BUFF	0x40200150
TCPWM_CNT1_PERIOD	0x40200154
TCPWM_CNT1_PERIOD_BUFF	0x40200158
TCPWM_CNT1_TR_CTRL0	0x40200160
TCPWM_CNT1_TR_CTRL1	0x40200164
TCPWM_CNT1_TR_CTRL2	0x40200168
TCPWM_CNT1_INTR	0x40200170
TCPWM_CNT1_INTR_SET	0x40200174
TCPWM_CNT1_INTR_MASK	0x40200178

Register Name	Address
TCPWM_CNT1_INTR_MASKED	0x4020017C
TCPWM_CNT2_CTRL	0x40200180
TCPWM_CNT2_STATUS	0x40200184
TCPWM_CNT2_COUNTER	0x40200188
TCPWM_CNT2_CC	0x4020018C
TCPWM_CNT2_CC_BUFF	0x40200190
TCPWM_CNT2_PERIOD	0x40200194
TCPWM_CNT2_PERIOD_BUFF	0x40200198
TCPWM_CNT2_TR_CTRL0	0x402001A0
TCPWM_CNT2_TR_CTRL1	0x402001A4
TCPWM_CNT2_TR_CTRL2	0x402001A8
TCPWM_CNT2_INTR	0x402001B0
TCPWM_CNT2_INTR_SET	0x402001B4
TCPWM_CNT2_INTR_MASK	0x402001B8
TCPWM_CNT2_INTR_MASKED	0x402001BC
TCPWM_CNT3_CTRL	0x402001C0
TCPWM_CNT3_STATUS	0x402001C4
TCPWM_CNT3_COUNTER	0x402001C8
TCPWM_CNT3_CC	0x402001CC
TCPWM_CNT3_CC_BUFF	0x402001D0
TCPWM_CNT3_PERIOD	0x402001D4
TCPWM_CNT3_PERIOD_BUFF	0x402001D8
TCPWM_CNT3_TR_CTRL0	0x402001E0
TCPWM_CNT3_TR_CTRL1	0x402001E4
TCPWM_CNT3_TR_CTRL2	0x402001E8
TCPWM_CNT3_INTR	0x402001F0
TCPWM_CNT3_INTR_SET	0x402001F4
TCPWM_CNT3_INTR_MASK	0x402001F8
TCPWM_CNT3_INTR_MASKED	0x402001FC
TCPWM_CNT4_CTRL	0x40200200
TCPWM_CNT4_STATUS	0x40200204
TCPWM_CNT4_COUNTER	0x40200208
TCPWM_CNT4_CC	0x4020020C
TCPWM_CNT4_CC_BUFF	0x40200210
TCPWM_CNT4_PERIOD	0x40200214
TCPWM_CNT4_PERIOD_BUFF	0x40200218
TCPWM_CNT4_TR_CTRL0	0x40200220
TCPWM_CNT4_TR_CTRL1	0x40200224
TCPWM_CNT4_TR_CTRL2	0x40200228
TCPWM_CNT4_INTR	0x40200230
TCPWM_CNT4_INTR_SET	0x40200234
TCPWM_CNT4_INTR_MASK	0x40200238

Register Name	Address
TCPWM_CNT4_INTR_MASKED	0x4020023C
TCPWM_CNT5_CTRL	0x40200240
TCPWM_CNT5_STATUS	0x40200244
TCPWM_CNT5_COUNTER	0x40200248
TCPWM_CNT5_CC	0x4020024C
TCPWM_CNT5_CC_BUFF	0x40200250
TCPWM_CNT5_PERIOD	0x40200254
TCPWM_CNT5_PERIOD_BUFF	0x40200258
TCPWM_CNT5_TR_CTRL0	0x40200260
TCPWM_CNT5_TR_CTRL1	0x40200264
TCPWM_CNT5_TR_CTRL2	0x40200268
TCPWM_CNT5_INTR	0x40200270
TCPWM_CNT5_INTR_SET	0x40200274
TCPWM_CNT5_INTR_MASK	0x40200278
TCPWM_CNT5_INTR_MASKED	0x4020027C
TCPWM_CNT6_CTRL	0x40200280
TCPWM_CNT6_STATUS	0x40200284
TCPWM_CNT6_COUNTER	0x40200288
TCPWM_CNT6_CC	0x4020028C
TCPWM_CNT6_CC_BUFF	0x40200290
TCPWM_CNT6_PERIOD	0x40200294
TCPWM_CNT6_PERIOD_BUFF	0x40200298
TCPWM_CNT6_TR_CTRL0	0x402002A0
TCPWM_CNT6_TR_CTRL1	0x402002A4
TCPWM_CNT6_TR_CTRL2	0x402002A8
TCPWM_CNT6_INTR	0x402002B0
TCPWM_CNT6_INTR_SET	0x402002B4
TCPWM_CNT6_INTR_MASK	0x402002B8
TCPWM_CNT6_INTR_MASKED	0x402002BC
TCPWM_CNT7_CTRL	0x402002C0
TCPWM_CNT7_STATUS	0x402002C4
TCPWM_CNT7_COUNTER	0x402002C8
TCPWM_CNT7_CC	0x402002CC
TCPWM_CNT7_CC_BUFF	0x402002D0
TCPWM_CNT7_PERIOD	0x402002D4
TCPWM_CNT7_PERIOD_BUFF	0x402002D8
TCPWM_CNT7_TR_CTRL0	0x402002E0
TCPWM_CNT7_TR_CTRL1	0x402002E4
TCPWM_CNT7_TR_CTRL2	0x402002E8
TCPWM_CNT7_INTR	0x402002F0
TCPWM_CNT7_INTR_SET	0x402002F4
TCPWM_CNT7_INTR_MASK	0x402002F8

Register Name	Address
TCPWM_CNT7_INTR_MASKED	0x402002FC

5.1.1 TCPWM_CNT0_CTRL

Counter control register

Address: 0x40200100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

(continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

(continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

5.1.2 TCPWM_CNT0_STATUS

Counter status register

Address: 0x40200104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

5.1.3 TCPWM_CNT0_COUNTER

Counter count register

Address: 0x40200108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

5.1.4 TCPWM_CNT0_CC

Counter compare/capture register

Address: 0x4020010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

5.1.5 TCPWM_CNT0_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

5.1.6 TCPWM_CNT0_PERIOD

Counter period register

Address: 0x40200114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

5.1.7 TCPWM_CNT0_PERIOD_BUFF

Counter buffered period register

Address: 0x40200118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

5.1.8 TCPWM_CNT0_TR_CTRL0

Counter trigger control register 0

Address: 0x40200120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

(continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

5.1.9 TCPWM_CNT0_TR_CTRL1

Counter trigger control register 1

Address: 0x40200124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

(continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

5.1.10 TCPWM_CNT0_TR_CTRL2

Counter trigger control register 2

Address: 0x40200128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

(continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

5.1.11 TCPWM_CNT0_INTR

Interrupt request register.

Address: 0x40200130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

5.1.12 TCPWM_CNT0_INTR_SET

Interrupt set request register.

Address: 0x40200134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

5.1.13 TCPWM_CNT0_INTR_MASK

Interrupt mask register.

Address: 0x40200138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

5.1.14 TCPWM_CNT0_INTR_MASKED

Interrupt masked request register

Address: 0x4020013C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

5.1.15 TCPWM_CNT1_CTRL

Counter control register

Address: 0x40200140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

(continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

(continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

5.1.16 TCPWM_CNT1_STATUS

Counter status register

Address: 0x40200144

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

5.1.17 TCPWM_CNT1_COUNTER

Counter count register

Address: 0x40200148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

5.1.18 TCPWM_CNT1_CC

Counter compare/capture register

Address: 0x4020014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

5.1.19 TCPWM_CNT1_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

5.1.20 TCPWM_CNT1_PERIOD

Counter period register

Address: 0x40200154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

5.1.21 TCPWM_CNT1_PERIOD_BUFF

Counter buffered period register

Address: 0x40200158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

5.1.22 TCPWM_CNT1_TR_CTRL0

Counter trigger control register 0

Address: 0x40200160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

(continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

5.1.23 TCPWM_CNT1_TR_CTRL1

Counter trigger control register 1

Address: 0x40200164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

(continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

5.1.24 TCPWM_CNT1_TR_CTRL2

Counter trigger control register 2

Address: 0x40200168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

(continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

5.1.25 TCPWM_CNT1_INTR

Interrupt request register.

Address: 0x40200170

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

5.1.26 TCPWM_CNT1_INTR_SET

Interrupt set request register.

Address: 0x40200174

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

5.1.27 TCPWM_CNT1_INTR_MASK

Interrupt mask register.

Address: 0x40200178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

5.1.28 TCPWM_CNT1_INTR_MASKED

Interrupt masked request register

Address: 0x4020017C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

5.1.29 TCPWM_CNT2_CTRL

Counter control register

Address: 0x40200180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

(continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

(continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

5.1.30 TCPWM_CNT2_STATUS

Counter status register

Address: 0x40200184

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

5.1.31 TCPWM_CNT2_COUNTER

Counter count register

Address: 0x40200188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

5.1.32 TCPWM_CNT2_CC

Counter compare/capture register

Address: 0x4020018C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

5.1.33 TCPWM_CNT2_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

5.1.34 TCPWM_CNT2_PERIOD

Counter period register

Address: 0x40200194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

5.1.35 TCPWM_CNT2_PERIOD_BUFF

Counter buffered period register

Address: 0x40200198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

5.1.36 TCPWM_CNT2_TR_CTRL0

Counter trigger control register 0

Address: 0x402001A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

(continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

5.1.37 TCPWM_CNT2_TR_CTRL1

Counter trigger control register 1

Address: 0x402001A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

(continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

5.1.38 TCPWM_CNT2_TR_CTRL2

Counter trigger control register 2

Address: 0x402001A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

(continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

5.1.39 TCPWM_CNT2_INTR

Interrupt request register.

Address: 0x402001B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

5.1.40 TCPWM_CNT2_INTR_SET

Interrupt set request register.

Address: 0x402001B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

5.1.41 TCPWM_CNT2_INTR_MASK

Interrupt mask register.

Address: 0x402001B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

5.1.42 TCPWM_CNT2_INTR_MASKED

Interrupt masked request register

Address: 0x402001BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

5.1.43 TCPWM_CNT3_CTRL

Counter control register

Address: 0x402001C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

(continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

(continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

5.1.44 TCPWM_CNT3_STATUS

Counter status register

Address: 0x402001C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

5.1.45 TCPWM_CNT3_COUNTER

Counter count register

Address: 0x402001C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

5.1.46 TCPWM_CNT3_CC

Counter compare/capture register

Address: 0x402001CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

5.1.47 TCPWM_CNT3_CC_BUFF

Counter buffered compare/capture register

Address: 0x402001D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

5.1.48 TCPWM_CNT3_PERIOD

Counter period register

Address: 0x402001D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

5.1.49 TCPWM_CNT3_PERIOD_BUFF

Counter buffered period register

Address: 0x402001D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

5.1.50 TCPWM_CNT3_TR_CTRL0

Counter trigger control register 0

Address: 0x402001E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

(continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

5.1.51 TCPWM_CNT3_TR_CTRL1

Counter trigger control register 1

Address: 0x402001E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

(continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

5.1.52 TCPWM_CNT3_TR_CTRL2

Counter trigger control register 2

Address: 0x402001E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

(continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

5.1.53 TCPWM_CNT3_INTR

Interrupt request register.

Address: 0x402001F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

5.1.54 TCPWM_CNT3_INTR_SET

Interrupt set request register.

Address: 0x402001F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

5.1.55 TCPWM_CNT3_INTR_MASK

Interrupt mask register.

Address: 0x402001F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

5.1.56 TCPWM_CNT3_INTR_MASKED

Interrupt masked request register

Address: 0x402001FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

5.1.57 TCPWM_CNT4_CTRL

Counter control register

Address: 0x40200200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

(continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

(continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

5.1.58 TCPWM_CNT4_STATUS

Counter status register

Address: 0x40200204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

5.1.59 TCPWM_CNT4_COUNTER

Counter count register

Address: 0x40200208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

5.1.60 TCPWM_CNT4_CC

Counter compare/capture register

Address: 0x4020020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

5.1.61 TCPWM_CNT4_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

5.1.62 TCPWM_CNT4_PERIOD

Counter period register

Address: 0x40200214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

5.1.63 TCPWM_CNT4_PERIOD_BUFF

Counter buffered period register

Address: 0x40200218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

5.1.64 TCPWM_CNT4_TR_CTRL0

Counter trigger control register 0

Address: 0x40200220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

(continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

5.1.65 TCPWM_CNT4_TR_CTRL1

Counter trigger control register 1

Address: 0x40200224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

(continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

5.1.66 TCPWM_CNT4_TR_CTRL2

Counter trigger control register 2

Address: 0x40200228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

(continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

5.1.67 TCPWM_CNT4_INTR

Interrupt request register.

Address: 0x40200230

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

5.1.68 TCPWM_CNT4_INTR_SET

Interrupt set request register.

Address: 0x40200234

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

5.1.69 TCPWM_CNT4_INTR_MASK

Interrupt mask register.

Address: 0x40200238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

5.1.70 TCPWM_CNT4_INTR_MASKED

Interrupt masked request register

Address: 0x4020023C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

5.1.71 TCPWM_CNT5_CTRL

Counter control register

Address: 0x40200240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

(continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

(continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

5.1.72 TCPWM_CNT5_STATUS

Counter status register

Address: 0x40200244

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

5.1.73 TCPWM_CNT5_COUNTER

Counter count register

Address: 0x40200248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

5.1.74 TCPWM_CNT5_CC

Counter compare/capture register

Address: 0x4020024C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

5.1.75 TCPWM_CNT5_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

5.1.76 TCPWM_CNT5_PERIOD

Counter period register

Address: 0x40200254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

5.1.77 TCPWM_CNT5_PERIOD_BUFF

Counter buffered period register

Address: 0x40200258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

5.1.78 TCPWM_CNT5_TR_CTRL0

Counter trigger control register 0

Address: 0x40200260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

(continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

5.1.79 TCPWM_CNT5_TR_CTRL1

Counter trigger control register 1

Address: 0x40200264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

(continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

5.1.80 TCPWM_CNT5_TR_CTRL2

Counter trigger control register 2

Address: 0x40200268

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

(continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

5.1.81 TCPWM_CNT5_INTR

Interrupt request register.

Address: 0x40200270

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

5.1.82 TCPWM_CNT5_INTR_SET

Interrupt set request register.

Address: 0x40200274

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

5.1.83 TCPWM_CNT5_INTR_MASK

Interrupt mask register.

Address: 0x40200278

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

5.1.84 TCPWM_CNT5_INTR_MASKED

Interrupt masked request register

Address: 0x4020027C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

5.1.85 TCPWM_CNT6_CTRL

Counter control register

Address: 0x40200280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

(continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

(continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

5.1.86 TCPWM_CNT6_STATUS

Counter status register

Address: 0x40200284

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

5.1.87 TCPWM_CNT6_COUNTER

Counter count register

Address: 0x40200288

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

5.1.88 TCPWM_CNT6_CC

Counter compare/capture register

Address: 0x4020028C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

5.1.89 TCPWM_CNT6_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200290

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

5.1.90 TCPWM_CNT6_PERIOD

Counter period register

Address: 0x40200294

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

5.1.91 TCPWM_CNT6_PERIOD_BUFF

Counter buffered period register

Address: 0x40200298

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

5.1.92 TCPWM_CNT6_TR_CTRL0

Counter trigger control register 0

Address: 0x402002A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

(continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

5.1.93 TCPWM_CNT6_TR_CTRL1

Counter trigger control register 1

Address: 0x402002A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

(continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

5.1.94 TCPWM_CNT6_TR_CTRL2

Counter trigger control register 2

Address: 0x402002A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

(continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

5.1.95 TCPWM_CNT6_INTR

Interrupt request register.

Address: 0x402002B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

5.1.96 TCPWM_CNT6_INTR_SET

Interrupt set request register.

Address: 0x402002B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

5.1.97 TCPWM_CNT6_INTR_MASK

Interrupt mask register.

Address: 0x402002B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

5.1.98 TCPWM_CNT6_INTR_MASKED

Interrupt masked request register

Address: 0x402002BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

5.1.99 TCPWM_CNT7_CTRL

Counter control register

Address: 0x402002C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

(continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

(continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

5.1.100 TCPWM_CNT7_STATUS

Counter status register

Address: 0x402002C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

5.1.101 TCPWM_CNT7_COUNTER

Counter count register

Address: 0x402002C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

5.1.102 TCPWM_CNT7_CC

Counter compare/capture register

Address: 0x402002CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

5.1.103 TCPWM_CNT7_CC_BUFF

Counter buffered compare/capture register

Address: 0x402002D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

5.1.104 TCPWM_CNT7_PERIOD

Counter period register

Address: 0x402002D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

5.1.105 TCPWM_CNT7_PERIOD_BUFF

Counter buffered period register

Address: 0x402002D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

5.1.106 TCPWM_CNT7_TR_CTRL0

Counter trigger control register 0

Address: 0x402002E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

(continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

5.1.107 TCPWM_CNT7_TR_CTRL1

Counter trigger control register 1

Address: 0x402002E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

(continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

5.1.108 TCPWM_CNT7_TR_CTRL2

Counter trigger control register 2

Address: 0x402002E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

(continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

5.1.109 TCPWM_CNT7_INTR

Interrupt request register.

Address: 0x402002F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

5.1.110 TCPWM_CNT7_INTR_SET

Interrupt set request register.

Address: 0x402002F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

5.1.111 TCPWM_CNT7_INTR_MASK

Interrupt mask register.

Address: 0x402002F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

5.1.112 TCPWM_CNT7_INTR_MASKED

Interrupt masked request register

Address: 0x402002FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

6 CPU Sub System Registers

This section discusses the CPU Sub System (CPUSS) registers. It lists all the registers in mapping tables, in address order.

6.1 Register Details

Register Name	Address
CPUSS_SYSREQ	0x40100004
CPUSS_SYSARG	0x40100008
CPUSS_FLASH_CTL	0x40100030
CPUSS_ROM_CTL	0x40100034
CPUSS_RAM_CTL	0x40100038
CPUSS_DMAC_CTL	0x4010003C
CPUSS_SL_CTL0	0x40100100
CPUSS_SL_CTL1	0x40100104
CPUSS_SL_CTL2	0x40100108

6.1.1 CPUSS_SYSREQ

SYSCALL control register

Address: 0x40100004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SYSCALL_COMMAND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	SYSCALL_COMMAND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R	R	RW	RW	None		
HW Access	R	W	RW	A	R	None		
Name	SY-SCALL_REQ	HMAS-TER_0	ROM_AC-CESS_EN	PRIVI-LEGED	DIS_RE-SET_VECT_REL	None [26:24]		

Bits	Name	Description
31	SYSCALL_REQ	CPU/DAP writes a '1' to this field to request a SystemCall. The HMASTER_0 field indicates the source of the write access. Setting this field to '1' immediate results in a NMI. The SystemCall NMI interrupt handler sets this field to '0' after servicing the request. Default Value: 0
30	HMASTER_0	Indicates the source of the write access to the SYSREQ register. '0': CPU write access. '1': DAP write access. HW sets this field when the SYSREQ register is written to and SYSCALL_REQ is '0' (the last time it is set is when SW sets SYSCALL_REQ from '0' to '1'). Default Value: 0
29	ROM_ACCESS_EN	Indicates that executing from Boot ROM is enabled. HW sets this field to '1', on reset or when the SystemCall NMI vector is fetched from Boot ROM. HW sets this field to '0', when the CPU is NOT executing from either Boot or System ROM. This bit is used for debug purposes only. Default Value: 1

(continued)

28	PRIVILEGED	Indicates whether the system is in privileged ('1') or user mode ('0'). Only CPU SW executing from ROM can set this field to '1' when ROM_ACCESS_EN is '1' (the CPU is executing a SystemCall NMI interrupt handler). Any other write to this field sets is to '0'. This field is used as the AHB-Lite hprot[1] signal to implement Cypress proprietary user/privileged modes. These modes are used to enable/disable access to specific MMIO registers and memory regions. Default Value: 1
27	DIS_RESET_VECT_REL	Disable Reset Vector fetch relocation: '0': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are redirected to ROM. '1': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are made to flash. Note that this field defaults to '0' on reset, ensuring actual reset vector fetches are always made to ROM. Note that this field does not affect DAP accesses. Flash DfT routines may set this bit to '1' to enable uninhibited read-back of programmed data in the first flash page. Default Value: 0
15 : 0	SYSCALL_COMMAND	Opcode of the system call being requested. Default Value: 0

6.1.2 CPUSS_SYSARG

SYSARG control register

Address: 0x40100008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [31:24]							

Bits	Name	Description
31 : 0	SYSCALL_ARG	Argument to System Call specified in SYSREQ. Semantics of argument depends on system call made. Typically a pointer to a parameter block. Default Value: 0

6.1.3 CPUSS_FLASH_CTL

FLASH control register

Address: 0x40100030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			PREF_EN	None [3:2]		FLASH_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW1C
Name	None [15:9]							FLASH_IN-VALIDATE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU has priority "1": DW/DMA has priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0
8	FLASH_INVALIDATE	1': Invalidates the content of the flash controller's buffers. Default Value: 0
4	PREF_EN	Prefetch enable: '0': disabled. This is a desirable seeting when FLASH_WS is "0" or when predictable execution behavior is required. '1': enabled. Default Value: 0

(continued)

1 : 0	FLASH_WS	Amount of ROM wait states: "0": 0 wait states (fast flash: [0, 24] MHz system frequency, slow flash: [0, 16] MHz system frequency) "1": 1 wait state (fast flash: [24, 48] MHz system frequency, slow flash: [16, 32] MHz system frequency) "2": 2 wait states (slow flash: [32, 48] MHz system frequency) "3": 3 wait states (can be used to give more time for flash access if 2 wait states are not sufficient) Default Value: 0

6.1.4 CPUSS_ROM_CTL

ROM control register

Address: 0x40100034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ROM_WS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ROM_WS	Amount of ROM wait states: '0': 0 wait states. Use this setting for newer, faster ROM design. Use this setting for older, slower ROM design and frequencies in the range [0, 24] MHz. '1': 1 wait state. Use this setting for older, slower ROM design and frequencies in the range <24, 48] MHz. CPUSSv2 supports two types of ROM memory: an older, slower design (operating at up to 24 MHz) and a newer, faster design (operating at up to 48 MHz). The older design requires 1 wait state for frequencies above 24 MHz. The newer design never requires wait states. All chips after Street Fighter will use the newer design. As a result, all chips after Street Fighter can always use 0 wait states. Default Value: 0

6.1.5 CPUSS_RAM_CTL

RAM control register

Address: 0x40100038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU has priority "1": DW/DMA has priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0

6.1.6 CPUSS_DMAC_CTL

DMA controller register

Address: 0x4010003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU has priority "1": DW/DMA has priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0

6.1.7 CPUSS_SL_CTL0

Slave control register

Address: 0x40100100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU priority "1": DMA priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0

6.1.8 CPUSS_SL_CTL1

Slave control register

Address: 0x40100104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU priority "1": DMA priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0

6.1.9 CPUSS_SL_CTL2

Slave control register

Address: 0x40100108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU priority "1": DMA priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0

7 True Random Number Generator Registers

This section discusses the True Random Number Generator (TRNG) registers. It lists all the registers in mapping tables, in address order.

7.1 Register Details

Register Name	Address
TRNG_CTL	0x402C0000
TRNG_TR_CTL0	0x402C0280
TRNG_TR_CTL1	0x402C0284
TRNG_TR_RESULT0	0x402C0288
TRNG_TR_RESULT1	0x402C028C
TRNG_TR_CMD	0x402C0290
TRNG_TR_GARO_CTL	0x402C02A0
TRNG_TR_FIRO_CTL	0x402C02A4
TRNG_INTR	0x402C07C0
TRNG_INTR_SET	0x402C07C4
TRNG_INTR_MASK	0x402C07C8
TRNG_INTR_MASKED	0x402C07CC

7.1.1 TRNG_CTL

Control

Address: 0x402C0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	IP enable: '0': Disabled. All non-retention registers (command and status registers) are reset to their default value when the IP is disabled. All retention registers retain their value when the IP is disabled. '1': Enabled. Default Value: 0

7.1.2 TRNG_TR_CTL0

True random control 0

Address: 0x402C0280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_CLOCK_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RED_CLOCK_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INIT_DELAY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							VON_NEU-MAN-N_CORR

Bits	Name	Description
24	VON_NEUMANN_CORR	Specifies if the "von Neumann corrector" is disabled or enabled: '0': disabled. '1': enabled. The "von Neumann corrector" post-processes the reduced bits to remove a '0' or '1' bias. The corrector operates on reduced bit pairs ("oldest bit, newest bit"): "00": no bit is produced. "01": '0' bit is produced (oldest bit). "10": '1' bit is produced (oldest bit). "11": no bit is produced. Note that the corrector produces bits at a random pace and at a frequency that is 1/4 of the reduced bit frequency (reduced bits are processed in pairs, and half of the pairs do NOT produce a bit). Default Value: 0

(continued)

23 : 16	INIT_DELAY	Specifies an initialization delay: number of removed/dropped samples before reduced bits are generated. This field should be programmed in the range [1, 255]. After starting the oscillators, at least the first 2 samples should be removed/dropped to clear the state of internal synchronizers. In addition, it is advised to drop the second 2 samples from the oscillators (to circumvent the semi-predictable oscillator startup behavior). This result in the default field value of "3". Field encoding is as follows: "0": 1 sample is dropped. "1": 2 samples are dropped. "255": 256 samples are dropped. The TR_INITIALIZED interrupt cause is set to '1', when the initialization delay is passed. Default Value: 3
15 : 8	RED_CLOCK_DIV	Specifies the clock divider that is used to produce reduced bits. "0": 1 reduced bit is produced for each sample. "1": 1 reduced bit is produced for each 2 samples. "255": 1 reduced bit is produced for each 256 samples. The reduced bits are considered random bits and shifted into TR_RESULT0.DATA32. Default Value: 0
7 : 0	SAMPLE_CLOCK_DIV	Specifies the clock divider that is used to sample oscillator data. This clock divider is wrt. "clk_sys". "0": sample clock is "clk_sys". "1": sample clock is "clk_sys"/2. "255": sample clock is "clk_sys"/256. Default Value: 0

7.1.3 TRNG_TR_CTL1

True random control 1

Address: 0x402C0284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		DATA_BIT_SIZE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	DATA_BIT_SIZE	Specifies the number of desired of bits in the generated random number (legal range: [1, 32]). The TR_DATA_AVAILABLE interrupt cause is set to '1' when TR_RESULT1.DATA_BIT_SIZE >= DATA_BIT_SIZE. Default Value: 32

7.1.4 TRNG_TR_RESULT0

True random result 0

Address: 0x402C0288

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Generated true random number. HW generates the number in this field. When a new random bit is generated, it is shifted into the lowest bit position (DATA32[0]) and the highest bit position (DATA32[31]) is shifted out. Note that SW can write this field. This functionality can be used prevent information leakage. Default Value: 0

7.1.5 TRNG_TR_RESULT1

True random result 1

Address: 0x402C028C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		DATA_BIT_SIZE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	DATA_BIT_SIZE	Specifies the number of bits in the generated true random number (TR_RESULT0.DATA32). When a new random bit is generated, this field is incremented by '1'. The value is in the range [0, 32] (a saturating counter is used). Note that SW can write this field. This functionality can be used prevent information leakage. Typically, this field is updated/decremented in the interrupt handler. The interrupt handler decrements the field by the number of consumed bits. If the interrupt handler does NOT update this field (and TR_RESULT.DATA_BIT_SIZE is unchanged), the TR_DATA_AVAILABLE interrupt cause will remain activated. Therefore, proper interrupt based usage is as follows: - Consume bits from TR_RESULT0. - Write consumed bits in TR_RESULT0 to '0's (if information leakage needs to prevented). - Decrement TR_RESULT1 by the number of consumed bits. - Deactivate INTR.TR_DATA_AVAILABLE. Default Value: 0

7.1.6 TRNG_TR_CMD

True random command

Address: 0x402C0290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:6]		START_-FIRO31	START_-FIRO15	START_GA-RO31	START_GA-RO15	START_RO 15	START_RO 11

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	START_FIRO31	SW sets this field to '1' to start the programmable Fibonacci ring oscillator with up to 31 inverters. The TR_FIRO_CTL register specifies the programmable polynomial. Default Value: 0
4	START_FIRO15	SW sets this field to '1' to start the fixed Fibonacci ring oscillator with 15 inverters. Default Value: 0
3	START_GARO31	SW sets this field to '1' to start the programmable Galois ring oscillator with up to 31 inverters. The TR_GARO_CTL register specifies the programmable polynomial. Default Value: 0
2	START_GARO15	SW sets this field to '1' to start the fixed Galois ring oscillator with 15 inverters. Default Value: 0
1	START_RO15	SW sets this field to '1' to start the ring oscillator with 15 inverters. Default Value: 0
0	START_RO11	SW sets this field to '1' to start the ring oscillator with 11 inverters. Default Value: 0

7.1.7 TRNG_TR_GARO_CTL

True random GARO control

Address: 0x402C02A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	POLYNOMIAL31 [30:24]						

Bits	Name	Description
30 : 0	POLYNOMIAL31	Polynomial for programmable Galois ring oscillator. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 30 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Default Value: 0

7.1.8 TRNG_TR_FIRO_CTL

True random FIRO control

Address: 0x402C02A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	POLYNOMIAL31 [30:24]						

Bits	Name	Description
30 : 0	POLYNOMIAL31	Polynomial for programmable Fibonacci ring oscillator. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 30 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Default Value: 0

7.1.9 TRNG_INTR

Interrupt request

Address: 0x402C07C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	None					
HW Access	RW1S	RW1S	None					
Name	TR_-DATA_AVAILABLE	TR_INI-TIALIZED	None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TR_DATA_AVAILABLE	This interrupt cause is activated (HW sets the field to '1') when the true random number generator has generated a data value of the specified bit size: (TR_RESULT.DATA_BIT_SIZE >= TR_CTL.DATA_BIT_SIZE). See TR_RESULT1.DATA_BIT_SIZE for proper deactivation of this interrupt cause. Default Value: 0
6	TR_INITIALIZED	This interrupt cause is activated (HW sets the field to '1') when the true random number generator is initialized. Default Value: 0

7.1.10 TRNG_INTR_SET

Interrupt set request

Address: 0x402C07C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	None					
HW Access	A	A	None					
Name	TR_-DATA_AVAILABLE	TR_INI-TIALIZED	None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TR_DATA_AVAILABLE	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
6	TR_INITIALIZED	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0

7.1.11 TRNG_INTR_MASK

Interrupt mask

Address: 0x402C07C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	TR_-DATA_AVAILABLE	TR_INI-TIALIZED	None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TR_DATA_AVAILABLE	Mask bit for corresponding field in interrupt request register. Default Value: 0
6	TR_INITIALIZED	Mask bit for corresponding field in interrupt request register. Default Value: 0

7.1.12 TRNG_INTR_MASKED

Interrupt masked

Address: 0x402C07CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	None					
HW Access	W	W	None					
Name	TR_-DATA_AVAILABLE	TR_INI-TIALIZED	None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TR_DATA_AVAILABLE	Logical and of corresponding request and mask bits. Default Value: 0
6	TR_INITIALIZED	Logical and of corresponding request and mask bits. Default Value: 0

8 CapSense Sigma Delta Registers

This section discusses the CapSense Sigma Delta (CSD) registers. It lists all the registers in mapping tables, in address order.

8.1 Register Details

Register Name	Address
CSD_CONFIG	0x40290000
CSD_STATUS	0x40290080
CSD_STAT_SEQ	0x40290084
CSD_STAT_CNTS	0x40290088
CSD_STAT_HCNT	0x4029008C
CSD_RESULT_VAL1	0x402900D0
CSD_RESULT_VAL2	0x402900D4
CSD_ADC_RES	0x402900E0
CSD_INTR	0x402900F0
CSD_INTR_SET	0x402900F4
CSD_INTR_MASK	0x402900F8
CSD_INTR_MASKED	0x402900FC
CSD_HSCMP	0x40290180
CSD_AMBUF	0x40290184
CSD_REFGEN	0x40290188
CSD_CSDCMP	0x4029018C
CSD_IDACA	0x402901C0
CSD_IDACB	0x402901C4
CSD_SW_RES	0x402901F0
CSD_SENSE_PERIOD	0x40290200
CSD_SENSE_DUTY	0x40290204
CSD_SW_HS_P_SEL	0x40290280
CSD_SW_HS_N_SEL	0x40290284
CSD_SW_SHIELD_SEL	0x40290288
CSD_SW_HS_P_SEL1	0x4029028C
CSD_SW_AMUXBUF_SEL	0x40290290
CSD_SW_BYP_SEL	0x40290294

Register Name	Address
CSD_SW_CMP_P_SEL	0x402902A0
CSD_SW_CMP_N_SEL	0x402902A4
CSD_SW_REFGEN_SEL	0x402902A8
CSD_SW_FW_MOD_SEL	0x402902B0
CSD_SW_FW_TANK_SEL	0x402902B4
CSD_SW_DSI_SEL	0x402902C0
CSD_SEQ_TIME	0x40290300
CSD_SEQ_INIT_CNT	0x40290310
CSD_SEQ_NORM_CNT	0x40290314
CSD_ADC_CTL	0x40290320
CSD_SEQ_START	0x40290340

8.1.1 CSD_CONFIG

Configuration and Control

Address: 0x40290000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			RW	None		
HW Access	None	R			R	None		
Name	None	FILTER_DELAY [6:4]			LOW_VD-DA	None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	None	RW	None		RW	
HW Access	None	R	None	R	None		R	
Name	None	CHARGE_-MODE	None	SENSE_EN	None [11:10]		SHIELD_DELAY [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	None
HW Access	None				R	R	R	None
Name	None [23:20]				CSX_DU-AL_CNT	MUTUAL_-CAP	FULL_-WAVE	None

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None		RW	RW	RW	RW
HW Access	R	R	None		R	R	R	R
Name	ENABLE	LP_MODE	None [29:28]		DSI_-SENSE_EN	SAM-PLE_SYNC	DSI_SAM-PLE_EN	DSI_COUN T_SEL

Bits	Name	Description
31	ENABLE	Enables CapSense block. 0: All CapSense components will be OFF and switches will be open 1: All CapSense components will be ON and switches will be controlled by firmware or the Se-quencer Default Value: 0
30	LP_MODE	Select the power mode for the CSD components (REFGEN, AMBUF, CSDCMP, HSCMP): 0: High Power mode 1: Low Power mode Default Value: 0
27	DSI_SENSE_EN	Enables the use of the dsi_sense_in input instead of the internally generated clock to drive Sen-seClk and ShieldClk signals. 1: SenseClk is driven directly by DSI 0: SenseClk is driven by PRS/divide-by-2/DIRECT_CLOCK Default Value: 0

(continued)

26	SAMPLE_SYNC	Enables double synchronizing of sample input from DSI (only relevant when DSI_SAMPLE_EN=1). Default Value: 1
25	DSI_SAMPLE_EN	Enables the use of the dsi_sample_in input instead of the comparator output to strobe COUNTER. T 0: Counter will count the samples generated by CSD modulator 1: Counter will count the samples generated by DSI Default Value: 0
24	DSI_COUNT_SEL	Select dsi_count bus signal. Default Value: 0 **0x0: CSD_RESULT:** depending on the dsi_count_val_sel input either output RESULT_VAL1.VALUE (0) or RESULT_VAL2.VALUE (1) on the dsi_count bus. Note that dsi_count_val_sel is not synchronized, i.e. it controls the mux combinatorially. **0x1: ADC_RESULT:** output ADC_RES.VIN_CNT on the dsi_count bus
19	CSX_DUAL_CNT	Enable the use of two counters for MUTUAL cap sensing mode (CSX), do not use when MUTUAL_CAP=0 Default Value: 0 **0x0: ONE:** Use one counter for both phases (source and sink). **0x1: TWO:** Use two counters, separate count for when SenseClk is high and when SenseClk is low.
18	MUTUAL_CAP	Enables mutual cap sensing mode Default Value: 0 **0x0: SELFCAP:** Enables Self-cap mode **0x1: MUTUALCAP:** Enables Mutual-cap mode
17	FULL_WAVE	Enables full wave cap sensing mode Default Value: 0 **0x0: HALFWAVE:** Half Wave mode (normal). In this mode the comparator always trips in the same direction (positive or negative edge) and the same Vref, i.e. no polarity change. **0x1: FULLWAVE:** Full Wave mode. In this mode the comparator trips in opposite direction and with different Vref in each phase, i.e. the polarity flips.
14	CHARGE_MODE	Enable charging of the Cmod/Csh_tank capacitor using the GPIO digital output buffer using the csd_charge signal. Note that using the GPIO requires proper configuraiton of the GPIO pin. Default Value: 0 **0x0: CHARGE_OFF:** Use this to keep csd_charge signal low. For charging Cmod/Csh_tank capacitor CSD internal switches (HCBV) can be used but that is a separate configuration. **0x1: CHARGE_IO:** Use csd_charge to enable the GPIO Driver to charge capacitor. The capacitor must be sensed with HSCMP using the appropriate switches (HMPM or HMPT).

(continued)

12	SENSE_EN	Enables the SenseClk and ShieldClk, CSD modulator output and turns on the IDAC compensation current as selected by CSD_IDAC. Default Value: 0
9 : 8	SHIELD_DELAY	Configures the delay between ShieldClk and SenseClk signal. Default Value: 0 **0x0: OFF:** Delay line is off; ShieldClk=SenseClk **0x1: D5NS:** ShieldClk is delayed by 5ns delay w.r.t SenseClk **0x2: D10NS:** ShieldClk is delayed by 10ns delay w.r.t SenseClk **0x3: D20NS:** ShieldClk is delayed by 20ns delay w.r.t SenseClk
6 : 4	FILTER_DELAY	This value determines the number of cycles that the digital filter makes the CSDCMP output ignored while the counter counts and IDAC is on. When set to 0 the digital filter is off. When set to any other value the ignoring will last for FILTER_DELAY clk_csd cycles after the start of each measurement and from the first comparator trip to the end of each measurement. Default Value: 0
3	LOW_VDDA	Set this bit when VDDA is known to be below ~2V, this bit is used to improve IDACs performance at low voltages. Default Value: 0

8.1.2 CSD_STATUS

Status Register

Address: 0x40290080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				CSDC-MP_OUT	HSC-MP_OUT	CSD_-SENSE	CS-D_CHARGE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	CSDCMP_OUT	Output of main sensing comparator (synchronized) Default Value: 0
2	HSCMP_OUT	Output of reference buffer comparator used to charge up Cmod and/or Csh_tank (synchronized) Default Value: 0 **0x0: C_LT_VREF:** Vin < Vref **0x1: C_GT_VREF:** Vin > Vref
1	CSD_SENSE	Signal used to drive the Cs switches. Default Value: 0
0	CSD_CHARGE	Qualified, and possible inverted value of COMP_OUT that is used to drive GPIO's charging Cmod or Csh_tank. Default Value: 0

8.1.3 CSD_STAT_SEQ

Current Sequencer status

Address: 0x40290084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R		
HW Access	None					RW		
Name	None [7:3]					SEQ_STATE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					R		
HW Access	None					RW		
Name	None [23:19]					ADC_STATE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18 : 16	ADC_STATE	Specifies ADC sequencer current state (only relevant after SEQ_STATE has reached SAMPLE_NORM and ADC sequencer has started). Default Value: 0
2 : 0	SEQ_STATE	Specifes CSD sequencer current state. Default Value: 0

8.1.4 CSD_STAT_CNTS

Current status counts

Address: 0x40290088

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NUM_CONV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NUM_CONV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NUM_CONV	Specifies the current number of conversions remaining when in Sample_* states. This counter is also used in AutoZero* states to count the remaining AutoZero cycles. Default Value: 0

8.1.5 CSD_STAT_HCNT

Current count of the HSCMP counter

Address: 0x4029008C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CNT	Current value of HSCMP counter Default Value: 0

8.1.6 CSD_RESULT_VAL1

Result CSD/CSX accumulation counter value 1

Address: 0x402900D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	BAD_CONVS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BAD_CONVS	Number of 'bad' conversion for which the CSD comparator did not trigger within the normal time window, either because Vref was not crossed at all, or if the Vref was already crossed before the window started. This counter is reset when the sequencer is started and will saturate at 255 when more than 255 conversions are bad. Default Value: 0
15 : 0	VALUE	Specifies the raw count value for current conversion. In case of mutual-capacitance measurement and if dual counter is enabed, this counter counts only when SenseClk is high. Default Value: 0

8.1.7 CSD_RESULT_VAL2

Result CSX accumulation counter value 2

Address: 0x402900D4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	VALUE	Specifies the raw count value of second counter when mutual capacitance measurement with dual counter is enabled. This counter counts only when SenseClk is low. Default Value: 0

8.1.8 CSD_ADC_RES

ADC measurement

Address: 0x402900E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VIN_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VIN_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							HSC-MP_POL

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	RW	RW	None					
Name	AD-C_ABORT	AD-C_OVER-FLOW	None [29:24]					

Bits	Name	Description
31	ADC_ABORT	This flag is set when the ADC sequencer was aborted before tripping HSCMP. Default Value: 0
30	ADC_OVERFLOW	This flag is set when the ADC counter overflows. This is an indication to the firmware that the IDACB current level is too low. Default Value: 0
16	HSCMP_POL	Polarity used for IDACB for the last ADC result. 0: IDACB was in source mode 1: IDACB was in sink mode Default Value: 0
15 : 0	VIN_CNT	Specifies ADC counter value. The ADC counter value is equal to the time required to charge/discharge CREF1 + CREF2 capacitors from Vin to Vref or Vssa. Default Value: 0

8.1.9 CSD_INTR

CSD Interrupt Request Register

Address: 0x402900F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	None
HW Access	None					RW1S	RW1S	None
Name	None [7:3]					INIT	SAMPLE	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [15:9]							ADC_RES

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	ADC_RES	Interrupt register for ADC sequencer. This bit is set when ADC sequencer completes either calibration or input voltage measurement. Default Value: 0
2	INIT	Interrupt register for CSD sequencer. This bit is set when coarse initialization or sample initialization is complete. Default Value: 0
1	SAMPLE	Interrupt register for CSD sequencer. This bit is set when the normal sample state is complete. Default Value: 0

8.1.10 CSD_INTR_SET

CSD Interrupt set register

Address: 0x402900F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	None
HW Access	None					A	A	None
Name	None [7:3]					INIT	SAMPLE	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							ADC_RES

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	ADC_RES	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	INIT	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	SAMPLE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

8.1.11 CSD_INTR_MASK

CSD Interrupt mask register

Address: 0x402900F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	None
HW Access	None					R	R	None
Name	None [7:3]					INIT	SAMPLE	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							ADC_RES

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	ADC_RES	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	INIT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	SAMPLE	Mask bit for corresponding bit in interrupt request register. Default Value: 0

8.1.12 CSD_INTR_MASKED

CSD Interrupt masked register

Address: 0x402900FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	None
HW Access	None					W	W	None
Name	None [7:3]					INIT	SAMPLE	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							ADC_RES

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	ADC_RES	Logical and of corresponding request and mask bits. Default Value: 0
2	INIT	Logical and of corresponding request and mask bits. Default Value: 0
1	SAMPLE	Logical and of corresponding request and mask bits. Default Value: 0

8.1.13 CSD_HSCMP

High Speed Comparator configuration

Address: 0x40290180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [7:5]			HSCMP_IN-VERT	None [3:1]			HSC-MP_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	AZ_EN	None [30:24]						

Bits	Name	Description
31	AZ_EN	Enables or Disables Auto-Zero for HSCOMP. 0: Disable AutoZero 1: Enable AutoZero Default Value: 0
4	HSCMP_INVERT	Inverts the output of HSCMP before it is used to control switches and the CSD sequencer. This bit does not affect the ADC sequencer or the STATUS.HSCMP_OUT. Default Value: 0
0	HSCMP_EN	Enables or Disables HSCOMP. Default Value: 0 **0x0: OFF:** HSCOMP is disabled. **0x1: ON:** HSCOMP is enabled. CONFIG.LP_MODE determines the power mode level.

8.1.14 CSD_AMBUF

Reference Generator configuration

Address: 0x40290184

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	PWR_MODE	This field specifies the AMUXBUFFER power level. Default Value: 0 **0x0: OFF:** AMUXBUFFER is disabled. **0x1: NORM:** Enable AMUXBUFFER. Power level can be configured as normal or low power depending on CONFIG.LP_MODE. **0x2: HI:** Enable AMUXBUFFER. Power level can be configured as high or low power depending on CONFIG.LP_MODE.

8.1.15 CSD_REFGEN

Reference Generator configuration

Address: 0x40290188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None			RW
HW Access	None	R	R	R	None			R
Name	None	RES_EN	VDDA_EN	BYPASS	None [3:1]			REF-GEN_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			GAIN [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None		RW				
HW Access	R	None		R				
Name	VRE-FLO_INT	None [22:21]		VREFLO_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	VREFLO_INT	This field selects the output of the resistor string tap to either Vreflo or Vreflo_int. 0: Output of resistor string is Vreflo 1: Output of resistor string is Vreflo_int Default Value: 0
20 : 16	VREFLO_SEL	Selects resistor string tap for Vreflo/Vreflo_int. 0: minimum vout 31: maximum vout = vrefhi (only works if the resistor string is enabled; RES_EN=1) Default Value: 0
12 : 8	GAIN	Specifies resistor string tap for feedback. 0: minimum vout 31: maximum vout = vrefhi -> gain=1 Only works if the resistor string is enabled; RES_EN=1 Default Value: 0
6	RES_EN	Enables or Disables resistor string. 0: Open switch on top of the resistor string (Vreflo=Vssa). 1: Connect VREFHI to the resistor string. Default Value: 0

(continued)

5	VDDA_EN	This field when set closes Vdda switch to top of resistor string. Default Value: 0
4	BYPASS	This field when set bypasses the selected input reference unbuffered to Vrefhi. Default Value: 0
0	REFGEN_EN	Enables/Disables Reference Generator (REFGEN). Default Value: 0 **0x0: OFF:** REFGEN is disabled. **0x1: ON:** REFGEN is enabled. CONFIG.LP_MODE determines the power mode level.

8.1.16 CSD_CSDCMP

CSD Comparator configuration

Address: 0x4029018C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		None			RW
HW Access	None		R		None			R
Name	None [7:6]		POLARITY_SEL [5:4]		None [3:1]			CSDC-MP_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						CMP_PHASE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW	RW	None			
HW Access	R	None	R	R	None			
Name	AZ_EN	None	FEED-BACK_-MODE	CMP_-MODE	None [27:24]			

Bits	Name	Description
31	AZ_EN	Enables or Disables Auto-Zero for CSDCOMP. 0: Disable AutoZero 1: Enable AutoZero Default Value: 0
29	FEEDBACK_MODE	This field controls whether the direct output from CSDCOMP or the flopped version of CSD-COMP is used for CapSense operations. The selected signal controls the IDAC(s) during Cap-Sense operation and in general purpose mode the signal goes out on the dsi_sample_out. Default Value: 0 **0x0: FLOP:** Use feedback from sampling flip-flop (used in most modes). **0x1: COMP:** Use feedback from comparator directly.
28	CMP_MODE	Selects which signal to output on dsi_sample_out. Default Value: 0

(continued)

		0x0: CSD: CSD mode: Outputs the filtered sample signal on dsi_sample_out. **0x1: GP:** General Purpose mode: Outputs the unfiltered sample, unfiltered comparator output, either asynchronous or flopped.
9 : 8	CMP_PHASE	This field is used to select in what phase(s) the CSDCOMP is active. This field also determines when a bad conversion is detected i.e. at the beginning and/or at the end of the comparator active phase. Default Value: 0 **0x0: FULL:** Comparator is active from start of Phi2 and kept active into Phi1. This mode is used for regular self-cap scanning. **0x1: PHI1:** Comparator is active during Phi1 only. This mode is not used currently. **0x2: PHI2:** Comparator is active during Phi2 only. This mode is used for low-EMI scanning. **0x3: PHI1_2:** Comparator is activated at the start of both Phi1 and Phi2 (non-overlap should be enabled). This mode is used for mutual-cap sensing.
5 : 4	POLARITY_SEL	This field selects which IDAC polarity to use to detect CSDCMP triggering. Default Value: 0 **0x0: IDACA_POL:** Use idaca_pol (firmware setting with CSX and optionally DSI mixed in) to determine the direction, this is the most common use-case, used for normal CSD and normal CSX **0x1: IDACB_POL:** Use idacb_pol (firmware setting with optional DSI mixed in) to determine the direction, this is only used for normal CSD if IDACB is used i.s.o. IDACA (not common) **0x2: DUAL_POL:** Use the expression (SenseClk? idaca_pol : idacb_pol) to determine the direction, this is only useful for the CSX with DUAL_IDAC use-case
0	CSDCMP_EN	This field is used to enable or disable CSD Comparator. Default Value: 0 **0x0: OFF:** Disable CSDCOMP. **0x1: ON:** Enable CSDCOMP. CONFIG.LP_MODE determines the power mode level.

8.1.17 CSD_IDACA

IDACA Configuration

Address: 0x402901C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	POL_DYN	VAL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				BAL_MODE [11:10]		POLARITY [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW	None	RW		RW	
HW Access	R		R	None	R		R	
Name	RANGE [23:22]		DSI_C-TRL_EN	None	LEG2_MODE [19:18]		LEG1_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						LEG2_EN	LEG1_EN

Bits	Name	Description
25	LEG2_EN	output enable for leg 2 to CSDBUSA Default Value: 0
24	LEG1_EN	output enable for leg 1 to CSDBUSA Default Value: 0
23 : 22	RANGE	IDAC multiplier Default Value: 0 **0x0: IDAC_LO:** 1 LSB = 37.5 nA **0x1: IDAC_MED:** 1 LSB = 300 nA **0x2: IDAC_HI:** 1 LSB = 2400 nA **0x3: IDAC_MED2:** 1 LSB = 1200 nA

(continued)

21	DSI_CTRL_EN	Mix DSI inputs with MMIO controls or not (before getting mixed with CSD controls if enabled). 0: no DSI control IDACA_POLARITY = IDACA.POLARITY IDACA_LEG1_EN = IDACA.LEG1_EN IDACA_LEG2_EN = IDACA.LEG2_EN 1: Mix MMIO with DSI control IDACA_POLARITY = IDACA.POLARITY EXOR dsi_idaca_pol IDACA_LEG1_EN = IDACA.LEG1_EN AND dsi_idaca_leg1_en IDACA_LEG2_EN = IDACA.LEG2_EN AND dsi_idaca_leg2_en Default Value: 0
19 : 18	LEG2_MODE	Controls the usage mode of LEG2 Default Value: 0 **0x0: GP_STATIC:** General Purpose static mode: LEG2 is controlled by MMIO and optionally mixed with DSI (see DSI_CTRL_EN). No shunting is used, this saves power when off but also any on/off switching will take longer. **0x1: GP:** General Purpose dynamic mode: LEG2 is controlled by MMIO and optionally mixed with DSI (see DSI_CTRL_EN). Shunting is used, so on/off switching is faster, but power is wasted when the leg is disabled. **0x2: CSD_STATIC:** CSD static mode: LEG2 can only be on when the CSD Sequencer is in the Sample_init or Sample_norm state. In those states LEG2 is controlled by LEG2_EN, csd_sense and the CSD configuration. Polarity is controlled by the CSD configuration and operation. In addition leg2 enable and polarity can optionally be mixed with DSI (see DSI_CTRL_EN). No shunting is used, this saves power when off but also any on/off switching will take longer. **0x3: CSD:** CSD dynamic mode: LEG2 can only be on when the CSD Sequencer is in the Sample_init or Sample_norm state. In those states LEG2 is controlled by LEG2_EN, the CSD configuration, csd_sense and the flopped CSDCMP output (CSDCMP_OUT_FF). In addition leg2 enable can optionally be mixed with DSI (see DSI_CTRL_EN). Shunting is used, so on/off switching is faster, but power is wasted when the leg is disabled.
17 : 16	LEG1_MODE	Controls the usage mode of LEG1 and the Polarity bit Default Value: 0 **0x0: GP_STATIC:** General Purpose static mode: LEG1 and POLARITY are controlled by MMIO and optionally mixed with DSI (see DSI_CTRL_EN). No shunting is used, this saves power when off but also any on/off switching will take longer. **0x1: GP:** General Purpose dynamic mode: LEG1 and POLARITY are controlled by MMIO and optionally mixed with DSI (see DSI_CTRL_EN). Shunting is used, so on/off switching is faster, but power is wasted when the leg is disabled. **0x2: CSD_STATIC:** CSD static mode: LEG1 can only be on when the CSD Sequencer is in the Sample_init or Sample_norm state. In those states LEG1 is controlled by LEG1_EN, csd_sense and the CSD configuration. Polarity is controlled by the CSD configuration and operation. In addition leg1 enable and polarity can optionally be mixed with DSI (see DSI_CTRL_EN). No shunting is used, this saves power when off but also any on/off switching will take longer.

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		0x3: CSD: CSD dynamic mode: LEG1 can only be on when the CSD Sequencer is in the Sample_init or Sample_norm state. In thoses states LEG1 is controlled by LEG1_EN, the CSD configuration, csd_sense and the flopped CSDCMP output (CSDCMP_OUT_FF). Polarity is controlled by the CSD configuration and operation. In addition leg1 enable and polarity can optionally be mixed with DSI (see DSI_CTRL_EN). Shunting is used, so on/off switching is faster, but power is wasted when the leg is disabled.
11 : 10	BAL_MODE	Balancing mode: only applies to legs configured as CSD. Default Value: 0 **0x0: FULL:** enabled from start of Phi2 until disabled by CSDCMP. Intended usage: legacy CSD for balancing over a full csd_sense period (non-overlap should be turned off) **0x1: PHI1:** enabled from start of Phi1 and disabled by CSDCMP or at end of Phi1. Enables dual IDAC CSX or Full-Wave, one for sourcing and the other for sinking. **0x2: PHI2:** enabled from start of Phi2 and disabled by CSDCMP or at end of Phi2. Intended usage: CSD Low EMI or dual IDAC CSX or Full-Wave. **0x3: PHI1_2:** enabled from start of both Phi1 and Phi2 and disabled by CSDCMP or at end of Phi1 or Phi2 (if non-overlap enabled). Intended usage: single IDAC CSX, or Full-Wave.
9 : 8	POLARITY	Selects the polarity of the IDAC (sensing operation). Normally the actual polarity depends on this bit, optionally mixed with DSI (see DSI_CTRL_EN) and if LEG1_MODE==CSD also mixed with the CSD configuration and operation. However in mutual cap mode with one IDAC (config.mutual_cap=1 & config.csx_dual_idac=0) the polarity of the IDAC is controlled by csd_sense. Default Value: 0 **0x0: VSSA_SRC:** Normal: sensor switching between Vssio and Cmod. For non-CSD application, IDAC1 will source current. **0x1: VDDA_SNK:** Inverted: sensor switch between Vddio and Cmod. For non-CSD application, IDAC1 will sink current. **0x2: SENSE:** The polarity of the IDAC will follow the csd_sense signal (POL_DYN bit should be set too). The intended usage is for CSX using a single IDAC. **0x3: SENSE_INV:** The polarity of the IDAC will follow the inverted csd_sense signal (POL_DYN bit should be set too). The intended usage is for CSX using a single IDAC.
7	POL_DYN	Polarity is dynamic, this bit does not influence the logic in the SoftIP, it only goes to the HardIP. Default Value: 0 **0x0: STATIC:** Static polarity. Polarity is expected to be stable, so to save power this avoids the shunting of the unused polarity, at the expense of response time. **0x1: DYNAMIC:** Dynamic polarity. Polarity is expected to change frequently (e.g. invert after every csd_sense phase), so to improve response time this keeps the shunt of the unused polarity on at the expense of power.
6 : 0	VAL	Current value setting for this IDAC (7 bits). Default Value: 0

8.1.18 CSD_IDACB

IDACB Configuration

Address: 0x402901C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	POL_DYN	VAL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				BAL_MODE [11:10]		POLARITY [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW	None	RW		RW	
HW Access	R		R	None	R		R	
Name	RANGE [23:22]		DSI_C-TRL_EN	None	LEG2_MODE [19:18]		LEG1_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [31:27]					LEG3_EN	LEG2_EN	LEG1_EN

Bits	Name	Description
26	LEG3_EN	output enable for leg3 to CSDBUSC, only allowed when RANGE = IDAC_LO. When this bit is set both other legs should be off. Note that leg3 can only be used for ADC mode, not GP mode. Which means that leg3 can only be on when the ADC Sequencer is in the ADC_measure or Calib_measure state. In those states leg3 is controlled by the ADC configuration and the HSCMP output. In addition this leg3 enable bit can optionally be mixed with DSI (see DSI_CTRL_EN). When LEG3_EN=1 also the IDACB polarity is controlled by the ADC sequencer. Default Value: 0
25	LEG2_EN	output enable for leg 2 to CSDBUSB or CSDBUSA Default Value: 0
24	LEG1_EN	output enable for leg 1 to CSDBUSB or CSDBUSA Default Value: 0
23 : 22	RANGE	IDAC multiplier Default Value: 0 **0x0: IDAC_LO:** 1 LSB = 37.5 nA

(continued)

		0x1: IDAC_MED: 1 LSB = 300 nA **0x2: IDAC_HI:** 1 LSB = 2400 nA **0x3: IDAC_MED2:** 1 LSB = 1200 nA
21	DSI_CTRL_EN	Mix DSI inputs with MMIO controls or not (before getting mixed with CSD controls if enabled) 0: no DSI control IDACB_POLARITY = IDACB.POLARITY IDACB_LEG1_EN = IDACB.LEG1_EN IDACB_LEG2_EN = IDACB.LEG2_EN IDACB_LEG3_EN = IDACB.LEG3_EN 1: Mix MMIO with DSI control IDACB_POLARITY = IDACB.POLARITY EXOR dsi_idacb_pol IDACB_LEG1_EN = IDACB.LEG1_EN AND dsi_idacb_leg1_en IDACB_LEG2_EN = IDACB.LEG2_EN AND dsi_idacb_leg2_en IDACB_LEG3_EN = IDACB.LEG3_EN AND dsi_idacb_leg3_en Default Value: 0
19 : 18	LEG2_MODE	Controls the usage mode of LEG2 Default Value: 0 **0x0: GP_STATIC:** same as corresponding IDACA.LEG2_MODE **0x1: GP:** same as corresponding IDACA.LEG2_MODE **0x2: CSD_STATIC:** same as corresponding IDACA.LEG2_MODE **0x3: CSD:** same as corresponding IDACA.LEG2_MODE
17 : 16	LEG1_MODE	Controls the usage mode of LEG1 and the Polarity bit Default Value: 0 **0x0: GP_STATIC:** same as corresponding IDACA.LEG1_MODE **0x1: GP:** same as corresponding IDACA.LEG1_MODE **0x2: CSD_STATIC:** same as corresponding IDACA.LEG1_MODE **0x3: CSD:** same as corresponding IDACA.LEG1_MODE
11 : 10	BAL_MODE	same as corresponding IDACA Balancing mode Default Value: 0 **0x0: FULL:** same as corresponding IDACA Balancing mode **0x1: PHI1:** same as corresponding IDACA Balancing mode **0x2: PHI2:** same as corresponding IDACA Balancing mode

(continued)

		0x3: PHI1_2: same as corresponding IDACA Balancing mode
9 : 8	POLARITY	Selects the polarity of the IDAC (sensing operation). Normally the actual polarity depends on this bit, optionally mixed with DSI (see DSI_CTRL_EN) and if LEG1_EN==1 and LEG1_-MODE==CSD also mixed with the CSD configuration and operation. In mutual cap mode however (see config.mutual_cap) the polarity of the IDAC is controlled by csd_sense. If LEG3_EN=1 (the other two legs must be off) then the ADC sequencer controls the IDACB polarity, optionally mixed with DSI. Default Value: 0 **0x0: VSSA_SRC:** Normal: sensor switching between Vssio and Cmod. For non-CSD application, IDAC1 will source current. **0x1: VDDA_SNK:** Inverted: sensor switch between Vddio and Cmod. For non-CSD application, IDAC1 will sink current. **0x2: SENSE:** The polarity of the IDAC will follow the csd_sense signal (POL_DYN bit should be set too). The intended usage is for CSX using a single IDAC. **0x3: SENSE_INV:** The polarity of the IDAC will follow the inverted csd_sense signal (POL_DYN bit should be set too). The intended usage is for CSX using a single IDAC.
7	POL_DYN	Polarity is dynamic, this bit does not influence the logic in the SoftIP, it only goes to the HardIP. Default Value: 0 **0x0: STATIC:** Static polarity. Polarity is expected to be stable, so to save power this avoids the shunting of the unused polarity, at the expense of response time. **0x1: DYNAMIC:** Dynamic polarity. Polarity is expected to change frequently (e.g. invert after every csd_sense phase), so to improve response time this keeps the shunt of the unused polarity on at the expense of power.
6 : 0	VAL	Current value setting for this IDAC (7 bits). Default Value: 0

8.1.19 CSD_SW_RES

Switch Resistance configuration

Address: 0x402901F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	RES_HCBG [7:6]		RES_HCBV [5:4]		RES_HCAG [3:2]		RES_HCAV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [23:20]				RES_F2PT [19:18]		RES_F1PM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 18	RES_F2PT	Select resistance for the corresponding switch Default Value: 0
17 : 16	RES_F1PM	Select resistance for the corresponding switch Default Value: 0 **0x0: LOW:** Low **0x1: MED:** Medium **0x2: HIGH:** High **0x3: RESERVED:** reserved
7 : 6	RES_HCBG	Select resistance or low EMI for the corresponding switch Default Value: 0
5 : 4	RES_HCBV	Select resistance or low EMI for the corresponding switch Default Value: 0

(continued)

3 : 2	RES_HCAG	Select resistance or low EMI for the corresponding switch Default Value: 0
1 : 0	RES_HCAV	Select resistance or low EMI (slow ramp) for the HCAV switch Default Value: 0 **0x0: LOW:** Low **0x1: MED:** Medium **0x2: HIGH:** High **0x3: LOWEMI:** Low EMI (slow ramp: 3 switches closed by fixed delay line)

8.1.20 CSD_SENSE_PERIOD

Sense clock period

Address: 0x40290200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SENSE_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				SENSE_DIV [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				None	RW		
HW Access	R				None	R		
Name	LFSR_SCALE [23:20]				None	LFSR_SIZE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW		RW	RW1S
HW Access	None				R		R	RW1C
Name	None [31:28]				LFSR_BITS [27:26]		SEL_LFS-R_MSB	LFSR_-CLEAR

Bits	Name	Description
27 : 26	LFSR_BITS	Selects the number of LSB bits to use from the LSFR to provide the clock dithering variation on the base period. Caveat make sure that SENSE_DIV > the maximum absolute range (e.g. for 4B SENSE_DIV > 8), otherwise results are undefined. Default Value: 3 **0x0: 2B:** use 2 bits: range = [-2,1] **0x1: 3B:** use 3 bits: range = [-4,3] **0x2: 4B:** use 4 bits: range = [-8,7] **0x3: 5B:** use 5 bits: range = [-16,15] (default)
25	SEL_LFSR_MSB	Use the MSB of configured LSFR size as SenseClk signal. Intended to be used only with bit 8 or 12-bit LFSR size. When this bit is set then clock divider dithering is disabled. Default Value: 0

(continued)

24	LFSR_CLEAR	When set, forces the LFSR to it's initial state (all ones). This bit is automatically cleared by hardware after the LFSR is cleared, which is at the next clk_csd positive edge. This bit should be set whenever this register is written and the LFSR is used. Note that the LFSR will also get reset to all ones during the AutoZero_1/2 states. Default Value: 0
23 : 20	LFSR_SCALE	Shift the LFSR output left by LSFR_SCALE bits before adding to SENSE_DIV. This dithering is disabled when SEL_LSFR_MSB is set. The clock divider to be used = (SENSE_DIV+1) + (SEL_LSFR_MSB ? 0 : (LFSR_OUT<_SCALE)). Note that the clock divider including the dithering term must fit in 12 bits, otherwise the result is undefined. Default Value: 0
18 : 16	LFSR_SIZE	Selects the length of the LFSR which determines the LFSR repeat period. LFSR_BITS LSB of the LFSR are used for the clock dithering variation on the base period. Whenever the LFSR is used (non zero value in this field) the LFSR_CLEAR bit should also be set. Default Value: 0 **0x0: OFF:** Don't use clock dithering (=spreadspectrum) (LFSR output value is zero) **0x1: 6B:** 6-bit LFSR (G(x)=X^6 +X^4+X^3+ X+1, period= 63) **0x2: 7B:** 7-bit LFSR (G(x)=X^7 +X^4+X^3+X^2+1, period= 127) **0x3: 9B:** 9-bit LFSR (G(x)=X^9 +X^4+X^3+ X+1, period= 511) **0x4: 10B:** 10-bit LFSR (G(x)=X^10+X^4+X^3+ X+1, period= 1023) **0x5: 8B:** 8-bit LFSR (G(x)=X^8+X^4+X^3+X^2+1, period= 255) **0x6: 12B:** 12-bit LFSR (G(x)=X^12+X^7+X^4+X^3+1, period= 4095)
11 : 0	SENSE_DIV	This field specifies the period of SenseClk interms of SampleClk period. The value in this register is the base divider. If clock dithering is enabled, the actual period changes depending on the LFSR value. Default Value: 0

8.1.21 CSD_SENSE_DUTY

Sense clock duty cycle

Address: 0x40290204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SENSE_WIDTH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				SENSE_WIDTH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	None	RW
HW Access	None				R	R	None	R
Name	None [23:20]				OVER-LAP_PHI2	OVER-LAP_PHI1	None	SENSE_POL

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	OVERLAP_PHI2	Same as OVERLAP_PHI1 but for Phi2 (csd_sense=1). Default Value: 0
18	OVERLAP_PHI1	This field specifies whether Ph1 signal is non-overlapping signal or 'NOT' of SenseClk. 0: Non-overlap for Phi1, the Phi1 signal is SenseClk inverted except that the signal goes low 1 SampleClk before SenseClk goes high. This mode is used for low EMI sensing and mutual-cap sensing with static GPIO. 1: Overlap for Phi1, the Phi1 signal is csd_sense inverted. This mode is used for normal self-cap sensing with GPIO switching. The GPIO internal circuit ensures that the switches are non-overlapping. Default Value: 0
16	SENSE_POL	This field specifies the polarity of the SenseClk 0 = start with low phase (Regular negative transfer SelfCap scanning) 1 = start with high phase Default Value: 0

(continued)

11 : 0	SENSE_WIDTH	Defines the length of the first phase of the SenseClk in terms of SampleClk cycles. A value of 0 disables this feature and the duty cycle of SenseClk will be 50%, which is equal to SENSE_WIDTH = (SENSE_DIV+1)/2, or when clock dithering is used that becomes [(SENSE_DIV+1) + (LFSR_OUT << LSFR_SCALE)]/2. At all times it must be assured that the phases are at least 2 SampleClk cycles (1 for non overlap), if this rule is violated the result is undefined. Default Value: 0

8.1.22 CSD_SW_HS_P_SEL

HSCMP Pos input switch Waveform selection

Address: 0x40290280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [7:5]			SW_HMPT	None [3:1]			SW_HMPM

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [15:13]			SW_HMMA	None [11:9]			SW_HMPS

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [23:21]			SW_HMCA	None [19:17]			SW_HMMB

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [31:29]			SW_HMRH	None [27:25]			SW_HMCB

Bits	Name	Description
28	SW_HMRH	Set corresponding switch Default Value: 0
24	SW_HMCB	Set corresponding switch Default Value: 0
20	SW_HMCA	Set corresponding switch Default Value: 0
16	SW_HMMB	Set corresponding switch Default Value: 0
12	SW_HMMA	Set corresponding switch Default Value: 0
8	SW_HMPS	Set corresponding switch Default Value: 0
4	SW_HMPT	Set corresponding switch Default Value: 0

(continued)

0	SW_HMPM	Set HMPM switch 0: static open 1: static closed Default Value: 0

8.1.23 CSD_SW_HS_N_SEL

HSCMP Neg input switch Waveform selection

Address: 0x40290284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [23:21]			SW_HCCD	None [19:17]			SW_HCCC

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	SW_HCRL [30:28]			None	SW_HCRH [26:24]		

Bits	Name	Description
30 : 28	SW_HCRL	Select waveform for corresponding switch Default Value: 0
26 : 24	SW_HCRH	Select waveform for corresponding switch Default Value: 0
20	SW_HCCD	Set corresponding switch Default Value: 0
16	SW_HCCC	Set corresponding switch Default Value: 0

8.1.24 CSD_SW_SHIELD_SEL

Shielding switches Waveform selection

Address: 0x40290288

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	SW_HCAG [6:4]			None	SW_HCAV [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	SW_HCBG [14:12]			None	SW_HCBV [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [23:21]			SW_HCCG	None [19:17]			SW_HCCV

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20	SW_HCCG	Set corresponding switch If the ADC is enabled then this switch is directly controlled by the ADC sequencer. Default Value: 0
16	SW_HCCV	Set corresponding switch Default Value: 0
14 : 12	SW_HCBG	Select waveform for corresponding switch, using csd_shield as base Default Value: 0
10 : 8	SW_HCBV	Select waveform for HCBV switch. The waveform for this switch follows the csd_shield signal, i.e. phi1 and phi2 are delayed with SHIELD_DELAY w.r.t. the csd_sense phases. Only this switch and HCBG use csd_shield as base all other switches use csd_sense as base. 0: static open 1: static closed 2: phi1_delay 3: phi2_delay 4: phi1_delay & HSCMP 5: phi2_delay & HSCMP 6: HSCMP (ignores phi1/2) 7: Reserved Default Value: 0

(continued)

6 : 4	SW_HCAG	Select waveform for corresponding switch Default Value: 0
2 : 0	SW_HCAV	Select waveform for HCAV switch using csd_sense as base 0: static open 1: static closed 2: phi1 3: phi2 4: phi1 & HSCMP 5: phi2 & HSCMP 6: HSCMP (ignores phi1/2) 7: Reserved Default Value: 0

8.1.25 CSD_SW_HS_P_SEL1

HSCMP Pos input switch Waveform selection 1

Address: 0x4029028C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							SW_HMRE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	SW_HMRE	Set HMRE switch 0: static open 1: static closed Default Value: 0

8.1.26 CSD_SW_AMUXBUF_SEL

Amuxbuffer switches Waveform selection

Address: 0x40290290

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None			
HW Access	None			R	None			
Name	None [7:5]			SW_IRBY	None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [15:13]			SW_ICA	None [11:9]			SW_IRLB

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	None	RW		
HW Access	None			R	None	R		
Name	None [23:21]			SW_IRLI	None	SW_ICB [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [31:29]			SW_IRL	None [27:25]			SW_IRH

Bits	Name	Description
28	SW_IRL	Set corresponding switch Default Value: 0
24	SW_IRH	Set corresponding switch Default Value: 0
20	SW_IRLI	Set corresponding switch Default Value: 0
18 : 16	SW_ICB	Select waveform for corresponding switch Default Value: 0
12	SW_ICA	Set corresponding switch Default Value: 0
8	SW_IRLB	Set corresponding switch Default Value: 0
4	SW_IRBY	Set corresponding switch Default Value: 0

8.1.27 CSD_SW_BYP_SEL

AMUXBUS bypass switches Waveform selection

Address: 0x40290294

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None			
HW Access	None			R	None			
Name	None [15:13]			SW_BYA	None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [23:21]			SW_CBCC	None [19:17]			SW_BYB

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20	SW_CBCC	Set corresponding switch If the ADC is enabled then this switch is directly controlled by the ADC sequencer. Default Value: 0
16	SW_BYB	Set corresponding switch Default Value: 0
12	SW_BYA	Set corresponding switch Default Value: 0

8.1.28 CSD_SW_CMP_P_SEL

CSDCMP Pos Switch Waveform selection

Address: 0x402902A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	SW_SFPT [6:4]			None	SW_SFPM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None	RW		
HW Access	None			R	None	R		
Name	None [15:13]			SW_SFMA	None	SW_SFPS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [23:21]			SW_SFCA	None [19:17]			SW_SFMB

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							SW_SFCB

Bits	Name	Description
24	SW_SFCB	Set corresponding switch Default Value: 0
20	SW_SFCA	Set corresponding switch Default Value: 0
16	SW_SFMB	Set corresponding switch Default Value: 0
12	SW_SFMA	Set corresponding switch Default Value: 0
10 : 8	SW_SFPS	Select waveform for corresponding switch Default Value: 0
6 : 4	SW_SFPT	Select waveform for corresponding switch Default Value: 0
2 : 0	SW_SFPM	Select waveform for corresponding switch Default Value: 0

8.1.29 CSD_SW_CMP_N_SEL

CSDCMP Neg Switch Waveform selection

Address: 0x402902A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	SW_SCRL [30:28]			None	SW_SCRH [26:24]		

Bits	Name	Description
30 : 28	SW_SCRL	Select waveform for corresponding switch Default Value: 0
26 : 24	SW_SCRH	Select waveform for corresponding switch Default Value: 0

8.1.30 CSD_SW_REFGEN_SEL

Reference Generator Switch Waveform selection

Address: 0x402902A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [7:5]			SW_IBCB	None [3:1]			SW_IAIB

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							SW_SGMB

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [31:29]			SW_SGR	None [27:25]			SW_SGRE

Bits	Name	Description
28	SW_SGR	Set corresponding switch Default Value: 0
24	SW_SGRE	Set corresponding switch Default Value: 0
16	SW_SGMB	Set corresponding switch Default Value: 0
4	SW_IBCB	Set corresponding switch Default Value: 0
0	SW_IAIB	Set corresponding switch Default Value: 0

8.1.31 CSD_SW_FW_MOD_SEL

Full Wave Cmod Switch Waveform selection

Address: 0x402902B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							SW_F1PM

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					SW_F1MA [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	None	RW		
HW Access	None			R	None	R		
Name	None [23:21]			SW_C1CC	None	SW_F1CA [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [31:29]			SW_C1F1	None [27:25]			SW_C1CD

Bits	Name	Description
28	SW_C1F1	Set corresponding switch Default Value: 0
24	SW_C1CD	Set corresponding switch Default Value: 0
20	SW_C1CC	Set corresponding switch Default Value: 0
18 : 16	SW_F1CA	Select waveform for corresponding switch Default Value: 0
10 : 8	SW_F1MA	Select waveform for corresponding switch Default Value: 0
0	SW_F1PM	Set corresponding switch Default Value: 0

8.1.32 CSD_SW_FW_TANK_SEL

Full Wave Csh_tank Switch Waveform selection

Address: 0x402902B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None			
HW Access	None			R	None			
Name	None [7:5]			SW_F2PT	None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	SW_F2CA [14:12]			None	SW_F2MA [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	None	RW		
HW Access	None			R	None	R		
Name	None [23:21]			SW_C2CC	None	SW_F2CB [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	None			RW
HW Access	None			R	None			R
Name	None [31:29]			SW_C2F2	None [27:25]			SW_C2CD

Bits	Name	Description
28	SW_C2F2	Set corresponding switch Default Value: 0
24	SW_C2CD	Set corresponding switch Default Value: 0
20	SW_C2CC	Set corresponding switch Default Value: 0
18 : 16	SW_F2CB	Select waveform for corresponding switch Default Value: 0
14 : 12	SW_F2CA	Select waveform for corresponding switch Default Value: 0
10 : 8	SW_F2MA	Select waveform for corresponding switch Default Value: 0
4	SW_F2PT	Set corresponding switch Default Value: 0

8.1.33 CSD_SW_DSI_SEL

DSI output switch control Waveform selection

Address: 0x402902C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	DSI_CMOD [6:4]			None	DSI_CSH_TANK [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 4	DSI_CMOD	This field selects waveform for dsi_cmod signal. Default Value: 0
2 : 0	DSI_CSH_TANK	This field selects waveform for dsi_csh_tank signal. Default Value: 0

8.1.34 CSD_SEQ_TIME

Sequencer Timing

Address: 0x40290300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	AZ_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	AZ_TIME	This field specifies the AutoZero duration in terms of SenseClk cycles. Default Value: 0

8.1.35 CSD_SEQ_INIT_CNT

Sequencer Initial conversion and sample counts

Address: 0x40290310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONV_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONV_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONV_CNT	Number of conversion per sample, if set to 0 the Sample_init state will be skipped. Default Value: 0

8.1.36 CSD_SEQ_NORM_CNT

Sequencer Normal conversion and sample counts

Address: 0x40290314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONV_CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONV_CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONV_CNT	Number of conversion per sample, if set to 0 the Sample_norm state will be skipped. Sample window size = SEQ_NORM_CNT.CONV_CNT * (SENSE_PERIOD.SENSE_DIV+1). Default Value: 0

8.1.37 CSD_ADC_CTL

ADC Control

Address: 0x40290320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADC_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ADC_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ADC_MODE	Enables ADC measurement. When enabled the ADC sequencer will be started when the CSD sequencer goes to the SAMPLE_NORM state. Default Value: 0 **0x0: OFF:** No ADC measurement **0x1: VREF_CNT:** Count time A to bring Cref1 + Cref2 up from Vssa to Vrefhi with IDACB. **0x2: VREF_BY2_CNT:** Count time B to bring Cref1 + Cref2 back up to Vrefhi with IDACB (after bringing them down for time A/2 cycles with IDACB sinking). **0x3: VIN_CNT:** Determine HSCMP polarity and count time C to source/sink Cref1 + Cref2 from Vin to Vrefhi.
7 : 0	ADC_TIME	This field specifies the duration for which ADC captures the input voltage or discharges the CREF1 and CREF2 capacitors. The duration is specified interms of SenseClk cycles. Default Value: 0

8.1.38 CSD_SEQ_START

Sequencer start

Address: 0x40290340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW1C	None	RW	RW1S
HW Access	None			R	A	None	R	RW1C
Name	None [7:5]			DSI_START _EN	ABORT	None	SEQ_- MODE	START

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						AZ1_SKIP	AZ0_SKIP

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	AZ1_SKIP	When set the AutoZero_1 state will be skipped Default Value: 0
8	AZ0_SKIP	When set the AutoZero_0 state will be skipped Default Value: 0
4	DSI_START_EN	When this bit is set a positive edge on dsi_start will start the CSD sequencer and if enabled also the ADC sequencer. Default Value: 0
3	ABORT	When a 1 is written the CSD and ADC sequencers will be aborted (if they are running) and the START bit will be cleared. This bit always read as 0. Default Value: 0
1	SEQ_MODE	0 = regular CSD scan + optional ADC 1 = coarse initialization, the Sequencer will go to the INIT_COARSE state. Default Value: 0

(continued)

0	START	Start the CSD sequencer. The sequencer will clear this bit when it is done. Depending on the mode the sequencer is done when a sample has been accumulated, when the high speed comparator trips or if the sequencer is aborted. When the ADC is enabled the ADC sequencer will start when the CSD sequencer reaches the Sample_norm state (only with the regular CSD scan mode). Default Value: 0

9 Continuous Time Block Mini Registers

This section discusses the Continuous Time Block Mini (CTBM) registers. It lists all the registers in mapping tables, in address order.

9.1 Register Details

Register Name	Address
CTBM0_CTB_CTRL	0x40300000
CTBM0_OA_RES0_CTRL	0x40300004
CTBM0_OA_RES1_CTRL	0x40300008
CTBM0_COMP_STAT	0x4030000C
CTBM0_INTR	0x40300020
CTBM0_INTR_SET	0x40300024
CTBM0_INTR_MASK	0x40300028
CTBM0_INTR_MASKED	0x4030002C
CTBM0_DFT_CTRL	0x40300030
CTBM0_OA0_SW	0x40300080
CTBM0_OA0_SW_CLEAR	0x40300084
CTBM0_OA1_SW	0x40300088
CTBM0_OA1_SW_CLEAR	0x4030008C
CTBM0_CTB_SW_HW_CTRL	0x403000C0
CTBM0_CTB_SW_STATUS	0x403000C4
CTBM0_OA0_OFFSET_TRIM	0x40300F00
CTBM0_OA0_SLOPE_OFFSET_TRIM	0x40300F04
CTBM0_OA0_COMP_TRIM	0x40300F08
CTBM0_OA1_OFFSET_TRIM	0x40300F0C
CTBM0_OA1_SLOPE_OFFSET_TRIM	0x40300F10
CTBM0_OA1_COMP_TRIM	0x40300F14

9.1.1 CTBM0_CTB_CTRL

global CTB and power control

Address: 0x40300000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	DEEPS-LEEP_ON	None [29:24]					

Bits	Name	Description
31	ENABLED	0: CTBm block disabled (analog in power down, all switches open) 1: CTBm block enabled Default Value: 0
30	DEEPSLEEP_ON	0: CTBm block disabled off during Deep Sleep power mode 1: CTBm block remains enabled during Deep Sleep power mode (if ENABLED=1) Default Value: 0

9.1.2 CTBM0_OA_RES0_CTRL

Opamp0 and resistor0 control

Address: 0x40300004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	
HW Access	R	R	R	R	None	R	R	
Name	OA0_DSI_LEVEL	OA0_BY-PASS_DSI_SYNC	OA0_HYST_EN	OA0_COM-P_EN	None	OA0_DRIVE_STR_-SEL	OA0_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				OA0_PUMP_EN	None	OA0_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	OA0_PUMP_EN	Opamp 0 pump enable Default Value: 0
9 : 8	OA0_COMPINT	Opamp 0 comparator edge detect for interrupt and pulse mode of DSI output Default Value: 0 **0x0: DISABLE:** Disabled, no interrupts will be detected **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

(continued)

7	OA0_DSI_LEVEL	Opamp 0 comparator output (DSI) output type 0: Pulse (each time an edge is detected (see OA0_COMPINT bit), a pulse is sent out on DSI) 1: Level (DSI output is a synchronized version of the comparator output) Default Value: 0
6	OA0_BY-PASS_DSI_SYNC	Opamp 0 bypass comparator output (DSI) synchronization 0: Synchronize (level or pulse) 1: Bypass (output async) Default Value: 0
5	OA0_HYST_EN	Opamp 0 hysteresis (10mV) enable 0: Hysteresis disabled 1: Hysteresis enabled Default Value: 0
4	OA0_COMP_EN	Opamp 0 comparator mode enable 0: Opamp mode 1: Comparator mode Default Value: 0
2	OA0_DRIVE_STR_SEL	Opamp 0 output strength select 0: 1x 1: 10x Default Value: 0
1 : 0	OA0_PWR_MODE	Sets the opamp 0 power level Default Value: 0 **0x0: OFF:** Off **0x1: LOW:** Low Power **0x2: MEDIUM:** Medium Power **0x3: HIGH:** High Power

9.1.3 CTBM0_OA_RES1_CTRL

Opamp1 and resistor1 control

Address: 0x40300008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	
HW Access	R	R	R	R	None	R	R	
Name	OA1_DSI_LEVEL	OA1_BY-PASS_DSI_SYNC	OA1_HYST_EN	OA1_COM-P_EN	None	OA1_DRIVE_STR_-SEL	OA1_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				OA1_PUMP_EN	None	OA1_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	OA1_PUMP_EN	Opamp 1 pump enable Default Value: 0
9 : 8	OA1_COMPINT	Opamp 1 comparator edge detect for interrupt and pulse mode of DSI output Default Value: 0 **0x0: DISABLE:** Disabled, no interrupts will be detected **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

(continued)

7	OA1_DSI_LEVEL	Opamp 1 comparator output (DSI) output type 0: Pulse (each time an edge is detected (see OA0_COMPINT bit), a pulse is sent out on DSI) 1: Level (DSI output is a synchronized version of the comparator output) Default Value: 0
6	OA1_BY-PASS_DSI_SYNC	Opamp 1 bypass comparator output (DSI) synchronization 0: Synchronize (level or pulse) 1: Bypass (output async) Default Value: 0
5	OA1_HYST_EN	Opamp 1 hysteresis (10mV) enable 0: Hysteresis disabled 1: Hysteresis enabled Default Value: 0
4	OA1_COMP_EN	Opamp 1 comparator mode enable 0: Opamp mode 1: Comparator mode Default Value: 0
2	OA1_DRIVE_STR_SEL	Opamp 1 output strength select 0: 1x 1: 10x Default Value: 0
1 : 0	OA1_PWR_MODE	Sets the opamp 1 power level 0: Off 1: Low 2: Medium 3: High Default Value: 0

9.1.4 CTBM0_COMP_STAT

Comparator status

Address: 0x4030000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							OA0_-COMP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							OA1_-COMP

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	OA1_COMP	Opamp1 current comparator status Default Value: 0
0	OA0_COMP	Opamp0 current comparator status Default Value: 0

9.1.5 CTBM0_INTR

Interrupt request register

Address: 0x40300020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 1 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP0	Comparator 0 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

9.1.6 CTBM0_INTR_SET

Interrupt request set register

Address: 0x40300024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP1_SET	COMP0_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

9.1.7 CTBM0_INTR_MASK

Interrupt request mask

Address: 0x40300028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP1_MASK	COMP0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

9.1.8 CTBM0_INTR_MASKED

Interrupt request masked

Address: 0x4030002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP1_MASKED	COMP0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

9.1.9 CTBM0_DFT_CTRL

Was 'Analog DfT controls', now used as Risk Mitigation bits (RMP)

Address: 0x40300030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DFT_MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DFT_EN	None [30:24]						

Bits	Name	Description
31	DFT_EN	this bit is combined with the 3 bits 2:0, to form RMP[3:0] Default Value: 0
2 : 0	DFT_MODE	this bit is combined with bit 31, to form RMP[3:0], it must always be written with '3' for correct operation. Default Value: 0

9.1.10 CTBM0_OA0_SW

Opamp0 switch control

Address: 0x40300080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	None	RW1S
HW Access	None				RW1C	RW1C	None	RW1C
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None		RW1S	None	
HW Access	None		RW1C	None		RW1C	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	Shorts 1x and 10x output drive of Opamp 0 Default Value: 0
18	OA0O_D51	Connects Opamp 0 output to sarbus0 Default Value: 0
14	OA0M_A81	Connects Opamp 0 negative terminal to Opamp 0 output Default Value: 0
8	OA0M_A11	Connects Opamp 0 negative terminal to P1[1] Default Value: 0
3	OA0P_A30	Connects Opamp 0 positive terminal to ctbbus0 Default Value: 0
2	OA0P_A20	Connects Opamp 0 positive terminal to P1[0] Default Value: 0
0	OA0P_A00	Connects Opamp 0 positive terminal to AMUXBUSA Default Value: 0

9.1.11 CTBM0_OA0_SW_CLEAR

Opamp0 switch control clear

Address: 0x40300084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	None	RW1C
HW Access	None				A	A	None	A
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None		RW1C	None	
HW Access	None		A	None		A	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	see corresponding bit in OA0_SW Default Value: 0
18	OA0O_D51	see corresponding bit in OA0_SW Default Value: 0
14	OA0M_A81	see corresponding bit in OA0_SW Default Value: 0
8	OA0M_A11	see corresponding bit in OA0_SW Default Value: 0
3	OA0P_A30	see corresponding bit in OA0_SW Default Value: 0
2	OA0P_A20	see corresponding bit in OA0_SW Default Value: 0
0	OA0P_A00	see corresponding bit in OA0_SW Default Value: 0

9.1.12 CTBM0_OA1_SW

Opamp1 switch control

Address: 0x40300088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None		RW1S	RW1S
HW Access	None			RW1C	None		RW1C	RW1C
Name	None [7:5]			OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None	RW1S	RW1S	None	
HW Access	None		RW1C	None	RW1C	RW1C	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	Shorts 1x and 10x output drive of Opamp 0 Default Value: 0
19	OA1O_D62	Connects Opamp 1 output to sarbus1 Default Value: 0
18	OA1O_D52	Connects Opamp 1 output to sarbus0 Default Value: 0
14	OA1M_A82	Connects Opamp 1 negative terminal to Opamp 1 output Default Value: 0
8	OA1M_A22	Connects Opamp 1 negative terminal to P1[4] Default Value: 0
4	OA1P_A43	Connects Opamp 1 positive terminal to ctbbus1 Default Value: 0
1	OA1P_A13	Connects Opamp 1 positive terminal to P1[5] Default Value: 0
0	OA1P_A03	Connects Opamp 1 positive terminal to AMUXBUSB Default Value: 0

9.1.13 CTBM0_OA1_SW_CLEAR

Opamp1 switch control clear

Address: 0x4030008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None		RW1C	RW1C
HW Access	None			A	None		A	A
Name	None [7:5]			OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None	RW1C	RW1C	None	
HW Access	None		A	None	A	A	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	see corresponding bit in OA1_SW Default Value: 0
19	OA1O_D62	see corresponding bit in OA1_SW Default Value: 0
18	OA1O_D52	see corresponding bit in OA1_SW Default Value: 0
14	OA1M_A82	see corresponding bit in OA1_SW Default Value: 0
8	OA1M_A22	see corresponding bit in OA1_SW Default Value: 0
4	OA1P_A43	see corresponding bit in OA1_SW Default Value: 0
1	OA1P_A13	see corresponding bit in OA1_SW Default Value: 0
0	OA1P_A03	see corresponding bit in OA1_SW Default Value: 0

9.1.14 CTBM0_CTB_SW_HW_CTRL

CTB bus switch control

Address: 0x403000C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [7:4]				P3_HW_C-TRL	P2_HW_C-TRL	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	P3_HW_CTRL	Hardware control of switch D52 and D62 Default Value: 0
2	P2_HW_CTRL	Hardware control of switch D51 Default Value: 0

9.1.15 CTBM0_CTB_SW_STATUS

CTB bus switch control status

Address: 0x403000C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	R	R	R	None			
HW Access	None	W	W	W	None			
Name	None	OA1O_D62_STAT	OA1O_D52_STAT	OA0O_D51_STAT	None [27:24]			

Bits	Name	Description
30	OA1O_D62_STAT	Switch D62 status Default Value: 0
29	OA1O_D52_STAT	Switch D52 status Default Value: 0
28	OA0O_D51_STAT	Switch D51 status Default Value: 0

9.1.16 CTBM0_OA0_OFFSET_TRIM

Opamp0 trim control

Address: 0x40300F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_OFFSET_TRIM	Opamp 0 Offset Trim. Bits[4:0] controls the amount of offset and bit[5] controls the polarity of offset ('1' indicates positive offset and '0' indicates negative offset) Default Value: 0

9.1.17 CTBM0_OA0_SLOPE_OFFSET_TRIM

Opamp0 trim control

Address: 0x40300F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_SLOPE_OFF-SET_TRIM	Opamp 0 offset temperature compensation bits. Bits[4:0] controls the slope magnitude and bit[5] controls the polarity ('1' indicates positive trim direction and '0' indicates negative trim direction) Default Value: 0

9.1.18 CTBM0_OA0_COMP_TRIM

Opamp0 trim control

Address: 0x40300F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA0_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA0_COMP_TRIM	Opamp0 Compenation Capacitor Trim Default Value: 0

9.1.19 CTBM0_OA1_OFFSET_TRIM

Opamp1 trim control

Address: 0x40300F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_OFFSET_TRIM	Opamp 1 Offset Trim. Bits[4:0] controls the amount of offset and bit[5] controls the polarity of offset ('1' indicates positive offset and '0' indicates negative offset) Default Value: 0

9.1.20 CTBM0_OA1_SLOPE_OFFSET_TRIM

Opamp1 trim control

Address: 0x40300F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_SLOPE_OFF-SET_TRIM	Opamp 1 offset temperature compensation bits. Bits[4:0] controls the slope magnitude and bit[5] controls the polarity ('1' indicates positive trim direction and '0' indicates negative trim direction) Default Value: 0

9.1.21 CTBM0_OA1_COMP_TRIM

Opamp1 trim control

Address: 0x40300F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA1_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA1_COMP_TRIM	Opamp1 Compenation Capacitor Trim Default Value: 0

10 Direct-Memory Access Registers

This section discusses the Direct-Memory Access (DMAC) registers. It lists all the registers in mapping tables, in address order.

10.1 Register Details

Register Name	Address
DMAC_CTL	0x40101000
DMAC_STATUS	0x40101010
DMAC_STATUS_SRC_ADDR	0x40101014
DMAC_STATUS_DST_ADDR	0x40101018
DMAC_STATUS_CH_ACT	0x4010101C
DMAC_CH_CTL0	0x40101080
DMAC_CH_CTL1	0x40101084
DMAC_CH_CTL2	0x40101088
DMAC_CH_CTL3	0x4010108C
DMAC_CH_CTL4	0x40101090
DMAC_CH_CTL5	0x40101094
DMAC_CH_CTL6	0x40101098
DMAC_CH_CTL7	0x4010109C
DMAC_INTR	0x401017F0
DMAC_INTR_SET	0x401017F4
DMAC_INTR_MASK	0x401017F8
DMAC_INTR_MASKED	0x401017FC

10.1.1 DMAC_CTL

Control register

Address: 0x40101000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	0': IP is disabled. Non-retainable MMIO registers and logic functionality are reset (retainable MMIO registers are NOT reset): - INTR register is set to "0". - DW/DMA functionality is aborted. - DW/DMA controller input/pending triggers are de-activated. - DW/DMA controller output triggers are de-activated. Disabling the IP has the same effect as an active "rst_sys_act_n" reset in DeepSleep power mode. To prevent a loss of active (pending) DW/DMA triggers when disabling the IP or when transitioning from Active to DeepSleep power mode, the STATUS.ACTIVE and STATUS_CH_ACTIVE.CH fields can be used. Note that most MMIO registers are retainable, and a transition from DeepSleep to Active/Sleep power modes makes the DW/DMA controller operational, and ready to react to DW/DMA input triggers that are activated after the transition. Triggers are Active/Sleep functionality. '1': IP is enabled. Default Value: 0

10.1.2 DMAC_STATUS

Status register

Address: 0x40101010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					R		
HW Access	None					W		
Name	None [23:19]					CH_ADDR [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R		None	R		
HW Access	W	W	W		None	W		
Name	ACTIVE	PING_PONG	PRIO [29:28]		None	STATE [26:24]		

Bits	Name	Description
31	ACTIVE	Specifies if there is a currently active (pending) channel in the data transfer engine: 0: no currently active channel. 1: currently active channel. Default Value: 0
30	PING_PONG	Specifies whether the PING descriptor (0) or PONG descriptor (1) of the channel is currently in use. Default Value: Undefined
29 : 28	PRIO	Specifies the priority of the currently active channel. Default Value: Undefined
26 : 24	STATE	State of the data transfer engine. 0: DEFAULT state. 1: Loading descriptor (SRC, DST, CONTROL and STATUS words). 2: Loading data element from source location. 3: Storing data element to destination location. 4: Storing descriptor (STATUS word). 5: Wait for trigger de-activation. 6: Storing descriptor with error response (STATUS word). Default Value: 0

(continued)

18 : 16	CH_ADDR	Specifies the channel number of the currently active channel. E.g. if we have 32 channels, the channel number address with CH_ADDR_WIDTH is LOG2 (32) = 5, and this field is a 5-bit field. If channel 7 is active, STATUS.ACTIVE is '1' and STATUS.CH_ADDR is "7". Default Value: Undefined
15 : 0	DATA_NR	Specifies the index of the currently active data transfer. This value increases from "0" to CONTROL.DATA_NR. Default Value: Undefined

10.1.3 DMAC_STATUS_SRC_ADDR

Source address status register

Address: 0x40101014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address or current address of source location of currently active channel. The specific address information is cycle dependent. This is field is provided for debug purposes. Functionally, no assumption should be made on whether the base or current address is provided. The specifics of the currently active channel are available through STATUS. Note while reading the STATUS, STATUS_SRC and STATUS_DST registers, the transfer engine may have moved from one active channel to another. Default Value: Undefined

10.1.4 DMAC_STATUS_DST_ADDR

Destination address register

Address: 0x40101018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address or current address of destination location of currently active channel. The specific address information is cycle dependent. This is field is provided for debug purposes. Functionally, no assumption should be made on whether the base or current address is provided. The specifics of the currently active channel are available through STATUS. Note while reading the STATUS, STATUS_SRC and STATUS_DST registers, the transfer engine may have moved from one active channel to another. Default Value: Undefined

10.1.5 DMAC_STATUS_CH_ACT

Channel activation status register

Address: 0x4010101C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Channel activation status. Bit i is associated to channel i, with i = 0, , CH_NR-1. Software reads this field to get information on all actively pending channels (either in pending or in the data transfer engine). Default Value: 0

10.1.6 DMAC_CH_CTL0

Channel control register

Address: 0x40101080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.7 DMAC_CH_CTL1

Channel control register

Address: 0x40101084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.8 DMAC_CH_CTL2

Channel control register

Address: 0x40101088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.9 DMAC_CH_CTL3

Channel control register

Address: 0x4010108C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.10 DMAC_CH_CTL4

Channel control register

Address: 0x40101090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.11 DMAC_CH_CTL5

Channel control register

Address: 0x40101094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.12 DMAC_CH_CTL6

Channel control register

Address: 0x40101098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.13 DMAC_CH_CTL7

Channel control register

Address: 0x4010109C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.14 DMAC_INTR

Interrupt register

Address: 0x401017F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. Default Value: 0

10.1.15 DMAC_INTR_SET

Interrupt set register

Address: 0x401017F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0

10.1.16 DMAC_INTR_MASK

Interrupt mask register

Address: 0x401017F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Mask for corresponding field in INTR register. Default Value: 0

10.1.17 DMAC_INTR_MASKED

Interrupt masked register

Address: 0x401017FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Logical and of corresponding request and mask fields. Default Value: 0

11 Direct-Memory Access Descriptor Registers

This section discusses the Direct-Memory Access Descriptor (DMAC_DESCR) registers. It lists all the registers in mapping tables, in address order.

11.1 Register Details

Register Name	Address
DMAC_DESCR0_PING_SRC	0x40101800
DMAC_DESCR0_PING_DST	0x40101804
DMAC_DESCR0_PING_CTL	0x40101808
DMAC_DESCR0_PING_STATUS	0x4010180C
DMAC_DESCR0_PONG_SRC	0x40101810
DMAC_DESCR0_PONG_DST	0x40101814
DMAC_DESCR0_PONG_CTL	0x40101818
DMAC_DESCR0_PONG_STATUS	0x4010181C
DMAC_DESCR1_PING_SRC	0x40101820
DMAC_DESCR1_PING_DST	0x40101824
DMAC_DESCR1_PING_CTL	0x40101828
DMAC_DESCR1_PING_STATUS	0x4010182C
DMAC_DESCR1_PONG_SRC	0x40101830
DMAC_DESCR1_PONG_DST	0x40101834
DMAC_DESCR1_PONG_CTL	0x40101838
DMAC_DESCR1_PONG_STATUS	0x4010183C
DMAC_DESCR2_PING_SRC	0x40101840
DMAC_DESCR2_PING_DST	0x40101844
DMAC_DESCR2_PING_CTL	0x40101848
DMAC_DESCR2_PING_STATUS	0x4010184C
DMAC_DESCR2_PONG_SRC	0x40101850
DMAC_DESCR2_PONG_DST	0x40101854
DMAC_DESCR2_PONG_CTL	0x40101858
DMAC_DESCR2_PONG_STATUS	0x4010185C
DMAC_DESCR3_PING_SRC	0x40101860
DMAC_DESCR3_PING_DST	0x40101864
DMAC_DESCR3_PING_CTL	0x40101868

Register Name	Address
DMAC_DESCR3_PING_STATUS	0x4010186C
DMAC_DESCR3_PONG_SRC	0x40101870
DMAC_DESCR3_PONG_DST	0x40101874
DMAC_DESCR3_PONG_CTL	0x40101878
DMAC_DESCR3_PONG_STATUS	0x4010187C
DMAC_DESCR4_PING_SRC	0x40101880
DMAC_DESCR4_PING_DST	0x40101884
DMAC_DESCR4_PING_CTL	0x40101888
DMAC_DESCR4_PING_STATUS	0x4010188C
DMAC_DESCR4_PONG_SRC	0x40101890
DMAC_DESCR4_PONG_DST	0x40101894
DMAC_DESCR4_PONG_CTL	0x40101898
DMAC_DESCR4_PONG_STATUS	0x4010189C
DMAC_DESCR5_PING_SRC	0x401018A0
DMAC_DESCR5_PING_DST	0x401018A4
DMAC_DESCR5_PING_CTL	0x401018A8
DMAC_DESCR5_PING_STATUS	0x401018AC
DMAC_DESCR5_PONG_SRC	0x401018B0
DMAC_DESCR5_PONG_DST	0x401018B4
DMAC_DESCR5_PONG_CTL	0x401018B8
DMAC_DESCR5_PONG_STATUS	0x401018BC
DMAC_DESCR6_PING_SRC	0x401018C0
DMAC_DESCR6_PING_DST	0x401018C4
DMAC_DESCR6_PING_CTL	0x401018C8
DMAC_DESCR6_PING_STATUS	0x401018CC
DMAC_DESCR6_PONG_SRC	0x401018D0
DMAC_DESCR6_PONG_DST	0x401018D4
DMAC_DESCR6_PONG_CTL	0x401018D8
DMAC_DESCR6_PONG_STATUS	0x401018DC
DMAC_DESCR7_PING_SRC	0x401018E0
DMAC_DESCR7_PING_DST	0x401018E4
DMAC_DESCR7_PING_CTL	0x401018E8
DMAC_DESCR7_PING_STATUS	0x401018EC
DMAC_DESCR7_PONG_SRC	0x401018F0
DMAC_DESCR7_PONG_DST	0x401018F4
DMAC_DESCR7_PONG_CTL	0x401018F8
DMAC_DESCR7_PONG_STATUS	0x401018FC

11.1.1 DMAC_DESCR0_PING_SRC

Ping source address

Address: 0x40101800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.2 DMAC_DESCR0_PING_DST

Ping destination address

Address: 0x40101804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.3 DMAC_DESCR0_PING_CTL

Ping control word

Address: 0x40101808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.4 DMAC_DESCR0_PING_STATUS

Ping status word

Address: 0x4010180C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.5 DMAC_DESCR0_PONG_SRC

Pong source address

Address: 0x40101810

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.6 DMAC_DESCR0_PONG_DST

Pong destination address

Address: 0x40101814

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.7 DMAC_DESCR0_PONG_CTL

Pong control word

Address: 0x40101818

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.8 DMAC_DESCR0_PONG_STATUS

Pong status word

Address: 0x4010181C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

11.1.9 DMAC_DESCR1_PING_SRC

Ping source address

Address: 0x40101820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.10 DMAC_DESCR1_PING_DST

Ping destination address

Address: 0x40101824

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.11 DMAC_DESCR1_PING_CTL

Ping control word

Address: 0x40101828

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.12 DMAC_DESCR1_PING_STATUS

Ping status word

Address: 0x4010182C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.13 DMAC_DESCR1_PONG_SRC

Pong source address

Address: 0x40101830

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.14 DMAC_DESCR1_PONG_DST

Pong destination address

Address: 0x40101834

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.15 DMAC_DESCR1_PONG_CTL

Pong control word

Address: 0x40101838

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.16 DMAC_DESCR1_PONG_STATUS

Pong status word

Address: 0x4010183C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

11.1.17 DMAC_DESCR2_PING_SRC

Ping source address

Address: 0x40101840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.18 DMAC_DESCR2_PING_DST

Ping destination address

Address: 0x40101844

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.19 DMAC_DESCR2_PING_CTL

Ping control word

Address: 0x40101848

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.20 DMAC_DESCR2_PING_STATUS

Ping status word

Address: 0x4010184C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.21 DMAC_DESCR2_PONG_SRC

Pong source address

Address: 0x40101850

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.22 DMAC_DESCR2_PONG_DST

Pong destination address

Address: 0x40101854

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.23 DMAC_DESCR2_PONG_CTL

Pong control word

Address: 0x40101858

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.24 DMAC_DESCR2_PONG_STATUS

Pong status word

Address: 0x4010185C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

11.1.25 DMAC_DESCR3_PING_SRC

Ping source address

Address: 0x40101860

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.26 DMAC_DESCR3_PING_DST

Ping destination address

Address: 0x40101864

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.27 DMAC_DESCR3_PING_CTL

Ping control word

Address: 0x40101868

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.28 DMAC_DESCR3_PING_STATUS

Ping status word

Address: 0x4010186C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.29 DMAC_DESCR3_PONG_SRC

Pong source address

Address: 0x40101870

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.30 DMAC_DESCR3_PONG_DST

Pong destination address

Address: 0x40101874

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.31 DMAC_DESCR3_PONG_CTL

Pong control word

Address: 0x40101878

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.32 DMAC_DESCR3_PONG_STATUS

Pong status word

Address: 0x4010187C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

11.1.33 DMAC_DESCR4_PING_SRC

Ping source address

Address: 0x40101880

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.34 DMAC_DESCR4_PING_DST

Ping destination address

Address: 0x40101884

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.35 DMAC_DESCR4_PING_CTL

Ping control word

Address: 0x40101888

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.36 DMAC_DESCR4_PING_STATUS

Ping status word

Address: 0x4010188C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.37 DMAC_DESCR4_PONG_SRC

Pong source address

Address: 0x40101890

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.38 DMAC_DESCR4_PONG_DST

Pong destination address

Address: 0x40101894

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.39 DMAC_DESCR4_PONG_CTL

Pong control word

Address: 0x40101898

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.40 DMAC_DESCR4_PONG_STATUS

Pong status word

Address: 0x4010189C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

11.1.41 DMAC_DESCR5_PING_SRC

Ping source address

Address: 0x401018A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.42 DMAC_DESCR5_PING_DST

Ping destination address

Address: 0x401018A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.43 DMAC_DESCR5_PING_CTL

Ping control word

Address: 0x401018A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.44 DMAC_DESCR5_PING_STATUS

Ping status word

Address: 0x401018AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.45 DMAC_DESCR5_PONG_SRC

Pong source address

Address: 0x401018B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.46 DMAC_DESCR5_PONG_DST

Pong destination address

Address: 0x401018B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.47 DMAC_DESCR5_PONG_CTL

Pong control word

Address: 0x401018B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.48 DMAC_DESCR5_PONG_STATUS

Pong status word

Address: 0x401018BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

11.1.49 DMAC_DESCR6_PING_SRC

Ping source address

Address: 0x401018C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.50 DMAC_DESCR6_PING_DST

Ping destination address

Address: 0x401018C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.51 DMAC_DESCR6_PING_CTL

Ping control word

Address: 0x401018C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.52 DMAC_DESCR6_PING_STATUS

Ping status word

Address: 0x401018CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.53 DMAC_DESCR6_PONG_SRC

Pong source address

Address: 0x401018D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.54 DMAC_DESCR6_PONG_DST

Pong destination address

Address: 0x401018D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.55 DMAC_DESCR6_PONG_CTL

Pong control word

Address: 0x401018D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.56 DMAC_DESCR6_PONG_STATUS

Pong status word

Address: 0x401018DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

11.1.57 DMAC_DESCR7_PING_SRC

Ping source address

Address: 0x401018E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.58 DMAC_DESCR7_PING_DST

Ping destination address

Address: 0x401018E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.59 DMAC_DESCR7_PING_CTL

Ping control word

Address: 0x401018E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.60 DMAC_DESCR7_PING_STATUS

Ping status word

Address: 0x401018EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.61 DMAC_DESCR7_PONG_SRC

Pong source address

Address: 0x401018F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.62 DMAC_DESCR7_PONG_DST

Pong destination address

Address: 0x401018F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.63 DMAC_DESCR7_PONG_CTL

Pong control word

Address: 0x401018F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.64 DMAC_DESCR7_PONG_STATUS

Pong status word

Address: 0x401018FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

12 Deep Sleep Amplifier Bias Registers

This section discusses the Deep Sleep Amplifier Bias (DSAB) registers. It lists all the registers in mapping tables, in address order.

12.1 Register Details

Register Name	Address
PASS_DSAB_DSAB_DFT	0x403F0E00
PASS_DSAB_DSAB_DFT	0x403F0E04

12.1.1 PASS_DSAB_DSAB_CTRL

global DSAB control

Address: 0x403F0E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		CURRENT_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				SEL_OUT [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				REF_SWAP_EN [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW	None			RW
HW Access	R	None		R	None			R
Name	ENABLED	None [30:29]		START-UP_RM	None [27:25]			BYPASS_-MODE_EN

Bits	Name	Description
31	ENABLED	This field (along with SEL_OUT and REF_SWAP_EN) provides bitwise selection of the current sources that drive the DSAB ZTC and PTAT outputs. See SEL_OUT field for truth tables. In SRSSLT devices, in active mode, this bit is overridden to '1', that is - it is always enabled in active mode. Default Value: 0
28	STARTUP_RM	Risk mitigation control 1 - Force start the startup circuit Default Value: 0
24	BYPASS_MODE_EN	0 - DSAB PTAT generator is powered from DSAB regulator: VDDA must be at least 2.4V 1 - DSAB PTAT generator is pwoered directly from VDDA: VDDA cannot exceed 4.0V Default Value: 0
19 : 16	REF_SWAP_EN	This field (along with SEL_OUT and ENABLED) provides bitwise selection of the current sources that drive the DSAB ZTC and PTAT outputs. See SEL_OUT field for truth tables. Default Value: 0

(continued)

11 : 8	SEL_OUT	This field (along with REF_SWAP_EN and ENABLED) provides bitwise selection of the current sources that drive the DSAB ZTC and PTAT outputs. The available current sources are a function of the type of SRSS. The SRSS current sources are disabled in chip DeepSleep mode which is indicated by () entries in the truth table. CTB(m) factory trim has SRSS-ZTC and either SRSS-PTAT (SRSSv2) or DSAB_PTAT (SRSS-LITE) enabled. If different settings are used, then a periodic re-trim of CTB(m) offset should be performed.

Truth Table with SRSSv2 (backwards compatible with PSoC4A family)

ENABLED	SEL_OUT	REF_SWAP_EN	"Chip Power Mode"	ZTC Output	PTAT Output
0	X	X	Active	SRSS-ZTC	SRSS-PTAT
0	X	X	Deepsleep	(SRSS-ZTC)	(SRSS-PTAT)
1	0	0	Active	SRSS-ZTC	SRSS-PTAT
1	0	0	DeepSleep	(SRSS-ZTC)	(SRSS-PTAT)
1	0	1	Active	SRSS-PTAT	SRSS-ZTC
1	0	1	DeepSleep	(SRSS-PTAT)	(SRSS-ZTC)
1	1	0	Active	DSAB-PTAT	SRSS-PTAT
1	1	0	DeepSleep	DSAB-PTAT	(SRSS-PTAT)
1	1	1	Active	SRSS-PTAT	DSAB-PTAT
1	1	1	DeepSleep	(SRSS-PTAT)	DSAB-PTAT

Truth Table with SRSS-LITE

ENABLED	SEL_OUT	REF_SWAP_EN	"Chip Power Mode"	ZTC Output	PTAT Output
0	X	X	Active	SRSS-ZTC	DSAB-PTAT
0	X	X	Deepsleep	(SRSS-ZTC)	--
1	0	0	Active	SRSS-ZTC	DSAB-PTAT
1	0	0	DeepSleep	(SRSS-ZTC)	--
1	0	1	Active	DSAB-PTAT	SRSS-ZTC
1	0	1	DeepSleep	DSAB-PTAT	(SRSS-ZTC)
1	1	0	Active	DSAB-PTAT	--
1	1	0	DeepSleep	DSAB-PTAT	--
1	1	1	Active	--	DSAB-PTAT
1	1	1	DeepSleep	--	DSAB-PTAT

Default Value: 0

5 : 0	CURRENT_SEL	DSAB DAC control field Nominal DSAB Output Current = CURRENT_SEL * 0.075 uA In products with SRSS-LITE, this setting impacts the CTB(m) offset. A value of 0x20 is used during factory trim and is required to maintain low offsets across temperature variation. If a different setting is used then a periodic re-trim of CTB(m) offset should be performed. Default Value: 0

12.1.2 PASS_DSAB_DSAB_DFT

DFT bits

Address: 0x403F0E04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				EN_DFT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	EN_DFT	- 0: DSAB DFT disabled - 1: DSAB DFT enabled (connect output to amuxbus) 0001 - PTAT<0> 0010 - PTAT<1> 0011 - PTAT<1:0> 0100 - PTAT<2> 0111 - PTAT<2:0> 1000 - PTAT<3> 1111 - PTAT<3:0> 1001 - DSAB Reg Out Default Value: 0

13 External Clock Registers

This section discusses the External Clock (EXCO) registers. It lists all the registers in mapping tables, in address order.

13.1 Register Details

Register Name	Address
EXCO_CLK_SELECT	0x402F0000
EXCO_ECO_CONFIG	0x402F0008
EXCO_ECO_STATUS	0x402F000C
EXCO_PLL_CONFIG	0x402F0014
EXCO_PLL_STATUS	0x402F0018
EXCO_PLL_TEST	0x402F001C
EXCO_PGM_CLK	0x402F0020
EXCO_ECO_TRIM0	0x402FFF00
EXCO_ECO_TRIM1	0x402FFF04
EXCO_PLL_TRIM	0x402FFF0C

13.1.1 EXCO_CLK_SELECT

Clock Select Register

Address: 0x402F0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						REF_SEL	CLK_SE-LECT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	REF_SEL	Select source for PLL reference 0: from ECO 1: from external reference Default Value: 0
0	CLK_SELECT	When PLL_CONFIG.ENABLE=0, then clk_eco=clk_osc. When PLL_CONFIG.ENABLE=1 then BYPASS_SEL and PLL_STATUS.LOCKED also affect this control point. CLK_SELECT: 0: PLL_CONFIG.BYPASS=0x, PLL_STATUS.LOCKED = 0: clk_eco=clk_osc PLL_CONFIG.BYPASS=0x, PLL_STATUS.LOCKED = 1: clk_eco=clk_pll PLL_CONFIG.BYPASS=10, PLL_STATUS.LOCKED = x: clk_eco=clk_osc PLL_CONFIG.BYPASS=11, PLL_STATUS.LOCKED = x: clk_eco=clk_pll 1: PLL_CONFIG.BYPASS=xx, PLL_STATUS.LOCKED = x: clk_eco=clk_pl Default Value: 0

13.1.2 EXCO_ECO_CONFIG

ECO Configuration Register

Address: 0x402F0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						AGC_EN	CLK_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for ECO oscillator. Refer to CLK_EN for sequencing. Default Value: 0
1	AGC_EN	Automatic Gain Control (AGC) enable. When set, the oscillation amplitude is controlled to the level selected by ECO_TRIM0.ATRIM. When low, the amplitude is not explicitly controlled and will grow until it saturates to the supply rail (1.8V nom). WARNING: use care when disabling AGC because driving a crystal beyond its rated limit can permanently damage the crystal. Default Value: 1
0	CLK_EN	Clock Enable. When enabling the clock, first write ENABLE=1, wait at least 10us, and then write CLK_EN=1. When disabling, clearing both CLK_EN=0 and ENABLE=0 can be done in the same AHB write Default Value: 0

13.1.3 EXCO_ECO_STATUS

ECO Status Register

Address: 0x402F000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							WATCH-DOG_ER-ROR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WATCHDOG_ERROR	This bit is set to 1 if the oscillator is stuck. The ECO clock is gated off during a watchdog error condition. Due to internal synchonization, the clock is stopped two cycles after an error condition is observed and ungated two cycles after the error condition is resolved. Default Value: 0

13.1.4 EXCO_PLL_CONFIG

PLL Configuration Register

Address: 0x402F0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FEEDBACK_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW					
HW Access	R		R					
Name	OUTPUT_DIV [15:14]		REFERENCE_DIV [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW		
HW Access	None		R		None	R		
Name	None [23:22]		BYPASS_SEL [21:20]		None	ICP_SEL [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLE	ISOLATE_N	None [29:24]					

Bits	Name	Description
31	ENABLE	Master enable for PLL power gate. Refer to ISOLATE_N field for required sequencing. 0: Block is powered off, also forces clk_eco = clk_osc - See CLK_SELECT.CLK_SELECT description. 1: Block is powered on Default Value: 0
30	ISOLATE_N	Isolation control of PLL outputs. This also internally resets the PLL. De-assert >= 5us after ENABLE=1. Assertion can happen in same write as ENABLE=0. Do not change while PLL output is selected. 0: Isolate outputs; Precharge PLL control voltage if PLL0_TEST.FAST_LOCK_EN is set to 1. 1: Do not isolate outputs Default Value: 0
21 : 20	BYPASS_SEL	Selects the source of the system PLL0 clock. See also CLK_SELECT.CLK_SELECT for effect on clk_eco selection. Default Value: 0 **0x0: AUTO:** Automatic using lock indicator. When unlocked, automatically selects PLL reference input (bypass mode). When locked, automatically selects PLL output.

(continued)

		0x1: AUTO1: Same as AUTO **0x2: PLL_REF:** Select PLL reference input (bypass mode). Ignores lock indicator **0x3: PLL_OUT:** Select PLL output. Ignores lock indicator.
18 : 16	ICP_SEL	Programmable charge pump current between 0uA and 7uA. Do not change while the PLL output is selected. For functional operation, the value must be set according to the PLL output frequency Fout (measured before the output divider): 0: 0uA (Hi-Z) Engineering use only 1: 1uA. Engineering use only 2: 2uA. Use when Fout <= 67MHz 3: 3uA. Use when Fout > 67MHz 4-7: 4uA-7uA. Engineering use only Default Value: 2
15 : 14	OUTPUT_DIV	Control bits for Output divider. Do not change while PLL output is selected. Default Value: 0 **0x0: PASS:** Pass Through **0x1: DIV2:** Divide by 2 **0x2: DIV4:** Divide by 4 **0x3: DIV8:** Divide by 8
13 : 8	REFERENCE_DIV	Control bits for reference divider: Divide by 2=0001, , divide by 64=111111. Do not change while PLL output is selected. Default Value: 0
7 : 0	FEEDBACK_DIV	Control bits for feedback divider: Valid divide is 8-255. Do not change while PLL output is selected. Default Value: 0

13.1.5 EXCO_PLL_STATUS

PLL Status Register

Address: 0x402F0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							LOCKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	LOCKED	PLL Lock Indicator - See CLK_SELECT.CLK_SELECT description for interaction with clk_eco selection. Default Value: 0

13.1.6 EXCO_PLL_TEST

PLL Test Register

Address: 0x402F001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW	RW		
HW Access	None			A	R	R		
Name	None [7:5]			UN-LOCK_OC-CURRED	FAST_LOCK_EN	TEST_MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UNLOCK_OCCURRED	This bit sets whenever the PLL Lock bit goes low, and stays set until cleared by firmware. This is a diagnostic bit used for char and validation. Default Value: 0
3	FAST_LOCK_EN	Fast Lock Enable - Speeds up the lock time when set to 1. When ISOLATE_N is high, the PLL control voltage will be precharged to reduce time spent acquiring frequency lock. Default Value: 1
2 : 0	TEST_MODE	Test Mode Default Value: 0 **0x0: NORMAL:** Normal Operation **0x1: TEST_VC_LKG:** Vcontrol Leakage Test Mode Measure frequency drift over time to indirectly measure leakage on Vcontrol

(continued)

0x2: TEST_CP_DN:
Charge Pump Down Current Test Mode
With ICPSEL>0, directly measure charge pump up current on Vcontrol
With ICPSEL=0, directly measure leakage on Vcontrol
With ICPSEL=0, FAST_LOCK_EN=0 and ISOLATE_N=0, directly measure discharge current on Vcontrol
With ICPSEL=0, FAST_LOCK_EN=1 and ISOLATE_N=0, directly measure precharge current on Vcontrol

0x3: TEST_CP_UP:
Charge Pump Up Current Test Mode
With ICPSEL>0, directly measure charge pump up current on Vcontrol
With ICPSEL=0, directly measure leakage on Vcontrol
With ICPSEL=0, FAST_LOCK_EN=0 and ISOLATE_N=0, directly measure discharge current on Vcontrol
With ICPSEL=0, FAST_LOCK_EN=1 and ISOLATE_N=0, directly measure precharge current on Vcontrol

0x4: USER_EXT_FL:
User Mode with Extended Fast Lock Precharge

0x5: TEST_CTR_PQ:
Reference and Feedback Counter Test Mode

0x6: TEST_LD_DLY:
Lock Detector Delay Line Test Mode

0x7: TEST_CTR_ALT:
Lock Detector Wait and Extended Fast Lock Counter Test Mode
With ICPSEL=0 and Reference Clock stopped directly measure precharge current on Vcontrol
With ICPSEL=0 and Reference Clock running directly measure leakage on Vcontrol

13.1.7 EXCO_PGM_CLK

EXCO Program Clock

Address: 0x402F0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	R	RW	None
HW Access	None			R	R	RW	R	None
Name	None [7:5]			EN_-CLK_PLL0	CLK_PLL0_OUT	CLK_PLL0_IN	CLK_ECO	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable PLL enable capability in this register. Please refer to the CLK_ECO bit description in the register for usage. Default Value: 0
4	EN_CLK_PLL0	Reserved. Leave at default value. Default Value: 0
3	CLK_PLL0_OUT	Reserved. Leave at default value. Default Value: 0
2	CLK_PLL0_IN	Reserved. Leave at default value. Default Value: 0
1	CLK_ECO	When IMO is used as reference to the PLL and the ECO is disabled or ECO crystal is not mounted on the board, this bit is used to start the PLL. Toggle this bit five times in firmware by alternatively writing 0 and 1, with the ENABLE bit high in the same register. Then, clear the ENABLE bit to start the PLL. This procedure should be used when the chip exits from DeepSleep low power mode. Note that the system clock (HFCLK/SYSCLK) source should be changed from PLL to IMO before the chip enters Deep Sleep. After Deep Sleep wakeup, the system clock source can be changed back from IMO to the PLL. Default Value: 0

13.1.8 EXCO_ECO_TRIM0

ECO Trim0 Register

Address: 0x402FFF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [7:5]			ATRIM [4:2]			WDTRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 2	ATRIM	Amplitude trim to set the crystal drive level when ECO_CONFIG.AGC_EN=1. WARNING: use care when setting this field because driving a crystal beyond its rated limit can permanently damage the crystal. 0x0 - 0.3Vpp 0x1 - 0.4Vpp 0x2 - 0.5Vpp 0x3 - 0.6Vpp 0x4 - 0.7Vpp 0x5 - 0.8Vpp 0x6 - 0.9Vpp 0x7 - 1.0Vpp Default Value: 0
1 : 0	WDTRIM	Watch Dog Trim - Delta voltage below stead state level 0x0 - 0.05V 0x1 - 0.1V 0x2 - 0.15V 0x3 - 0.2V Default Value: 0

13.1.9 EXCO_ECO_TRIM1

ECO Trim1 Register

Address: 0x402FFF04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		GTRIM [5:4]		RTRIM [3:2]		FTRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	GTRIM	Gain Trim - Startup time Default Value: 1
3 : 2	RTRIM	Feedback resistor Trim Default Value: 1
1 : 0	FTRIM	Filter Trim - 3rd harmonic oscillation Default Value: 1

13.1.10 EXCO_PLL_TRIM

PLL Trim Register

Address: 0x402FFF0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		LOCK_DELAY [5:4]		LOCK_WINDOW [3:2]		VCO_GAIN [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	LOCK_DELAY	Selects the number of PLL phase frequency detector cycles that the phase error must be in range before declaring lock. (PFD clock cycle = Clock Reference Period/REFERENCE_DIV) Default Value: 1 **0x0: PFD_CLK_16:** 16 PFD clock cycles **0x1: PFD_CLK_32:** 32 PFD clock cycles **0x2: PFD_CLK_48:** 48 PFD clock cycles **0x3: PFD_CLK_64:** 64 PFD clock cycles
3 : 2	LOCK_WINDOW	Selects the allowed phase error before declaring the PLL Unlocked Default Value: 0 **0x0: DELAY_25NS:** Delay 25 ns

(continued)

		0x1: DELAY_50NS: Delay 50 ns **0x2: DELAY_75NS:** Delay 75 ns **0x3: DELAY_100NS:** Delay 100 ns
1 : 0	VCO_GAIN	Programmable VCO frequency characteristic at high freq - set to <10> Default Value: 2

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14 General Purpose I/O Registers

This section discusses the General Purpose I/O Registers (GPIO) registers. It lists all the registers in mapping tables, in address order.

14.1 Register Details

Register Name	Address
GPIO_INTR_CAUSE	0x40041000

14.1.1 GPIO_INTR_CAUSE

Interrupt port cause register

Address: 0x40041000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PORT_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PORT_INT	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects "gpio_interrupts[i]" for IO port i). The register is used when the system uses a shared/combined interrupt line "gpio_interrupt". The SW ISR reads the register to determine which IO port(s) is responsible for the shared/combined interrupt line "gpio_interrupt". Once, the IO port(s) is determined, the IO port's INTR register is read to determine the IO pad(s) in the IO port that caused the interrupt. Default Value: 0

15 GPIO - Port Specific Registers

This section discusses the GPIO Port (GPIO_PRT) registers. It lists all the registers in mapping tables, in address order.

15.1 Register Details

Register Name	Address
GPIO_PRT0_DR	0x40040000
GPIO_PRT0_PS	0x40040004
GPIO_PRT0_PC	0x40040008
GPIO_PRT0_INTR_CFG	0x4004000C
GPIO_PRT0_INTR	0x40040010
GPIO_PRT0_PC2	0x40040018
GPIO_PRT0_DR_SET	0x40040040
GPIO_PRT0_DR_CLR	0x40040044
GPIO_PRT0_DR_INV	0x40040048
GPIO_PRT1_DR	0x40040100
GPIO_PRT1_PS	0x40040104
GPIO_PRT1_PC	0x40040108
GPIO_PRT1_INTR_CFG	0x4004010C
GPIO_PRT1_INTR	0x40040110
GPIO_PRT1_PC2	0x40040118
GPIO_PRT1_DR_SET	0x40040140
GPIO_PRT1_DR_CLR	0x40040144
GPIO_PRT1_DR_INV	0x40040148
GPIO_PRT2_DR	0x40040200
GPIO_PRT2_PS	0x40040204
GPIO_PRT2_PC	0x40040208
GPIO_PRT2_INTR_CFG	0x4004020C
GPIO_PRT2_INTR	0x40040210
GPIO_PRT2_PC2	0x40040218
GPIO_PRT2_DR_SET	0x40040240
GPIO_PRT2_DR_CLR	0x40040244
GPIO_PRT2_DR_INV	0x40040248

Register Name	Address
GPIO_PRT3_DR	0x40040300
GPIO_PRT3_PS	0x40040304
GPIO_PRT3_PC	0x40040308
GPIO_PRT3_INTR_CFG	0x4004030C
GPIO_PRT3_INTR	0x40040310
GPIO_PRT3_PC2	0x40040318
GPIO_PRT3_DR_SET	0x40040340
GPIO_PRT3_DR_CLR	0x40040344
GPIO_PRT3_DR_INV	0x40040348
GPIO_PRT4_DR	0x40040400
GPIO_PRT4_PS	0x40040404
GPIO_PRT4_PC	0x40040408
GPIO_PRT4_INTR_CFG	0x4004040C
GPIO_PRT4_INTR	0x40040410
GPIO_PRT4_PC2	0x40040418
GPIO_PRT4_DR_SET	0x40040440
GPIO_PRT4_DR_CLR	0x40040444
GPIO_PRT4_DR_INV	0x40040448
GPIO_PRT5_DR	0x40040500
GPIO_PRT5_PS	0x40040504
GPIO_PRT5_PC	0x40040508
GPIO_PRT5_INTR_CFG	0x4004050C
GPIO_PRT5_INTR	0x40040510
GPIO_PRT5_PC2	0x40040518
GPIO_PRT5_DR_SET	0x40040540
GPIO_PRT5_DR_CLR	0x40040544
GPIO_PRT5_DR_INV	0x40040548
GPIO_PRT6_DR	0x40040600
GPIO_PRT6_PS	0x40040604
GPIO_PRT6_PC	0x40040608
GPIO_PRT6_INTR_CFG	0x4004060C
GPIO_PRT6_INTR	0x40040610
GPIO_PRT6_PC2	0x40040618
GPIO_PRT6_DR_SET	0x40040640
GPIO_PRT6_DR_CLR	0x40040644
GPIO_PRT6_DR_INV	0x40040648
GPIO_PRT7_DR	0x40040700
GPIO_PRT7_PS	0x40040704
GPIO_PRT7_PC	0x40040708
GPIO_PRT7_INTR_CFG	0x4004070C
GPIO_PRT7_INTR	0x40040710
GPIO_PRT7_PC2	0x40040718

Register Name	Address
GPIO_PRT7_DR_SET	0x40040740
GPIO_PRT7_DR_CLR	0x40040744
GPIO_PRT7_DR_INV	0x40040748

15.1.1 GPIO_PRT0_DR

Port output data register

Address: 0x40040000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

15.1.2 GPIO_PRT0_PS

Port IO pad state register

Address: 0x40040004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

(continued)

0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

15.1.3 GPIO_PRT0_PC

Port configuration register

Address: 0x40040008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0

(continued)

24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for IO pad 7. Default Value: 0
20 : 18	DM6	The GPIO drive mode for IO pad 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

15.1.4 GPIO_PRT0_INTR_CFG

Port interrupt configuration register

Address: 0x4004000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0

(continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

15.1.5 GPIO_PRT0_INTR

Port interrupt status register

Address: 0x40040010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

(continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

15.1.6 GPIO_PRT0_PC2

Port configuration register 2

Address: 0x40040018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

(continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

15.1.7 GPIO_PRT0_DR_SET

Port output data set register

Address: 0x40040040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

15.1.8 GPIO_PRT0_DR_CLR

Port output data clear register

Address: 0x40040044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

15.1.9 GPIO_PRT0_DR_INV

Port output data invert register

Address: 0x40040048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

15.1.10 GPIO_PRT1_DR

Port output data register

Address: 0x40040100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

15.1.11 GPIO_PRT1_PS

Port IO pad state register

Address: 0x40040104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

(continued)

0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

15.1.12 GPIO_PRT1_PC

Port configuration register

Address: 0x40040108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0

(continued)

24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for IO pad 7. Default Value: 0
20 : 18	DM6	The GPIO drive mode for IO pad 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

15.1.13 GPIO_PRT1_INTR_CFG

Port interrupt configuration register

Address: 0x4004010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0

(continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

15.1.14 GPIO_PRT1_INTR

Port interrupt status register

Address: 0x40040110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

(continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

15.1.15 GPIO_PRT1_PC2

Port configuration register 2

Address: 0x40040118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

(continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

15.1.16 GPIO_PRT1_DR_SET

Port output data set register

Address: 0x40040140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

15.1.17 GPIO_PRT1_DR_CLR

Port output data clear register

Address: 0x40040144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

15.1.18 GPIO_PRT1_DR_INV

Port output data invert register

Address: 0x40040148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

15.1.19 GPIO_PRT2_DR

Port output data register

Address: 0x40040200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

15.1.20 GPIO_PRT2_PS

Port IO pad state register

Address: 0x40040204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

(continued)

0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

15.1.21 GPIO_PRT2_PC

Port configuration register

Address: 0x40040208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0

(continued)

24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for IO pad 7. Default Value: 0
20 : 18	DM6	The GPIO drive mode for IO pad 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

15.1.22 GPIO_PRT2_INTR_CFG

Port interrupt configuration register

Address: 0x4004020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0

(continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

15.1.23 GPIO_PRT2_INTR

Port interrupt status register

Address: 0x40040210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

(continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

15.1.24 GPIO_PRT2_PC2

Port configuration register 2

Address: 0x40040218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

(continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

15.1.25 GPIO_PRT2_DR_SET

Port output data set register

Address: 0x40040240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

15.1.26 GPIO_PRT2_DR_CLR

Port output data clear register

Address: 0x40040244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

15.1.27 GPIO_PRT2_DR_INV

Port output data invert register

Address: 0x40040248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

15.1.28 GPIO_PRT3_DR

Port output data register

Address: 0x40040300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

15.1.29 GPIO_PRT3_PS

Port IO pad state register

Address: 0x40040304

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

(continued)

0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

15.1.30 GPIO_PRT3_PC

Port configuration register

Address: 0x40040308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0

(continued)

24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for IO pad 7. Default Value: 0
20 : 18	DM6	The GPIO drive mode for IO pad 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

15.1.31 GPIO_PRT3_INTR_CFG

Port interrupt configuration register

Address: 0x4004030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0

(continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

15.1.32 GPIO_PRT3_INTR

Port interrupt status register

Address: 0x40040310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

(continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

15.1.33 GPIO_PRT3_PC2

Port configuration register 2

Address: 0x40040318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

(continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

15.1.34 GPIO_PRT3_DR_SET

Port output data set register

Address: 0x40040340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

15.1.35 GPIO_PRT3_DR_CLR

Port output data clear register

Address: 0x40040344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

15.1.36 GPIO_PRT3_DR_INV

Port output data invert register

Address: 0x40040348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

15.1.37 GPIO_PRT4_DR

Port output data register

Address: 0x40040400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

15.1.38 GPIO_PRT4_PS

Port IO pad state register

Address: 0x40040404

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

(continued)

0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

15.1.39 GPIO_PRT4_PC

Port configuration register

Address: 0x40040408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0

(continued)

24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for IO pad 7. Default Value: 0
20 : 18	DM6	The GPIO drive mode for IO pad 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

15.1.40 GPIO_PRT4_INTR_CFG

Port interrupt configuration register

Address: 0x4004040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0

(continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

15.1.41 GPIO_PRT4_INTR

Port interrupt status register

Address: 0x40040410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

(continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

15.1.42 GPIO_PRT4_PC2

Port configuration register 2

Address: 0x40040418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

(continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

15.1.43 GPIO_PRT4_DR_SET

Port output data set register

Address: 0x40040440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

15.1.44 GPIO_PRT4_DR_CLR

Port output data clear register

Address: 0x40040444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

15.1.45 GPIO_PRT4_DR_INV

Port output data invert register

Address: 0x40040448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

15.1.46 GPIO_PRT5_DR

Port output data register

Address: 0x40040500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

15.1.47 GPIO_PRT5_PS

Port IO pad state register

Address: 0x40040504

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

(continued)

0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

15.1.48 GPIO_PRT5_PC

Port configuration register

Address: 0x40040508

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0

(continued)

24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for IO pad 7. Default Value: 0
20 : 18	DM6	The GPIO drive mode for IO pad 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

15.1.49 GPIO_PRT5_INTR_CFG

Port interrupt configuration register

Address: 0x4004050C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0

(continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

15.1.50 GPIO_PRT5_INTR

Port interrupt status register

Address: 0x40040510

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

(continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

15.1.51 GPIO_PRT5_PC2

Port configuration register 2

Address: 0x40040518

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

(continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

15.1.52 GPIO_PRT5_DR_SET

Port output data set register

Address: 0x40040540

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

15.1.53 GPIO_PRT5_DR_CLR

Port output data clear register

Address: 0x40040544

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

15.1.54 GPIO_PRT5_DR_INV

Port output data invert register

Address: 0x40040548

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

15.1.55 GPIO_PRT6_DR

Port output data register

Address: 0x40040600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

15.1.56 GPIO_PRT6_PS

Port IO pad state register

Address: 0x40040604

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

(continued)

0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

15.1.57 GPIO_PRT6_PC

Port configuration register

Address: 0x40040608

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0

(continued)

24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

15.1.58 GPIO_PRT6_INTR_CFG

Port interrupt configuration register

Address: 0x4004060C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0

(continued)

7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

15.1.59 GPIO_PRT6_INTR

Port interrupt status register

Address: 0x40040610

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		A	A	A	A	A	A
Name	None [7:6]		DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [23:22]		PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0

(continued)

4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

15.1.60 GPIO_PRT6_PC2

Port configuration register 2

Address: 0x40040618

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0
0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

15.1.61 GPIO_PRT6_DR_SET

Port output data set register

Address: 0x40040640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

15.1.62 GPIO_PRT6_DR_CLR

Port output data clear register

Address: 0x40040644

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

15.1.63 GPIO_PRT6_DR_INV

Port output data invert register

Address: 0x40040648

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

15.1.64 GPIO_PRT7_DR

Port output data register

Address: 0x40040700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					RW	RW	RW
Name	None [7:3]					DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

15.1.65 GPIO_PRT7_PS

Port IO pad state register

Address: 0x40040704

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0
0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

15.1.66 GPIO_PRT7_PC

Port configuration register

Address: 0x40040708

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							DM2

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0

(continued)

24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

15.1.67 GPIO_PRT7_INTR_CFG

Port interrupt configuration register

Address: 0x4004070C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0

(continued)

1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

15.1.68 GPIO_PRT7_INTR

Port interrupt status register

Address: 0x40040710

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					A	A	A
Name	None [7:3]					DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [23:19]					PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

15.1.69 GPIO_PRT7_PC2

Port configuration register 2

Address: 0x40040718

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0
0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

15.1.70 GPIO_PRT7_DR_SET

Port output data set register

Address: 0x40040740

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

15.1.71 GPIO_PRT7_DR_CLR

Port output data clear register

Address: 0x40040744

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

15.1.72 GPIO_PRT7_DR_INV

Port output data invert register

Address: 0x40040748

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

16 High Speed IO Matrix Registers

This section discusses the High Speed IO Matrix (HSIOM) common registers. It lists all the registers in mapping tables, in address order.

16.1 Register Details

Register Name	Address
HSIOM_AMUX_SPLIT_CTL0	0x40022100
HSIOM_AMUX_SPLIT_CTL0	0x40022104

16.1.1 HSIOM_AMUX_SPLIT_CTL0

AMUX splitter cell control

Address: 0x40022100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_B-B_S0	SWITCH_B-B_SR	SWITCH_B-B_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

(continued)

0	SWITCH_AA_SL	T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

16.1.2 HSIOM_AMUX_SPLIT_CTL1

AMUX splitter cell control

Address: 0x40022104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_B-B_S0	SWITCH_B-B_SR	SWITCH_B-B_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

(continued)

0	SWITCH_AA_SL	T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

17 HSIOM - Port Specific Registers

This section discusses the HSIOM Port Specific (HSIOM_PRT) registers. It lists all the registers in mapping tables, in address order.

17.1 Register Details

Register Name	Address
HSIOM_PORT_SEL0	0x40020000
HSIOM_PORT_SEL1	0x40020100
HSIOM_PORT_SEL2	0x40020200
HSIOM_PORT_SEL3	0x40020300
HSIOM_PORT_SEL4	0x40020400
HSIOM_PORT_SEL5	0x40020500
HSIOM_PORT_SEL6	0x40020600
HSIOM_PORT_SEL7	0x40020700

17.1.1 HSIOM_PORT_SEL0

Port selection register

Address: 0x40020000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

(continued)

0x0: GPIO:
SW controlled GPIO.

0x1: GPIO_DSI:
SW controlled "out", DSI controlled "oe_n".

0x2: DSI_DSI:
DSI controlled "out" and "oe_n".

0x3: DSI_GPIO:
DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE:
CSD sense connection (analog mode)

0x5: CSD_SHIELD:
CSD shield connection (analog mode)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

17.1.2 HSIOM_PORT_SEL1

Port selection register

Address: 0x40020100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

(continued)

0x0: GPIO:
SW controlled GPIO.

0x1: GPIO_DSI:
SW controlled "out", DSI controlled "oe_n".

0x2: DSI_DSI:
DSI controlled "out" and "oe_n".

0x3: DSI_GPIO:
DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE:
CSD sense connection (analog mode)

0x5: CSD_SHIELD:
CSD shield connection (analog mode)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

17.1.3 HSIOM_PORT_SEL2

Port selection register

Address: 0x40020200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

(continued)

0x0: GPIO:
SW controlled GPIO.

0x1: GPIO_DSI:
SW controlled "out", DSI controlled "oe_n".

0x2: DSI_DSI:
DSI controlled "out" and "oe_n".

0x3: DSI_GPIO:
DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE:
CSD sense connection (analog mode)

0x5: CSD_SHIELD:
CSD shield connection (analog mode)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

17.1.4 HSIOM_PORT_SEL3

Port selection register

Address: 0x40020300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

(continued)

0x0: GPIO:
SW controlled GPIO.

0x1: GPIO_DSI:
SW controlled "out", DSI controlled "oe_n".

0x2: DSI_DSI:
DSI controlled "out" and "oe_n".

0x3: DSI_GPIO:
DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE:
CSD sense connection (analog mode)

0x5: CSD_SHIELD:
CSD shield connection (analog mode)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

17.1.5 HSIOM_PORT_SEL4

Port selection register

Address: 0x40020400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

(continued)

0x0: GPIO:
SW controlled GPIO.

0x1: GPIO_DSI:
SW controlled "out", DSI controlled "oe_n".

0x2: DSI_DSI:
DSI controlled "out" and "oe_n".

0x3: DSI_GPIO:
DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE:
CSD sense connection (analog mode)

0x5: CSD_SHIELD:
CSD shield connection (analog mode)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

17.1.6 HSIOM_PORT_SEL5

Port selection register

Address: 0x40020500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

(continued)

0x0: GPIO:
SW controlled GPIO.

0x1: GPIO_DSI:
SW controlled "out", DSI controlled "oe_n".

0x2: DSI_DSI:
DSI controlled "out" and "oe_n".

0x3: DSI_GPIO:
DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE:
CSD sense connection (analog mode)

0x5: CSD_SHIELD:
CSD shield connection (analog mode)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

17.1.7 HSIOM_PORT_SEL6

Port selection register

Address: 0x40020600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0 **0x0: GPIO:** SW controlled GPIO. **0x1: GPIO_DSI:** SW controlled "out", DSI controlled "oe_n".

(continued)

0x2: DSI_DSI:
DSI controlled "out" and "oe_n".

0x3: DSI_GPIO:
DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE:
CSD sense connection (analog mode)

0x5: CSD_SHIELD:
CSD shield connection (analog mode)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

17.1.8 HSIOM_PORT_SEL7

Port selection register

Address: 0x40020700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				RW			
Name	None [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0 **0x0: GPIO:** SW controlled GPIO. **0x1: GPIO_DSI:** SW controlled "out", DSI controlled "oe_n". **0x2: DSI_DSI:** DSI controlled "out" and "oe_n". **0x3: DSI_GPIO:** DSI controlled "out", SW controlled "oe_n". **0x4: CSD_SENSE:** CSD sense connection (analog mode)

(continued)

0x5: CSD_SHIELD:
CSD shield connection (analog mode)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

18 LCD Registers

This section discusses the LCD registers. It lists all the registers in mapping tables, in address order.

18.1 Register Details

Register Name	Address
LCD_ID	0x402A0000
LCD_DIVIDER	0x402A0004
LCD_CONTROL	0x402A0008
LCD_DATA00	0x402A0100
LCD_DATA01	0x402A0104
LCD_DATA02	0x402A0108
LCD_DATA03	0x402A010C
LCD_DATA04	0x402A0110
LCD_DATA05	0x402A0114
LCD_DATA06	0x402A0118
LCD_DATA07	0x402A011C
LCD_DATA10	0x402A0200
LCD_DATA11	0x402A0204
LCD_DATA12	0x402A0208
LCD_DATA13	0x402A020C
LCD_DATA14	0x402A0210
LCD_DATA15	0x402A0214
LCD_DATA16	0x402A0218
LCD_DATA17	0x402A021C

18.1.1 LCD_ID

ID & Revision

Address: 0x402A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	the version number is 0x0001 Default Value: 1
15 : 0	ID	the ID of LCD controller peripheral is 0xF0F0 Default Value: 61680

18.1.2 LCD_DIVIDER

LCD Divider Register

Address: 0x402A0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBFR_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SUBFR_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEAD_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DEAD_DIV [31:24]							

Bits	Name	Description
31 : 16	DEAD_DIV	Length of the dead time period in cycles. When set to zero, no dead time period exists. Default Value: 0
15 : 0	SUBFR_DIV	Input clock frequency divide value, to generate the 1/4 sub-frame period. The sub-frame period is 4*(SUBFR_DIV+1) cycles long. Default Value: 0

18.1.3 LCD_CONTROL

LCD Configuration Register

Address: 0x402A0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW	RW	RW	RW	RW
HW Access	None	R		R	R	R	R	R
Name	None	BIAS [6:5]		OP_MODE	TYPE	LCD_-MODE	HS_EN	LS_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				COM_NUM [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	LS_EN_STAT	None [30:24]						

Bits	Name	Description
31	LS_EN_STAT	LS enable status bit. This bit is a copy of LS_EN that is synchronized to the low speed clock domain and back to the system clock domain. Firmware can use this bit to observe whether LS_EN has taken effect in the low speed clock domain. Firmware should never change the configuration for the LS generator without ensuring this bit is 0. The following procedure should be followed to disable the LS generator: 1. If LS_EN=0 we are done. Exit the procedure. 2. Check that LS_EN_STAT=1. If not, wait until it is. This will catch the case of a recent enable (LS_EN=1) that has not taken effect yet. 3. Set LS_EN=0. 4. Wait until LS_EN_STAT=0. Default Value: 0

(continued)

11 : 8	COM_NUM	The number of COM connections minus 2. So: 0: 2 COM's 1: 3 COM's ... 13: 15 COM's 14: 16 COM's 15: undefined Default Value: 0
6 : 5	BIAS	PWM bias selection Default Value: 0 **0x0: HALF:** 1/2 Bias **0x1: THIRD:** 1/3 Bias **0x2: FOURTH:** 1/4 Bias (not supported by LS generator) **0x3: FIFTH:** 1/5 Bias (not supported by LS generator)
4	OP_MODE	Driving mode configuration Default Value: 0 **0x0: PWM:** PWM Mode **0x1: CORRELATION:** Digital Correlation Mode
3	TYPE	LCD driving waveform type configuration. Default Value: 0 **0x0: TYPE_A:** Type A - Each frame addresses each COM pin only once with a balanced (DC=0) waveform. **0x1: TYPE_B:** Type B - Each frame addresses each COM pin twice in sequence with a positive and negative waveform that together are balanced (DC=0).
2	LCD_MODE	HS/LS Mode selection Default Value: 0 **0x0: LS:** Select Low Speed (32kHz) Generator (Works in Active, Sleep and DeepSleep power modes). **0x1: HS:** Select High Speed (system clock) Generator (Works in Active and Sleep power modes only).
1	HS_EN	High speed (HS) generator enable 1: enable 0: disable Default Value: 0
0	LS_EN	Low speed (LS) generator enable 1: enable 0: disable Default Value: 0

18.1.4 LCD_DATA00

LCD Pin Data Registers

Address: 0x402A0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

18.1.5 LCD_DATA01

LCD Pin Data Registers

Address: 0x402A0104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

18.1.6 LCD_DATA02

LCD Pin Data Registers

Address: 0x402A0108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

18.1.7 LCD_DATA03

LCD Pin Data Registers

Address: 0x402A010C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

18.1.8 LCD_DATA04

LCD Pin Data Registers

Address: 0x402A0110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

18.1.9 LCD_DATA05

LCD Pin Data Registers

Address: 0x402A0114

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

18.1.10 LCD_DATA06

LCD Pin Data Registers

Address: 0x402A0118

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

18.1.11 LCD_DATA07

LCD Pin Data Registers

Address: 0x402A011C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

18.1.12 LCD_DATA10

LCD Pin Data Registers

Address: 0x402A0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

18.1.13 LCD_DATA11

LCD Pin Data Registers

Address: 0x402A0204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

18.1.14 LCD_DATA12

LCD Pin Data Registers

Address: 0x402A0208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

18.1.15 LCD_DATA13

LCD Pin Data Registers

Address: 0x402A020C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

18.1.16 LCD_DATA14

LCD Pin Data Registers

Address: 0x402A0210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

18.1.17 LCD_DATA15

LCD Pin Data Registers

Address: 0x402A0214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

18.1.18 LCD_DATA16

LCD Pin Data Registers

Address: 0x402A0218

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

18.1.19 LCD_DATA17

LCD Pin Data Registers

Address: 0x402A021C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

19 Low Power Comparator Registers

This section discusses the Low Power Comparator (LPCOMP) registers. It lists all the registers in mapping tables, in address order.

19.1 Register Details

Register Name	Address
LPCOMP_ID	0x402B0000
LPCOMP_CONFIG	0x402B0004
LPCOMP_INTR	0x402B0010
LPCOMP_INTR_SET	0x402B0014
LPCOMP_INTR_MASK	0x402B0018
LPCOMP_INTR_MASKED	0x402B001C
LPCOMP_TRIM1	0x402BFF00
LPCOMP_TRIM2	0x402BFF04
LPCOMP_TRIM3	0x402BFF08
LPCOMP_TRIM4	0x402BFF0C

19.1.1 LPCOMP_ID

ID & Revision

Address: 0x402B0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	the version number is 0x0001 Default Value: 1
15 : 0	ID	the ID of LPCOMP peripheral is 0xE0E0 Default Value: 57568

19.1.2 LPCOMP_CONFIG

LPCOMP Configuration Register

Address: 0x402B0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	R	RW		RW	RW	RW	
HW Access	R	RW	R		R	R	R	
Name	ENABLE1	OUT1	INTTYPE1 [5:4]		FILTER1	HYST1	MODE1 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	R	RW		RW	RW	RW	
HW Access	R	RW	R		R	R	R	
Name	ENABLE2	OUT2	INTTYPE2 [13:12]		FILTER2	HYST2	MODE2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	None		RW	RW
HW Access	None		R	R	None		R	R
Name	None [23:22]		DSI_LEV-EL2	DSI_BY-PASS2	None [19:18]		DSI_LEV-EL1	DSI_BY-PASS1

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	DSI_LEVEL2	Comparator 1 DSI output type when synchronization is enabled 0: Pulse 1: Level Default Value: 0
20	DSI_BYPASS2	Comparator 1 bypass synchronization for DSI output 0: Synchronize (level or pulse), 1: Bypass (output async) Note that in DeepSleep mode this bit needs to be set to observe the DSI output on the dedicated pin. Default Value: 0
17	DSI_LEVEL1	Comparator 0 DSI output type when synchronization is enabled 0: Pulse 1: Level Default Value: 0

(continued)

16	DSI_BYPASS1	Comparator 0 bypass synchronization for DSI output 0: Synchronize (level or pulse), 1: Bypass (output async) Note that in DeepSleep mode this bit needs to be set to observe the output on the dedicated pin. Default Value: 0
15	ENABLE2	Enable Comparator 1 Default Value: 0
14	OUT2	Current output value of the Comparator 1 Default Value: 0
13 : 12	INTTYPE2	Sets which edge in the Comparator 1 output triggers an interrupt Default Value: 0 **0x0: DISABLE:** Disabled, no interrupts will be generated **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
11	FILTER2	Reserved bit - It should be set to 0. Default Value: 0
10	HYST2	10mV hysteresis for Comparator 1 0: Enable Hysteresis 1: Disable Hysteresis Default Value: 0
9 : 8	MODE2	Sets the operating mode for Comparator 1 Default Value: 0 **0x0: SLOW:** Slow operating mode **0x1: FAST:** Fast operating mode (Highest block current) **0x2: ULP:** Ultra low power operating mode (lowest block current)
7	ENABLE1	Enable Comparator 0 Default Value: 0
6	OUT1	Current output value of the Comparator 0 Default Value: 0
5 : 4	INTTYPE1	Sets which edge in the Comparator 0 output triggers an interrupt Default Value: 0 **0x0: DISABLE:** Disabled, no interrupts will be generated **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge

(continued)

		0x3: BOTH: Both rising and falling edges
3	FILTER1	Reserved bit - It should be set to 0. Default Value: 0
2	HYST1	10mV hysteresis for Comparator 0 0: Enable Hysteresis 1: Disable Hysteresis Default Value: 0
1 : 0	MODE1	Sets the operating mode for Comparator 0 Default Value: 0 **0x0: SLOW:** Slow operating mode **0x1: FAST:** Fast operating mode (Highest block current) **0x2: ULP:** Ultra low power operating mode (lowest block current)

19.1.3 LPCOMP_INTR

LPCOMP Interrupt request register

Address: 0x402B0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						COMP2	COMP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2	Comparator 1 Interrupt: Hardware sets this bit when comparator 1 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP1	Comparator 0 Interrupt: Hardware sets this bit when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

19.1.4 LPCOMP_INTR_SET

LPCOMP Interrupt set register

Address: 0x402B0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP2	COMP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2	Write with '1' to set COMP2 bit in the interrupt request register. This triggers Comparator 1 interrupt. Default Value: 0
0	COMP1	Write with '1' to set COMP1 bit in the interrupt request register. This triggers Comparator 0 interrupt. Default Value: 0

19.1.5 LPCOMP_INTR_MASK

LPCOMP Interrupt request mask

Address: 0x402B0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP2_MASK	COMP1_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2_MASK	Interrupt mask bit for Comparator 1 Default Value: 0
0	COMP1_MASK	Interrupt mask bit for Comparator 0 Default Value: 0

19.1.6 LPCOMP_INTR_MASKED

LPCOMP Interrupt request masked

Address: 0x402B001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP2_MASKED	COMP1_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2_MASKED	Logical AND of the Comparator 1 interrupt request register bit and the interrupt mask bit. Default Value: 0
0	COMP1_MASKED	Logical AND of the Comparator 0 interrupt request register bit and the interrupt mask bit. Default Value: 0

19.1.7 LPCOMP_TRIM1

LPCOMP Trim Register

Address: 0x402BFF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP1_TRIMA [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP1_TRIMA	Trim A for Comparator 0. These bits are used to correct/trim the comparator offset (Coarse tuning bits). Trim A bits[3:0] control the amount of offset and Trim A bit[4] controls the polarity of offset ('1' indicates positive offset and '0' indicates negative offset) Default Value: 0

19.1.8 LPCOMP_TRIM2

LPCOMP Trim Register

Address: 0x402BFF04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP1_TRIMB [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP1_TRIMB	Trim B for Comparator 0. These bits are used to correct/trim the comparator offset (fine tuning bits). These bits must be tuned after tuning Trim A bits for the comparator. Default Value: 0

19.1.9 LPCOMP_TRIM3

LPCOMP Trim Register

Address: 0x402BFF08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP2_TRIMA [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP2_TRIMA	Trim A for Comparator 1. These bits are used to correct/trim the comparator offset (Coarse tuning bits) . Trim A bits[3:0] control the amount of offset and Trim A bit[4] controls the polarity of offset ('1' indicates positive offset and '0' indicates negative offset) Default Value: 0

19.1.10 LPCOMP_TRIM4

LPCOMP Trim Register

Address: 0x402BFF0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP2_TRIMB [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP2_TRIMB	Trim B for Comparator 1. These bits are used to correct/trim the comparator offset (fine tuning bits). These bits must be tuned after tuning Trim A bits for the comparator. Default Value: 0

20 PASS MMIO Registers

This section discusses the Programmable Analog Sub System Memory Mapped IO (PASS MMIO) registers. It lists all the registers in mapping tables, in address order.

20.1 Register Details

Register Name	Address
PASS_INTR_CAUSE	0x403F0000
PASS_DFT_CTRL	0x403F0030
PASS_PASS_CTRL	0x403F0108
PASS_DSAB_TRIM	0x403F0F00

20.1.1 PASS_INTR_CAUSE

Interrupt cause register

Address: 0x403F0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							CTB0_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CTB0_INT	CTB0 interrupt pending Default Value: 0

20.1.2 PASS_DFT_CTRL

DFT control register

Address: 0x403F0030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DSAB_ADFT_RES_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	DSAB_ADFT_RES_EN	Close the switch to connect the DSAB ADFT resistor to the AMUXBUS Default Value: 0

20.1.3 PASS_PASS_CTRL

PASS Control

Address: 0x403F0108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						PMP-CLK_SRC	PMP-CLK_BYP

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RMB_BITS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	RMB_BITS	Risk mitigation bits Default Value: 0
1	PMPCLK_SRC	- 0: Pump clk is clk_hf - 1: Pump clk is direct from SRSS Default Value: 0
0	PMPCLK_BYP	- 0: Pump clk is clk_hf/2 - 1: Pump clk is selected from PMPCLK_SRC Default Value: 0

20.1.4 PASS_DSAB_TRIM

DSAB Trim bits

Address: 0x403F0F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [7:6]		DSAB_RMB_BITS [5:4]		IBIAS_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	DSAB_RMB_BITS	Risk mitigation bits Default Value: 0
3 : 0	IBIAS_TRIM	1111=lowest, 0000=highest Default Value: 0

21 Peripheral Interconnect Registers

This section discusses the Clock Dividers and Peripheral Interconnect (PERI) registers. It lists all the registers in mapping tables, in address order.

21.1 Register Details

Register Name	Address
PERI_DIV_CMD	0x40010000
PERI_PCLK_CTL0	0x40010100
PERI_PCLK_CTL1	0x40010104
PERI_PCLK_CTL2	0x40010108
PERI_PCLK_CTL3	0x4001010C
PERI_PCLK_CTL4	0x40010110
PERI_PCLK_CTL5	0x40010114
PERI_PCLK_CTL6	0x40010118
PERI_PCLK_CTL7	0x4001011C
PERI_PCLK_CTL8	0x40010120
PERI_PCLK_CTL9	0x40010124
PERI_PCLK_CTL10	0x40010128
PERI_PCLK_CTL11	0x4001012C
PERI_PCLK_CTL12	0x40010130
PERI_PCLK_CTL13	0x40010134
PERI_PCLK_CTL14	0x40010138
PERI_PCLK_CTL15	0x4001013C
PERI_PCLK_CTL16	0x40010140
PERI_PCLK_CTL17	0x40010144
PERI_PCLK_CTL18	0x40010148
PERI_DIV_16_CTL0	0x40010300
PERI_DIV_16_CTL1	0x40010304
PERI_DIV_16_CTL2	0x40010308
PERI_DIV_16_CTL3	0x4001030C
PERI_DIV_16_CTL4	0x40010310
PERI_DIV_16_CTL5	0x40010314
PERI_DIV_16_CTL6	0x40010318

Register Name	Address
PERI_DIV_16_CTL7	0x4001031C
PERI_DIV_16_CTL8	0x40010320
PERI_DIV_16_CTL9	0x40010324
PERI_DIV_16_CTL10	0x40010328
PERI_DIV_16_CTL11	0x4001032C
PERI_DIV_16_5_CTL0	0x40010400
PERI_DIV_16_5_CTL1	0x40010404
PERI_DIV_16_5_CTL2	0x40010408
PERI_DIV_16_5_CTL3	0x4001040C
PERI_DIV_16_5_CTL4	0x40010410
PERI_DIV_24_5_CTL	0x40010500
PERI_TR_CTL	0x40010600

21.1.1 PERI_DIV_CMD

Divider command register

Address: 0x40010000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	SEL_TYPE [7:6]		SEL_DIV [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW					
HW Access	R		R					
Name	PA_SEL_TYPE [15:14]		PA_SEL_DIV [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	RW1C	RW1C	None					
Name	ENABLE	DISABLE	None [29:24]					

Bits	Name	Description
31	ENABLE	Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to "0". If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the DIV_CMD.DISABLE field. 1: Configure the divider's DIV_XXX_CTL register. 2: Enable the divider using the DIV_CMD_ENABLE field. The SEL_DIV and SEL_TYPE fields specify which divider is to be enabled. The enabled divider may be phase aligned to either HFCLK (typical usage) or to ANY enabled divider. The PA_SEL_DIV and P_SEL_TYPE fields specify the reference divider. The HW sets the ENABLE field to '0' when the enabling is performed and the HW set the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of HFCLK/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to HFCLK takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process. Default Value: 0

(continued)

30	DISABLE	Clock divider disable command (mutually exlusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'. The SEL_DIV and SEL_TYPE fields specify which divider is to be disabled. The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately. Default Value: 0
15 : 14	PA_SEL_TYPE	Specifies the divider type of the divider to which phase alignment is performed for the clock enable command: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
13 : 8	PA_SEL_DIV	(PA_SEL_TYPE, PA_SEL_DIV) pecifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times. If PA_SEL_DIV is "63" and "PA_SEL_TYPE" is "3", HFCLK is used as reference. Default Value: 63
7 : 6	SEL_TYPE	Specifies the divider type of the divider on which the command is performed: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
5 : 0	SEL_DIV	(SEL_TYPE, SEL_DIV) specifies the divider on which the command (DISABLE/ENABLE) is performed. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock signal(s) are generated. Default Value: 63

21.1.2 PERI_PCLK_CTL0

Programmable clock control register

Address: 0x40010100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.3 PERI_PCLK_CTL1

Programmable clock control register

Address: 0x40010104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.4 PERI_PCLK_CTL2

Programmable clock control register

Address: 0x40010108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.5 PERI_PCLK_CTL3

Programmable clock control register

Address: 0x4001010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.6 PERI_PCLK_CTL4

Programmable clock control register

Address: 0x40010110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.7 PERI_PCLK_CTL5

Programmable clock control register

Address: 0x40010114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.8 PERI_PCLK_CTL6

Programmable clock control register

Address: 0x40010118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.9 PERI_PCLK_CTL7

Programmable clock control register

Address: 0x4001011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.10 PERI_PCLK_CTL8

Programmable clock control register

Address: 0x40010120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.11 PERI_PCLK_CTL9

Programmable clock control register

Address: 0x40010124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.12 PERI_PCLK_CTL10

Programmable clock control register

Address: 0x40010128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.13 PERI_PCLK_CTL11

Programmable clock control register

Address: 0x4001012C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.14 PERI_PCLK_CTL12

Programmable clock control register

Address: 0x40010130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.15 PERI_PCLK_CTL13

Programmable clock control register

Address: 0x40010134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.16 PERI_PCLK_CTL14

Programmable clock control register

Address: 0x40010138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.17 PERI_PCLK_CTL15

Programmable clock control register

Address: 0x4001013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.18 PERI_PCLK_CTL16

Programmable clock control register

Address: 0x40010140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.19 PERI_PCLK_CTL17

Programmable clock control register

Address: 0x40010144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.20 PERI_PCLK_CTL18

Programmable clock control register

Address: 0x40010148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one HFCLK cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

21.1.21 PERI_DIV_16_CTL0

Divider control register (for 16.0 divider)

Address: 0x40010300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.22 PERI_DIV_16_CTL1

Divider control register (for 16.0 divider)

Address: 0x40010304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.23 PERI_DIV_16_CTL2

Divider control register (for 16.0 divider)

Address: 0x40010308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.24 PERI_DIV_16_CTL3

Divider control register (for 16.0 divider)

Address: 0x4001030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.25 PERI_DIV_16_CTL4

Divider control register (for 16.0 divider)

Address: 0x40010310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.26 PERI_DIV_16_CTL5

Divider control register (for 16.0 divider)

Address: 0x40010314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.27 PERI_DIV_16_CTL6

Divider control register (for 16.0 divider)

Address: 0x40010318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.28 PERI_DIV_16_CTL7

Divider control register (for 16.0 divider)

Address: 0x4001031C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.29 PERI_DIV_16_CTL8

Divider control register (for 16.0 divider)

Address: 0x40010320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.30 PERI_DIV_16_CTL9

Divider control register (for 16.0 divider)

Address: 0x40010324

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.31 PERI_DIV_16_CTL10

Divider control register (for 16.0 divider)

Address: 0x40010328

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.32 PERI_DIV_16_CTL11

Divider control register (for 16.0 divider)

Address: 0x4001032C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.33 PERI_DIV_16_5_CTL0

Divider control register (for 16.5 divider)

Address: 0x40010400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 HFCLK cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

(continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.34 PERI_DIV_16_5_CTL1

Divider control register (for 16.5 divider)

Address: 0x40010404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 HFCLK cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

(continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.35 PERI_DIV_16_5_CTL2

Divider control register (for 16.5 divider)

Address: 0x40010408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 HFCLK cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

(continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.36 PERI_DIV_16_5_CTL3

Divider control register (for 16.5 divider)

Address: 0x4001040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 HFCLK cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

(continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.37 PERI_DIV_16_5_CTL4

Divider control register (for 16.5 divider)

Address: 0x40010410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 HFCLK cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

(continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.38 PERI_DIV_24_5_CTL

Divider control register (for 24.5 divider)

Address: 0x40010500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT24_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT24_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INT24_DIV [31:24]							

Bits	Name	Description
31 : 8	INT24_DIV	Integer division by (1+INT24_DIV). Allows for integer divisions in the range [1, 16,777,216]. Note: combined with fractional division, this divider type allows for a division in the range [1, 16,777,216 31/32] in 1/32 increments. For the generation of a divided clock, the integer division range is restricted to [2, 16,777,216 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 16,777,216]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 HFCLK cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

(continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

21.1.39 PERI_TR_CTL

Trigger control register

Address: 0x40010600

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TR_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				TR_GROUP [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	TR_COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	RW1C	R	None					
Name	TR_ACT	TR_OUT	None [29:24]					

Bits	Name	Description
31	TR_ACT	SW sets this field to '1' by to activate (set to '1') a trigger as identified by TR_SEL and TR_OUT for TR_COUNT cycles. HW sets this field to '0' when the cycle counter is decremented to "0". Note: a TR_COUNT value of 255 is a special case and trigger activation is under direct control of the TR_ACT field (the counter is not decremented). Default Value: 0
30	TR_OUT	Specifies whether trigger activation is for a specific input or ouput trigger of the trigger multiplexer. Activation of a specific input trigger, will result in activation of all output triggers that have the specific input trigger selected through their TR_OUT_CTL.SEL field. Activation of a specific output trigger, will result in activation of the specified TR_SEL output trigger only. '0': TR_SEL selection and trigger activation is for an input trigger to the trigger multiplexer. '1': TR_SEL selection and trigger activation is for an output trigger from the trigger multiplexer. Default Value: 0
23 : 16	TR_COUNT	Amount of cycles a specific trigger is activated. During activation (TR_ACT is '1'), HW decrements this field to "0" using a cycle counter. During activation, SW should not modify this register field. A value of 255 is a special case: HW does NOT decrement this field to "0" and trigger activation is under direct control of TR_ACT: when TR_ACT is '1' the trigger is activated and when TR_ACT is '0' the trigger is deactivated. Default Value: 0

(continued)

11 : 8	TR_GROUP	Specifies the trigger group. Default Value: 0
6 : 0	TR_SEL	Specifies the activated trigger when TR_ACT is '1'. TR_OUT specifies whether the activated trigger is an input trigger or output trigger to the trigger multiplexer. During activation (TR_ACT is '1'), SW should not modify this register field. If the specified trigger is not present, the trigger activation has no effect. Default Value: 0

22 Programmable IO Registers

This section discusses the Programmable IO (PRGIO) registers. It lists all the registers in mapping tables, in address order.

22.1 Register Details

Register Name	Address
PRGIO_PRT0_CTL	0x40050000
PRGIO_PRT0_SYNC_CTL	0x40050010
PRGIO_PRT0_LUT_SEL0	0x40050020
PRGIO_PRT0_LUT_SEL1	0x40050024
PRGIO_PRT0_LUT_SEL2	0x40050028
PRGIO_PRT0_LUT_SEL3	0x4005002C
PRGIO_PRT0_LUT_SEL4	0x40050030
PRGIO_PRT0_LUT_SEL5	0x40050034
PRGIO_PRT0_LUT_SEL6	0x40050038
PRGIO_PRT0_LUT_SEL7	0x4005003C
PRGIO_PRT0_LUT_CTL0	0x40050040
PRGIO_PRT0_LUT_CTL1	0x40050044
PRGIO_PRT0_LUT_CTL2	0x40050048
PRGIO_PRT0_LUT_CTL3	0x4005004C
PRGIO_PRT0_LUT_CTL4	0x40050050
PRGIO_PRT0_LUT_CTL5	0x40050054
PRGIO_PRT0_LUT_CTL6	0x40050058
PRGIO_PRT0_LUT_CTL7	0x4005005C
PRGIO_PRT0_DU_SEL	0x400500C0
PRGIO_PRT0_DU_CTL	0x400500C4
PRGIO_PRT0_DATA	0x400500F0
PRGIO_PRT1_CTL	0x40050100
PRGIO_PRT1_SYNC_CTL	0x40050110
PRGIO_PRT1_LUT_SEL0	0x40050120
PRGIO_PRT1_LUT_SEL1	0x40050124
PRGIO_PRT1_LUT_SEL2	0x40050128
PRGIO_PRT1_LUT_SEL3	0x4005012C

Register Name	Address
PRGIO_PRT1_LUT_SEL4	0x40050130
PRGIO_PRT1_LUT_SEL5	0x40050134
PRGIO_PRT1_LUT_SEL6	0x40050138
PRGIO_PRT1_LUT_SEL7	0x4005013C
PRGIO_PRT1_LUT_CTL0	0x40050140
PRGIO_PRT1_LUT_CTL1	0x40050144
PRGIO_PRT1_LUT_CTL2	0x40050148
PRGIO_PRT1_LUT_CTL3	0x4005014C
PRGIO_PRT1_LUT_CTL4	0x40050150
PRGIO_PRT1_LUT_CTL5	0x40050154
PRGIO_PRT1_LUT_CTL6	0x40050158
PRGIO_PRT1_LUT_CTL7	0x4005015C
PRGIO_PRT1_DU_SEL	0x400501C0
PRGIO_PRT1_DU_CTL	0x400501C4
PRGIO_PRT1_DATA	0x400501F0
PRGIO_PRT2_CTL	0x40050200
PRGIO_PRT2_SYNC_CTL	0x40050210
PRGIO_PRT2_LUT_SEL0	0x40050220
PRGIO_PRT2_LUT_SEL1	0x40050224
PRGIO_PRT2_LUT_SEL2	0x40050228
PRGIO_PRT2_LUT_SEL3	0x4005022C
PRGIO_PRT2_LUT_SEL4	0x40050230
PRGIO_PRT2_LUT_SEL5	0x40050234
PRGIO_PRT2_LUT_SEL6	0x40050238
PRGIO_PRT2_LUT_SEL7	0x4005023C
PRGIO_PRT2_LUT_CTL0	0x40050240
PRGIO_PRT2_LUT_CTL1	0x40050244
PRGIO_PRT2_LUT_CTL2	0x40050248
PRGIO_PRT2_LUT_CTL3	0x4005024C
PRGIO_PRT2_LUT_CTL4	0x40050250
PRGIO_PRT2_LUT_CTL5	0x40050254
PRGIO_PRT2_LUT_CTL6	0x40050258
PRGIO_PRT2_LUT_CTL7	0x4005025C
PRGIO_PRT2_DU_SEL	0x400502C0
PRGIO_PRT2_DU_CTL	0x400502C4
PRGIO_PRT2_DATA	0x400502F0

22.1.1 PRGIO_PRT0_CTL

Control register

Address: 0x40050000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BYPASS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			CLOCK_SRC [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	RW
HW Access	R	None					R	R
Name	ENABLED	None [30:26]					PIPE-LINE_EN	HLD_OVR

Bits	Name	Description
31	ENABLED	Enable for programmable IO. Should only be set to '1' when the programmable IO is completely configured: '0': Disabled (signals are bypassed; behavior as if BYPASS is 0xFF). When disabled, the fabric (data unit and LUTs) reset is activated. If the block is disabled: - The PIPELINE_EN register field should be set to '1', to ensure low power consumption by preventing combinatorial loops. - The CLOCK_SRC register field should be set to "20"-"30" (clock is constant '0'), to ensure low power consumption. '1': Enabled. Once enabled, it takes 3 "clk_block" clock cycles till the block reset is de-activated and the block becomes fully functional. This ensures that the IO pins' input synchronizer states are flushed when the block is fully functional. Default Value: 0
25	PIPELINE_EN	Enable for pipeline register: '0': Disabled (register is bypassed). '1': Enabled. Default Value: 1

(continued)

24	HLD_OVR	IO cell hold override functionality. In DeepSleep power mode, the HSIOM holds the IO cell output and output enable signals by default. This is undesirable if the PRGIO is supposed to deliver DeepSleep output functionality on these IO pads. This field is used to control the hold override functionality from the PRGIO: GPIO hold-override functionality in DeepSleep: '0': The HSIOM controls the GPIO functionality in DeepSleep '1': In bypass mode (ENABLED is '0' or BYPASS[i] is '1'), the HSIOM controls GPIO. In NON bypass mode (ENABLED is '1' and BYPASS[i] is '0'), the PRGIO controls the GPIO functionality in DeepSleep power mode. Default Value: Undefined
12 : 8	CLOCK_SRC	Clock ("clk_block") and reset ("rst_block_n") source selection: "0": io_data_in[0]/'1'. ... "7": io_data_in[7]/'1'. "8": chip_data[0]/'1'. ... "15": chip_data[7]/'1'. "16": clk_prgio/rst_sys_act_n. Used for Active mode synchronous logic on "clk_prgio". This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_prgio"). Note that the block's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". This selection asserts reset in any power mode other than Active i.e. PRGIO is active only in Active power mode with clock from peripheral divider "17": clk_prgio/rst_sys_dpslp_n. Used for DeepSleep mode synchronous logic on "clk_prgio" (note that "clk_prgio" is NOT available in DeepSleep power mode). This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_prgio"). This selection enables PRGIO in all power modes with clock from peripheral divider but the clock will not be active in DeepSleep power mode (i.e only asynchronous/combinational logics will work in DeepSleep). "19": clk_lf/rst_lf_dpslp_n (note that "clk_lf" is only available in DeepSleep power mode). This selection is intended for synchronous operation on"clk_lf". Note that the block's clocked elements are frequency aligned, but NOT phase aligned to other "clk_lf" clocked elements. This selection enables PRGIO in all power modes with clock from ILO (clk_lf) synchronous operations in DeepSleep will use clk_lf. "20"-"30": Clock source is constant '0'. Any of these clock sources should be selected when the IP is disabled to ensure low power consumption. "31": clk_sys/'1'. This selection is NOT intended for "clk_sys" operation, but for asynchronous operation: three "clk_sys" cycles after enabling the IP, the IP is fully functional (reset is de-activated). To be used for asynchronous (clockless) block functionality. Default Value: 20
7 : 0	BYPASS	Bypass of the programmable IO - BYPASS[i] is for IO pin i. '0': No bypass '1': Bypass Default Value: Undefined

22.1.2 PRGIO_PRT0_SYNC_CTL

Synchronization control register

Address: 0x40050010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IO_SYNC_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHIP_SYNC_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CHIP_SYNC_EN	Synchronization of the chip input signals to "clk_fabric", one bit for each input: CHIP_SYNC_EN[i] is for input i. '0': No synchronization. '1': Synchronization. Default Value: Undefined
7 : 0	IO_SYNC_EN	Synchronization of the IO pin input signals to "clk_fabric", one bit for each IO pin: IO_SYNC_EN[i] is for IO pin i. '0': No synchronization. '1': Synchronization. Default Value: Undefined

22.1.3 PRGIO_PRT0_LUT_SEL0

LUT component input selection

Address: 0x40050020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.4 PRGIO_PRT0_LUT_SEL1

LUT component input selection

Address: 0x40050024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.5 PRGIO_PRT0_LUT_SEL2

LUT component input selection

Address: 0x40050028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.6 PRGIO_PRT0_LUT_SEL3

LUT component input selection

Address: 0x4005002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.7 PRGIO_PRT0_LUT_SEL4

LUT component input selection

Address: 0x40050030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.8 PRGIO_PRT0_LUT_SEL5

LUT component input selection

Address: 0x40050034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.9 PRGIO_PRT0_LUT_SEL6

LUT component input selection

Address: 0x40050038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.10 PRGIO_PRT0_LUT_SEL7

LUT component input selection

Address: 0x4005003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.11 PRGIO_PRT0_LUT_CTL0

LUT component control register

Address: 0x40050040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.12 PRGIO_PRT0_LUT_CTL1

LUT component control register

Address: 0x40050044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.13 PRGIO_PRT0_LUT_CTL2

LUT component control register

Address: 0x40050048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.14 PRGIO_PRT0_LUT_CTL3

LUT component control register

Address: 0x4005004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.15 PRGIO_PRT0_LUT_CTL4

LUT component control register

Address: 0x40050050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.16 PRGIO_PRT0_LUT_CTL5

LUT component control register

Address: 0x40050054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.17 PRGIO_PRT0_LUT_CTL6

LUT component control register

Address: 0x40050058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.18 PRGIO_PRT0_LUT_CTL7

LUT component control register

Address: 0x4005005C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.19 PRGIO_PRT0_DU_SEL

Data unit component input selection

Address: 0x400500C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DU_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				DU_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None		RW	
HW Access	None		R		None		R	
Name	None [31:30]		DU_DATA1_SEL [29:28]		None [27:26]		DU_DATA0_SEL [25:24]	

Bits	Name	Description
29 : 28	DU_DATA1_SEL	Data unit input data "data1_in" source selection. Encoding is the same as for DU_DATA0_SEL. Default Value: Undefined
25 : 24	DU_DATA0_SEL	Data unit input data "data0_in" source selection: "0": Constant "0". "1": chip_data[7:0]. "2": io_data_in[7:0]. "3": DATA.DATA MMIO register field. Default Value: Undefined
19 : 16	DU_TR2_SEL	Data unit input signal "tr2_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined
11 : 8	DU_TR1_SEL	Data unit input signal "tr1_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined

(continued)

3 : 0	DU_TR0_SEL	Data unit input signal "tr0_in" source selection: "0": Constant '0'. "1": Constant '1'. "2": Data unit output. "10-3": LUT 7 - 0 outputs. Otherwise: Undefined. Default Value: Undefined

22.1.20 PRGIO_PRT0_DU_CTL

Data unit component control register

Address: 0x400500C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DU_SIZE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_OPC [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	DU_OPC	Data unit opcode specifies the data unit operation: "1": INCR "2": DECR "3": INCR_WRAP "4": DECR_WRAP "5": INCR_DECR "6": INCR_DECR_WRAP "7": ROR "8": SHR "9": AND_OR "10": SHR_MAJ3 "11": SHR_EQL. Otherwise: Undefined. Default Value: Undefined
2 : 0	DU_SIZE	Size/width of the data unit data operands (in bits) is DU_SIZE+1. E.g., if DU_SIZE is 7, the width is 8 bits. Default Value: Undefined

22.1.21 PRGIO_PRT0_DATA

Data register

Address: 0x400500F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Data unit input data source. Default Value: Undefined

22.1.22 PRGIO_PRT1_CTL

Control register

Address: 0x40050100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BYPASS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			CLOCK_SRC [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	RW
HW Access	R	None					R	R
Name	ENABLED	None [30:26]					PIPE-LINE_EN	HLD_OVR

Bits	Name	Description
31	ENABLED	Enable for programmable IO. Should only be set to '1' when the programmable IO is completely configured: '0': Disabled (signals are bypassed; behavior as if BYPASS is 0xFF). When disabled, the fabric (data unit and LUTs) reset is activated. If the block is disabled: - The PIPELINE_EN register field should be set to '1', to ensure low power consumption by preventing combinatorial loops. - The CLOCK_SRC register field should be set to "20"-"30" (clock is constant '0'), to ensure low power consumption. '1': Enabled. Once enabled, it takes 3 "clk_block" clock cycles till the block reset is de-activated and the block becomes fully functional. This ensures that the IO pins' input synchronizer states are flushed when the block is fully functional. Default Value: 0
25	PIPELINE_EN	Enable for pipeline register: '0': Disabled (register is bypassed). '1': Enabled. Default Value: 1

(continued)

24	HLD_OVR	IO cell hold override functionality. In DeepSleep power mode, the HSIOM holds the IO cell output and output enable signals by default. This is undesirable if the PRGIO is supposed to deliver DeepSleep output functionality on these IO pads. This field is used to control the hold override functionality from the PRGIO: GPIO hold-override functionality in DeepSleep: '0': The HSIOM controls the GPIO functionality in DeepSleep '1': In bypass mode (ENABLED is '0' or BYPASS[i] is '1'), the HSIOM controls GPIO. In NON bypass mode (ENABLED is '1' and BYPASS[i] is '0'), the PRGIO controls the GPIO functionality in DeepSleep power mode. Default Value: Undefined
12 : 8	CLOCK_SRC	Clock ("clk_block") and reset ("rst_block_n") source selection: "0": io_data_in[0]/'1'. ... "7": io_data_in[7]/'1'. "8": chip_data[0]/'1'. ... "15": chip_data[7]/'1'. "16": clk_prgio/rst_sys_act_n. Used for Active mode synchronous logic on "clk_prgio". This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_prgio"). Note that the block's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". This selection asserts reset in any power mode other than Active i.e. PRGIO is active only in Active power mode with clock from peripheral divider "17": clk_prgio/rst_sys_dpslp_n. Used for DeepSleep mode synchronous logic on "clk_prgio" (note that "clk_prgio" is NOT available in DeepSleep power mode). This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_prgio"). This selection enables PRGIO in all power modes with clock from peripheral divider but the clock will not be active in DeepSleep power mode (i.e only asynchronous/combinational logics will work in DeepSleep). "19": clk_lf/rst_lf_dpslp_n (note that "clk_lf" is only available in DeepSleep power mode). This selection is intended for synchronous operation on"clk_lf". Note that the block's clocked elements are frequency aligned, but NOT phase aligned to other "clk_lf" clocked elements. This selection enables PRGIO in all power modes with clock from ILO (clk_lf) synchronous operations in DeepSleep will use clk_lf. "20"-"30": Clock source is constant '0'. Any of these clock sources should be selected when the IP is disabled to ensure low power consumption. "31": clk_sys/'1'. This selection is NOT intended for "clk_sys" operation, but for asynchronous operation: three "clk_sys" cycles after enabling the IP, the IP is fully functional (reset is de-activated). To be used for asynchronous (clockless) block functionality. Default Value: 20
7 : 0	BYPASS	Bypass of the programmable IO - BYPASS[i] is for IO pin i. '0': No bypass '1': Bypass Default Value: Undefined

22.1.23 PRGIO_PRT1_SYNC_CTL

Synchronization control register

Address: 0x40050110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IO_SYNC_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHIP_SYNC_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CHIP_SYNC_EN	Synchronization of the chip input signals to "clk_fabric", one bit for each input: CHIP_SYNC_EN[i] is for input i. '0': No synchronization. '1': Synchronization. Default Value: Undefined
7 : 0	IO_SYNC_EN	Synchronization of the IO pin input signals to "clk_fabric", one bit for each IO pin: IO_SYNC_EN[i] is for IO pin i. '0': No synchronization. '1': Synchronization. Default Value: Undefined

22.1.24 PRGIO_PRT1_LUT_SEL0

LUT component input selection

Address: 0x40050120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.25 PRGIO_PRT1_LUT_SEL1

LUT component input selection

Address: 0x40050124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.26 PRGIO_PRT1_LUT_SEL2

LUT component input selection

Address: 0x40050128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.27 PRGIO_PRT1_LUT_SEL3

LUT component input selection

Address: 0x4005012C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.28 PRGIO_PRT1_LUT_SEL4

LUT component input selection

Address: 0x40050130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.29 PRGIO_PRT1_LUT_SEL5

LUT component input selection

Address: 0x40050134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.30 PRGIO_PRT1_LUT_SEL6

LUT component input selection

Address: 0x40050138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.31 PRGIO_PRT1_LUT_SEL7

LUT component input selection

Address: 0x4005013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.32 PRGIO_PRT1_LUT_CTL0

LUT component control register

Address: 0x40050140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.33 PRGIO_PRT1_LUT_CTL1

LUT component control register

Address: 0x40050144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.34 PRGIO_PRT1_LUT_CTL2

LUT component control register

Address: 0x40050148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.35 PRGIO_PRT1_LUT_CTL3

LUT component control register

Address: 0x4005014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.36 PRGIO_PRT1_LUT_CTL4

LUT component control register

Address: 0x40050150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.37 PRGIO_PRT1_LUT_CTL5

LUT component control register

Address: 0x40050154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.38 PRGIO_PRT1_LUT_CTL6

LUT component control register

Address: 0x40050158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.39 PRGIO_PRT1_LUT_CTL7

LUT component control register

Address: 0x4005015C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.40 PRGIO_PRT1_DU_SEL

Data unit component input selection

Address: 0x400501C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DU_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				DU_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None		RW	
HW Access	None		R		None		R	
Name	None [31:30]		DU_DATA1_SEL [29:28]		None [27:26]		DU_DATA0_SEL [25:24]	

Bits	Name	Description
29 : 28	DU_DATA1_SEL	Data unit input data "data1_in" source selection. Encoding is the same as for DU_DATA0_SEL. Default Value: Undefined
25 : 24	DU_DATA0_SEL	Data unit input data "data0_in" source selection: "0": Constant "0". "1": chip_data[7:0]. "2": io_data_in[7:0]. "3": DATA.DATA MMIO register field. Default Value: Undefined
19 : 16	DU_TR2_SEL	Data unit input signal "tr2_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined
11 : 8	DU_TR1_SEL	Data unit input signal "tr1_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined

(continued)

3 : 0	DU_TR0_SEL	Data unit input signal "tr0_in" source selection: "0": Constant '0'. "1": Constant '1'. "2": Data unit output. "10-3": LUT 7 - 0 outputs. Otherwise: Undefined. Default Value: Undefined

22.1.41 PRGIO_PRT1_DU_CTL

Data unit component control register

Address: 0x400501C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DU_SIZE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_OPC [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	DU_OPC	Data unit opcode specifies the data unit operation: "1": INCR "2": DECR "3": INCR_WRAP "4": DECR_WRAP "5": INCR_DECR "6": INCR_DECR_WRAP "7": ROR "8": SHR "9": AND_OR "10": SHR_MAJ3 "11": SHR_EQL. Otherwise: Undefined. Default Value: Undefined
2 : 0	DU_SIZE	Size/width of the data unit data operands (in bits) is DU_SIZE+1. E.g., if DU_SIZE is 7, the width is 8 bits. Default Value: Undefined

22.1.42 PRGIO_PRT1_DATA

Data register

Address: 0x400501F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Data unit input data source. Default Value: Undefined

22.1.43 PRGIO_PRT2_CTL

Control register

Address: 0x40050200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BYPASS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			CLOCK_SRC [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	RW
HW Access	R	None					R	R
Name	ENABLED	None [30:26]					PIPE-LINE_EN	HLD_OVR

Bits	Name	Description
31	ENABLED	Enable for programmable IO. Should only be set to '1' when the programmable IO is completely configured: '0': Disabled (signals are bypassed; behavior as if BYPASS is 0xFF). When disabled, the fabric (data unit and LUTs) reset is activated. If the block is disabled: - The PIPELINE_EN register field should be set to '1', to ensure low power consumption by preventing combinatorial loops. - The CLOCK_SRC register field should be set to "20"-"30" (clock is constant '0'), to ensure low power consumption. '1': Enabled. Once enabled, it takes 3 "clk_block" clock cycles till the block reset is de-activated and the block becomes fully functional. This ensures that the IO pins' input synchronizer states are flushed when the block is fully functional. Default Value: 0
25	PIPELINE_EN	Enable for pipeline register: '0': Disabled (register is bypassed). '1': Enabled. Default Value: 1

(continued)

24	HLD_OVR	IO cell hold override functionality. In DeepSleep power mode, the HSIOM holds the IO cell output and output enable signals by default. This is undesirable if the PRGIO is supposed to deliver DeepSleep output functionality on these IO pads. This field is used to control the hold override functionality from the PRGIO: GPIO hold-override functionality in DeepSleep: '0': The HSIOM controls the GPIO functionality in DeepSleep '1': In bypass mode (ENABLED is '0' or BYPASS[i] is '1'), the HSIOM controls GPIO. In NON bypass mode (ENABLED is '1' and BYPASS[i] is '0'), the PRGIO controls the GPIO functionality in DeepSleep power mode. Default Value: Undefined
12 : 8	CLOCK_SRC	Clock ("clk_block") and reset ("rst_block_n") source selection: "0": io_data_in[0]/'1'. ... "7": io_data_in[7]/'1'. "8": chip_data[0]/'1'. ... "15": chip_data[7]/'1'. "16": clk_prgio/rst_sys_act_n. Used for Active mode synchronous logic on "clk_prgio". This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_prgio"). Note that the block's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". This selection asserts reset in any power mode other than Active i.e. PRGIO is active only in Active power mode with clock from peripheral divider "17": clk_prgio/rst_sys_dpslp_n. Used for DeepSleep mode synchronous logic on "clk_prgio" (note that "clk_prgio" is NOT available in DeepSleep power mode). This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_prgio"). This selection enables PRGIO in all power modes with clock from peripheral divider but the clock will not be active in DeepSleep power mode (i.e only asynchronous/combinational logics will work in DeepSleep). "19": clk_lf/rst_lf_dpslp_n (note that "clk_lf" is only available in DeepSleep power mode). This selection is intended for synchronous operation on"clk_lf". Note that the block's clocked elements are frequency aligned, but NOT phase aligned to other "clk_lf" clocked elements. This selection enables PRGIO in all power modes with clock from ILO (clk_lf) synchronous operations in DeepSleep will use clk_lf. "20"-"30": Clock source is constant '0'. Any of these clock sources should be selected when the IP is disabled to ensure low power consumption. "31": clk_sys/'1'. This selection is NOT intended for "clk_sys" operation, but for asynchronous operation: three "clk_sys" cycles after enabling the IP, the IP is fully functional (reset is de-activated). To be used for asynchronous (clockless) block functionality. Default Value: 20
7 : 0	BYPASS	Bypass of the programmable IO - BYPASS[i] is for IO pin i. '0': No bypass '1': Bypass Default Value: Undefined

22.1.44 PRGIO_PRT2_SYNC_CTL

Synchronization control register

Address: 0x40050210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IO_SYNC_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHIP_SYNC_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CHIP_SYNC_EN	Synchronization of the chip input signals to "clk_fabric", one bit for each input: CHIP_SYNC_EN[i] is for input i. '0': No synchronization. '1': Synchronization. Default Value: Undefined
7 : 0	IO_SYNC_EN	Synchronization of the IO pin input signals to "clk_fabric", one bit for each IO pin: IO_SYNC_EN[i] is for IO pin i. '0': No synchronization. '1': Synchronization. Default Value: Undefined

22.1.45 PRGIO_PRT2_LUT_SEL0

LUT component input selection

Address: 0x40050220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.46 PRGIO_PRT2_LUT_SEL1

LUT component input selection

Address: 0x40050224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.47 PRGIO_PRT2_LUT_SEL2

LUT component input selection

Address: 0x40050228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.48 PRGIO_PRT2_LUT_SEL3

LUT component input selection

Address: 0x4005022C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.49 PRGIO_PRT2_LUT_SEL4

LUT component input selection

Address: 0x40050230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.50 PRGIO_PRT2_LUT_SEL5

LUT component input selection

Address: 0x40050234

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.51 PRGIO_PRT2_LUT_SEL6

LUT component input selection

Address: 0x40050238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.52 PRGIO_PRT2_LUT_SEL7

LUT component input selection

Address: 0x4005023C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

(continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

22.1.53 PRGIO_PRT2_LUT_CTL0

LUT component control register

Address: 0x40050240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.54 PRGIO_PRT2_LUT_CTL1

LUT component control register

Address: 0x40050244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.55 PRGIO_PRT2_LUT_CTL2

LUT component control register

Address: 0x40050248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.56 PRGIO_PRT2_LUT_CTL3

LUT component control register

Address: 0x4005024C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.57 PRGIO_PRT2_LUT_CTL4

LUT component control register

Address: 0x40050250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.58 PRGIO_PRT2_LUT_CTL5

LUT component control register

Address: 0x40050254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.59 PRGIO_PRT2_LUT_CTL6

LUT component control register

Address: 0x40050258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.60 PRGIO_PRT2_LUT_CTL7

LUT component control register

Address: 0x4005025C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

(continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

22.1.61 PRGIO_PRT2_DU_SEL

Data unit component input selection

Address: 0x400502C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DU_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				DU_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None		RW	
HW Access	None		R		None		R	
Name	None [31:30]		DU_DATA1_SEL [29:28]		None [27:26]		DU_DATA0_SEL [25:24]	

Bits	Name	Description
29 : 28	DU_DATA1_SEL	Data unit input data "data1_in" source selection. Encoding is the same as for DU_DATA0_SEL. Default Value: Undefined
25 : 24	DU_DATA0_SEL	Data unit input data "data0_in" source selection: "0": Constant "0". "1": chip_data[7:0]. "2": io_data_in[7:0]. "3": DATA.DATA MMIO register field. Default Value: Undefined
19 : 16	DU_TR2_SEL	Data unit input signal "tr2_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined
11 : 8	DU_TR1_SEL	Data unit input signal "tr1_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined

(continued)

3 : 0	DU_TR0_SEL	Data unit input signal "tr0_in" source selection: "0": Constant '0'. "1": Constant '1'. "2": Data unit output. "10-3": LUT 7 - 0 outputs. Otherwise: Undefined. Default Value: Undefined

22.1.62 PRGIO_PRT2_DU_CTL

Data unit component control register

Address: 0x400502C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DU_SIZE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_OPC [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	DU_OPC	Data unit opcode specifies the data unit operation: "1": INCR "2": DECR "3": INCR_WRAP "4": DECR_WRAP "5": INCR_DECR "6": INCR_DECR_WRAP "7": ROR "8": SHR "9": AND_OR "10": SHR_MAJ3 "11": SHR_EQL. Otherwise: Undefined. Default Value: Undefined
2 : 0	DU_SIZE	Size/width of the data unit data operands (in bits) is DU_SIZE+1. E.g., if DU_SIZE is 7, the width is 8 bits. Default Value: Undefined

22.1.63 PRGIO_PRT2_DATA

Data register

Address: 0x400502F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Data unit input data source. Default Value: Undefined

23 ROM Table Registers

This section discusses the ROM Table registers. It lists all the registers in mapping tables, in address order.

23.1 Register Details

Register Name	Address
ROMTABLE_ADDR	0xF0000000
ROMTABLE_DID	0xF0000FCC
ROMTABLE_PID4	0xF0000FD0
ROMTABLE_PID5	0xF0000FD4
ROMTABLE_PID6	0xF0000FD8
ROMTABLE_PID7	0xF0000FDC
ROMTABLE_PID0	0xF0000FE0
ROMTABLE_PID1	0xF0000FE4
ROMTABLE_PID2	0xF0000FE8
ROMTABLE_PID3	0xF0000FEC
ROMTABLE_CID0	0xF0000FF0
ROMTABLE_CID1	0xF0000FF4
ROMTABLE_CID2	0xF0000FF8
ROMTABLE_CID3	0xF0000FFC

23.1.1 ROMTABLE_ADDR

Link to Cortex M0 ROM Table.

Address: 0xF0000000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						R	R
Name	None [7:2]						FOR-MAT_32BIT	PRESENT

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			
HW Access	R				None			
Name	ADDR_OFFSET [15:12]				None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [31:24]							

Bits	Name	Description
31 : 12	ADDR_OFFSET	Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000). ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. Default Value: 983295
1	FORMAT_32BIT	ROM Table format: '0: 8-bit format. '1': 32-bit format. Default Value: 1
0	PRESENT	Entry present. Default Value: 1

23.1.2 ROMTABLE_DID

Device Type Identifier register.

Address: 0xF0000FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 1

23.1.3 ROMTABLE_PID4

Peripheral Identification Register 4.

Address: 0xF0000FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	COUNT [7:4]				JEP_CONTINUATION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	COUNT	Size of ROM Table is 2^COUNT * 4 KByte. Default Value: 0
3 : 0	JEP_CONTINUATION	JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter. Default Value: Undefined

23.1.4 ROMTABLE_PID5

Peripheral Identification Register 5.

Address: 0xF0000FD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

23.1.5 ROMTABLE_PID6

Peripheral Identification Register 6.

Address: 0xF0000FD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

23.1.6 ROMTABLE_PID7

Peripheral Identification Register 7.

Address: 0xF0000FDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

23.1.7 ROMTABLE_PID0

Peripheral Identification Register 0.

Address: 0xF0000FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PN_MIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PN_MIN	JEP106 part number. 4 lsbs of CPUSS.PARTNUMBER parameter. These part numbers are maintained in spec 40-9500. Default Value: Undefined

23.1.8 ROMTABLE_PID1

Peripheral Identification Register 1.

Address: 0xF0000FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	JEPID_MIN [7:4]				PN_MAJ [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	JEPID_MIN	JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter. This number is maintained in spec 40-9500. Default Value: Undefined
3 : 0	PN_MAJ	JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter. These part numbers are maintained in spec 40-9500. Default Value: Undefined

23.1.9 ROMTABLE_PID2

Peripheral Identification Register 2.

Address: 0xF0000FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None	R		
HW Access	R				None	R		
Name	REV [7:4]				None	JEPID_MAJ [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV	Major REVision number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is implemented in RTL by an ECO-able tie-off structure and is incremented on subsequent tape outs. Default Value: Undefined
2 : 0	JEPID_MAJ	JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter. This number is maintained in spec 40-9500. Default Value: Undefined

23.1.10 ROMTABLE_PID3

Peripheral Identification Register 3.

Address: 0xF0000FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	REV_AND [7:4]				CM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV_AND	Minor REVision number (chip specific). For first tape out: 0x1. This field is implemented in RTL by an ECO-able tie-off structure and is incremented on subsequent tape outs. Default Value: Undefined
3 : 0	CM	Customer modified field. This field is used to track modifications to the original component design as a result of componenet IP reuse. Default Value: 0

23.1.11 ROMTABLE_CID0

Component Identification Register 0.

Address: 0xF0000FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 0 of 4-byte component identification 0xB105:100D. Default Value: 13

23.1.12 ROMTABLE_CID1

Component Identification Register 1.

Address: 0xF0000FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: "ROM Table". Default Value: 16

23.1.13 ROMTABLE_CID2

Component Identification Register 2.

Address: 0xF0000FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 2 of 4-byte component identification 0xB105:100D. Default Value: 5

23.1.14 ROMTABLE_CID3

Component Identification Register 3.

Address: 0xF0000FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 3 of 4-byte component identification 0xB105:100D. Default Value: 177

24 SAR Registers

This section discusses the SAR registers. It lists all the registers in mapping tables, in address order.

24.1 Register Details

Register Name	Address
SAR_CTRL	0x403A0000
SAR_SAMPLE_CTRL	0x403A0004
SAR_SAMPLE_TIME01	0x403A0010
SAR_SAMPLE_TIME23	0x403A0014
SAR_RANGE_THRES	0x403A0018
SAR_RANGE_COND	0x403A001C
SAR_CHAN_EN	0x403A0020
SAR_START_CTRL	0x403A0024
SAR_DFT_CTRL	0x403A0030
SAR_CHAN_CONFIG0	0x403A0080
SAR_CHAN_CONFIG1	0x403A0084
SAR_CHAN_CONFIG2	0x403A0088
SAR_CHAN_CONFIG3	0x403A008C
SAR_CHAN_CONFIG4	0x403A0090
SAR_CHAN_CONFIG5	0x403A0094
SAR_CHAN_CONFIG6	0x403A0098
SAR_CHAN_CONFIG7	0x403A009C
SAR_CHAN_CONFIG8	0x403A00A0
SAR_CHAN_CONFIG9	0x403A00A4
SAR_CHAN_CONFIG10	0x403A00A8
SAR_CHAN_CONFIG11	0x403A00AC
SAR_CHAN_CONFIG12	0x403A00B0
SAR_CHAN_CONFIG13	0x403A00B4
SAR_CHAN_CONFIG14	0x403A00B8
SAR_CHAN_CONFIG15	0x403A00BC
SAR_CHAN_WORK0	0x403A0100
SAR_CHAN_WORK1	0x403A0104

Register Name	Address
SAR_CHAN_WORK2	0x403A0108
SAR_CHAN_WORK3	0x403A010C
SAR_CHAN_WORK4	0x403A0110
SAR_CHAN_WORK5	0x403A0114
SAR_CHAN_WORK6	0x403A0118
SAR_CHAN_WORK7	0x403A011C
SAR_CHAN_WORK8	0x403A0120
SAR_CHAN_WORK9	0x403A0124
SAR_CHAN_WORK10	0x403A0128
SAR_CHAN_WORK11	0x403A012C
SAR_CHAN_WORK12	0x403A0130
SAR_CHAN_WORK13	0x403A0134
SAR_CHAN_WORK14	0x403A0138
SAR_CHAN_WORK15	0x403A013C
SAR_CHAN_RESULT0	0x403A0180
SAR_CHAN_RESULT1	0x403A0184
SAR_CHAN_RESULT2	0x403A0188
SAR_CHAN_RESULT3	0x403A018C
SAR_CHAN_RESULT4	0x403A0190
SAR_CHAN_RESULT5	0x403A0194
SAR_CHAN_RESULT6	0x403A0198
SAR_CHAN_RESULT7	0x403A019C
SAR_CHAN_RESULT8	0x403A01A0
SAR_CHAN_RESULT9	0x403A01A4
SAR_CHAN_RESULT10	0x403A01A8
SAR_CHAN_RESULT11	0x403A01AC
SAR_CHAN_RESULT12	0x403A01B0
SAR_CHAN_RESULT13	0x403A01B4
SAR_CHAN_RESULT14	0x403A01B8
SAR_CHAN_RESULT15	0x403A01BC
SAR_CHAN_WORK_VALID	0x403A0200
SAR_CHAN_RESULT_VALID	0x403A0204
SAR_STATUS	0x403A0208
SAR_AVG_STAT	0x403A020C
SAR_INTR	0x403A0210
SAR_INTR_SET	0x403A0214
SAR_INTR_MASK	0x403A0218
SAR_INTR_MASKED	0x403A021C
SAR_SATURATE_INTR	0x403A0220
SAR_SATURATE_INTR_SET	0x403A0224
SAR_SATURATE_INTR_MASK	0x403A0228
SAR_SATURATE_INTR_MASKED	0x403A022C

Register Name	Address
SAR_RANGE_INTR	0x403A0230
SAR_RANGE_INTR_SET	0x403A0234
SAR_RANGE_INTR_MASK	0x403A0238
SAR_RANGE_INTR_MASKED	0x403A023C
SAR_INTR_CAUSE	0x403A0240
SAR_INJ_CHAN_CONFIG	0x403A0280
SAR_INJ_RESULT	0x403A0290
SAR_MUX_SWITCH0	0x403A0300
SAR_MUX_SWITCH_CLEAR0	0x403A0304
SAR_MUX_SWITCH1	0x403A0308
SAR_MUX_SWITCH_CLEAR1	0x403A030C
SAR_MUX_SWITCH_HW_CTRL	0x403A0340
SAR_MUX_SWITCH_STATUS	0x403A0348
SAR_PUMP_CTRL	0x403A0380
SAR_ANA_TRIM	0x403A0F00
SAR_WOUNDING	0x403A0F04

24.1.1 SAR_CTRL

Analog control register.

Address: 0x403A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			None			
HW Access	R	R			None			
Name	VREF_BY-P_CAP_EN	VREF_SEL [6:4]			None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	None	RW			None
HW Access	R		R	None	R			None
Name	PWR_CTRL_VREF [15:14]		SAR_HW_CTRL_NEG VREF	None	NEG_SEL [11:9]			None

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [23:21]			BOOST-PUMP_EN	SPARE [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	None	RW	
HW Access	R	R	R	R	R	None	R	
Name	ENABLED	SWITCH_-DISABLE	DSI_MODE	DSI_SYN-C_CONFIG	DEEPS-LEEP_ON	None	ICONT_LV [25:24]	

Bits	Name	Description
31	ENABLED	0: SAR Disabled (power downs the analog and stops the clocks) 1: SAR Enabled (before enabling make sure SAR is idle - STATUS.BUSY is 0) Default Value: 0
30	SWITCH_DISABLE	Disable SAR sequencer from enabling routing switches (note firmware can always close switch-es independent of this control) 0: Normal mode, SAR sequencer changes switches according to pin address in channel config-urations 1: Switches disabled, SAR sequencer does not enable any switches, it is the responsibility of the firmware to set the switches to route the signal to be converted through the SARMUX Default Value: 0
29	DSI_MODE	Reserved Default Value: 0
28	DSI_SYNC_CONFIG	Reserved Default Value: 1

(continued)

27	DEEPSLEEP_ON	0: SARMUX disabled during deep-sleep power mode 1: SARMUX remains enabled during deep-sleep power mode if ENABLED bit is 1. Default Value: 0
25 : 24	ICONT_LV	SAR ADC Low Power Mode Default Value: 0 **0x0: NORMAL_PWR:** Normal Power (maximum ADC clock frequency of 18MHz) **0x1: HALF_PWR:** 1/2 Power (maximum ADC clock frequency of 9MHz) **0x2: MORE_PWR:** 4/3 Power (maximum ADC clock frequency of 18MHz) **0x3: QUARTER_PWR:** 1/4 Power (maximum ADC clock frequency of 4.5MHz)
20	BOOSTPUMP_EN	SARADC Internal Pump Enable Default Value: 0
19 : 16	SPARE	Reserved bits Default Value: 0
15 : 14	PWR_CTRL_VREF	VREF buffer power mode control Default Value: 0 **0x0: NORMAL_PWR:** Normal power (default), bypass cap, maximum SAR clock frequency is 18MHz **0x1: HALF_PWR:** Deprecated **0x2: THIRD_PWR:** 2X power, no bypass cap, maximum SAR clock frequency is 1.8MHz **0x3: QUARTER_PWR:** Deprecated
13	SAR_HW_C-TRL_NEGVREF	Hardware control: 0: Only firmware control 1: Hardware control masked by firmware setting for VREF to NEG switch. Default Value: 0
11 : 9	NEG_SEL	SARADC negative input seletcion for single ended conversion Default Value: 0 **0x0: VSSA_KELVIN:** Negative input connected to internal Vssa **0x1: ART_VSSA:** Reserved **0x2: P1:** Negative input connected to P2[1] if SARMUX is being used **0x3: P3:** Negative input connected to P2[3] if SARMUX is being used **0x4: P5:** Negative input connected to P2[5] if SARMUX is being used **0x5: P7:** Negative input connected to P2[7] if SARMUX is being used

(continued)

		0x6: ACORE: Reserved **0x7: VREF:** Selected SARADC VREF
7	VREF_BYP_CAP_EN	VREF bypass cap enable when VREF buffer is ON Default Value: 0
6 : 4	VREF_SEL	SARADC VREF Selection Default Value: 0 **0x0: VREF0:** Reserved **0x1: VREF1:** Reserved **0x2: VREF2:** Reserved **0x3: VREF_AROUTE:** Reserved **0x4: VBGR:** Internal bandgap reference 1.2V (VREFbuffer ON) **0x5: VREF_EXT:** External reference from pin P1[7] **0x6: VDDA_DIV_2:** VDDA/2 (VREF buffer ON) **0x7: VDDA:** VDDA

24.1.2 SAR_SAMPLE_CTRL

Sample control register.

Address: 0x403A0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	AVG_SHIFT	AVG_CNT [6:4]			DIFFEREN-TIAL_-SIGNED	SIN-GLE_END-ED_SIGNE D	LEFT_ALIG N	SUB_RES-OLUTION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [23:20]				DSI_SYN-C_TRIG-GER	DSI_TRIG-GER_LEV-EL	DSI_TRIG-GER_EN	CONTINU-OUS

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	EO-S_DSI_OU T_EN	None [30:24]						

Bits	Name	Description
31	EOS_DSI_OUT_EN	Enable to output EOS_INTR to DSI. When enabled each time EOS_INTR is set by the hardware, a pulse is sent on the dsi_eos signal. Default Value: 0
19	DSI_SYNC_TRIGGER	0: bypass clock domain synchronisation of the DSI trigger signal. 1: synchronize the DSI trigger signal to the SAR clock domain, if needed an edge detect is done in the peripheral clock domain. Default Value: 1
18	DSI_TRIGGER_LEVEL	0: DSI trigger signal is a pulse input, a positive edge detected on the DSI trigger signal triggers a new scan. 1: DSI trigger signal is a level input, as long as the DSI trigger signal remains high the SAR will do continuous scans. Default Value: 0

(continued)

17	DSI_TRIGGER_EN	0: Firmware trigger only: disable hardware (DSI) trigger. 1: Enable hardware (DSI) trigger (e.g. from TCPWM, GPIO). Default Value: 0
16	CONTINUOUS	0: Wait for next FW_TRIGGER (one shot) or hardware (DSI) trigger (e.g. from TPWM for periodic triggering) before scanning enabled channels. 1: Continuously scan enabled channels, ignore triggers. Default Value: 0
7	AVG_SHIFT	Averaging shifting: after averaging, the result is shifted right to fit in the sample resolution. Default Value: 0
6 : 4	AVG_CNT	Averaging Count for channels that have over sampling enabled (AVG_EN). A channel will be sampled back to back (1<<(AVG_CNT+1)) = [2..256] times before the result is stored and the next enabled channel is sampled (1st order accumulate and dump filter). If shifting is not enabled (AVG_SHIFT=0) then the result is forced to shift right so that is fits in 16 bits, so right shift is done by max(0,AVG_CNT-3). Default Value: 0
3	DIFFERENTIAL_SIGNED	Output result from a differential conversion Default Value: 1 **0x0: UNSIGNED:** Unsigned (with zero extension if needed) **0x1: SIGNED:** Signed (with sign extension if needed) - default
2	SINGLE_ENDED_-SIGNED	Output result from a single ended conversion Default Value: 0 **0x0: UNSIGNED:** Unsigned (with zero extension if needed) - default **0x1: SIGNED:** Signed (with sign extension if needed)
1	LEFT_ALIGN	Left align data in data[15:0], default data is right aligned in data[11:0], with sign extension to 16 bits if the channel is differential. Default Value: 0
0	SUB_RESOLUTION	Conversion resolution for channels that have sub-resolution enabled (otherwise resolution is 12-bit) Default Value: 0 **0x0: 8B:** 8-bit **0x1: 10B:** 10-bit

24.1.3 SAR_SAMPLE_TIME01

Sample time specification ST0 and ST1

Address: 0x403A0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME0 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAMPLE_TIME1 [25:24]	

Bits	Name	Description
25 : 16	SAMPLE_TIME1	Sample time1 Default Value: 4
9 : 0	SAMPLE_TIME0	Sample time0 (aperture) in ADC clock cycles. Note that actual sample time is half a clock less than specified here. The minimum sample time is 194ns, which is 3.5 cycles (4 in this field) with an 18MHz clock. Minimum legal value in this register is 2. Default Value: 4

24.1.4 SAR_SAMPLE_TIME23

Sample time specification ST2 and ST3

Address: 0x403A0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAMPLE_TIME3 [25:24]	

Bits	Name	Description
25 : 16	SAMPLE_TIME3	Sample time3 Default Value: 4
9 : 0	SAMPLE_TIME2	Sample time2 Default Value: 4

24.1.5 SAR_RANGE_THRES

Global range detect threshold register.

Address: 0x403A0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [31:24]							

Bits	Name	Description
31 : 16	RANGE_HIGH	High threshold for range detect. Default Value: 0
15 : 0	RANGE_LOW	Low threshold for range detect. Default Value: 0

24.1.6 SAR_RANGE_COND

Global range detect mode register.

Address: 0x403A001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	RANGE_COND [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	RANGE_COND	Range condition select. Default Value: 0 **0x0: BELOW:** result < RANGE_LOW **0x1: INSIDE:** RANGE_LOW <= result < RANGE_HIGH **0x2: ABOVE:** RANGE_HIGH <= result **0x3: OUTSIDE:** result < RANGE_LOW || RANGE_HIGH <= result

24.1.7 SAR_CHAN_EN

Enable bits for the channels

Address: 0x403A0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CHAN_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHAN_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_EN	Channel enable. - 0: the corresponding channel is disabled. - 1: the corresponding channel is enabled, it will be included in the next scan. Default Value: 0

24.1.8 SAR_START_CTRL

Start control register (firmware trigger).

Address: 0x403A0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							FW_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FW_TRIGGER	When firmware writes a 1 here it will trigger the next scan of enabled channels, hardware clears this bit when the scan started with this trigger is completed. If scanning continuously the trigger is ignored and hardware clears this bit after the next scan is done. This bit is also cleared when the SAR is disabled. Default Value: 0

24.1.9 SAR_DFT_CTRL

DFT control register.

Address: 0x403A0030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						HIZ	DLY_INC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			RW			
HW Access	None	R			R			
Name	None	DFT_OUTC [22:20]			DFT_INC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW	RW	RW			
HW Access	R	None	R	R	R			
Name	AD-FT_OVER-RIDE	None	DCEN	EN_CSEL_DFT	SEL_CSEL_DFT [27:24]			

Bits	Name	Description
31	ADFT_OVERRIDE	During deepsleep/ hibernate mode keep SARMUX active, i.e. do not open all switches (disconnect), to be used for ADFT Default Value: 0
29	DCEN	Delay Control Enable for latch. - 0: doubles the latch enable time. - 1: normal latch enable time (default). Default Value: 0
28	EN_CSEL_DFT	Mux select signal for DAC control Default Value: 0
27 : 24	SEL_CSEL_DFT	Usage 1: DFT bits for DAC array Usage 2: For [0]=1 (when dcen=0): Delay timing for latch enable increased by 20% [1]=1: comparator preamp power level increased by 25% Default Value: 0
22 : 20	DFT_OUTC	DFT control for preamp outputs Default Value: 0

(continued)

19 : 16	DFT_INC	DFT control for preamp inputs Default Value: 0
1	HIZ	DFT control for getting higher input impedance, must be 1 (0 is deprecated) Default Value: 1
0	DLY_INC	DFT control: Control for delay circuits on sampling phase, =1 doubes the non-overlap delay Default Value: 0

24.1.10 SAR_CHAN_CONFIG0

Channel configuration register.

Address: 0x403A0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.11 SAR_CHAN_CONFIG1

Channel configuration register.

Address: 0x403A0084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.12 SAR_CHAN_CONFIG2

Channel configuration register.

Address: 0x403A0088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.13 SAR_CHAN_CONFIG3

Channel configuration register.

Address: 0x403A008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.14 SAR_CHAN_CONFIG4

Channel configuration register.

Address: 0x403A0090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.15 SAR_CHAN_CONFIG5

Channel configuration register.

Address: 0x403A0094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.16 SAR_CHAN_CONFIG6

Channel configuration register.

Address: 0x403A0098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.17 SAR_CHAN_CONFIG7

Channel configuration register.

Address: 0x403A009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.18 SAR_CHAN_CONFIG8

Channel configuration register.

Address: 0x403A00A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.19 SAR_CHAN_CONFIG9

Channel configuration register.

Address: 0x403A00A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.20 SAR_CHAN_CONFIG10

Channel configuration register.

Address: 0x403A00A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.21 SAR_CHAN_CONFIG11

Channel configuration register.

Address: 0x403A00AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.22 SAR_CHAN_CONFIG12

Channel configuration register.

Address: 0x403A00B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.23 SAR_CHAN_CONFIG13

Channel configuration register.

Address: 0x403A00B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.24 SAR_CHAN_CONFIG14

Channel configuration register.

Address: 0x403A00B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.25 SAR_CHAN_CONFIG15

Channel configuration register.

Address: 0x403A00BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	Reserved Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set, this bit is ignored and always a 12-bit resolution is used for this channel. Default Value: 0 **0x0: MAXRES:** The maximum resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.

(continued)

8	DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x5: AROUTE_VIRT2:** Reserved **0x6: AROUTE_VIRT1:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0) (On-Chip Temperature Sensor)
2 : 0	PIN_ADDR	When PORT_ADDR is set to SARMUX pins, PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then PIN_ADDR[0] is ignored and considered to be 0, that is, PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When PORT_ADDR is set to CTBm 0, PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When PORT_ADDR is set to SARMUX virtual port (VPORT0) to connect the on-chip temperature sensor, PIN_ADDR should be set to '0'. Default Value: 0

24.1.26 SAR_CHAN_WORK0

Channel working data register

Address: 0x403A0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.27 SAR_CHAN_WORK1

Channel working data register

Address: 0x403A0104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.28 SAR_CHAN_WORK2

Channel working data register

Address: 0x403A0108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.29 SAR_CHAN_WORK3

Channel working data register

Address: 0x403A010C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.30 SAR_CHAN_WORK4

Channel working data register

Address: 0x403A0110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.31 SAR_CHAN_WORK5

Channel working data register

Address: 0x403A0114

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.32 SAR_CHAN_WORK6

Channel working data register

Address: 0x403A0118

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.33 SAR_CHAN_WORK7

Channel working data register

Address: 0x403A011C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.34 SAR_CHAN_WORK8

Channel working data register

Address: 0x403A0120

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.35 SAR_CHAN_WORK9

Channel working data register

Address: 0x403A0124

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.36 SAR_CHAN_WORK10

Channel working data register

Address: 0x403A0128

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.37 SAR_CHAN_WORK11

Channel working data register

Address: 0x403A012C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.38 SAR_CHAN_WORK12

Channel working data register

Address: 0x403A0130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.39 SAR_CHAN_WORK13

Channel working data register

Address: 0x403A0134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.40 SAR_CHAN_WORK14

Channel working data register

Address: 0x403A0138

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.41 SAR_CHAN_WORK15

Channel working data register

Address: 0x403A013C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

24.1.42 SAR_CHAN_RESULT0

Channel result data register

Address: 0x403A0180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.43 SAR_CHAN_RESULT1

Channel result data register

Address: 0x403A0184

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.44 SAR_CHAN_RESULT2

Channel result data register

Address: 0x403A0188

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.45 SAR_CHAN_RESULT3

Channel result data register

Address: 0x403A018C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.46 SAR_CHAN_RESULT4

Channel result data register

Address: 0x403A0190

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.47 SAR_CHAN_RESULT5

Channel result data register

Address: 0x403A0194

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.48 SAR_CHAN_RESULT6

Channel result data register

Address: 0x403A0198

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.49 SAR_CHAN_RESULT7

Channel result data register

Address: 0x403A019C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.50 SAR_CHAN_RESULT8

Channel result data register

Address: 0x403A01A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.51 SAR_CHAN_RESULT9

Channel result data register

Address: 0x403A01A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.52 SAR_CHAN_RESULT10

Channel result data register

Address: 0x403A01A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.53 SAR_CHAN_RESULT11

Channel result data register

Address: 0x403A01AC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.54 SAR_CHAN_RESULT12

Channel result data register

Address: 0x403A01B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.55 SAR_CHAN_RESULT13

Channel result data register

Address: 0x403A01B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.56 SAR_CHAN_RESULT14

Channel result data register

Address: 0x403A01B8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.57 SAR_CHAN_RESULT15

Channel result data register

Address: 0x403A01BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

24.1.58 SAR_CHAN_WORK_VALID

Channel working data register valid bits

Address: 0x403A0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CHAN_WORK_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CHAN_WORK_VALID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_WORK_VALID	If set the corresponding WORK data is valid, i.e. was already sampled during the current scan. Default Value: 0

24.1.59 SAR_CHAN_RESULT_VALID

Channel result data register valid bits

Address: 0x403A0204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CHAN_RESULT_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CHAN_RESULT_VALID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_RESULT_VALID	If set the corresponding RESULT data is valid, i.e. was sampled during the last scan. Default Value: 0

24.1.60 SAR_STATUS

Current status of internal SAR registers (mostly for debug)

Address: 0x403A0208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			CUR_CHAN [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	BUSY	SW_VREF_NEG	None [29:24]					

Bits	Name	Description
31	BUSY	If high then the SAR is busy with a conversion. This bit is always high when CONTINUOUS is set. Firmware should wait for this bit to be low before putting the SAR in power down. Default Value: 0
30	SW_VREF_NEG	the current switch status, including DSI and sequencer controls, of the switch in the SARADC that shorts NEG with VREF input (see NEG_SEL). Default Value: 0
4 : 0	CUR_CHAN	current channel being sampled (channel 16 indicates the injection channel), only valid if BUSY. Default Value: 0

24.1.61 SAR_AVG_STAT

Current averaging status (for debug)

Address: 0x403A020C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				CUR_AVG_ACCU [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	CUR_AVG_CNT [31:24]							

Bits	Name	Description
31 : 24	CUR_AVG_CNT	the current value of the averaging counter. Note that the value shown is updated after the sampling time and therefore runs ahead of the accumulator update. Default Value: 0
19 : 0	CUR_AVG_ACCU	the current value of the averaging accumulator Default Value: 0

24.1.62 SAR_INTR

Interrupt request register.

Address: 0x403A0210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	INJ_COLLI-SION_INTR	IN-J_RANGE_I NTR	INJ_SATU-RATE_INTR	IN-J_EOC_IN-TR	DSI_COLLI-SION_INTR	FW_COLLI-SION_INTR	OVER-FLOW_IN-TR	EOS_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_INTR	Injection Collision Interrupt: hardware sets this interrupt when the injection trigger signal is asserted (INJ_START_EN==1 && INJ_TAILGATING==0) while the SAR is BUSY. Raising this interrupt is delayed to when the sampling of the injection channel has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the injection channel was sampled later than was intended. Write with '1' to clear bit. Default Value: 0
6	INJ_RANGE_INTR	Injection Range detect Interrupt: hardware sets this interrupt if the injection conversion result (after averaging) met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0
5	INJ_SATURATE_INTR	Injection Saturation Interrupt: hardware sets this interrupt if an injection conversion result (before averaging) is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0

(continued)

4	INJ_EOC_INTR	Injection End of Conversion Interrupt: hardware sets this interrupt after completing the conversion for the injection channel (irrespective of if tailgating was used). Write with '1' to clear bit. Default Value: 0
3	DSI_COLLISION_INTR	DSI Collision Interrupt: hardware sets this interrupt when the DSI trigger signal is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the DSI trigger has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. Default Value: 0
2	FW_COLLISION_INTR	Firmware Collision Interrupt: hardware sets this interrupt when FW_TRIGGER is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the FW_TRIGGER has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. Default Value: 0
1	OVERFLOW_INTR	Overflow Interrupt: hardware sets this interrupt when it sets a new EOS_INTR while that bit was not yet cleared by the firmware. Write with '1' to clear bit. Default Value: 0
0	EOS_INTR	End Of Scan Interrupt: hardware sets this interrupt after completing a scan of all the enabled channels. Write with '1' to clear bit. Default Value: 0

24.1.63 SAR_INTR_SET

Interrupt set request register

Address: 0x403A0214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	INJ_COLLI-SION_SET	IN-J_RANGE_SET	INJ_SATU-RATE_SET	IN-J_EOC_SET	DSI_COLLI-SION_SET	FW_COLLI-SION_SET	OVER-FLOW_SET	EOS_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	INJ_RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	INJ_SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	INJ_EOC_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	DSI_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	FW_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	OVERFLOW_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

0	EOS_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

24.1.64 SAR_INTR_MASK

Interrupt mask register.

Address: 0x403A0218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INJ_COLLI-SION_MASK	IN-J_RANGE_MASK	INJ_SATU-RATE_MASK	IN-J_EOC_MASK	DSI_COLLI-SION_MASK	FW_COLLI-SION_MASK	OVER-FLOW_MASK	EOS_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	INJ_RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	INJ_SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	INJ_EOC_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	DSI_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	FW_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	OVERFLOW_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

0	EOS_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

24.1.65 SAR_INTR_MASKED

Interrupt masked request register

Address: 0x403A021C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INJ_COLLI-SION_MASKED	IN-J_RANGE_MASKED	INJ_SATU-RATE_MASKED	IN-J_EOC_MASKED	DSI_COLLI-SION_MASKED	FW_COLLI-SION_MASKED	OVER-FLOW_MASKED	EO-S_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLI-SION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
6	INJ_RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
5	INJ_SATU-RATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
4	INJ_EOC_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
3	DSI_COLLI-SION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
2	FW_COLLI-SION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
1	OVERFLOW_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

0	EOS_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

24.1.66 SAR_SATURATE_INTR

Saturate interrupt request register.

Address: 0x403A0220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	SATURATE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	SATURATE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_INTR	Saturate Interrupt: hardware sets this interrupt for each channel if a conversion result (before averaging) of that channel is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0

24.1.67 SAR_SATURATE_INTR_SET

Saturate interrupt set request register

Address: 0x403A0224

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	SATURATE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	SATURATE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

24.1.68 SAR_SATURATE_INTR_MASK

Saturate interrupt mask register.

Address: 0x403A0228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SATURATE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SATURATE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

24.1.69 SAR_SATURATE_INTR_MASKED

Saturate interrupt masked request register

Address: 0x403A022C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SATURATE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SATURATE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

24.1.70 SAR_RANGE_INTR

Range detect interrupt request register.

Address: 0x403A0230

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_INTR	Range detect Interrupt: hardware sets this interrupt for each channel if the conversion result (after averaging) of that channel met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0

24.1.71 SAR_RANGE_INTR_SET

Range detect interrupt set request register

Address: 0x403A0234

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

24.1.72 SAR_RANGE_INTR_MASK

Range detect interrupt mask register.

Address: 0x403A0238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

24.1.73 SAR_RANGE_INTR_MASKED

Range interrupt masked request register

Address: 0x403A023C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RANGE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RANGE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

24.1.74 SAR_INTR_CAUSE

Interrupt cause register

Address: 0x403A0240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INJ_COLLI-SION_MASKED_MIR	IN-J_RANGE_MASKED_MIR	INJ_SATU-RATE_MASKED_MIR	IN-J_EOC_MASKED_MIR	DSI_COLLI-SION_MASKED_MIR	FW_COLLI-SION_MASKED_MIR	OVER-FLOW_MASKED_MIR	EO-S_MASKED_MIR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	RANGE_MASKED_RED	SATU-RATE_MASKED_RED	None [29:24]					

Bits	Name	Description
31	RANGE_MASKED_RED	Reduction OR of all SAR_RANGE_INTR_MASKED bits Default Value: 0
30	SATU-RATE_MASKED_RED	Reduction OR of all SAR_SATURATION_INTR_MASKED bits Default Value: 0
7	INJ_COLLI-SION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
6	IN-J_RANGE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
5	INJ_SATU-RATE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
4	INJ_EOC_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0

(continued)

3	DSI_COLLI-SION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
2	FW_COLLI-SION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
1	OVER-FLOW_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
0	EOS_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0

24.1.75 SAR_INJ_CHAN_CONFIG

Injection channel configuration register.

Address: 0x403A0280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	INJ_PORT_ADDR [6:4]			None	INJ_PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		INJ_SAMPLE_TIME_SEL [13:12]		None	IN-J_AVG_EN	INJ_RESO-LUTION	INJ_DIF-FEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW	None					
HW Access	RW1C	R	None					
Name	IN-J_START_EN	INJ_TAIL-GATING	None [29:24]					

Bits	Name	Description
31	INJ_START_EN	Set by firmware to enable the injection channel. If INJ_TAILGATING is not set this bit also functions as trigger for this channel. Cleared by hardware after this channel has been sampled (i.e. this channel is always one shot even if CONTINUOUS is set). Also cleared if the SAR is disabled. Default Value: 0
30	INJ_TAILGATING	Injection channel tailgating. 0: No tailgating for this channel, SAR is immediately triggered when the INJ_START_EN bit is set. 1: Injection channel tailgating. The addressed pin is sampled after the next trigger and after all enabled channels have been scanned. Default Value: 0
13 : 12	INJ_SAMPLE_TIME_SEL	Injection sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	INJ_AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0

(continued)

9	INJ_RESOLUTION	Resolution for this channel Default Value: 0 **0x0: 12B:** 12-bit resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	INJ_DIFFERENTIAL_EN	Differential enable for this channel. 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (INJ_PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	INJ_PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX Pins (Port 2) **0x1: CTB0:** CTBm 0 **0x2: CTB1:** Reserved **0x3: CTB2:** Reserved **0x4: CTB3:** Reserved **0x6: AROUTE_VIRT:** Reserved **0x7: SARMUX_VIRT:** SARMUX virtual port
2 : 0	INJ_PIN_ADDR	When INJ_PORT_ADDR is set to SARMUX pins, INJ_PIN_ADDR selects the pin (0 to 7). If differential channel is enabled, then INJ_PIN_ADDR[0] is ignored and considered to be 0, that is, INJ_PIN_ADDR points to the even pin of a pin pair. For differential channel, the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. When INJ_PORT_ADDR is set to CTBm 0, INJ_PIN_ADDR selects the opamp output. '2' means Opamp 0 output and '3' means Opamp 1 output. When INJ_PORT_ADDR is set to SARMUX virtual port to connect the on-chip temperature sensor, INJ_PIN_ADDR should be set to '0'. Default Value: 0

24.1.76 SAR_INJ_RESULT

Injection channel result register

Address: 0x403A0290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	INJ_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	INJ_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	None			
HW Access	W	W	W	W	None			
Name	INJ_EOC_INTR_MIR	INJ_RANGE_INTR_MIR	INJ_SATURATE_INTR_MIR	INJ_COLLISION_INTR_MIR	None [27:24]			

Bits	Name	Description
31	INJ_EOC_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
30	INJ_RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
29	INJ_SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
28	INJ_COLLISION_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
15 : 0	INJ_RESULT	SAR conversion result of the channel. Default Value: Undefined

24.1.77 SAR_MUX_SWITCH0

SARMUX Firmware switch controls

Address: 0x403A0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_F-W_P7_VPLUS	MUX_F-W_P6_VPLUS	MUX_F-W_P5_VPLUS	MUX_F-W_P4_VPLUS	MUX_F-W_P3_VPLUS	MUX_F-W_P2_VPLUS	MUX_F-W_P1_VPLUS	MUX_F-W_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_F-W_P7_VMINUS	MUX_F-W_P6_VMINUS	MUX_F-W_P5_VMINUS	MUX_F-W_P4_VMINUS	MUX_F-W_P3_VMINUS	MUX_F-W_P2_VMINUS	MUX_F-W_P1_VMINUS	MUX_F-W_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_F-W_SARBUS1_VPLUS	MUX_F-W_SARBUS0_VPLUS	MUX_F-W_AMUXBUSB_VMINUS	MUX_F-W_AMUXBUSA_VMINUS	MUX_F-W_AMUXBUSB_VPLUS	MUX_F-W_AMUXBUSA_VPLUS	MUX_FW_-TEMP_VPLUS	MUX_F-W_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [31:30]		MUX_F-W_P7_COREIO3	MUX_F-W_P6_COREIO2	MUX_F-W_P5_COREIO1	MUX_F-W_P4_COREIO0	MUX_F-W_SARBUS1_VMINUS	MUX_F-W_SARBUS0_VMINUS

Bits	Name	Description
29	MUX_FW_P7_COREIO3	Firmware control: 0: Open 1: Close switch between P2[7] and coreio3 signal. Write with '1' to set bit. Default Value: 0
28	MUX_FW_P6_COREIO2	Firmware control: 0: Open 1: Close switch between P2[6] and coreio2 signal. Write with '1' to set bit. Default Value: 0

(continued)

27	MUX_FW_P5_COREIO1	Firmware control: 0: Open 1: Close switch between P2[5] and coreio1 signal. Write with '1' to set bit. Default Value: 0
26	MUX_FW_P4_COREIO0	Firmware control: 0: Open 1: Close switch between P2[4] and coreio0 signal. Write with '1' to set bit. Default Value: 0
25	MUX_FW_SAR-BUS1_VMINUS	Firmware control: 0: Open 1: Close switch between sarbus1 and vminus signal. Write with '1' to set bit. Default Value: 0
24	MUX_FW_SAR-BUS0_VMINUS	Firmware control: 0: Open 1: Close switch between sarbus0 and vminus signal. Write with '1' to set bit. Default Value: 0
23	MUX_FW_SAR-BUS1_VPLUS	Firmware control: 0: Open 1: Close switch between sarbus1 and vplus signal. Write with '1' to set bit. Default Value: 0
22	MUX_FW_SAR-BUS0_VPLUS	Firmware control: 0: Open 1: Close switch between sarbus0 and vplus signal. Write with '1' to set bit. Default Value: 0
21	MUX_FW_AMUXBUS-B_VMINUS	Firmware control: 0: Open 1: Close switch between amuxbusb and vminus signal. Write with '1' to set bit. Default Value: 0
20	MUX_FW_AMUX-BUSA_VMINUS	Firmware control: 0: Open 1: Close switch between amuxbusa and vminus signal. Write with '1' to set bit. Default Value: 0
19	MUX_FW_AMUXBUS-B_VPLUS	Firmware control: 0: Open 1: Close switch between amuxbusb and vplus signal. Write with '1' to set bit. Default Value: 0
18	MUX_FW_AMUX-BUSA_VPLUS	Firmware control: 0: Open 1: Close switch between amuxbusa and vplus signal. Write with '1' to set bit. Default Value: 0
17	MUX_FW_TEMP_VPLUS	Firmware control: 0: Open 1: Close switch between temperature sensor and vplus signal, also powers on the temperature sensor. Write with '1' to set bit. Default Value: 0
16	MUX_FW_VSSA_VMI-NUS	Firmware control: 0: Open 1: Close switch between vssa_kelvin and vminus signal. Write with '1' to set bit. Default Value: 0

(continued)

15	MUX_FW_P7_VMINUS	Firmware control: 0: Open 1: Close switch between pin P2[7] and vminus signal. Write with '1' to set bit. Default Value: 0
14	MUX_FW_P6_VMINUS	Firmware control: 0: Open 1: Close switch between pin P2[6] and vminus signal. Write with '1' to set bit. Default Value: 0
13	MUX_FW_P5_VMINUS	Firmware control: 0: Open 1: Close switch between pin P2[5] and vminus signal. Write with '1' to set bit. Default Value: 0
12	MUX_FW_P4_VMINUS	Firmware control: 0: Open 1: Close switch between pin P2[4] and vminus signal. Write with '1' to set bit. Default Value: 0
11	MUX_FW_P3_VMINUS	Firmware control: 0: Open 1: Close switch between pin P2[3] and vminus signal. Write with '1' to set bit. Default Value: 0
10	MUX_FW_P2_VMINUS	Firmware control: 0: Open 1: Close switch between pin P2[2] and vminus signal. Write with '1' to set bit. Default Value: 0
9	MUX_FW_P1_VMINUS	Firmware control: 0: Open 1: Close switch between pin P2[1] and vminus signal. Write with '1' to set bit. Default Value: 0
8	MUX_FW_P0_VMINUS	Firmware control: 0: Open 1: Close switch between pin P2[0] and vminus signal. Write with '1' to set bit. Default Value: 0
7	MUX_FW_P7_VPLUS	Firmware control: 0: Open 1: Close switch between pin P2[7] and vplus signal. Write with '1' to set bit. Default Value: 0
6	MUX_FW_P6_VPLUS	Firmware control: 0: Open 1: Close switch between pin P2[6] and vplus signal. Write with '1' to set bit. Default Value: 0
5	MUX_FW_P5_VPLUS	Firmware control: 0: Open 1: Close switch between pin P2[5] and vplus signal. Write with '1' to set bit. Default Value: 0
4	MUX_FW_P4_VPLUS	Firmware control: 0: Open 1: Close switch between pin P2[4] and vplus signal. Write with '1' to set bit. Default Value: 0

(continued)

3	MUX_FW_P3_VPLUS	Firmware control: 0: Open 1: Close switch between pin P2[3] and vplus signal. Write with '1' to set bit. Default Value: 0
2	MUX_FW_P2_VPLUS	Firmware control: 0: Open 1: Close switch between pin P2[2] and vplus signal. Write with '1' to set bit. Default Value: 0
1	MUX_FW_P1_VPLUS	Firmware control: 0: Open 1: Close switch between pin P2[1] and vplus signal. Write with '1' to set bit. Default Value: 0
0	MUX_FW_P0_VPLUS	Firmware control: 0: Open 1: Close switch between pin P2[0] and vplus signal. Write with '1' to set bit. Default Value: 0

24.1.78 SAR_MUX_SWITCH_CLEAR0

SARMUX Firmware switch control clear

Address: 0x403A0304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_F-W_P7_VPLUS	MUX_F-W_P6_VPLUS	MUX_F-W_P5_VPLUS	MUX_F-W_P4_VPLUS	MUX_F-W_P3_VPLUS	MUX_F-W_P2_VPLUS	MUX_F-W_P1_VPLUS	MUX_F-W_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_F-W_P7_VMINUS	MUX_F-W_P6_VMINUS	MUX_F-W_P5_VMINUS	MUX_F-W_P4_VMINUS	MUX_F-W_P3_VMINUS	MUX_F-W_P2_VMINUS	MUX_F-W_P1_VMINUS	MUX_F-W_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_F-W_SARBUS1_VPLUS	MUX_F-W_SARBUS0_VPLUS	MUX_F-W_AMUXBUSB_VMINUS	MUX_F-W_AMUXBUSA_VMINUS	MUX_F-W_AMUXBUSB_VPLUS	MUX_F-W_AMUXBUSA_VPLUS	MUX_FW_-TEMP_VPLUS	MUX_F-W_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		A	A	A	A	A	A
Name	None [31:30]		MUX_F-W_P7_COREIO3	MUX_F-W_P6_COREIO2	MUX_F-W_P5_COREIO1	MUX_F-W_P4_COREIO0	MUX_F-W_SARBUS1_VMINUS	MUX_F-W_SARBUS0_VMINUS

Bits	Name	Description
29	MUX_FW_P7_COREIO3	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
28	MUX_FW_P6_COREIO2	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
27	MUX_FW_P5_COREIO1	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
26	MUX_FW_P4_COREIO0	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

(continued)

25	MUX_FW_SAR-BUS1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
24	MUX_FW_SAR-BUS0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
23	MUX_FW_SAR-BUS1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
22	MUX_FW_SAR-BUS0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
21	MUX_FW_AMUXBUS-B_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
20	MUX_FW_AMUX-BUSA_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
19	MUX_FW_AMUXBUS-B_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
18	MUX_FW_AMUX-BUSA_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
17	MUX_FW_TEMP_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
16	MUX_FW_VSSA_VMI-NUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
15	MUX_FW_P7_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
14	MUX_FW_P6_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
13	MUX_FW_P5_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
12	MUX_FW_P4_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
11	MUX_FW_P3_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
10	MUX_FW_P2_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
9	MUX_FW_P1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
8	MUX_FW_P0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
7	MUX_FW_P7_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
6	MUX_FW_P6_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
5	MUX_FW_P5_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
4	MUX_FW_P4_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

(continued)

3	MUX_FW_P3_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
2	MUX_FW_P2_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
1	MUX_FW_P1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
0	MUX_FW_P0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

24.1.79 SAR_MUX_SWITCH1

SARMUX Firmware switch controls

Address: 0x403A0308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				RW1C	RW1C	RW1C	RW1C
Name	None [7:4]				MUX_FW_ADFT1_SARBUS1	MUX_FW_ADFT0_SARBUS0	MUX_FW_P5_DFT_INM	MUX_FW_P4_DFT_INP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	MUX_FW_ADFT1_SARBUS1	Firmware control: 0=open, 1=close switch between adft1 signal and sarbus1 signal. Write with '1' to set bit. Default Value: 0
2	MUX_FW_ADFT0_SARBUS0	Firmware control: 0=open, 1=close switch between adft0 signal and sarbus0 signal. Write with '1' to set bit. Default Value: 0
1	MUX_FW_P5_DFT_INM	Firmware control: 0=open, 1=close switch between P5 pin and dft_inm signal. Write with '1' to set bit. Default Value: 0
0	MUX_FW_P4_DFT_INP	Firmware control: 0=open, 1=close switch between P4 pin and dft_inp signal. Write with '1' to set bit. Default Value: 0

24.1.80 SAR_MUX_SWITCH_CLEAR1

SARMUX Firmware switch control clear

Address: 0x403A030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				MUX_FW_ADFT1_SARBUS1	MUX_FW_ADFT0_SARBUS0	MUX_FW_P5_DFT_INM	MUX_FW_P4_DFT_INP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	MUX_FW_ADFT1_SARBUS1	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0
2	MUX_FW_ADFT0_SARBUS0	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0
1	MUX_FW_P5_DFT_INM	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0
0	MUX_FW_P4_DFT_INP	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0

24.1.81 SAR_MUX_SWITCH_HW_CTRL

SARMUX switch hardware control

Address: 0x403A0340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	MUX-_HW_C-TRL_P7	MUX-_HW_C-TRL_P6	MUX-_HW_C-TRL_P5	MUX-_HW_C-TRL_P4	MUX-_HW_C-TRL_P3	MUX-_HW_C-TRL_P2	MUX-_HW_C-TRL_P1	MUX-_HW_C-TRL_P0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None		RW	RW	RW	RW
HW Access	R	R	None		R	R	R	R
Name	MUX-_HW_C-TRL_SARBUS1	MUX-_HW_C-TRL_SARBUS0	None [21:20]		MUX-_HW_C-TRL_AMUXBUSB	MUX-_HW_C-TRL_AMUXBUSA	MUX-_HW_C-TRL_TEMP	MUX-_HW_C-TRL_VSSA

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	MUX_HW_CTRL_SAR-BUS1	Hardware control: 0: Only firmware control 1: Hardware control masked by firmware setting for sarbus1 switches. Default Value: 0
22	MUX_HW_CTRL_SAR-BUS0	Hardware control: 0: Only firmware control 1: Hardware control masked by firmware setting for sarbus0 switches. Default Value: 0
19	MUX_HW_CTRL_AMUX-BUSB	Hardware control: 0: Only firmware control 1: Hardware control masked by firmware setting for amuxbusb switches. Default Value: 0

(continued)

18	MUX_HW_CTRL_AMUX-BUSA	Hardware control: 0: Only firmware control 1: Hardware control masked by firmware setting for amuxbusa switches. Default Value: 0
17	MUX_HW_CTRL_TEMP	Hardware control: 0: Only firmware control 1: Hardware control masked by firmware setting for temp switch. Default Value: 0
16	MUX_HW_CTRL_VSSA	Hardware control: 0: Only firmware control 1: Hardware control masked by firmware setting for vssa switch. Default Value: 0
7	MUX_HW_CTRL_P7	Hardware control: 0: Only firmware control, 1: Hardware control masked by firmware setting for pin P2[7] switches. Default Value: 0
6	MUX_HW_CTRL_P6	Hardware control: 0: Only firmware control, 1: Hardware control masked by firmware setting for pin P2[6] switches. Default Value: 0
5	MUX_HW_CTRL_P5	Hardware control: 0: Only firmware control 1: Hardware control masked by firmware setting for pin P2[5] switches. Default Value: 0
4	MUX_HW_CTRL_P4	Hardware control: 0: Only firmware control 1: Hardware control masked by firmware setting for pin P2[4] switches. Default Value: 0
3	MUX_HW_CTRL_P3	Hardware control: 0: Only firmware control 1: Hardware control masked by firmware setting for pin P2[3] switches. Default Value: 0
2	MUX_HW_CTRL_P2	Hardware control: 0: Only firmware control 1: Hardware control masked by firmware setting for pin P2[2] switches. Default Value: 0
1	MUX_HW_CTRL_P1	Hardware control: 0: Only firmware control 1: Hardware control masked by firmware setting for pin P2[1] switches. Default Value: 0
0	MUX_HW_CTRL_P0	Hardware control: 0: Only firmware control 1: Hardware control masked by firmware setting for pin P2[0] switches. Default Value: 0

24.1.82 SAR_MUX_SWITCH_STATUS

SARMUX switch status

Address: 0x403A0348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_F-W_P7_VPLUS	MUX_F-W_P6_VPLUS	MUX_F-W_P5_VPLUS	MUX_F-W_P4_VPLUS	MUX_F-W_P3_VPLUS	MUX_F-W_P2_VPLUS	MUX_F-W_P1_VPLUS	MUX_F-W_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_F-W_P7_VMINUS	MUX_F-W_P6_VMINUS	MUX_F-W_P5_VMINUS	MUX_F-W_P4_VMINUS	MUX_F-W_P3_VMINUS	MUX_F-W_P2_VMINUS	MUX_F-W_P1_VMINUS	MUX_F-W_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_F-W_SARBUS1_VPLUS	MUX_F-W_SARBUS0_VPLUS	MUX_F-W_AMUXBUSB_VMINUS	MUX_F-W_AMUXBUSA_VMINUS	MUX_F-W_AMUXBUSB_VPLUS	MUX_F-W_AMUXBUSA_VPLUS	MUX_FW_-TEMP_VPLUS	MUX_F-W_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						W	W
Name	None [31:26]						MUX_F-W_SARBUS1_VMINUS	MUX_F-W_SARBUS0_VMINUS

Bits	Name	Description
25	MUX_FW_SARBUS1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
24	MUX_FW_SARBUS0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
23	MUX_FW_SARBUS1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
22	MUX_FW_SARBUS0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0

(continued)

21	MUX_FW_AMUXBUS-B_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
20	MUX_FW_AMUX-BUSA_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
19	MUX_FW_AMUXBUS-B_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
18	MUX_FW_AMUX-BUSA_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
17	MUX_FW_TEMP_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
16	MUX_FW_VSSA_VMI-NUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
15	MUX_FW_P7_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
14	MUX_FW_P6_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
13	MUX_FW_P5_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
12	MUX_FW_P4_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
11	MUX_FW_P3_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
10	MUX_FW_P2_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
9	MUX_FW_P1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
8	MUX_FW_P0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
7	MUX_FW_P7_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
6	MUX_FW_P6_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
5	MUX_FW_P5_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
4	MUX_FW_P4_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
3	MUX_FW_P3_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
2	MUX_FW_P2_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
1	MUX_FW_P1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
0	MUX_FW_P0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0

24.1.83 SAR_PUMP_CTRL

Switch pump control

Address: 0x403A0380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CLOCK_-SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	0=disabled: pump output is VDDA_PUMP, 1=enabled: pump output is boosted. Default Value: 0
0	CLOCK_SEL	Clock select: 0=external clock, 1=internal clock (deprecated). Default Value: 0

24.1.84 SAR_ANA_TRIM

Analog trim register.

Address: 0x403A0F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW		
HW Access	None				R	R		
Name	None [7:4]				TRIMUNIT	CAP_TRIM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	TRIMUNIT	Attenuation cap trimming Default Value: 0
2 : 0	CAP_TRIM	Attenuation cap trimming Default Value: 0

24.1.85 SAR_WOUNDING

SAR wounding register

Address: 0x403A0F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	
HW Access	None						R	
Name	None [7:2]						WOUND_RESOLUTION [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	WOUND_RESOLUTION	Maximum SAR resolution allowed Default Value: 0 **0x0: 12BIT:** unwounded: up to full 12-bit SAR resolution allowed **0x1: 10BIT:** wounded: max resolution upto 10-bit SAR resolution allowed **0x2: 8BIT:** wounded: only 8-bit SAR resolution allowed **0x3: 8BIT_TOO:** wounded: only 8-bit SAR resolution allowed

25 Serial Communication Block Registers

This section discusses the Serial Communication Block (SCB) registers. It lists all the registers in mapping tables, in address order.

25.1 Register Details

Register Name	Address
SCB0_CTRL	0x40240000
SCB0_STATUS	0x40240004
SCB0_SPI_CTRL	0x40240020
SCB0_SPI_STATUS	0x40240024
SCB0_UART_CTRL	0x40240040
SCB0_UART_TX_CTRL	0x40240044
SCB0_UART_RX_CTRL	0x40240048
SCB0_UART_RX_STATUS	0x4024004C
SCB0_UART_FLOW_CTRL	0x40240050
SCB0_I2C_CTRL	0x40240060
SCB0_I2C_STATUS	0x40240064
SCB0_I2C_M_CMD	0x40240068
SCB0_I2C_S_CMD	0x4024006C
SCB0_I2C_CFG	0x40240070
SCB0_TX_CTRL	0x40240200
SCB0_TX_FIFO_CTRL	0x40240204
SCB0_TX_FIFO_STATUS	0x40240208
SCB0_TX_FIFO_WR	0x40240240
SCB0_RX_CTRL	0x40240300
SCB0_RX_FIFO_CTRL	0x40240304
SCB0_RX_FIFO_STATUS	0x40240308
SCB0_RX_MATCH	0x40240310
SCB0_RX_FIFO_RD	0x40240340
SCB0_RX_FIFO_RD_SILENT	0x40240344
SCB0_EZ_DATA0	0x40240400
SCB0_EZ_DATA1	0x40240404
SCB0_EZ_DATA2	0x40240408

Register Name	Address
SCB0_EZ_DATA3	0x4024040C
SCB0_EZ_DATA4	0x40240410
SCB0_EZ_DATA5	0x40240414
SCB0_EZ_DATA6	0x40240418
SCB0_EZ_DATA7	0x4024041C
SCB0_EZ_DATA8	0x40240420
SCB0_EZ_DATA9	0x40240424
SCB0_EZ_DATA10	0x40240428
SCB0_EZ_DATA11	0x4024042C
SCB0_EZ_DATA12	0x40240430
SCB0_EZ_DATA13	0x40240434
SCB0_EZ_DATA14	0x40240438
SCB0_EZ_DATA15	0x4024043C
SCB0_EZ_DATA16	0x40240440
SCB0_EZ_DATA17	0x40240444
SCB0_EZ_DATA18	0x40240448
SCB0_EZ_DATA19	0x4024044C
SCB0_EZ_DATA20	0x40240450
SCB0_EZ_DATA21	0x40240454
SCB0_EZ_DATA22	0x40240458
SCB0_EZ_DATA23	0x4024045C
SCB0_EZ_DATA24	0x40240460
SCB0_EZ_DATA25	0x40240464
SCB0_EZ_DATA26	0x40240468
SCB0_EZ_DATA27	0x4024046C
SCB0_EZ_DATA28	0x40240470
SCB0_EZ_DATA29	0x40240474
SCB0_EZ_DATA30	0x40240478
SCB0_EZ_DATA31	0x4024047C
SCB0_INTR_CAUSE	0x40240E00
SCB0_INTR_I2C_EC	0x40240E80
SCB0_INTR_I2C_EC_MASK	0x40240E88
SCB0_INTR_I2C_EC_MASKED	0x40240E8C
SCB0_INTR_SPI_EC	0x40240EC0
SCB0_INTR_SPI_EC_MASK	0x40240EC8
SCB0_INTR_SPI_EC_MASKED	0x40240ECC
SCB0_INTR_M	0x40240F00
SCB0_INTR_M_SET	0x40240F04
SCB0_INTR_M_MASK	0x40240F08
SCB0_INTR_M_MASKED	0x40240F0C
SCB0_INTR_S	0x40240F40
SCB0_INTR_S_SET	0x40240F44

Register Name	Address
SCB0_INTR_S_MASK	0x40240F48
SCB0_INTR_S_MASKED	0x40240F4C
SCB0_INTR_TX	0x40240F80
SCB0_INTR_TX_SET	0x40240F84
SCB0_INTR_TX_MASK	0x40240F88
SCB0_INTR_TX_MASKED	0x40240F8C
SCB0_INTR_RX	0x40240FC0
SCB0_INTR_RX_SET	0x40240FC4
SCB0_INTR_RX_MASK	0x40240FC8
SCB0_INTR_RX_MASKED	0x40240FCC
SCB1_CTRL	0x40250000
SCB1_STATUS	0x40250004
SCB1_SPI_CTRL	0x40250020
SCB1_SPI_STATUS	0x40250024
SCB1_UART_CTRL	0x40250040
SCB1_UART_TX_CTRL	0x40250044
SCB1_UART_RX_CTRL	0x40250048
SCB1_UART_RX_STATUS	0x4025004C
SCB1_UART_FLOW_CTRL	0x40250050
SCB1_I2C_CTRL	0x40250060
SCB1_I2C_STATUS	0x40250064
SCB1_I2C_M_CMD	0x40250068
SCB1_I2C_S_CMD	0x4025006C
SCB1_I2C_CFG	0x40250070
SCB1_TX_CTRL	0x40250200
SCB1_TX_FIFO_CTRL	0x40250204
SCB1_TX_FIFO_STATUS	0x40250208
SCB1_TX_FIFO_WR	0x40250240
SCB1_RX_CTRL	0x40250300
SCB1_RX_FIFO_CTRL	0x40250304
SCB1_RX_FIFO_STATUS	0x40250308
SCB1_RX_MATCH	0x40250310
SCB1_RX_FIFO_RD	0x40250340
SCB1_RX_FIFO_RD_SILENT	0x40250344
SCB1_EZ_DATA0	0x40250400
SCB1_EZ_DATA1	0x40250404
SCB1_EZ_DATA2	0x40250408
SCB1_EZ_DATA3	0x4025040C
SCB1_EZ_DATA4	0x40250410
SCB1_EZ_DATA5	0x40250414
SCB1_EZ_DATA6	0x40250418
SCB1_EZ_DATA7	0x4025041C

Register Name	Address
SCB1_EZ_DATA8	0x40250420
SCB1_EZ_DATA9	0x40250424
SCB1_EZ_DATA10	0x40250428
SCB1_EZ_DATA11	0x4025042C
SCB1_EZ_DATA12	0x40250430
SCB1_EZ_DATA13	0x40250434
SCB1_EZ_DATA14	0x40250438
SCB1_EZ_DATA15	0x4025043C
SCB1_EZ_DATA16	0x40250440
SCB1_EZ_DATA17	0x40250444
SCB1_EZ_DATA18	0x40250448
SCB1_EZ_DATA19	0x4025044C
SCB1_EZ_DATA20	0x40250450
SCB1_EZ_DATA21	0x40250454
SCB1_EZ_DATA22	0x40250458
SCB1_EZ_DATA23	0x4025045C
SCB1_EZ_DATA24	0x40250460
SCB1_EZ_DATA25	0x40250464
SCB1_EZ_DATA26	0x40250468
SCB1_EZ_DATA27	0x4025046C
SCB1_EZ_DATA28	0x40250470
SCB1_EZ_DATA29	0x40250474
SCB1_EZ_DATA30	0x40250478
SCB1_EZ_DATA31	0x4025047C
SCB1_INTR_CAUSE	0x40250E00
SCB1_INTR_I2C_EC	0x40250E80
SCB1_INTR_I2C_EC_MASK	0x40250E88
SCB1_INTR_I2C_EC_MASKED	0x40250E8C
SCB1_INTR_SPI_EC	0x40250EC0
SCB1_INTR_SPI_EC_MASK	0x40250EC8
SCB1_INTR_SPI_EC_MASKED	0x40250ECC
SCB1_INTR_M	0x40250F00
SCB1_INTR_M_SET	0x40250F04
SCB1_INTR_M_MASK	0x40250F08
SCB1_INTR_M_MASKED	0x40250F0C
SCB1_INTR_S	0x40250F40
SCB1_INTR_S_SET	0x40250F44
SCB1_INTR_S_MASK	0x40250F48
SCB1_INTR_S_MASKED	0x40250F4C
SCB1_INTR_TX	0x40250F80
SCB1_INTR_TX_SET	0x40250F84
SCB1_INTR_TX_MASK	0x40250F88

Register Name	Address
SCB1_INTR_TX_MASKED	0x40250F8C
SCB1_INTR_RX	0x40250FC0
SCB1_INTR_RX_SET	0x40250FC4
SCB1_INTR_RX_MASK	0x40250FC8
SCB1_INTR_RX_MASKED	0x40250FCC
SCB2_CTRL	0x40260000
SCB2_STATUS	0x40260004
SCB2_SPI_CTRL	0x40260020
SCB2_SPI_STATUS	0x40260024
SCB2_UART_CTRL	0x40260040
SCB2_UART_TX_CTRL	0x40260044
SCB2_UART_RX_CTRL	0x40260048
SCB2_UART_RX_STATUS	0x4026004C
SCB2_UART_FLOW_CTRL	0x40260050
SCB2_I2C_CTRL	0x40260060
SCB2_I2C_STATUS	0x40260064
SCB2_I2C_M_CMD	0x40260068
SCB2_I2C_S_CMD	0x4026006C
SCB2_I2C_CFG	0x40260070
SCB2_TX_CTRL	0x40260200
SCB2_TX_FIFO_CTRL	0x40260204
SCB2_TX_FIFO_STATUS	0x40260208
SCB2_TX_FIFO_WR	0x40260240
SCB2_RX_CTRL	0x40260300
SCB2_RX_FIFO_CTRL	0x40260304
SCB2_RX_FIFO_STATUS	0x40260308
SCB2_RX_MATCH	0x40260310
SCB2_RX_FIFO_RD	0x40260340
SCB2_RX_FIFO_RD_SILENT	0x40260344
SCB2_EZ_DATA0	0x40260400
SCB2_EZ_DATA1	0x40260404
SCB2_EZ_DATA2	0x40260408
SCB2_EZ_DATA3	0x4026040C
SCB2_EZ_DATA4	0x40260410
SCB2_EZ_DATA5	0x40260414
SCB2_EZ_DATA6	0x40260418
SCB2_EZ_DATA7	0x4026041C
SCB2_EZ_DATA8	0x40260420
SCB2_EZ_DATA9	0x40260424
SCB2_EZ_DATA10	0x40260428
SCB2_EZ_DATA11	0x4026042C
SCB2_EZ_DATA12	0x40260430

Register Name	Address
SCB2_EZ_DATA13	0x40260434
SCB2_EZ_DATA14	0x40260438
SCB2_EZ_DATA15	0x4026043C
SCB2_EZ_DATA16	0x40260440
SCB2_EZ_DATA17	0x40260444
SCB2_EZ_DATA18	0x40260448
SCB2_EZ_DATA19	0x4026044C
SCB2_EZ_DATA20	0x40260450
SCB2_EZ_DATA21	0x40260454
SCB2_EZ_DATA22	0x40260458
SCB2_EZ_DATA23	0x4026045C
SCB2_EZ_DATA24	0x40260460
SCB2_EZ_DATA25	0x40260464
SCB2_EZ_DATA26	0x40260468
SCB2_EZ_DATA27	0x4026046C
SCB2_EZ_DATA28	0x40260470
SCB2_EZ_DATA29	0x40260474
SCB2_EZ_DATA30	0x40260478
SCB2_EZ_DATA31	0x4026047C
SCB2_INTR_CAUSE	0x40260E00
SCB2_INTR_I2C_EC	0x40260E80
SCB2_INTR_I2C_EC_MASK	0x40260E88
SCB2_INTR_I2C_EC_MASKED	0x40260E8C
SCB2_INTR_SPI_EC	0x40260EC0
SCB2_INTR_SPI_EC_MASK	0x40260EC8
SCB2_INTR_SPI_EC_MASKED	0x40260ECC
SCB2_INTR_M	0x40260F00
SCB2_INTR_M_SET	0x40260F04
SCB2_INTR_M_MASK	0x40260F08
SCB2_INTR_M_MASKED	0x40260F0C
SCB2_INTR_S	0x40260F40
SCB2_INTR_S_SET	0x40260F44
SCB2_INTR_S_MASK	0x40260F48
SCB2_INTR_S_MASKED	0x40260F4C
SCB2_INTR_TX	0x40260F80
SCB2_INTR_TX_SET	0x40260F84
SCB2_INTR_TX_MASK	0x40260F88
SCB2_INTR_TX_MASKED	0x40260F8C
SCB2_INTR_RX	0x40260FC0
SCB2_INTR_RX_SET	0x40260FC4
SCB2_INTR_RX_MASK	0x40260FC8
SCB2_INTR_RX_MASKED	0x40260FCC

Register Name	Address
SCB3_CTRL	0x40270000
SCB3_STATUS	0x40270004
SCB3_SPI_CTRL	0x40270020
SCB3_SPI_STATUS	0x40270024
SCB3_UART_CTRL	0x40270040
SCB3_UART_TX_CTRL	0x40270044
SCB3_UART_RX_CTRL	0x40270048
SCB3_UART_RX_STATUS	0x4027004C
SCB3_UART_FLOW_CTRL	0x40270050
SCB3_I2C_CTRL	0x40270060
SCB3_I2C_STATUS	0x40270064
SCB3_I2C_M_CMD	0x40270068
SCB3_I2C_S_CMD	0x4027006C
SCB3_I2C_CFG	0x40270070
SCB3_TX_CTRL	0x40270200
SCB3_TX_FIFO_CTRL	0x40270204
SCB3_TX_FIFO_STATUS	0x40270208
SCB3_TX_FIFO_WR	0x40270240
SCB3_RX_CTRL	0x40270300
SCB3_RX_FIFO_CTRL	0x40270304
SCB3_RX_FIFO_STATUS	0x40270308
SCB3_RX_MATCH	0x40270310
SCB3_RX_FIFO_RD	0x40270340
SCB3_RX_FIFO_RD_SILENT	0x40270344
SCB3_EZ_DATA0	0x40270400
SCB3_EZ_DATA1	0x40270404
SCB3_EZ_DATA2	0x40270408
SCB3_EZ_DATA3	0x4027040C
SCB3_EZ_DATA4	0x40270410
SCB3_EZ_DATA5	0x40270414
SCB3_EZ_DATA6	0x40270418
SCB3_EZ_DATA7	0x4027041C
SCB3_EZ_DATA8	0x40270420
SCB3_EZ_DATA9	0x40270424
SCB3_EZ_DATA10	0x40270428
SCB3_EZ_DATA11	0x4027042C
SCB3_EZ_DATA12	0x40270430
SCB3_EZ_DATA13	0x40270434
SCB3_EZ_DATA14	0x40270438
SCB3_EZ_DATA15	0x4027043C
SCB3_EZ_DATA16	0x40270440
SCB3_EZ_DATA17	0x40270444

Register Name	Address
SCB3_EZ_DATA18	0x40270448
SCB3_EZ_DATA19	0x4027044C
SCB3_EZ_DATA20	0x40270450
SCB3_EZ_DATA21	0x40270454
SCB3_EZ_DATA22	0x40270458
SCB3_EZ_DATA23	0x4027045C
SCB3_EZ_DATA24	0x40270460
SCB3_EZ_DATA25	0x40270464
SCB3_EZ_DATA26	0x40270468
SCB3_EZ_DATA27	0x4027046C
SCB3_EZ_DATA28	0x40270470
SCB3_EZ_DATA29	0x40270474
SCB3_EZ_DATA30	0x40270478
SCB3_EZ_DATA31	0x4027047C
SCB3_INTR_CAUSE	0x40270E00
SCB3_INTR_I2C_EC	0x40270E80
SCB3_INTR_I2C_EC_MASK	0x40270E88
SCB3_INTR_I2C_EC_MASKED	0x40270E8C
SCB3_INTR_SPI_EC	0x40270EC0
SCB3_INTR_SPI_EC_MASK	0x40270EC8
SCB3_INTR_SPI_EC_MASKED	0x40270ECC
SCB3_INTR_M	0x40270F00
SCB3_INTR_M_SET	0x40270F04
SCB3_INTR_M_MASK	0x40270F08
SCB3_INTR_M_MASKED	0x40270F0C
SCB3_INTR_S	0x40270F40
SCB3_INTR_S_SET	0x40270F44
SCB3_INTR_S_MASK	0x40270F48
SCB3_INTR_S_MASKED	0x40270F4C
SCB3_INTR_TX	0x40270F80
SCB3_INTR_TX_SET	0x40270F84
SCB3_INTR_TX_MASK	0x40270F88
SCB3_INTR_TX_MASKED	0x40270F8C
SCB3_INTR_RX	0x40270FC0
SCB3_INTR_RX_SET	0x40270FC4
SCB3_INTR_RX_MASK	0x40270FC8
SCB3_INTR_RX_MASKED	0x40270FCC
SCB4_CTRL	0x40280000
SCB4_STATUS	0x40280004
SCB4_SPI_CTRL	0x40280020
SCB4_SPI_STATUS	0x40280024
SCB4_UART_CTRL	0x40280040

Register Name	Address
SCB4_UART_TX_CTRL	0x40280044
SCB4_UART_RX_CTRL	0x40280048
SCB4_UART_RX_STATUS	0x4028004C
SCB4_UART_FLOW_CTRL	0x40280050
SCB4_I2C_CTRL	0x40280060
SCB4_I2C_STATUS	0x40280064
SCB4_I2C_M_CMD	0x40280068
SCB4_I2C_S_CMD	0x4028006C
SCB4_I2C_CFG	0x40280070
SCB4_TX_CTRL	0x40280200
SCB4_TX_FIFO_CTRL	0x40280204
SCB4_TX_FIFO_STATUS	0x40280208
SCB4_TX_FIFO_WR	0x40280240
SCB4_RX_CTRL	0x40280300
SCB4_RX_FIFO_CTRL	0x40280304
SCB4_RX_FIFO_STATUS	0x40280308
SCB4_RX_MATCH	0x40280310
SCB4_RX_FIFO_RD	0x40280340
SCB4_RX_FIFO_RD_SILENT	0x40280344
SCB4_EZ_DATA0	0x40280400
SCB4_EZ_DATA1	0x40280404
SCB4_EZ_DATA2	0x40280408
SCB4_EZ_DATA3	0x4028040C
SCB4_EZ_DATA4	0x40280410
SCB4_EZ_DATA5	0x40280414
SCB4_EZ_DATA6	0x40280418
SCB4_EZ_DATA7	0x4028041C
SCB4_EZ_DATA8	0x40280420
SCB4_EZ_DATA9	0x40280424
SCB4_EZ_DATA10	0x40280428
SCB4_EZ_DATA11	0x4028042C
SCB4_EZ_DATA12	0x40280430
SCB4_EZ_DATA13	0x40280434
SCB4_EZ_DATA14	0x40280438
SCB4_EZ_DATA15	0x4028043C
SCB4_EZ_DATA16	0x40280440
SCB4_EZ_DATA17	0x40280444
SCB4_EZ_DATA18	0x40280448
SCB4_EZ_DATA19	0x4028044C
SCB4_EZ_DATA20	0x40280450
SCB4_EZ_DATA21	0x40280454
SCB4_EZ_DATA22	0x40280458

Register Name	Address
SCB4_EZ_DATA23	0x4028045C
SCB4_EZ_DATA24	0x40280460
SCB4_EZ_DATA25	0x40280464
SCB4_EZ_DATA26	0x40280468
SCB4_EZ_DATA27	0x4028046C
SCB4_EZ_DATA28	0x40280470
SCB4_EZ_DATA29	0x40280474
SCB4_EZ_DATA30	0x40280478
SCB4_EZ_DATA31	0x4028047C
SCB4_INTR_CAUSE	0x40280E00
SCB4_INTR_I2C_EC	0x40280E80
SCB4_INTR_I2C_EC_MASK	0x40280E88
SCB4_INTR_I2C_EC_MASKED	0x40280E8C
SCB4_INTR_SPI_EC	0x40280EC0
SCB4_INTR_SPI_EC_MASK	0x40280EC8
SCB4_INTR_SPI_EC_MASKED	0x40280ECC
SCB4_INTR_M	0x40280F00
SCB4_INTR_M_SET	0x40280F04
SCB4_INTR_M_MASK	0x40280F08
SCB4_INTR_M_MASKED	0x40280F0C
SCB4_INTR_S	0x40280F40
SCB4_INTR_S_SET	0x40280F44
SCB4_INTR_S_MASK	0x40280F48
SCB4_INTR_S_MASKED	0x40280F4C
SCB4_INTR_TX	0x40280F80
SCB4_INTR_TX_SET	0x40280F84
SCB4_INTR_TX_MASK	0x40280F88
SCB4_INTR_TX_MASKED	0x40280F8C
SCB4_INTR_RX	0x40280FC0
SCB4_INTR_RX_SET	0x40280FC4
SCB4_INTR_RX_MASK	0x40280FC8
SCB4_INTR_RX_MASKED	0x40280FCC

25.1.1 SCB0_CTRL

Generic control register.

Address: 0x40240000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BYTE_-MODE	EZ_MODE	EC_OP_-MODE	EC_AM_-MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_AC-CEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL register to enable SCB, select the specific operation mode and oversampling factor. When this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3

(continued)

		0x0: I2C: Inter-Integrated Circuits (I2C) mode. **0x1: SPI:** Serial Peripheral Interface (SPI) mode. **0x2: UART:** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the internal CPU accesses to EZ memory coincide/collide, this bit determines whether the CPU access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is 0 and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: INTR_TX.BLOCKED and INTR_RX.BLOCKED. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not seperated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	EC_OP_MODE	This field specifies the clocking for the SCB block '0': Internally clocked mode '1': externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0

(continued)

8	EC_AM_MODE	This field specifies the clocking for the address matching (I2C) or slave selection detection logic (SPI) '0': Internally clocked mode '1': Externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0

(continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. OVS + 1 SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps. As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. SCB clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. SCB clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. SCB clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. SCB clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. SCB clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. SCB clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

25.1.2 SCB0_STATUS

Generic status register.

Address: 0x40240004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

25.1.3 SCB0_SPI_CTRL

SPI control register.

Address: 0x40240020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_-CONTINU-OUS	LATE_MISO_SAMPLE	CPOL	CPHA	SE-LECT_PRE-CEDE	CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_PO-LARITY3	SSEL_PO-LARITY2	SSEL_PO-LARITY1	SSEL_PO-LARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_-MODE	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SLAVE_SELECT	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. SCB block should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

(continued)

		0x0: SPI_MOTOROLA: SPI Motorola submode. In master mode, when not transmitting data (Slave SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive. **0x1: SPI_TI:** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS:** SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': No local loopback '1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loop-back mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode). Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode). Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode). Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). only SPI_SELECT[0] is used in slave mode. For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Istruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0

(continued)

4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0
3	CPOL	Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is 0: SCLK is 0 when not transmitting data. - CPOL is 1: SCLK is 1 when not transmitting data. Default Value: 0
2	CPHA	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is 0, CPHA is 0: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is 0, CPHA is 1: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is 1, CPHA is 0: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is 1, CPHA is 1: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily seperated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always seperated by slave deselection: independent of the availability of TX FIFO data frames, data frames are sent out with slave deselection. Default Value: 0

25.1.4 SCB0_SPI_STATUS

SPI status register.

Address: 0x40240024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

25.1.5 SCB0_UART_CTRL

UART control register.

Address: 0x40240040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD:** Standard UART submode. **0x1: UART_SMARTCARD:** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA:** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS should be set to 15.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). 0: Loopback is not enabled 1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS. This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

25.1.6 SCB0_UART_TX_CTRL

UART transmitter control register.

Address: 0x40240044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

25.1.7 SCB0_UART_RX_CTRL

UART receiver control register.

Address: 0x40240048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

(continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behaviour when a parity check fails. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

(continued)

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value. Default Value: 2

25.1.8 SCB0_UART_RX_STATUS

UART receiver status register.

Address: 0x4024004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

25.1.9 SCB0_UART_FLOW_CTRL

UART flow control register

Address: 0x40240050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_PO-LARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_EN-ABLED	CTS_PO-LARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal by the UART transmitter: '0': Disabled. The UART transmitter ignores the CTS input signal and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses CTS input signal to qualify the transmission of data. It transmits when CTS input signal is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', the CTS input signal is driven by the RTS output signal locally in SCB (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal '0': CTS is active low ; '1': CTS is active high; Default Value: 0

(continued)

16	RTS_POLARITY	Polarity of the RTS output signal: '0': RTS is active low; '1': RTS is active high; During SCB reset (Hibernate system power mode), RTS output signal is '1'. This represents an inactive state assuming an active low polarity. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal is activated. By setting this field to "0", flow control is effectively disabled (may be useful for debug purposes). Default Value: 0

25.1.10 SCB0_I2C_CTRL

I2C control register.

Address: 0x40240060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_-DATA_NACK	S_NOT_READY_AD-DR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENER-AL_IGNORE	None	M_NOT_READY_-DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_-MODE	SLAVE_-MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', no loopback When '1', loopback is enabled internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0

(continued)

15	S_NOT_READY_-DATA_NACK	Only used when: - non EZ mode Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1
14	S_NOT_READY_AD-DR_NACK	This field is used during an address match or general call address in internally clocked mode Only used when: - EC_AM_MODE is '0', EC_OP_MODE is '0', S_GENERAL_IGNORE is '0] and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the SCB clock is available (in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2).SCB clock is not present (in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the SCB clock is available). The logic will handle the ongoing transfer as soon as the clock is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_-DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1

(continued)

7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 SCB clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular (no stretching) interface (IF) low time to guarantee functionally correct behavior. With input signal median filtering, the IF low time should be >= 8 SCB clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 SCB clock cycles and <= 16 SCB clock cycles. Default Value: 8
3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 SCB clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 SCB clock cycles and <= 16 SCB clock cycles. Without input signal median filtering, the IF high time should be >= 5 SCB clock cycles and <= 16 SCB clock cycles. Default Value: 8

25.1.11 SCB0_I2C_STATUS

I2C status register.

Address: 0x40240064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". Default Value: 0

(continued)

1	I2C_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

25.1.12 SCB0_I2C_M_CMD

I2C master command register.

Address: 0x40240068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0

(continued)

1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0
0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

25.1.13 SCB0_I2C_S_CMD

I2C slave command register.

Address: 0x4024006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

25.1.14 SCB0_I2C_CFG

I2C configuration register.

Address: 0x40240070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_-FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_-FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative filter delay on SDA output to meet tHD_DAT parameter "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2

(continued)

12	SCL_IN_FILT_SEL	Enable for 50ns glitch filter on SCL input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 0
4	SDA_IN_FILT_SEL	Enable for 50ns glitch filter on SDA input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 3

25.1.15 SCB0_TX_CTRL

Transmitter control register.

Address: 0x40240200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

25.1.16 SCB0_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x40240204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

25.1.17 SCB0_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x40240208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

25.1.18 SCB0_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x40240240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

25.1.19 SCB0_RX_CTRL

Receiver control register.

Address: 0x40240300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

25.1.20 SCB0_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x40240304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

25.1.21 SCB0_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x40240308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

25.1.22 SCB0_RX_MATCH

Slave address and mask register.

Address: 0x40240310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the slave address bits take part in the matching. MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

25.1.23 SCB0_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x40240340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. When this register is read through the debugger, the data frame will not be removed from the FIFO. Similar in operation to RX_FIFO_RD_SILENT Default Value: Undefined

25.1.24 SCB0_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x40240344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.BYTE_-MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

25.1.25 SCB0_EZ_DATA0

Memory buffer registers.

Address: 0x40240400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.26 SCB0_EZ_DATA1

Memory buffer registers.

Address: 0x40240404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.27 SCB0_EZ_DATA2

Memory buffer registers.

Address: 0x40240408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.28 SCB0_EZ_DATA3

Memory buffer registers.

Address: 0x4024040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.29 SCB0_EZ_DATA4

Memory buffer registers.

Address: 0x40240410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.30 SCB0_EZ_DATA5

Memory buffer registers.

Address: 0x40240414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.31 SCB0_EZ_DATA6

Memory buffer registers.

Address: 0x40240418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.32 SCB0_EZ_DATA7

Memory buffer registers.

Address: 0x4024041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.33 SCB0_EZ_DATA8

Memory buffer registers.

Address: 0x40240420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.34 SCB0_EZ_DATA9

Memory buffer registers.

Address: 0x40240424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.35 SCB0_EZ_DATA10

Memory buffer registers.

Address: 0x40240428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.36 SCB0_EZ_DATA11

Memory buffer registers.

Address: 0x4024042C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.37 SCB0_EZ_DATA12

Memory buffer registers.

Address: 0x40240430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.38 SCB0_EZ_DATA13

Memory buffer registers.

Address: 0x40240434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.39 SCB0_EZ_DATA14

Memory buffer registers.

Address: 0x40240438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.40 SCB0_EZ_DATA15

Memory buffer registers.

Address: 0x4024043C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.41 SCB0_EZ_DATA16

Memory buffer registers.

Address: 0x40240440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.42 SCB0_EZ_DATA17

Memory buffer registers.

Address: 0x40240444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.43 SCB0_EZ_DATA18

Memory buffer registers.

Address: 0x40240448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.44 SCB0_EZ_DATA19

Memory buffer registers.

Address: 0x4024044C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.45 SCB0_EZ_DATA20

Memory buffer registers.

Address: 0x40240450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.46 SCB0_EZ_DATA21

Memory buffer registers.

Address: 0x40240454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.47 SCB0_EZ_DATA22

Memory buffer registers.

Address: 0x40240458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.48 SCB0_EZ_DATA23

Memory buffer registers.

Address: 0x4024045C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.49 SCB0_EZ_DATA24

Memory buffer registers.

Address: 0x40240460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.50 SCB0_EZ_DATA25

Memory buffer registers.

Address: 0x40240464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.51 SCB0_EZ_DATA26

Memory buffer registers.

Address: 0x40240468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.52 SCB0_EZ_DATA27

Memory buffer registers.

Address: 0x4024046C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.53 SCB0_EZ_DATA28

Memory buffer registers.

Address: 0x40240470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.54 SCB0_EZ_DATA29

Memory buffer registers.

Address: 0x40240474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.55 SCB0_EZ_DATA30

Memory buffer registers.

Address: 0x40240478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.56 SCB0_EZ_DATA31

Memory buffer registers.

Address: 0x4024047C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.57 SCB0_INTR_CAUSE

Active clocked interrupt signal register

Address: 0x40240E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

25.1.58 SCB0_INTR_I2C_EC

Externally clocked I2C interrupt request register

Address: 0x40240E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0

(continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

25.1.59 SCB0_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask register

Address: 0x40240E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.60 SCB0_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40240E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

25.1.61 SCB0_INTR_SPI_EC

Externally clocked SPI interrupt request register

Address: 0x40240EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when CTRL.EC_OP_MODE is '1'. Default Value: 0

(continued)

0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

25.1.62 SCB0_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask register

Address: 0x40240EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.63 SCB0_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40240ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

25.1.64 SCB0_INTR_M

Master interrupt request register.

Address: 0x40240F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0
0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

25.1.65 SCB0_INTR_M_SET

Master interrupt set request register

Address: 0x40240F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.66 SCB0_INTR_M_MASK

Master interrupt mask register.

Address: 0x40240F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.67 SCB0_INTR_M_MASKED

Master interrupt masked request register

Address: 0x40240F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

25.1.68 SCB0_INTR_S

Slave interrupt request register.

Address: 0x40240F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

(continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

25.1.69 SCB0_INTR_S_SET

Slave interrupt set request register.

Address: 0x40240F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.70 SCB0_INTR_S_MASK

Slave interrupt mask register.

Address: 0x40240F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.71 SCB0_INTR_S_MASKED

Slave interrupt masked request register

Address: 0x40240F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

25.1.72 SCB0_INTR_TX

Transmitter interrupt request register.

Address: 0x40240F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

(continued)

6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.BYTE_MODE: BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode. Default Value: 0

25.1.73 SCB0_INTR_TX_SET

Transmitter interrupt set request register

Address: 0x40240F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.74 SCB0_INTR_TX_MASK

Transmitter interrupt mask register.

Address: 0x40240F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.75 SCB0_INTR_TX_MASKED

Transmitter interrupt masked request register

Address: 0x40240F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

25.1.76 SCB0_INTR_RX

Receiver interrupt request register.

Address: 0x40240FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is ecpected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STA-TUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guaran-tee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

(continued)

9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_-FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODET: BYTE_MODE is '0': # entries == FF_DATA_NR/2. BYTE_MODE is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FI-FO_CTL. Only used in FIFO mode. Default Value: 0

25.1.77 SCB0_INTR_RX_SET

Receiver interrupt set request register.

Address: 0x40240FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

(continued)

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.78 SCB0_INTR_RX_MASK

Receiver interrupt mask register.

Address: 0x40240FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.79 SCB0_INTR_RX_MASKED

Receiver interrupt masked request register

Address: 0x40240FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

25.1.80 SCB1_CTRL

Generic control register.

Address: 0x40250000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BYTE_-MODE	EZ_MODE	EC_OP_-MODE	EC_AM_-MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_AC-CEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL register to enable SCB, select the specific operation mode and oversampling factor. When this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3

(continued)

		0x0: I2C: Inter-Integrated Circuits (I2C) mode. **0x1: SPI:** Serial Peripheral Interface (SPI) mode. **0x2: UART:** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the internal CPU accesses to EZ memory coincide/collide, this bit determines whether the CPU access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is 0 and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: INTR_TX.BLOCKED and INTR_RX.BLOCKED. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not seperated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	EC_OP_MODE	This field specifies the clocking for the SCB block '0': Internally clocked mode '1': externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0

(continued)

8	EC_AM_MODE	This field specifies the clocking for the address matching (I2C) or slave selection detection logic (SPI) '0': Internally clocked mode '1': Externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0

(continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. OVS + 1 SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps. As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. SCB clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. SCB clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. SCB clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. SCB clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. SCB clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. SCB clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

25.1.81 SCB1_STATUS

Generic status register.

Address: 0x40250004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

25.1.82 SCB1_SPI_CTRL

SPI control register.

Address: 0x40250020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_-CONTINU-OUS	LATE_MISO_SAMPLE	CPOL	CPHA	SE-LECT_PRE-CEDE	CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_PO-LARITY3	SSEL_PO-LARITY2	SSEL_PO-LARITY1	SSEL_PO-LARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_-MODE	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SLAVE_SELECT	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. SCB block should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

(continued)

		0x0: SPI_MOTOROLA: SPI Motorola submode. In master mode, when not transmitting data (Slave SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive. **0x1: SPI_TI:** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS:** SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': No local loopback '1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loop-back mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode). Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode). Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode). Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). only SPI_SELECT[0] is used in slave mode. For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Istruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0

(continued)

4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0
3	CPOL	Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is 0: SCLK is 0 when not transmitting data. - CPOL is 1: SCLK is 1 when not transmitting data. Default Value: 0
2	CPHA	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is 0, CPHA is 0: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is 0, CPHA is 1: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is 1, CPHA is 0: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is 1, CPHA is 1: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily seperated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always seperated by slave deselection: independent of the availability of TX FIFO data frames, data frames are sent out with slave deselection. Default Value: 0

25.1.83 SCB1_SPI_STATUS

SPI status register.

Address: 0x40250024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

25.1.84 SCB1_UART_CTRL

UART control register.

Address: 0x40250040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD:** Standard UART submode. **0x1: UART_SMARTCARD:** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA:** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS should be set to 15.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). 0: Loopback is not enabled 1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS. This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

25.1.85 SCB1_UART_TX_CTRL

UART transmitter control register.

Address: 0x40250044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

25.1.86 SCB1_UART_RX_CTRL

UART receiver control register.

Address: 0x40250048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

(continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behaviour when a parity check fails. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

(continued)

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value. Default Value: 2

25.1.87 SCB1_UART_RX_STATUS

UART receiver status register.

Address: 0x4025004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

25.1.88 SCB1_UART_FLOW_CTRL

UART flow control register

Address: 0x40250050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal by the UART transmitter: '0': Disabled. The UART transmitter ignores the CTS input signal and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses CTS input signal to qualify the transmission of data. It transmits when CTS input signal is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', the CTS input signal is driven by the RTS output signal locally in SCB (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal '0': CTS is active low ; '1': CTS is active high; Default Value: 0

(continued)

16	RTS_POLARITY	Polarity of the RTS output signal: '0': RTS is active low; '1': RTS is active high; During SCB reset (Hibernate system power mode), RTS output signal is '1'. This represents an inactive state assuming an active low polarity. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal is activated. By setting this field to "0", flow control is effectively disabled (may be useful for debug purposes). Default Value: 0

25.1.89 SCB1_I2C_CTRL

I2C control register.

Address: 0x40250060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_RE ADY_- DATA_NAC K	S_NOT_RE ADY_AD- DR_NACK	S_READY_ DATA_ACK	S_READY_ ADDR_ACK	S_GENER- AL_IGNOR E	None	M_NOT_RE ADY_- DATA_NAC K	M_READY_ DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_- MODE	SLAVE_- MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', no loopback When '1', loopback is enabled internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0

(continued)

15	S_NOT_READY_-DATA_NACK	Only used when: - non EZ mode Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1
14	S_NOT_READY_AD-DR_NACK	This field is used during an address match or general call address in internally clocked mode Only used when: - EC_AM_MODE is '0', EC_OP_MODE is '0', S_GENERAL_IGNORE is '0] and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the SCB clock is available (in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2).SCB clock is not present (in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the SCB clock is available). The logic will handle the ongoing transfer as soon as the clock is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_-DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1

(continued)

7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 SCB clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular (no stretching) interface (IF) low time to guarantee functionally correct behavior. With input signal median filtering, the IF low time should be >= 8 SCB clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 SCB clock cycles and <= 16 SCB clock cycles. Default Value: 8
3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 SCB clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 SCB clock cycles and <= 16 SCB clock cycles. Without input signal median filtering, the IF high time should be >= 5 SCB clock cycles and <= 16 SCB clock cycles. Default Value: 8

25.1.90 SCB1_I2C_STATUS

I2C status register.

Address: 0x40250064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". Default Value: 0

(continued)

1	I2C_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

25.1.91 SCB1_I2C_M_CMD

I2C master command register.

Address: 0x40250068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0

(continued)

1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0
0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

25.1.92 SCB1_I2C_S_CMD

I2C slave command register.

Address: 0x4025006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

25.1.93 SCB1_I2C_CFG

I2C configuration register.

Address: 0x40250070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_-FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_-FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative filter delay on SDA output to meet tHD_DAT parameter "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2

(continued)

12	SCL_IN_FILT_SEL	Enable for 50ns glitch filter on SCL input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 0
4	SDA_IN_FILT_SEL	Enable for 50ns glitch filter on SDA input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 3

25.1.94 SCB1_TX_CTRL

Transmitter control register.

Address: 0x40250200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

25.1.95 SCB1_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x40250204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

25.1.96 SCB1_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x40250208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

25.1.97 SCB1_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x40250240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

25.1.98 SCB1_RX_CTRL

Receiver control register.

Address: 0x40250300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

25.1.99 SCB1_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x40250304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

25.1.100 SCB1_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x40250308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

25.1.101 SCB1_RX_MATCH

Slave address and mask register.

Address: 0x40250310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the slave address bits take part in the matching. MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

25.1.102 SCB1_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x40250340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. When this register is read through the debugger, the data frame will not be removed from the FIFO. Similar in operation to RX_FIFO_RD_SILENT Default Value: Undefined

25.1.103 SCB1_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x40250344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.BYTE_-MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

25.1.104 SCB1_EZ_DATA0

Memory buffer registers.

Address: 0x40250400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.105 SCB1_EZ_DATA1

Memory buffer registers.

Address: 0x40250404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.106 SCB1_EZ_DATA2

Memory buffer registers.

Address: 0x40250408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.107 SCB1_EZ_DATA3

Memory buffer registers.

Address: 0x4025040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.108 SCB1_EZ_DATA4

Memory buffer registers.

Address: 0x40250410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.109 SCB1_EZ_DATA5

Memory buffer registers.

Address: 0x40250414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.110 SCB1_EZ_DATA6

Memory buffer registers.

Address: 0x40250418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.111 SCB1_EZ_DATA7

Memory buffer registers.

Address: 0x4025041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.112 SCB1_EZ_DATA8

Memory buffer registers.

Address: 0x40250420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.113 SCB1_EZ_DATA9

Memory buffer registers.

Address: 0x40250424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.114 SCB1_EZ_DATA10

Memory buffer registers.

Address: 0x40250428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.115 SCB1_EZ_DATA11

Memory buffer registers.

Address: 0x4025042C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.116 SCB1_EZ_DATA12

Memory buffer registers.

Address: 0x40250430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.117 SCB1_EZ_DATA13

Memory buffer registers.

Address: 0x40250434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.118 SCB1_EZ_DATA14

Memory buffer registers.

Address: 0x40250438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.119 SCB1_EZ_DATA15

Memory buffer registers.

Address: 0x4025043C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.120 SCB1_EZ_DATA16

Memory buffer registers.

Address: 0x40250440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.121 SCB1_EZ_DATA17

Memory buffer registers.

Address: 0x40250444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.122 SCB1_EZ_DATA18

Memory buffer registers.

Address: 0x40250448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.123 SCB1_EZ_DATA19

Memory buffer registers.

Address: 0x4025044C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.124 SCB1_EZ_DATA20

Memory buffer registers.

Address: 0x40250450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.125 SCB1_EZ_DATA21

Memory buffer registers.

Address: 0x40250454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.126 SCB1_EZ_DATA22

Memory buffer registers.

Address: 0x40250458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.127 SCB1_EZ_DATA23

Memory buffer registers.

Address: 0x4025045C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.128 SCB1_EZ_DATA24

Memory buffer registers.

Address: 0x40250460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.129 SCB1_EZ_DATA25

Memory buffer registers.

Address: 0x40250464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.130 SCB1_EZ_DATA26

Memory buffer registers.

Address: 0x40250468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.131 SCB1_EZ_DATA27

Memory buffer registers.

Address: 0x4025046C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.132 SCB1_EZ_DATA28

Memory buffer registers.

Address: 0x40250470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.133 SCB1_EZ_DATA29

Memory buffer registers.

Address: 0x40250474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.134 SCB1_EZ_DATA30

Memory buffer registers.

Address: 0x40250478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.135 SCB1_EZ_DATA31

Memory buffer registers.

Address: 0x4025047C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.136 SCB1_INTR_CAUSE

Active clocked interrupt signal register

Address: 0x40250E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

25.1.137 SCB1_INTR_I2C_EC

Externally clocked I2C interrupt request register

Address: 0x40250E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0

(continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

25.1.138 SCB1_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask register

Address: 0x40250E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.139 SCB1_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40250E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_ STOP	EZ_WRITE _STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

25.1.140 SCB1_INTR_SPI_EC

Externally clocked SPI interrupt request register

Address: 0x40250EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when CTRL.EC_OP_MODE is '1'. Default Value: 0

(continued)

0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

25.1.141 SCB1_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask register

Address: 0x40250EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.142 SCB1_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40250ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

25.1.143 SCB1_INTR_M

Master interrupt request register.

Address: 0x40250F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0
0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

25.1.144 SCB1_INTR_M_SET

Master interrupt set request register

Address: 0x40250F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.145 SCB1_INTR_M_MASK

Master interrupt mask register.

Address: 0x40250F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.146 SCB1_INTR_M_MASKED

Master interrupt masked request register

Address: 0x40250F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

25.1.147 SCB1_INTR_S

Slave interrupt request register.

Address: 0x40250F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

(continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

25.1.148 SCB1_INTR_S_SET

Slave interrupt set request register.

Address: 0x40250F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.149 SCB1_INTR_S_MASK

Slave interrupt mask register.

Address: 0x40250F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.150 SCB1_INTR_S_MASKED

Slave interrupt masked request register

Address: 0x40250F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

25.1.151 SCB1_INTR_TX

Transmitter interrupt request register.

Address: 0x40250F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

(continued)

6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.BYTE_MODE: BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode. Default Value: 0

25.1.152 SCB1_INTR_TX_SET

Transmitter interrupt set request register

Address: 0x40250F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.153 SCB1_INTR_TX_MASK

Transmitter interrupt mask register.

Address: 0x40250F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.154 SCB1_INTR_TX_MASKED

Transmitter interrupt masked request register

Address: 0x40250F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

25.1.155 SCB1_INTR_RX

Receiver interrupt request register.

Address: 0x40250FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is ecpected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STA-TUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guaran-tee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

(continued)

9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_-FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODET: BYTE_MODE is '0': # entries == FF_DATA_NR/2. BYTE_MODE is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FI-FO_CTL. Only used in FIFO mode. Default Value: 0

25.1.156 SCB1_INTR_RX_SET

Receiver interrupt set request register.

Address: 0x40250FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

(continued)

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.157 SCB1_INTR_RX_MASK

Receiver interrupt mask register.

Address: 0x40250FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.158 SCB1_INTR_RX_MASKED

Receiver interrupt masked request register

Address: 0x40250FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

25.1.159 SCB2_CTRL

Generic control register.

Address: 0x40260000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BYTE_-MODE	EZ_MODE	EC_OP_-MODE	EC_AM_-MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_AC-CEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL register to enable SCB, select the specific operation mode and oversampling factor. When this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3

(continued)

		0x0: I2C: Inter-Integrated Circuits (I2C) mode. **0x1: SPI:** Serial Peripheral Interface (SPI) mode. **0x2: UART:** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the internal CPU accesses to EZ memory coincide/collide, this bit determines whether the CPU access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is 0 and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: INTR_TX.BLOCKED and INTR_RX.BLOCKED. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not seperated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	EC_OP_MODE	This field specifies the clocking for the SCB block '0': Internally clocked mode '1': externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0

(continued)

8	EC_AM_MODE	This field specifies the clocking for the address matching (I2C) or slave selection detection logic (SPI) '0': Internally clocked mode '1': Externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0

(continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. OVS + 1 SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps. As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. SCB clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. SCB clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. SCB clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. SCB clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. SCB clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. SCB clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

25.1.160 SCB2_STATUS

Generic status register.

Address: 0x40260004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

25.1.161 SCB2_SPI_CTRL

SPI control register.

Address: 0x40260020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_-CONTINU-OUS	LATE_MISO_SAMPLE	CPOL	CPHA	SE-LECT_PRE-CEDE	CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_PO-LARITY3	SSEL_PO-LARITY2	SSEL_PO-LARITY1	SSEL_PO-LARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_-MODE	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SLAVE_SELECT	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. SCB block should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

(continued)

		0x0: SPI_MOTOROLA: SPI Motorola submode. In master mode, when not transmitting data (Slave SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive. **0x1: SPI_TI:** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS:** SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': No local loopback '1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loop-back mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode). Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode). Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode). Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). only SPI_SELECT[0] is used in slave mode. For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Istruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0

(continued)

4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0
3	CPOL	Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is 0: SCLK is 0 when not transmitting data. - CPOL is 1: SCLK is 1 when not transmitting data. Default Value: 0
2	CPHA	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is 0, CPHA is 0: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is 0, CPHA is 1: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is 1, CPHA is 0: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is 1, CPHA is 1: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily seperated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always seperated by slave deselection: independent of the availability of TX FIFO data frames, data frames are sent out with slave deselection. Default Value: 0

25.1.162 SCB2_SPI_STATUS

SPI status register.

Address: 0x40260024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

25.1.163 SCB2_UART_CTRL

UART control register.

Address: 0x40260040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD:** Standard UART submode. **0x1: UART_SMARTCARD:** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA:** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS should be set to 15.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). 0: Loopback is not enabled 1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS. This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

25.1.164 SCB2_UART_TX_CTRL

UART transmitter control register.

Address: 0x40260044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

25.1.165 SCB2_UART_RX_CTRL

UART receiver control register.

Address: 0x40260048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

(continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behaviour when a parity check fails. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

(continued)

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value. Default Value: 2

25.1.166 SCB2_UART_RX_STATUS

UART receiver status register.

Address: 0x4026004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

25.1.167 SCB2_UART_FLOW_CTRL

UART flow control register

Address: 0x40260050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal by the UART transmitter: '0': Disabled. The UART transmitter ignores the CTS input signal and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses CTS input signal to qualify the transmission of data. It transmits when CTS input signal is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', the CTS input signal is driven by the RTS output signal locally in SCB (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal '0': CTS is active low ; '1': CTS is active high; Default Value: 0

(continued)

16	RTS_POLARITY	Polarity of the RTS output signal: '0': RTS is active low; '1': RTS is active high; During SCB reset (Hibernate system power mode), RTS output signal is '1'. This represents an inactive state assuming an active low polarity. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal is activated. By setting this field to "0", flow control is effectively disabled (may be useful for debug purposes). Default Value: 0

25.1.168 SCB2_I2C_CTRL

I2C control register.

Address: 0x40260060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_RE ADY_- DATA_NAC K	S_NOT_RE ADY_AD- DR_NACK	S_READY_ DATA_ACK	S_READY_ ADDR_ACK	S_GENER- AL_IGNOR E	None	M_NOT_RE ADY_- DATA_NAC K	M_READY_ DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_- MODE	SLAVE_- MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', no loopback When '1', loopback is enabled internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0

(continued)

15	S_NOT_READY_-DATA_NACK	Only used when: - non EZ mode Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1
14	S_NOT_READY_AD-DR_NACK	This field is used during an address match or general call address in internally clocked mode Only used when: - EC_AM_MODE is '0', EC_OP_MODE is '0', S_GENERAL_IGNORE is '0] and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the SCB clock is available (in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2).SCB clock is not present (in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the SCB clock is available). The logic will handle the ongoing transfer as soon as the clock is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_-DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1

(continued)

7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 SCB clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular (no stretching) interface (IF) low time to guarantee functionally correct behavior. With input signal median filtering, the IF low time should be >= 8 SCB clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 SCB clock cycles and <= 16 SCB clock cycles. Default Value: 8
3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 SCB clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 SCB clock cycles and <= 16 SCB clock cycles. Without input signal median filtering, the IF high time should be >= 5 SCB clock cycles and <= 16 SCB clock cycles. Default Value: 8

25.1.169 SCB2_I2C_STATUS

I2C status register.

Address: 0x40260064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". Default Value: 0

(continued)

1	I2C_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

25.1.170 SCB2_I2C_M_CMD

I2C master command register.

Address: 0x40260068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0

(continued)

1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0
0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

25.1.171 SCB2_I2C_S_CMD

I2C slave command register.

Address: 0x4026006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

25.1.172 SCB2_I2C_CFG

I2C configuration register.

Address: 0x40260070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_-FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_-FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative filter delay on SDA output to meet tHD_DAT parameter "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2

(continued)

12	SCL_IN_FILT_SEL	Enable for 50ns glitch filter on SCL input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 0
4	SDA_IN_FILT_SEL	Enable for 50ns glitch filter on SDA input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 3

25.1.173 SCB2_TX_CTRL

Transmitter control register.

Address: 0x40260200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

25.1.174 SCB2_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x40260204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

25.1.175 SCB2_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x40260208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

25.1.176 SCB2_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x40260240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

25.1.177 SCB2_RX_CTRL

Receiver control register.

Address: 0x40260300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

25.1.178 SCB2_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x40260304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

25.1.179 SCB2_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x40260308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

25.1.180 SCB2_RX_MATCH

Slave address and mask register.

Address: 0x40260310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the slave address bits take part in the matching. MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

25.1.181 SCB2_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x40260340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. When this register is read through the debugger, the data frame will not be removed from the FIFO. Similar in operation to RX_FIFO_RD_SILENT Default Value: Undefined

25.1.182 SCB2_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x40260344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.BYTE_-MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

25.1.183 SCB2_EZ_DATA0

Memory buffer registers.

Address: 0x40260400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.184 SCB2_EZ_DATA1

Memory buffer registers.

Address: 0x40260404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.185 SCB2_EZ_DATA2

Memory buffer registers.

Address: 0x40260408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.186 SCB2_EZ_DATA3

Memory buffer registers.

Address: 0x4026040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.187 SCB2_EZ_DATA4

Memory buffer registers.

Address: 0x40260410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.188 SCB2_EZ_DATA5

Memory buffer registers.

Address: 0x40260414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.189 SCB2_EZ_DATA6

Memory buffer registers.

Address: 0x40260418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.190 SCB2_EZ_DATA7

Memory buffer registers.

Address: 0x4026041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.191 SCB2_EZ_DATA8

Memory buffer registers.

Address: 0x40260420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.192 SCB2_EZ_DATA9

Memory buffer registers.

Address: 0x40260424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.193 SCB2_EZ_DATA10

Memory buffer registers.

Address: 0x40260428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.194 SCB2_EZ_DATA11

Memory buffer registers.

Address: 0x4026042C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.195 SCB2_EZ_DATA12

Memory buffer registers.

Address: 0x40260430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.196 SCB2_EZ_DATA13

Memory buffer registers.

Address: 0x40260434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.197 SCB2_EZ_DATA14

Memory buffer registers.

Address: 0x40260438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.198 SCB2_EZ_DATA15

Memory buffer registers.

Address: 0x4026043C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.199 SCB2_EZ_DATA16

Memory buffer registers.

Address: 0x40260440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.200 SCB2_EZ_DATA17

Memory buffer registers.

Address: 0x40260444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.201 SCB2_EZ_DATA18

Memory buffer registers.

Address: 0x40260448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.202 SCB2_EZ_DATA19

Memory buffer registers.

Address: 0x4026044C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.203 SCB2_EZ_DATA20

Memory buffer registers.

Address: 0x40260450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.204 SCB2_EZ_DATA21

Memory buffer registers.

Address: 0x40260454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.205 SCB2_EZ_DATA22

Memory buffer registers.

Address: 0x40260458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.206 SCB2_EZ_DATA23

Memory buffer registers.

Address: 0x4026045C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.207 SCB2_EZ_DATA24

Memory buffer registers.

Address: 0x40260460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.208 SCB2_EZ_DATA25

Memory buffer registers.

Address: 0x40260464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.209 SCB2_EZ_DATA26

Memory buffer registers.

Address: 0x40260468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.210 SCB2_EZ_DATA27

Memory buffer registers.

Address: 0x4026046C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.211 SCB2_EZ_DATA28

Memory buffer registers.

Address: 0x40260470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.212 SCB2_EZ_DATA29

Memory buffer registers.

Address: 0x40260474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.213 SCB2_EZ_DATA30

Memory buffer registers.

Address: 0x40260478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.214 SCB2_EZ_DATA31

Memory buffer registers.

Address: 0x4026047C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.215 SCB2_INTR_CAUSE

Active clocked interrupt signal register

Address: 0x40260E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

25.1.216 SCB2_INTR_I2C_EC

Externally clocked I2C interrupt request register

Address: 0x40260E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0

(continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

25.1.217 SCB2_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask register

Address: 0x40260E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.218 SCB2_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40260E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

25.1.219 SCB2_INTR_SPI_EC

Externally clocked SPI interrupt request register

Address: 0x40260EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when CTRL.EC_OP_MODE is '1'. Default Value: 0

(continued)

0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

25.1.220 SCB2_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask register

Address: 0x40260EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.221 SCB2_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40260ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

25.1.222 SCB2_INTR_M

Master interrupt request register.

Address: 0x40260F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0
0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

25.1.223 SCB2_INTR_M_SET

Master interrupt set request register

Address: 0x40260F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.224 SCB2_INTR_M_MASK

Master interrupt mask register.

Address: 0x40260F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.225 SCB2_INTR_M_MASKED

Master interrupt masked request register

Address: 0x40260F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

25.1.226 SCB2_INTR_S

Slave interrupt request register.

Address: 0x40260F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

(continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

25.1.227 SCB2_INTR_S_SET

Slave interrupt set request register.

Address: 0x40260F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.228 SCB2_INTR_S_MASK

Slave interrupt mask register.

Address: 0x40260F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.229 SCB2_INTR_S_MASKED

Slave interrupt masked request register

Address: 0x40260F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

25.1.230 SCB2_INTR_TX

Transmitter interrupt request register.

Address: 0x40260F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

(continued)

6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.BYTE_MODE: BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode. Default Value: 0

25.1.231 SCB2_INTR_TX_SET

Transmitter interrupt set request register

Address: 0x40260F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.232 SCB2_INTR_TX_MASK

Transmitter interrupt mask register.

Address: 0x40260F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.233 SCB2_INTR_TX_MASKED

Transmitter interrupt masked request register

Address: 0x40260F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

25.1.234 SCB2_INTR_RX

Receiver interrupt request register.

Address: 0x40260FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is ecpected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STA-TUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guaran-tee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

(continued)

9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_-FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODET: BYTE_MODE is '0': # entries == FF_DATA_NR/2. BYTE_MODE is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FI-FO_CTL. Only used in FIFO mode. Default Value: 0

25.1.235 SCB2_INTR_RX_SET

Receiver interrupt set request register.

Address: 0x40260FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

(continued)

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.236 SCB2_INTR_RX_MASK

Receiver interrupt mask register.

Address: 0x40260FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.237 SCB2_INTR_RX_MASKED

Receiver interrupt masked request register

Address: 0x40260FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

25.1.238 SCB3_CTRL

Generic control register.

Address: 0x40270000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BYTE_-MODE	EZ_MODE	EC_OP_-MODE	EC_AM_-MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_AC-CEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL register to enable SCB, select the specific operation mode and oversampling factor. When this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3

(continued)

		0x0: I2C: Inter-Integrated Circuits (I2C) mode. **0x1: SPI:** Serial Peripheral Interface (SPI) mode. **0x2: UART:** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the internal CPU accesses to EZ memory coincide/collide, this bit determines whether the CPU access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is 0 and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: INTR_TX.BLOCKED and INTR_RX.BLOCKED. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not seperated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	EC_OP_MODE	This field specifies the clocking for the SCB block '0': Internally clocked mode '1': externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0

(continued)

8	EC_AM_MODE	This field specifies the clocking for the address matching (I2C) or slave selection detection logic (SPI) '0': Internally clocked mode '1': Externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0

(continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. OVS + 1 SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps. As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. SCB clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. SCB clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. SCB clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. SCB clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. SCB clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. SCB clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

25.1.239 SCB3_STATUS

Generic status register.

Address: 0x40270004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

25.1.240 SCB3_SPI_CTRL

SPI control register.

Address: 0x40270020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_-CONTINU-OUS	LATE_MISO_SAMPLE	CPOL	CPHA	SE-LECT_PRE-CEDE	CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_PO-LARITY3	SSEL_PO-LARITY2	SSEL_PO-LARITY1	SSEL_PO-LARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_-MODE	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SLAVE_SELECT	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. SCB block should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

(continued)

		0x0: SPI_MOTOROLA: SPI Motorola submode. In master mode, when not transmitting data (Slave SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive. **0x1: SPI_TI:** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS:** SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': No local loopback '1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loop-back mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode). Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode). Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode). Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). only SPI_SELECT[0] is used in slave mode. For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Istruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0

(continued)

4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0
3	CPOL	Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is 0: SCLK is 0 when not transmitting data. - CPOL is 1: SCLK is 1 when not transmitting data. Default Value: 0
2	CPHA	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is 0, CPHA is 0: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is 0, CPHA is 1: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is 1, CPHA is 0: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is 1, CPHA is 1: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily seperated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always seperated by slave deselection: independent of the availability of TX FIFO data frames, data frames are sent out with slave deselection. Default Value: 0

25.1.241 SCB3_SPI_STATUS

SPI status register.

Address: 0x40270024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

25.1.242 SCB3_UART_CTRL

UART control register.

Address: 0x40270040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD:** Standard UART submode. **0x1: UART_SMARTCARD:** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA:** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS should be set to 15.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). 0: Loopback is not enabled 1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS. This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

25.1.243 SCB3_UART_TX_CTRL

UART transmitter control register.

Address: 0x40270044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

25.1.244 SCB3_UART_RX_CTRL

UART receiver control register.

Address: 0x40270048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

(continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behaviour when a parity check fails. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

(continued)

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value. Default Value: 2

25.1.245 SCB3_UART_RX_STATUS

UART receiver status register.

Address: 0x4027004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

25.1.246 SCB3_UART_FLOW_CTRL

UART flow control register

Address: 0x40270050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal by the UART transmitter: '0': Disabled. The UART transmitter ignores the CTS input signal and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses CTS input signal to qualify the transmission of data. It transmits when CTS input signal is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', the CTS input signal is driven by the RTS output signal locally in SCB (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal '0': CTS is active low ; '1': CTS is active high; Default Value: 0

(continued)

16	RTS_POLARITY	Polarity of the RTS output signal: '0': RTS is active low; '1': RTS is active high; During SCB reset (Hibernate system power mode), RTS output signal is '1'. This represents an inactive state assuming an active low polarity. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal is activated. By setting this field to "0", flow control is effectively disabled (may be useful for debug purposes). Default Value: 0

25.1.247 SCB3_I2C_CTRL

I2C control register.

Address: 0x40270060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_RE ADY_- DATA_NAC K	S_NOT_RE ADY_AD- DR_NACK	S_READY_ DATA_ACK	S_READY_ ADDR_ACK	S_GENER- AL_IGNOR E	None	M_NOT_RE ADY_- DATA_NAC K	M_READY_ DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_- MODE	SLAVE_- MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', no loopback When '1', loopback is enabled internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0

(continued)

15	S_NOT_READY_-DATA_NACK	Only used when: - non EZ mode Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1
14	S_NOT_READY_AD-DR_NACK	This field is used during an address match or general call address in internally clocked mode Only used when: - EC_AM_MODE is '0', EC_OP_MODE is '0', S_GENERAL_IGNORE is '0] and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the SCB clock is available (in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2).SCB clock is not present (in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the SCB clock is available). The logic will handle the ongoing transfer as soon as the clock is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_-DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1

(continued)

7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 SCB clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular (no stretching) interface (IF) low time to guarantee functionally correct behavior. With input signal median filtering, the IF low time should be >= 8 SCB clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 SCB clock cycles and <= 16 SCB clock cycles. Default Value: 8
3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 SCB clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 SCB clock cycles and <= 16 SCB clock cycles. Without input signal median filtering, the IF high time should be >= 5 SCB clock cycles and <= 16 SCB clock cycles. Default Value: 8

25.1.248 SCB3_I2C_STATUS

I2C status register.

Address: 0x40270064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". Default Value: 0

(continued)

1	I2C_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

25.1.249 SCB3_I2C_M_CMD

I2C master command register.

Address: 0x40270068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0

(continued)

1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0
0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

25.1.250 SCB3_I2C_S_CMD

I2C slave command register.

Address: 0x4027006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

25.1.251 SCB3_I2C_CFG

I2C configuration register.

Address: 0x40270070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_-FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_-FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative filter delay on SDA output to meet tHD_DAT parameter "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2

(continued)

12	SCL_IN_FILT_SEL	Enable for 50ns glitch filter on SCL input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 0
4	SDA_IN_FILT_SEL	Enable for 50ns glitch filter on SDA input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 3

25.1.252 SCB3_TX_CTRL

Transmitter control register.

Address: 0x40270200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

25.1.253 SCB3_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x40270204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

25.1.254 SCB3_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x40270208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

25.1.255 SCB3_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x40270240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

25.1.256 SCB3_RX_CTRL

Receiver control register.

Address: 0x40270300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

25.1.257 SCB3_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x40270304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

25.1.258 SCB3_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x40270308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

25.1.259 SCB3_RX_MATCH

Slave address and mask register.

Address: 0x40270310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the slave address bits take part in the matching. MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

25.1.260 SCB3_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x40270340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. When this register is read through the debugger, the data frame will not be removed from the FIFO. Similar in operation to RX_FIFO_RD_SILENT Default Value: Undefined

25.1.261 SCB3_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x40270344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.BYTE_-MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

25.1.262 SCB3_EZ_DATA0

Memory buffer registers.

Address: 0x40270400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.263 SCB3_EZ_DATA1

Memory buffer registers.

Address: 0x40270404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.264 SCB3_EZ_DATA2

Memory buffer registers.

Address: 0x40270408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.265 SCB3_EZ_DATA3

Memory buffer registers.

Address: 0x4027040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.266 SCB3_EZ_DATA4

Memory buffer registers.

Address: 0x40270410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.267 SCB3_EZ_DATA5

Memory buffer registers.

Address: 0x40270414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.268 SCB3_EZ_DATA6

Memory buffer registers.

Address: 0x40270418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.269 SCB3_EZ_DATA7

Memory buffer registers.

Address: 0x4027041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.270 SCB3_EZ_DATA8

Memory buffer registers.

Address: 0x40270420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.271 SCB3_EZ_DATA9

Memory buffer registers.

Address: 0x40270424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.272 SCB3_EZ_DATA10

Memory buffer registers.

Address: 0x40270428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.273 SCB3_EZ_DATA11

Memory buffer registers.

Address: 0x4027042C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.274 SCB3_EZ_DATA12

Memory buffer registers.

Address: 0x40270430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.275 SCB3_EZ_DATA13

Memory buffer registers.

Address: 0x40270434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.276 SCB3_EZ_DATA14

Memory buffer registers.

Address: 0x40270438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.277 SCB3_EZ_DATA15

Memory buffer registers.

Address: 0x4027043C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.278 SCB3_EZ_DATA16

Memory buffer registers.

Address: 0x40270440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.279 SCB3_EZ_DATA17

Memory buffer registers.

Address: 0x40270444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.280 SCB3_EZ_DATA18

Memory buffer registers.

Address: 0x40270448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.281 SCB3_EZ_DATA19

Memory buffer registers.

Address: 0x4027044C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.282 SCB3_EZ_DATA20

Memory buffer registers.

Address: 0x40270450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.283 SCB3_EZ_DATA21

Memory buffer registers.

Address: 0x40270454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.284 SCB3_EZ_DATA22

Memory buffer registers.

Address: 0x40270458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.285 SCB3_EZ_DATA23

Memory buffer registers.

Address: 0x4027045C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.286 SCB3_EZ_DATA24

Memory buffer registers.

Address: 0x40270460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.287 SCB3_EZ_DATA25

Memory buffer registers.

Address: 0x40270464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.288 SCB3_EZ_DATA26

Memory buffer registers.

Address: 0x40270468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.289 SCB3_EZ_DATA27

Memory buffer registers.

Address: 0x4027046C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.290 SCB3_EZ_DATA28

Memory buffer registers.

Address: 0x40270470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.291 SCB3_EZ_DATA29

Memory buffer registers.

Address: 0x40270474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.292 SCB3_EZ_DATA30

Memory buffer registers.

Address: 0x40270478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.293 SCB3_EZ_DATA31

Memory buffer registers.

Address: 0x4027047C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.294 SCB3_INTR_CAUSE

Active clocked interrupt signal register

Address: 0x40270E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

25.1.295 SCB3_INTR_I2C_EC

Externally clocked I2C interrupt request register

Address: 0x40270E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0

(continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

25.1.296 SCB3_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask register

Address: 0x40270E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.297 SCB3_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40270E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

25.1.298 SCB3_INTR_SPI_EC

Externally clocked SPI interrupt request register

Address: 0x40270EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when CTRL.EC_OP_MODE is '1'. Default Value: 0

(continued)

0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

25.1.299 SCB3_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask register

Address: 0x40270EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.300 SCB3_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40270ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

25.1.301 SCB3_INTR_M

Master interrupt request register.

Address: 0x40270F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0
0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

25.1.302 SCB3_INTR_M_SET

Master interrupt set request register

Address: 0x40270F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.303 SCB3_INTR_M_MASK

Master interrupt mask register.

Address: 0x40270F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.304 SCB3_INTR_M_MASKED

Master interrupt masked request register

Address: 0x40270F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

25.1.305 SCB3_INTR_S

Slave interrupt request register.

Address: 0x40270F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

(continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

25.1.306 SCB3_INTR_S_SET

Slave interrupt set request register.

Address: 0x40270F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.307 SCB3_INTR_S_MASK

Slave interrupt mask register.

Address: 0x40270F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.308 SCB3_INTR_S_MASKED

Slave interrupt masked request register

Address: 0x40270F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

25.1.309 SCB3_INTR_TX

Transmitter interrupt request register.

Address: 0x40270F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

(continued)

6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.BYTE_MODE: BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode. Default Value: 0

25.1.310 SCB3_INTR_TX_SET

Transmitter interrupt set request register

Address: 0x40270F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.311 SCB3_INTR_TX_MASK

Transmitter interrupt mask register.

Address: 0x40270F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.312 SCB3_INTR_TX_MASKED

Transmitter interrupt masked request register

Address: 0x40270F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

25.1.313 SCB3_INTR_RX

Receiver interrupt request register.

Address: 0x40270FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is ecpected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STA-TUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guaran-tee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

(continued)

9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_-FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODET: BYTE_MODE is '0': # entries == FF_DATA_NR/2. BYTE_MODE is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FI-FO_CTL. Only used in FIFO mode. Default Value: 0

25.1.314 SCB3_INTR_RX_SET

Receiver interrupt set request register.

Address: 0x40270FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

(continued)

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.315 SCB3_INTR_RX_MASK

Receiver interrupt mask register.

Address: 0x40270FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.316 SCB3_INTR_RX_MASKED

Receiver interrupt masked request register

Address: 0x40270FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

25.1.317 SCB4_CTRL

Generic control register.

Address: 0x40280000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BYTE_-MODE	EZ_MODE	EC_OP_-MODE	EC_AM_-MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_AC-CEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL register to enable SCB, select the specific operation mode and oversampling factor. When this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3

(continued)

		0x0: I2C: Inter-Integrated Circuits (I2C) mode. **0x1: SPI:** Serial Peripheral Interface (SPI) mode. **0x2: UART:** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the internal CPU accesses to EZ memory coincide/collide, this bit determines whether the CPU access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is 0 and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: INTR_TX.BLOCKED and INTR_RX.BLOCKED. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not seperated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	EC_OP_MODE	This field specifies the clocking for the SCB block '0': Internally clocked mode '1': externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0

(continued)

8	EC_AM_MODE	This field specifies the clocking for the address matching (I2C) or slave selection detection logic (SPI) '0': Internally clocked mode '1': Externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0

(continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. OVS + 1 SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps. As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. SCB clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. SCB clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. SCB clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. SCB clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. SCB clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. SCB clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

25.1.318 SCB4_STATUS

Generic status register.

Address: 0x40280004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

25.1.319 SCB4_SPI_CTRL

SPI control register.

Address: 0x40280020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_-CONTINU-OUS	LATE_MISO_SAMPLE	CPOL	CPHA	SE-LECT_PRE-CEDE	CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_PO-LARITY3	SSEL_PO-LARITY2	SSEL_PO-LARITY1	SSEL_PO-LARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_-MODE	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SLAVE_SELECT	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. SCB block should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

(continued)

		0x0: SPI_MOTOROLA: SPI Motorola submode. In master mode, when not transmitting data (Slave SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive. **0x1: SPI_TI:** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS:** SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': No local loopback '1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loop-back mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode). Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode). Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode). Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). only SPI_SELECT[0] is used in slave mode. For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Istruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0

(continued)

4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0
3	CPOL	Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is 0: SCLK is 0 when not transmitting data. - CPOL is 1: SCLK is 1 when not transmitting data. Default Value: 0
2	CPHA	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is 0, CPHA is 0: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is 0, CPHA is 1: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is 1, CPHA is 0: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is 1, CPHA is 1: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily seperated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always seperated by slave deselection: independent of the availability of TX FIFO data frames, data frames are sent out with slave deselection. Default Value: 0

25.1.320 SCB4_SPI_STATUS

SPI status register.

Address: 0x40280024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

25.1.321 SCB4_UART_CTRL

UART control register.

Address: 0x40280040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD:** Standard UART submode. **0x1: UART_SMARTCARD:** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA:** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS should be set to 15.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). 0: Loopback is not enabled 1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS. This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

25.1.322 SCB4_UART_TX_CTRL

UART transmitter control register.

Address: 0x40280044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

25.1.323 SCB4_UART_RX_CTRL

UART receiver control register.

Address: 0x40280048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

(continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behaviour when a parity check fails. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

(continued)

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value. Default Value: 2

25.1.324 SCB4_UART_RX_STATUS

UART receiver status register.

Address: 0x4028004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

25.1.325 SCB4_UART_FLOW_CTRL

UART flow control register

Address: 0x40280050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal by the UART transmitter: '0': Disabled. The UART transmitter ignores the CTS input signal and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses CTS input signal to qualify the transmission of data. It transmits when CTS input signal is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', the CTS input signal is driven by the RTS output signal locally in SCB (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal '0': CTS is active low ; '1': CTS is active high; Default Value: 0

(continued)

16	RTS_POLARITY	Polarity of the RTS output signal: '0': RTS is active low; '1': RTS is active high; During SCB reset (Hibernate system power mode), RTS output signal is '1'. This represents an inactive state assuming an active low polarity. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal is activated. By setting this field to "0", flow control is effectively disabled (may be useful for debug purposes). Default Value: 0

25.1.326 SCB4_I2C_CTRL

I2C control register.

Address: 0x40280060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_-DATA_NACK	S_NOT_READY_AD-DR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENER-AL_IGNORE	None	M_NOT_READY_-DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_-MODE	SLAVE_-MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', no loopback When '1', loopback is enabled internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0

(continued)

15	S_NOT_READY_-DATA_NACK	Only used when: - non EZ mode Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1
14	S_NOT_READY_AD-DR_NACK	This field is used during an address match or general call address in internally clocked mode Only used when: - EC_AM_MODE is '0', EC_OP_MODE is '0', S_GENERAL_IGNORE is '0] and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the SCB clock is available (in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2).SCB clock is not present (in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the SCB clock is available). The logic will handle the ongoing transfer as soon as the clock is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_-DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1

(continued)

7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 SCB clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular (no stretching) interface (IF) low time to guarantee functionally correct behavior. With input signal median filtering, the IF low time should be >= 8 SCB clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 SCB clock cycles and <= 16 SCB clock cycles. Default Value: 8
3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 SCB clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 SCB clock cycles and <= 16 SCB clock cycles. Without input signal median filtering, the IF high time should be >= 5 SCB clock cycles and <= 16 SCB clock cycles. Default Value: 8

25.1.327 SCB4_I2C_STATUS

I2C status register.

Address: 0x40280064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". Default Value: 0

(continued)

1	I2C_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

25.1.328 SCB4_I2C_M_CMD

I2C master command register.

Address: 0x40280068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0

(continued)

1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0
0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

25.1.329 SCB4_I2C_S_CMD

I2C slave command register.

Address: 0x4028006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

25.1.330 SCB4_I2C_CFG

I2C configuration register.

Address: 0x40280070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_-FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_-FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative filter delay on SDA output to meet tHD_DAT parameter "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim settings for the 50ns delay filter on SDA output used to gurantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2

(continued)

12	SCL_IN_FILT_SEL	Enable for 50ns glitch filter on SCL input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 0
4	SDA_IN_FILT_SEL	Enable for 50ns glitch filter on SDA input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 3

25.1.331 SCB4_TX_CTRL

Transmitter control register.

Address: 0x40280200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

25.1.332 SCB4_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x40280204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

25.1.333 SCB4_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x40280208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

25.1.334 SCB4_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x40280240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

25.1.335 SCB4_RX_CTRL

Receiver control register.

Address: 0x40280300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

25.1.336 SCB4_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x40280304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

25.1.337 SCB4_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x40280308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

25.1.338 SCB4_RX_MATCH

Slave address and mask register.

Address: 0x40280310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the slave address bits take part in the matching. MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

25.1.339 SCB4_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x40280340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. When this register is read through the debugger, the data frame will not be removed from the FIFO. Similar in operation to RX_FIFO_RD_SILENT Default Value: Undefined

25.1.340 SCB4_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x40280344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.BYTE_-MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

25.1.341 SCB4_EZ_DATA0

Memory buffer registers.

Address: 0x40280400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.342 SCB4_EZ_DATA1

Memory buffer registers.

Address: 0x40280404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.343 SCB4_EZ_DATA2

Memory buffer registers.

Address: 0x40280408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.344 SCB4_EZ_DATA3

Memory buffer registers.

Address: 0x4028040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.345 SCB4_EZ_DATA4

Memory buffer registers.

Address: 0x40280410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.346 SCB4_EZ_DATA5

Memory buffer registers.

Address: 0x40280414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.347 SCB4_EZ_DATA6

Memory buffer registers.

Address: 0x40280418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.348 SCB4_EZ_DATA7

Memory buffer registers.

Address: 0x4028041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.349 SCB4_EZ_DATA8

Memory buffer registers.

Address: 0x40280420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.350 SCB4_EZ_DATA9

Memory buffer registers.

Address: 0x40280424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.351 SCB4_EZ_DATA10

Memory buffer registers.

Address: 0x40280428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.352 SCB4_EZ_DATA11

Memory buffer registers.

Address: 0x4028042C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.353 SCB4_EZ_DATA12

Memory buffer registers.

Address: 0x40280430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.354 SCB4_EZ_DATA13

Memory buffer registers.

Address: 0x40280434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.355 SCB4_EZ_DATA14

Memory buffer registers.

Address: 0x40280438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.356 SCB4_EZ_DATA15

Memory buffer registers.

Address: 0x4028043C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.357 SCB4_EZ_DATA16

Memory buffer registers.

Address: 0x40280440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.358 SCB4_EZ_DATA17

Memory buffer registers.

Address: 0x40280444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.359 SCB4_EZ_DATA18

Memory buffer registers.

Address: 0x40280448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.360 SCB4_EZ_DATA19

Memory buffer registers.

Address: 0x4028044C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.361 SCB4_EZ_DATA20

Memory buffer registers.

Address: 0x40280450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.362 SCB4_EZ_DATA21

Memory buffer registers.

Address: 0x40280454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.363 SCB4_EZ_DATA22

Memory buffer registers.

Address: 0x40280458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.364 SCB4_EZ_DATA23

Memory buffer registers.

Address: 0x4028045C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.365 SCB4_EZ_DATA24

Memory buffer registers.

Address: 0x40280460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.366 SCB4_EZ_DATA25

Memory buffer registers.

Address: 0x40280464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.367 SCB4_EZ_DATA26

Memory buffer registers.

Address: 0x40280468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.368 SCB4_EZ_DATA27

Memory buffer registers.

Address: 0x4028046C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.369 SCB4_EZ_DATA28

Memory buffer registers.

Address: 0x40280470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.370 SCB4_EZ_DATA29

Memory buffer registers.

Address: 0x40280474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.371 SCB4_EZ_DATA30

Memory buffer registers.

Address: 0x40280478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.372 SCB4_EZ_DATA31

Memory buffer registers.

Address: 0x4028047C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

25.1.373 SCB4_INTR_CAUSE

Active clocked interrupt signal register

Address: 0x40280E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

25.1.374 SCB4_INTR_I2C_EC

Externally clocked I2C interrupt request register

Address: 0x40280E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0

(continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

25.1.375 SCB4_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask register

Address: 0x40280E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.376 SCB4_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40280E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

25.1.377 SCB4_INTR_SPI_EC

Externally clocked SPI interrupt request register

Address: 0x40280EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when CTRL.EC_OP_MODE is '1'. Default Value: 0

(continued)

0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

25.1.378 SCB4_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask register

Address: 0x40280EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.379 SCB4_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40280ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

25.1.380 SCB4_INTR_M

Master interrupt request register.

Address: 0x40280F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0
0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

25.1.381 SCB4_INTR_M_SET

Master interrupt set request register

Address: 0x40280F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.382 SCB4_INTR_M_MASK

Master interrupt mask register.

Address: 0x40280F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.383 SCB4_INTR_M_MASKED

Master interrupt masked request register

Address: 0x40280F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

25.1.384 SCB4_INTR_S

Slave interrupt request register.

Address: 0x40280F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

(continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

25.1.385 SCB4_INTR_S_SET

Slave interrupt set request register.

Address: 0x40280F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.386 SCB4_INTR_S_MASK

Slave interrupt mask register.

Address: 0x40280F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.387 SCB4_INTR_S_MASKED

Slave interrupt masked request register

Address: 0x40280F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

25.1.388 SCB4_INTR_TX

Transmitter interrupt request register.

Address: 0x40280F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

(continued)

6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.BYTE_MODE: BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode. Default Value: 0

25.1.389 SCB4_INTR_TX_SET

Transmitter interrupt set request register

Address: 0x40280F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.390 SCB4_INTR_TX_MASK

Transmitter interrupt mask register.

Address: 0x40280F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.391 SCB4_INTR_TX_MASKED

Transmitter interrupt masked request register

Address: 0x40280F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

25.1.392 SCB4_INTR_RX

Receiver interrupt request register.

Address: 0x40280FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is ecpected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STA-TUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guaran-tee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

(continued)

9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_-FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODET: BYTE_MODE is '0': # entries == FF_DATA_NR/2. BYTE_MODE is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FI-FO_CTL. Only used in FIFO mode. Default Value: 0

25.1.393 SCB4_INTR_RX_SET

Receiver interrupt set request register.

Address: 0x40280FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

(continued)

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.394 SCB4_INTR_RX_MASK

Receiver interrupt mask register.

Address: 0x40280FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.395 SCB4_INTR_RX_MASKED

Receiver interrupt masked request register

Address: 0x40280FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

26 Supervisory Flash Registers

This section discusses the Supervisory Flash (SFLASH) registers. It lists all the registers in mapping tables, in address order.

26.1 Register Details

Register Name	Address
SFLASH_SILICON_ID	0x0FFFF244
SFLASH_HIB_KEY_DELAY	0x0FFFF250
SFLASH_DPSLP_KEY_DELAY	0x0FFFF252
SFLASH_SWD_CONFIG	0x0FFFF254
SFLASH_SWD_LISTEN	0x0FFFF258
SFLASH_FLASH_START	0x0FFFF25C
SFLASH_CSDV2_CSD0_ADC_TRIM1	0x0FFFF260
SFLASH_CSDV2_CSD0_ADC_TRIM2	0x0FFFF261
SFLASH_SAR_TEMP_MULTIPLIER	0x0FFFF264
SFLASH_SAR_TEMP_OFFSET	0x0FFFF266
SFLASH_IMO_TRIM_USBMODE_24	0x0FFFF33E
SFLASH_IMO_TRIM_USBMODE_48	0x0FFFF33F
SFLASH_IMO_TCTRIM_LT0	0x0FFFF34C
SFLASH_IMO_TCTRIM_LT1	0x0FFFF34D
SFLASH_IMO_TCTRIM_LT2	0x0FFFF34E
SFLASH_IMO_TCTRIM_LT3	0x0FFFF34F
SFLASH_IMO_TCTRIM_LT4	0x0FFFF350
SFLASH_IMO_TCTRIM_LT5	0x0FFFF351
SFLASH_IMO_TCTRIM_LT6	0x0FFFF352
SFLASH_IMO_TCTRIM_LT7	0x0FFFF353
SFLASH_IMO_TCTRIM_LT8	0x0FFFF354
SFLASH_IMO_TCTRIM_LT9	0x0FFFF355
SFLASH_IMO_TCTRIM_LT10	0x0FFFF356
SFLASH_IMO_TCTRIM_LT11	0x0FFFF357
SFLASH_IMO_TCTRIM_LT12	0x0FFFF358
SFLASH_IMO_TCTRIM_LT13	0x0FFFF359
SFLASH_IMO_TCTRIM_LT14	0x0FFFF35A

Register Name	Address
SFLASH_IMO_TCTRIM_LT15	0x0FFFF35B
SFLASH_IMO_TCTRIM_LT16	0x0FFFF35C
SFLASH_IMO_TCTRIM_LT17	0x0FFFF35D
SFLASH_IMO_TCTRIM_LT18	0x0FFFF35E
SFLASH_IMO_TCTRIM_LT19	0x0FFFF35F
SFLASH_IMO_TCTRIM_LT20	0x0FFFF360
SFLASH_IMO_TCTRIM_LT21	0x0FFFF361
SFLASH_IMO_TCTRIM_LT22	0x0FFFF362
SFLASH_IMO_TCTRIM_LT23	0x0FFFF363
SFLASH_IMO_TCTRIM_LT24	0x0FFFF364
SFLASH_IMO_TRIM_LT0	0x0FFFF365
SFLASH_IMO_TRIM_LT1	0x0FFFF366
SFLASH_IMO_TRIM_LT2	0x0FFFF367
SFLASH_IMO_TRIM_LT3	0x0FFFF368
SFLASH_IMO_TRIM_LT4	0x0FFFF369
SFLASH_IMO_TRIM_LT5	0x0FFFF36A
SFLASH_IMO_TRIM_LT6	0x0FFFF36B
SFLASH_IMO_TRIM_LT7	0x0FFFF36C
SFLASH_IMO_TRIM_LT8	0x0FFFF36D
SFLASH_IMO_TRIM_LT9	0x0FFFF36E
SFLASH_IMO_TRIM_LT10	0x0FFFF36F
SFLASH_IMO_TRIM_LT11	0x0FFFF370
SFLASH_IMO_TRIM_LT12	0x0FFFF371
SFLASH_IMO_TRIM_LT13	0x0FFFF372
SFLASH_IMO_TRIM_LT14	0x0FFFF373
SFLASH_IMO_TRIM_LT15	0x0FFFF374
SFLASH_IMO_TRIM_LT16	0x0FFFF375
SFLASH_IMO_TRIM_LT17	0x0FFFF376
SFLASH_IMO_TRIM_LT18	0x0FFFF377
SFLASH_IMO_TRIM_LT19	0x0FFFF378
SFLASH_IMO_TRIM_LT20	0x0FFFF379
SFLASH_IMO_TRIM_LT21	0x0FFFF37A
SFLASH_IMO_TRIM_LT22	0x0FFFF37B
SFLASH_IMO_TRIM_LT23	0x0FFFF37C
SFLASH_IMO_TRIM_LT24	0x0FFFF37D

26.1.1 SFLASH_SILICON_ID

Silicon ID

Address: 0x0FFFF244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ID	Silicon ID Default Value: X

26.1.2 SFLASH_HIB_KEY_DELAY

Hibernate wakeup value for PWR_KEY_DELAY

Address: 0x0FFFF250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

26.1.3 SFLASH_DPSLP_KEY_DELAY

DeepSleep wakeup value for PWR_KEY_DELAY

Address: 0x0FFFF252

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

26.1.4 SFLASH_SWD_CONFIG

SWD pinout selector (not present in TSG4/TSG5-M)

Address: 0x0FFFF254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							None
Name	None [7:1]							SWD_SE-LECT

Bits	Name	Description
0	SWD_SELECT	0: Use Primary SWD location 1: Use Alternate SWD location Default Value: X

26.1.5 SFLASH_SWD_LISTEN

Listen Window Length

Address: 0x0FFFF258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	CYCLES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	CYCLES [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	CYCLES [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	CYCLES [31:24]							

Bits	Name	Description
31 : 0	CYCLES	Number of clock cycles Default Value: X

26.1.6 SFLASH_FLASH_START

Flash Image Start Address

Address: 0x0FFFF25C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	ADDRESS [31:24]							

Bits	Name	Description
31 : 0	ADDRESS	Start Address Default Value: X

26.1.7 SFLASH_CSDV2_CSD0_ADC_TRIM1

CSDV2 CSD0 ADC TRIM 1

Address: 0x0FFFF260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	CSD_ADC_CAL_LSB [7:0]							

Bits	Name	Description
7 : 0	CSD_ADC_CAL_LSB	Low byte of CSDv2 Calibration Default Value: X

26.1.8 SFLASH_CSDV2_CSD0_ADC_TRIM2

CSDV2 CSD0 ADC TRIM2

Address: 0x0FFFF261

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	CSD_ADC_CAL_MSB [7:0]							

Bits	Name	Description
7 : 0	CSD_ADC_CAL_MSB	High byte of CSDv2 Calibration Default Value: X

26.1.9 SFLASH_SAR_TEMP_MULTIPLIER

SAR Temperature Sensor Multiplication Factor

Address: 0x0FFFF264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TEMP_MULTIPLIER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	TEMP_MULTIPLIER [15:8]							

Bits	Name	Description
15 : 0	TEMP_MULTIPLIER	Multiplier value for SAR temperature sensor in fixed point 0.16 format. Note: this field exists in products that contain SAR (m0s8sar) only. Default Value: X

26.1.10 SFLASH_SAR_TEMP_OFFSET

SAR Temperature Sensor Offset

Address: 0x0FFFF266

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TEMP_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	TEMP_OFFSET [15:8]							

Bits	Name	Description
15 : 0	TEMP_OFFSET	Offset value for SAR temperature sensor in fixed point 10.6 format. Note: this field exists in products that contain SAR (m0s8sar) only. Default Value: X

26.1.11 SFLASH_IMO_TRIM_USBMODE_24

USB IMO TRIM 24MHz

Address: 0x0FFFF33E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM_24 [7:0]							

Bits	Name	Description
7 : 0	TRIM_24	TRIM value for IMO with USB at 24MHz Default Value: X

26.1.12 SFLASH_IMO_TRIM_USBMODE_48

USB IMO TRIM 48MHz

Address: 0x0FFFF33F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM_24 [7:0]							

Bits	Name	Description
7 : 0	TRIM_24	TRIM value for IMO with USB at 24MHz Default Value: X

26.1.13 SFLASH_IMO_TCTRIM_LT0

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF34C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.14 SFLASH_IMO_TCTRIM_LT1

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF34D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.15 SFLASH_IMO_TCTRIM_LT2

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF34E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.16 SFLASH_IMO_TCTRIM_LT3

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF34F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.17 SFLASH_IMO_TCTRIM_LT4

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF350

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.18 SFLASH_IMO_TCTRIM_LT5

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF351

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.19 SFLASH_IMO_TCTRIM_LT6

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF352

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.20 SFLASH_IMO_TCTRIM_LT7

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF353

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.21 SFLASH_IMO_TCTRIM_LT8

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF354

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.22 SFLASH_IMO_TCTRIM_LT9

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF355

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.23 SFLASH_IMO_TCTRIM_LT10

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF356

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.24 SFLASH_IMO_TCTRIM_LT11

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF357

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.25 SFLASH_IMO_TCTRIM_LT12

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF358

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.26 SFLASH_IMO_TCTRIM_LT13

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF359

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.27 SFLASH_IMO_TCTRIM_LT14

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF35A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.28 SFLASH_IMO_TCTRIM_LT15

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF35B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.29 SFLASH_IMO_TCTRIM_LT16

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF35C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.30 SFLASH_IMO_TCTRIM_LT17

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF35D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.31 SFLASH_IMO_TCTRIM_LT18

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF35E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.32 SFLASH_IMO_TCTRIM_LT19

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF35F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.33 SFLASH_IMO_TCTRIM_LT20

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.34 SFLASH_IMO_TCTRIM_LT21

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF361

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.35 SFLASH_IMO_TCTRIM_LT22

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF362

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.36 SFLASH_IMO_TCTRIM_LT23

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF363

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.37 SFLASH_IMO_TCTRIM_LT24

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFF364

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

26.1.38 SFLASH_IMO_TRIM_LT0

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF365

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.39 SFLASH_IMO_TRIM_LT1

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF366

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.40 SFLASH_IMO_TRIM_LT2

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF367

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.41 SFLASH_IMO_TRIM_LT3

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF368

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.42 SFLASH_IMO_TRIM_LT4

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF369

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.43 SFLASH_IMO_TRIM_LT5

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF36A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.44 SFLASH_IMO_TRIM_LT6

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF36B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.45 SFLASH_IMO_TRIM_LT7

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF36C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.46 SFLASH_IMO_TRIM_LT8

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF36D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.47 SFLASH_IMO_TRIM_LT9

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF36E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.48 SFLASH_IMO_TRIM_LT10

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF36F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.49 SFLASH_IMO_TRIM_LT11

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF370

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.50 SFLASH_IMO_TRIM_LT12

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF371

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.51 SFLASH_IMO_TRIM_LT13

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF372

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.52 SFLASH_IMO_TRIM_LT14

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF373

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.53 SFLASH_IMO_TRIM_LT15

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF374

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.54 SFLASH_IMO_TRIM_LT16

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF375

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.55 SFLASH_IMO_TRIM_LT17

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF376

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.56 SFLASH_IMO_TRIM_LT18

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF377

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.57 SFLASH_IMO_TRIM_LT19

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF378

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.58 SFLASH_IMO_TRIM_LT20

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF379

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.59 SFLASH_IMO_TRIM_LT21

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF37A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.60 SFLASH_IMO_TRIM_LT22

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF37B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.61 SFLASH_IMO_TRIM_LT23

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF37C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

26.1.62 SFLASH_IMO_TRIM_LT24

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFF37D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

27 SPC Interface Registers

This section discusses the System Performance Controller Interface (SPCIF) registers. It lists all the registers in mapping tables, in address order.

27.1 Register Details

Register Name	Address
SPCIF_GEOMETRY	0x40110000
SPCIF_INTR	0x401107F0
SPCIF_INTR_SET	0x401107F4
SPCIF_INTR_MASK	0x401107F8
SPCIF_INTR_MASKED	0x401107FC

27.1.1 SPCIF_GEOMETRY

Flash/NVL geometry information

Address: 0x40110000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	FLASH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R		R					
HW Access	W		W					
Name	SFLASH [15:14]		FLASH [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	R		R		R			
HW Access	W		W		W			
Name	FLASH_ROW [23:22]		NUM_FLASH [21:20]		SFLASH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	None	None						
Name	DE_CP-D_LP	None [30:24]						

Bits	Name	Description
31	DE_CPD_LP	0': SRAM busy wait loop has not been copied. '1': Busy wait loop has been written into SRAM. Default Value: 0
23 : 22	FLASH_ROW	Page size in 64 Byte multiples (chip dependent): "0": 64 byte "1": 128 byte "2": 192 byte "3": 256 byte The page size is used to detemine the number of Bytes in a page for Flash page based operations (e.g. PGM_PAGE). Note: the field name FLASH_ROW is misleading, as this field specifies the number of Bytes in a page, rather than the number of Bytes in a row. In a single plane flash macro architecture, a page consists of a single row. However, in a multi plane flash macro architecture, a page consists of multiple rows from different planes. Default Value: Undefined

(continued)

21 : 20	NUM_FLASH	Number of flash macros (chip dependent): "0": 1 flash macro "1": 2 flash macros "2": 3 flash macros "3": 4 flash macros Default Value: Undefined
19 : 14	SFLASH	Supervisory flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the supervisory flash capacity of all flash macros together: "0": 256 Bytes. "1": 2*256 Bytes. ... "63": 64*256 Bytes. Default Value: Undefined
13 : 0	FLASH	Regular flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the flash capacity of all flash macros together: "0": 256 Bytes. "1": 2*256 Bytes. ... "16383": 16384*256 Bytes. Default Value: Undefined

27.1.2 SPCIF_INTR

SPCIF interrupt request register

Address: 0x401107F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Timer counter value reaches "0". Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. Default Value: 0

27.1.3 SPCIF_INTR_SET

SPCIF interrupt set request register

Address: 0x401107F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Write INTR_SET field with '1' to set corresponding INTR field. Default Value: 0

27.1.4 SPCIF_INTR_MASK

SPCIF interrupt mask register

Address: 0x401107F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Mask for corresponding field in INTR register. Default Value: 0

27.1.5 SPCIF_INTR_MASKED

SPCIF interrupt masked request register

Address: 0x401107FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Logical and of corresponding request and mask fields. Default Value: 0

28 System Resources Sub System Registers

This section discusses the System Resources Sub System (SRSS) registers. It lists all the registers in mapping tables, in address order.

28.1 Register Details

Register Name	Address
PWR_CONTROL	0x40030000
PWR_KEY_DELAY	0x40030004
PWR_DDFT_SELECT	0x4003000C
TST_MODE	0x40030014
CLK_SELECT	0x40030028
CLK_ILO_CONFIG	0x4003002C
CLK_IMO_CONFIG	0x40030030
CLK_DFT_SELECT	0x40030034
WDT_DISABLE_KEY	0x40030038
WDT_COUNTER	0x4003003C
WDT_MATCH	0x40030040
SRSS_INTR	0x40030044
SRSS_INTR_SET	0x40030048
SRSS_INTR_MASK	0x4003004C
RES_CAUSE	0x40030054
CLK_IMO_SELECT	0x40030F08
CLK_IMO_TRIM1	0x40030F0C
CLK_IMO_TRIM2	0x40030F10
PWR_PWRSYS_TRIM1	0x40030F14
CLK_IMO_TRIM3	0x40030F18

28.1.1 PWR_CONTROL

Power Mode Control

Address: 0x40030000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R			
HW Access	None		RW	RW	RW			
Name	None [7:6]		LP-M_READY	DEBUG_-SESSION	POWER_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None			R		RW	RW
HW Access	A	None			RW		R	R
Name	EXT_VCCD	None [22:20]			SPARE [19:18]		OVER_-TEMP_-THRESH	OVER_-TEMP_EN

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	EXT_VCCD	Always write 0 except as noted below. Setting this bit turns off the active regulator and will lead to system reset (BOD) unless both Vddd and Vccd pins are supplied externally. This register bit only resets for XRES, POR, or a detected BOD. Default Value: 0
19 : 18	SPARE	Spare AHB readback bits that are hooked to PWR_PWRSYS_TRIM1.SPARE_TRIM[1:0] through spare logic equivalent to bitwise inversion. Engineering only. Default Value: 0
17	OVER_TEMP_THRESH	Over-temperature threshold. 0: TEMP_HIGH condition occurs between 120C and 125C. 1: TEMP_HIGH condition occurs between 60C and 75C (used for testing). Default Value: 0
16	OVER_TEMP_EN	Enables the die over temperature sensor. Must be enabled when using the TEMP_HIGH interrupt. Default Value: 0

(continued)

5	LPM_READY	Indicates whether the low power mode regulator is ready to enter DEEPSLEEP mode. 0: If DEEPSLEEP mode is requested, device will enter SLEEP mode. When low power regulators are ready, device will automatically enter the originally requested mode. 1: Normal operation. DEEPSLEEP works as described. Default Value: 0
4	DEBUG_SESSION	Indicates whether a debug session is active (CDBGPWRUPREQ signal is 1) Default Value: 0 **0x0: NO_SESSION:** No debug session active **0x1: SESSION_ACTIVE:** Debug session is active
3 : 0	POWER_MODE	Current power mode of the device. Default Value: 0 **0x0: RESET:** RESET state **0x1: ACTIVE:** ACTIVE state **0x2: SLEEP:** SLEEP state **0x3: DEEP_SLEEP:** DEEP_SLEEP state

28.1.2 PWR_KEY_DELAY

Power System Key Register

Address: 0x40030004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (number of HFCLK cycles) to wait for references to settle on wakeup from deepsleep. BOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. The default assumes the output of the predivider is 48MHz + 3%. Firmware may scale this setting according to the fastest actual clock frequency that can occur when waking from DEEPSLEEP. Default Value: 248

28.1.3 PWR_DDFT_SELECT

Power DDFT Mode Selection Register

Address: 0x4003000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DDFT1_SEL [7:4]				DDFT0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	DDFT1_SEL	Select signal for power DDFT output #1 Default Value: 0 **0x0: WAKEUP:** wakeup **0x1: AWAKE:** awake **0x2: ACT_POWER_EN:** act_power_en **0x3: ACT_POWER_UP:** act_power_up **0x4: ACT_POWER_GOOD:** act_power_good **0x5: ACT_REF_VALID:** act_ref_valid **0x6: ACT_REG_VALID:** act_reg_valid

(continued)

		0x7: ACT_COMP_OUT: act_comp_out **0x8: ACT_TEMP_HIGH:** act_temp_high **0x9: DPSLP_COMP_OUT:** dpslp_comp_out **0xa: DPSLP_POWER_UP:** dpslp_power_up **0xb: AWAKE_DELAYED:** awake_delayed **0xc: LPM_READY:** lpm_ready **0xd: SLEEPHOLDACK_N:** sleepholdack_n **0xe: GND:** 1'b0 **0xf: PWR:** 1'b1
3 : 0	DDFT0_SEL	Select signal for power DDFT output #0 Default Value: 0 **0x0: WAKEUP:** wakeup **0x1: AWAKE:** awake **0x2: ACT_POWER_EN:** act_power_en **0x3: ACT_POWER_UP:** act_power_up **0x4: ACT_POWER_GOOD:** act_power_good **0x5: ACT_REF_EN:** srss_adft_control_act_ref_en **0x6: ACT_COMP_EN:** srss_adft_control_act_comp_en **0x7: DPSLP_REF_EN:** srss_adft_control_dpslp_ref_en **0x8: DPSLP_REG_EN:** srss_adft_control_dpslp_reg_en **0x9: DPSLP_COMP_EN:** srss_adft_control_dpslp_comp_en **0xa: OVER_TEMP_EN:** pwr_control_over_temp_en **0xb: SLEEPHOLDREQ_N:** sleepholdreq_n

(continued)

0xc: ADFT_BUF_EN:
adft_buf_en

0xd: ATPG_OBSERVE:
ATPG observe point (no functional purpose)

0xe: GND:
1'b0

0xf: PWR:
1'b1

28.1.4 TST_MODE

Test Mode Control Register

Address: 0x40030014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	None	
HW Access	None					RW	None	
Name	None [7:3]					SWD_CON-NECTED	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R	None	RW	None			
HW Access	R	RW	None	A	None			
Name	TEST_-MODE	TEST_KEY _DFT_EN	None	BLOCK_AL T_XRES	None [27:24]			

Bits	Name	Description
31	TEST_MODE	0: Normal operation mode 1: Test mode (any test mode) Setting this bit will prevent BootROM from yielding execution to Flash image. Default Value: 0
30	TEST_KEY_DFT_EN	This bit is set when a XRES test mode key is shifted in. It is the value of the test_key_dft_en signal. When this bit is set, the BootROM will not yield execution to the FLASH image (same function as setting TEST_MODE bit below). Default Value: 0
28	BLOCK_ALT_XRES	Relevant only for parts that have the alternate XRES mechanism of overloading a GPIO pin temporarily as alternate XRES during test. When set, this bit blocks the alternate XRES function, such that the pin can be used for normal I/O or for ddft/adft observation. This register bit only resets for XRES, POR, or a detected BOD. Default Value: 0

(continued)

2	SWD_CONNECTED	0: SWD not active 1: SWD activated (Line Reset & Connect sequence passed) (Note: this bit replaces TST_CTRL.SWD_CONNECTED and is present in all M0S8 products except TSG4) Default Value: 0

28.1.5 CLK_SELECT

Clock Select Register

Address: 0x40030028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	SYSCLK_DIV [7:6]		PUMP_SEL [5:4]		HFCLK_DIV [3:2]		HFCLK_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SYSCLK_DIV	Select SYSCLK prescaler value. Default Value: 0 **0x0: NO_DIV:** SYSCLK= HFCLK/1 **0x1: DIV_BY_2:** SYSCLK= HFCLK/2 **0x2: DIV_BY_4:** SYSCLK= HFCLK/4 **0x3: DIV_BY_8:** SYSCLK= HFCLK/8
5 : 4	PUMP_SEL	Selects clock source for charge pump clock (AMUX charge pump). This clock is not guaranteed to be glitch free when changing any of its sources or settings. Default Value: 0 **0x0: GND:** No clock, connect to gnd

(continued)

		0x1: IMO: Use main IMO output **0x2: HFCLK:** Use HFCLK (using selected source after predivider but before prescaler)
3 : 2	HFCLK_DIV	Selects HFCLK predivider value. Default Value: 2 **0x0: NO_DIV:** Transparent mode, feed through selected clock source w/o dividing. **0x1: DIV_BY_2:** Divide selected clock source by 2 **0x2: DIV_BY_4:** Divide selected clock source by 4 **0x3: DIV_BY_8:** Divide selected clock source by 8
1 : 0	HFCLK_SEL	Selects a source for HFCLK Default Value: 0 **0x0: IMO:** IMO **0x1: EXTCLK:** EXTCLK **0x2: ECO:** ECO - External-Crystal Oscillator or PLL subsystem output

28.1.6 CLK_ILO_CONFIG

ILO Configuration

Address: 0x4003002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for ILO oscillator. This bit is hardware set whenever the WD_DISABLE_KEY is not set to the magic value (0xACED8865). Default Value: 1

28.1.7 CLK_IMO_CONFIG

IMO Configuration

Address: 0x40030030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for IMO oscillator. Clearing this bit will disable the IMO. Don't do this if the system is running off it. Default Value: 1

28.1.8 CLK_DFT_SELECT

Clock DFT Mode Selection Register

Address: 0x40030034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	R	R		R			
Name	None	DFT_EDGE0	DFT_DIV0 [5:4]		DFT_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW		RW			
HW Access	None	R	R		R			
Name	None	DFT_EDGE1	DFT_DIV1 [13:12]		DFT_SEL1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	DFT_EDGE1	Edge sensitivity for in-line divider on output #1 (only relevant when DIV1>0). Default Value: 0 **0x0: POSEDGE:** Use posedge for divider **0x1: NEGEDGE:** Use negedge for divider
13 : 12	DFT_DIV1	DFT Output Divide Down. Default Value: 0 **0x0: NO_DIV:** Direct Output **0x1: DIV_BY_2:** Divide by 2 **0x2: DIV_BY_4:** Divide by 4

(continued)

		0x3: DIV_BY_8: Divide by 8
11 : 8	DFT_SEL1	Select signal for DFT output #1 Default Value: 0 **0x0: NC:** Disabled - output is 0 **0x1: ILO:** clk_ilo: ILO output **0x2: IMO:** clk_imo: IMO primary output **0x3: ECO:** clk_eco: ECO output **0x4: EXTCLK:** clk_ext: external clock input **0x5: HFCLK:** clk_hf: root of the high-speed clock tree **0x6: LFCLK:** clk_lf: root of the low-speed clock tree **0x7: SYSCLK:** clk_sys: root of the CPU/AHB clock tree (gated version of clk_hf) **0x8: PUMPCLK:** clk_pump: clock provided to charge pumps in FLASH and PA **0x9: SLPCTRLCLK:** clk_slpctrl: clock provided to SleepController
6	DFT_EDGE0	Edge sensitivity for in-line divider on output #0 (only relevant when DIV0>0). Default Value: 0 **0x0: POSEDGE:** Use posedge for divider **0x1: NEGEDGE:** Use negedge for divider
5 : 4	DFT_DIV0	DFT Output Divide Down. Default Value: 0 **0x0: NO_DIV:** Direct Output **0x1: DIV_BY_2:** Divide by 2 **0x2: DIV_BY_4:** Divide by 4 **0x3: DIV_BY_8:** Divide by 8
3 : 0	DFT_SEL0	Select signal for DFT output #0 Default Value: 0 **0x0: NC:** Disabled - output is 0

(continued)

0x1: ILO:
clk_ilo: ILO output

0x2: IMO:
clk_imo: IMO primary output

0x3: ECO:
clk_eco: ECO output

0x4: EXTCLK:
clk_ext: external clock input

0x5: HFCLK:
clk_hf: root of the high-speed clock tree

0x6: LFCLK:
clk_lf: root of the low-speed clock tree

0x7: SYSCLK:
clk_sys: root of the CPU/AHB clock tree (gated version of clk_hf)

0x8: PUMPCLK:
clk_pump: clock provided to charge pumps in FLASH and PA

0x9: SLPCTRLCLK:
clk_slpctrl: clock provided to SleepController

28.1.9 WDT_DISABLE_KEY

Watchdog Disable Key Register

Address: 0x40030038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Disables WDT reset when equal to 0xACED8865. The WDT reset functions normally for any other setting. Default Value: 0

28.1.10 WDT_COUNTER

Watchdog Counter Register

Address: 0x4003003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	Current value of WDT Counter Default Value: 0

28.1.11 WDT_MATCH

Watchdog Match Register

Address: 0x40030040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MATCH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MATCH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				IGNORE_BITS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	IGNORE_BITS	The number of MSB bits of the watchdog timer that are NOT checked against MATCH. This value provides control over the time-to-reset of the watchdog (which happens after 3 successive matches). Default Value: 0
15 : 0	MATCH	Match value for Watchdog counter. Every time WDT_COUNTER reaches MATCH an interrupt is generated. Two unserviced interrupts will lead to a system reset (i.e. at the third match). Default Value: 4096

28.1.12 SRSS_INTR

SRSS Interrupt Register

Address: 0x40030044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [7:2]						TEMP_HIGH	WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	TEMP_HIGH	Regulator over-temp interrupt. This interrupt can occur when a short circuit exists on the vccd pin or when extreme loads are applied on IO-cells causing the die to overheat. Firmware is encourage to shutdown all IO cells and then go to DeepSleep mode when this interrupt occurs if protection against such conditions is desired. Default Value: 0
0	WDT_MATCH	WDT Interrupt Request. This bit is set each time WDT_COUNTR==WDT_MATCH. Clearing this bit also feeds the watch dog. Missing 2 interrupts in a row will generate brown-out reset. It takes 2 SYSCLK cycles to update after a write 1 to clear. Default Value: 0

28.1.13 SRSS_INTR_SET

SRSS Interrupt Set Register

Address: 0x40030048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	None
HW Access	None						A	None
Name	None [7:2]						TEMP_HIGH	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	TEMP_HIGH	Writing 1 to this bit internally sets the overtemp interrupt. This can be observed by reading SRSS_INTR.TEMP_HIGH. This bit always reads back as zero. Default Value: 0

28.1.14 SRSS_INTR_MASK

SRSS Interrupt Mask Register

Address: 0x4003004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						TEMP_HIGH	WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	TEMP_HIGH	Masks REG_OVERTEMP interrupt Default Value: 0
0	WDT_MATCH	Clearing this bit will not forward the interrupt to the CPU. It will not, however, disable the WDT reset generation on 2 missed interrupts. Default Value: 0

28.1.15 RES_CAUSE

Reset Cause Observation Register

Address: 0x40030054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	None		RW1C
HW Access	None			A	A	None		A
Name	None [7:5]			RESET_-SOFT	RE-SET_PROT _FAULT	None [2:1]		RE-SET_WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	RESET_SOFT	Cortex-M0+ requested a system reset through its SYSRESETREQ. This can be done via a debugger probe or in firmware. Default Value: 0
3	RESET_PROT_FAULT	A protection violation occurred that requires a RESET. This includes, but is not limited to, hitting a debug breakpoint while in Privileged Mode. Default Value: 0
0	RESET_WDT	A WatchDog Timer reset has occurred since last power cycle. Default Value: 0

28.1.16 CLK_IMO_SELECT

IMO Frequency Select Register

Address: 0x40030F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					FREQ [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	FREQ	Select operating frequency Default Value: 0 **0x0: 24_MHZ:** IMO runs at 24 MHz **0x1: 28_MHZ:** IMO runs at 28 MHz **0x2: 32_MHZ:** IMO runs at 32 MHz **0x3: 36_MHZ:** IMO runs at 36 MHz **0x4: 40_MHZ:** IMO runs at 40 MHz **0x5: 44_MHZ:** IMO runs at 44 MHz **0x6: 48_MHZ:** IMO runs at 48 MHz

28.1.17 CLK_IMO_TRIM1

IMO Trim Register

Address: 0x40030F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. This field is hardware updated during USB osclock mode. This field is mapped to the most significant bits of the IMO trim imo_clk_trim[10:3]. The step size of 1 LSB on this field is approximately 120 kHz. Default Value: 128

28.1.18 CLK_IMO_TRIM2

IMO Trim Register

Address: 0x40030F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					RW		
Name	None [7:3]					FSOFFSET [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	FSOFFSET	Frequency trim bits. These bits are not trimmed during manufacturing and kept at 0 under normal operation. This field is hardware updated during USB osclock mode. This field is mapped to the least significant bits of the IMO trim imo_clk_trim[2:0]. The step size of 1 LSB on this field is approximately 15 kHz. Default Value: 0

28.1.19 PWR_PWRSYS_TRIM1

Power System Trim Register

Address: 0x40030F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SPARE_TRIM [7:4]				DPSLP_REF_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SPARE_TRIM	Active-Reference temperature compensation trim (repurposed from spare bits). Bits [7:6] - trim the Active-Reference IREF temperature coefficient (TC). 00: TC = 0 (unchanged) 01: TC = +80ppm/C 10: TC = -80ppm/C 11: TC = -150ppm/C Bits [5:4] - trim the Active-Reference VREF temperature coefficient (TC). 00: TC = 0 (unchanged) 01: TC = -50ppm/C 10: TC = -80ppm/C 11: TC = +150ppm/C Default Value: 0
3 : 0	DPSLP_REF_TRIM	Trims the DeepSleep reference that is used by the DeepSleep regulator and DeepSleep power comparator. Default Value: 0

28.1.20 CLK_IMO_TRIM3

IMO Trim Register

Address: 0x40030F18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

29 Timer, Counter, PWM Registers

This section discusses the Timer, Counter, PWM (TCPWM) registers. It lists all the registers in mapping tables, in address order.

29.1 Register Details

Register Name	Address
TCPWM_CTRL	0x40200000
TCPWM_CMD	0x40200008
TCPWM_INTR_CAUSE	0x4020000C

29.1.1 TCPWM_CTRL

TCPWM control register 0.

Address: 0x40200000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COUNTER_ENABLED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	COUNTER_ENABLED	Counter enables for counters 0 up to CNT_NR-1. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_CTRL0, TR_CTRL1, and TR_CTRL2 register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_overflow", "tr_underflow" and "tr_compare_match"). - the counter's line outputs ("line_out" and "line_compl_out"). Default Value: 0

29.1.2 TCPWM_CMD

TCPWM command register.

Address: 0x40200008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_CAPTURE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_RELOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_STOP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_START [31:24]							

Bits	Name	Description
31 : 24	COUNTER_START	Counters SW start trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
23 : 16	COUNTER_STOP	Counters SW stop trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
15 : 8	COUNTER_RELOAD	Counters SW reload trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
7 : 0	COUNTER_CAPTURE	Counters SW capture trigger. When written with '1', a capture trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.COUNTER_ENABLED, the field is immediately set to '0'. Default Value: 0

29.1.3 TCPWM_INTR_CAUSE

TCPWM Counter interrupt cause register.

Address: 0x4020000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	COUNTER_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	COUNTER_INT	Counters interrupt signal active. If the counter is disabled through CTRL.COUNTER_ENABLED, the associated interrupt field is immediately set to '0'. Default Value: 0

30 PERI Trigger Group Control Registers

This section discusses the PERI Trigger Group Control (TR_GROUP) registers. It lists all the registers in mapping tables, in address order.

30.1 Register Details

Register Name	Address
PERI_TR_GROUP0_TR_OUT_CTL0	0x40012000
PERI_TR_GROUP0_TR_OUT_CTL1	0x40012004
PERI_TR_GROUP0_TR_OUT_CTL2	0x40012008
PERI_TR_GROUP0_TR_OUT_CTL3	0x4001200C
PERI_TR_GROUP0_TR_OUT_CTL4	0x40012010
PERI_TR_GROUP0_TR_OUT_CTL5	0x40012014
PERI_TR_GROUP0_TR_OUT_CTL6	0x40012018
PERI_TR_GROUP0_TR_OUT_CTL7	0x4001201C
PERI_TR_GROUP1_TR_OUT_CTL0	0x40012200
PERI_TR_GROUP1_TR_OUT_CTL1	0x40012204
PERI_TR_GROUP1_TR_OUT_CTL2	0x40012208
PERI_TR_GROUP1_TR_OUT_CTL3	0x4001220C
PERI_TR_GROUP1_TR_OUT_CTL4	0x40012210
PERI_TR_GROUP1_TR_OUT_CTL5	0x40012214
PERI_TR_GROUP1_TR_OUT_CTL6	0x40012218
PERI_TR_GROUP2_TR_OUT_CTL	0x40012400
PERI_TR_GROUP3_TR_OUT_CTL	0x40012600

30.1.1 PERI_TR_GROUP0_TR_OUT_CTL0

Trigger control register

Address: 0x40012000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.2 PERI_TR_GROUP0_TR_OUT_CTL1

Trigger control register

Address: 0x40012004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.3 PERI_TR_GROUP0_TR_OUT_CTL2

Trigger control register

Address: 0x40012008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.4 PERI_TR_GROUP0_TR_OUT_CTL3

Trigger control register

Address: 0x4001200C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.5 PERI_TR_GROUP0_TR_OUT_CTL4

Trigger control register

Address: 0x40012010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.6 PERI_TR_GROUP0_TR_OUT_CTL5

Trigger control register

Address: 0x40012014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.7 PERI_TR_GROUP0_TR_OUT_CTL6

Trigger control register

Address: 0x40012018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.8 PERI_TR_GROUP0_TR_OUT_CTL7

Trigger control register

Address: 0x4001201C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.9 PERI_TR_GROUP1_TR_OUT_CTL0

Trigger control register

Address: 0x40012200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.10 PERI_TR_GROUP1_TR_OUT_CTL1

Trigger control register

Address: 0x40012204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.11 PERI_TR_GROUP1_TR_OUT_CTL2

Trigger control register

Address: 0x40012208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.12 PERI_TR_GROUP1_TR_OUT_CTL3

Trigger control register

Address: 0x4001220C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.13 PERI_TR_GROUP1_TR_OUT_CTL4

Trigger control register

Address: 0x40012210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.14 PERI_TR_GROUP1_TR_OUT_CTL5

Trigger control register

Address: 0x40012214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.15 PERI_TR_GROUP1_TR_OUT_CTL6

Trigger control register

Address: 0x40012218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.16 PERI_TR_GROUP2_TR_OUT_CTL

Trigger control register

Address: 0x40012400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

30.1.17 PERI_TR_GROUP3_TR_OUT_CTL

Trigger control register

Address: 0x40012600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typicallu connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

31 Watch Crystal Oscillator Registers

This section discusses the Watch Crystal Oscillator (WCO) registers. It lists all the registers in mapping tables, in address order.

31.1 Register Details

Register Name	Address
WCO_CONFIG	0x40220000
WCO_STATUS	0x40220004
WCO_DPLL	0x40220008
WCO_WDT_CTRLOW	0x40220200
WCO_WDT_CTRHIGH	0x40220204
WCO_WDT_MATCH	0x40220208
WCO_WDT_CONFIG	0x4022020C
WCO_WDT_CONTROL	0x40220210
WCO_WDT_CLKEN	0x40220214
WCO_TRIM	0x40220F00

31.1.1 WCO_CONFIG

WCO Configuration Register

Address: 0x40220000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					EXT_IN-PUT_EN	LPM_AUTO	LPM_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ENBUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	IP_ENABLE	DPLL_EN-ABLE	None [29:24]					

Bits	Name	Description
31	IP_ENABLE	Master enable for IP - disables both WCO and DPLL Default Value: 0
30	DPLL_ENABLE	Enable DPLL operation. The Oscillator is specified to be stable after 500 ms thus the DPLL should be asserted no sooner than that after IP_ENABLE is set. Default Value: 0
23 : 16	ENBUS	Test Mode Control bits enbus[7] - N/A enbus[6] - 1=enable both primary Beta Multipliers enbus[5] - N/A enbus[4] - N/A enbus[3] - Load Resistor Control enbus[2] - Load Resistor Control enbus[1] - Load Resistor Control enbus[0] - Load Resistor Control Default Value: 71
2	EXT_INPUT_EN	Disables the load resistor and allows external clock input for pad_xin Default Value: 0

(continued)

1	LPM_AUTO	Automatically control low power mode (only relevant when LPM_EN=0): 0: Do not enter low power mode (LPM) in DeepSleep 1: Enter low power mode (LPM) in DeepSleep. The logic monitors !act_power_en to determine the device has entered DeepSleep. Default Value: 1
0	LPM_EN	Force block into Low Power Mode: 0: Do not force low power mode (LPM) on 1: Force low power mode (LPM) on Default Value: 0

31.1.2 WCO_STATUS

WCO Status Register

Address: 0x40220004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							OUT-_BLNK_A

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	OUT_BLNK_A	Indicates that output has transitioned - This bit is intended for Test Mode Only and is not a reliable indicator. Default Value: 0

31.1.3 WCO_DPLL

WCO DPLL Register

Address: 0x40220008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DPLL_MULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					DPLL_MULT [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DPLL_LF_LIMIT [23:22]		DPLL_LF_PGAIN [21:19]			DPLL_LF_IGAIN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW					
HW Access	None		R					
Name	None [31:30]		DPLL_LF_LIMIT [29:24]					

Bits	Name	Description
29 : 22	DPLL_LF_LIMIT	Maximum IMO offset allowed (used to prevent DPLL dynamics from selecting an IMO frequency that the logic cannot support) Default Value: 255
21 : 19	DPLL_LF_PGAIN	DPLL Loop Filter Proportionial Gain Setting 0x0 - 0.0625 0x1 - 0.125 0x2 - 0.25 0x3 - 0.5 0x4 - 1.0 0x5 - 2.0 0x6 - 4.0 0x7 - 8.0 Default Value: 0

(continued)

18 : 16	DPLL_LF_IGAIN	DPLL Loop Filter Integral Gain Setting 0x0 - 0.0625 0x1 - 0.125 0x2 - 0.25 0x3 - 0.5 0x4 - 1.0 0x5 - 2.0 0x6 - 4.0 0x7 - 8.0 Default Value: 0
10 : 0	DPLL_MULT	Multiplier to determine IMO frequency in multiples of the WCO frequency Fimo = (DPLL_MULT + 1) * Fwco Default Value: 0

31.1.4 WCO_WDT_CTRLOW

Watchdog Counters 0/1

Address: 0x40220200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WDT_CTR0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WDT_CTR0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WDT_CTR1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WDT_CTR1 [31:24]							

Bits	Name	Description
31 : 16	WDT_CTR1	Current value of WDT Counter 1, the counter always counts up Default Value: 0
15 : 0	WDT_CTR0	Current value of WDT Counter 0, the counter always counts up Default Value: 0

31.1.5 WCO_WDT_CTRHIGH

Watchdog Counter 2

Address: 0x40220204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [31:24]							

Bits	Name	Description
31 : 0	WDT_CTR2	Current value of WDT Counter 2, the counter always counts up Default Value: 0

31.1.6 WCO_WDT_MATCH

Watchdog counter match values

Address: 0x40220208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [31:24]							

Bits	Name	Description
31 : 16	WDT_MATCH1	Match value for Watchdog Counter 1 Default Value: 0
15 : 0	WDT_MATCH0	Match value for Watchdog Counter 0 Default Value: 0

31.1.7 WCO_WDT_CONFIG

Watchdog Counters Configuration

Address: 0x4022020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [7:4]				WDT_CAS-CADE0_1	WDT_-CLEAR0	WDT_MODE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [15:12]				WDT_CAS-CADE1_2	WDT_-CLEAR1	WDT_MODE1 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							WDT_-MODE2

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None	RW				
HW Access	R		None	R				
Name	LFCLK_SEL [31:30]		None	WDT_BITS2 [28:24]				

Bits	Name	Description
31 : 30	LFCLK_SEL	Select source for LFCLK: 0: ILO - Internal R/C Oscillator 1: WCO - Internal Crystal Oscillator 2-3: Reserved - do not use Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. To safely change LFCLK_SEL wait for WDT_CTRLOW/WDT_CTRHIGH to change then change the setting immediately. Default Value: 0
28 : 24	WDT_BITS2	Bit to observe for WDT_INT2: 0: Assert when bit0 of WDT_CTR2 toggles (one int every tick) .. 31: Assert when bit31 of WDT_CTR2 toggles (one int every 2^31 ticks) Default Value: 0
16	WDT_MODE2	Watchdog Counter 2 Mode. Default Value: 0

(continued)

		0x0: NOTHING: Free running counter with no interrupt requests **0x1: INT:** Free running counter with interrupt request when a specified bit in CTR2 toggles (see WDT_BITS2)
11	WDT_CASCADE1_2	Cascade Watchdog Counters 1,2. Counter 2 increments the cycle after WDT_CTR1=WDT_-MATCH1. It is allowed to cascade all three WDT counters. 0: Independent counters 1: Cascaded counters. When cascading all three counters, WDT_CLEAR1 must be 1 Default Value: 0
10	WDT_CLEAR1	Clear Watchdog Counter when WDT_CTR1=WDT_MATCH1. In other words WDT_CTR1 divides LFCLK by (WDT_MATCH1+1). 0: Free running counter 1: Clear on match Default Value: 0
9 : 8	WDT_MODE1	Watchdog Counter Action on Match (WDT_CTR1=WDT_MATCH1). Default Value: 0 **0x0: NOTHING:** Do nothing **0x1: INT:** Assert WDT_INTx **0x2: RESET:** Assert WDT Reset - Not Supported - here for backwards compatibility **0x3: INT_THEN_RESET:** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt - Not supported - here for backwards compatibility.
3	WDT_CASCADE0_1	Cascade Watchdog Counters 0,1. Counter 1 increments the cycle after WDT_CTR0=WDT_-MATCH0. 0: Independent counters 1: Cascaded counters Default Value: 0
2	WDT_CLEAR0	Clear Watchdog Counter when WDT_CTR0=WDT_MATCH0. In other words WDT_CTR0 divides LFCLK by (WDT_MATCH0+1). 0: Free running counter 1: Clear on match Default Value: 0
1 : 0	WDT_MODE0	Watchdog Counter Action on Match (WDT_CTR0=WDT_MATCH0). Default Value: 0 **0x0: NOTHING:** Do nothing **0x1: INT:** Assert WDT_INTx **0x2: RESET:** Assert WDT Reset - Not Supported - here for backwards compatibility **0x3: INT_THEN_RESET:** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt. Not supported - here for Backwards compatibility.

31.1.8 WCO_WDT_CONTROL

Watchdog Counters Control

Address: 0x40220210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [7:4]				WDT_RESET0	WDT_INT0	WDT_ENABLED0	WDT_ENABLE0

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [15:12]				WDT_RESET1	WDT_INT1	WDT_ENABLED1	WDT_ENABLE1

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [23:20]				WDT_RESET2	WDT_INT2	WDT_ENABLED2	WDT_ENABLE2

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	WDT_RESET2	Resets counter 2 back to 0000_0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT. Default Value: 0
18	WDT_INT2	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. After W1C, WDT_CONTROL must be read for the hardware to internally remove the clear flag. Failure to do this may result in missing the next interrupt. Default Value: 0
17	WDT_ENABLED2	Indicates actual state of counter. May lag WDT_ENABLE2 by up to 3 LFCLK cycles. After changing WDT_ENABLE2, do not enter DEEPSLEEP mode until this field acknowledges the change. Default Value: 0

(continued)

16	WDT_ENABLE2	Enable Counter 2 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0
11	WDT_RESET1	Resets counter 1 back to 0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT. Default Value: 0
10	WDT_INT1	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. After W1C, WDT_CONTROL must be read for the hardware to internally remove the clear flag. Failure to do this may result in missing the next interrupt. Default Value: 0
9	WDT_ENABLED1	Indicates actual state of counter. May lag WDT_ENABLE1 by up to 3 LFCLK cycles. After changing WDT_ENABLE1, do not enter DEEPSLEEP mode until this field acknowledges the change. Default Value: 0
8	WDT_ENABLE1	Enable Counter 1 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0
3	WDT_RESET0	Resets counter 0 back to 0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT. Default Value: 0
2	WDT_INT0	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODEx=3. After W1C, WDT_CONTROL must be read for the hardware to internally remove the clear flag. Failure to do this may result in missing the next interrupt. Default Value: 0
1	WDT_ENABLED0	Indicates actual state of counter. May lag WDT_ENABLE0 by up to 3 LFCLK cycles. After changing WDT_ENABLE0, do not enter DEEPSLEEP mode until this field acknowledges the change. Default Value: 0
0	WDT_ENABLE0	Enable Counter 0 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0

31.1.9 WCO_WDT_CLKEN

Watchdog Counters Clock Enable

Address: 0x40220214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CLK_ILO_EN_-FOR_WDT	CLK_W-CO_EN_-FOR_WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CLK_ILO_EN_FOR_WDT	Enables the ILO clock for use by the WDT logic. Wait at least 4 ILO clock cycles for a change to take effect. Must be 0 when switching WDT_CONFIG.LFCLK_SEL. Should be 0 if CLK_W-CO_EN_FOR_WDT=1. Default Value: 0
0	CLK_WCO_EN_-FOR_WDT	Enables the WCO clock for use by the WDT logic. Wait at least 4 WCO clock cycles for a change to take effect. Must be 0 when switching WDT_CONFIG.LFCLK_SEL. Should be 0 if CLK_ILO_EN_FOR_WDT=1 Default Value: 0

31.1.10 WCO_TRIM

WCO Trim Register

Address: 0x40220F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		None	RW		
HW Access	None		R		None	R		
Name	None [7:6]		LPM_GM [5:4]		None	XGM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	LPM_GM	GM setting for LPM (bandwidth = DC/ms) - Used when WCO.LPM_AUTO=0 or when LPM_AUTO=1 and not in DeepSleep mode. Default Value: 1
2 : 0	XGM	Amplifier GM setting - Used when WCO.LPM_AUTO=0 or when LPM_AUTO=1 and not in DeepSleep mode. 0x0 - 3370 nA 0x1 - 2620 nA 0x2 - 2250 nA 0x3 - 1500 nA 0x4 - 1870 nA 0x5 - 1120 nA 0x6 - 750 nA 0x7 - 0 nA Default Value: 1

Revision History

Revision History

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Revision	**ECN#**	**Issue Date**	**Description of Changes**
**	5881501	09/18/2017	Specification for new silicon
*A	5910025	10/05/2017	Minor text updates
*B	5935038	10/20/2017	Updated External Clock Registers Section.
*C	5957598	14/12/2017	Changed the title “Cryptography Registers” to “True Random Number Generator” and updated the Section.
*D	8051222	07/29/2024	Fixed broken links.