Lecture-1

1. What is Moore's Law? Why and how was it modified in 1975?
2. What is the impact of Moore's law on the development of VLSI?
3. Explain the brief history of IC industry.
4. Explain the different steps in VLSI realization process.
5. What are the problems of VLSI design on today?
6. How do you define LSI and VLSI?
7. What is yield? How cost is related to yield in chip designing?
8. What are the design issues?
9. What do you mean by design synthesis?
10. What is verification? What is testing?
11. Explain VLSI design Cycle.
12. Explain the different steps in Physical Design.

Lecture-2

1. What is semiconductor?
2. Explain the Energy Band theory of crystal.
3. In the light of energy band theory, explain semiconductor, metal, insulator.
4. Why Si, Ge are semiconductors?
5. What are holes? Explain how holes can be carrier of electricity.
6. What is doping in semiconductor? What are its effects?
7. Explain donor and acceptor impurity in semiconductors?
8. What is semiconductor diode?
9. What is depletion region?
10. Explain the operation of semiconductor diode with both forward and reverse biased.
11. Explain Bipolar junction transistor (BJT).
12. Explain its three modes of operation of BJT.
13. How does a transistor act as an amplifier?
14. How does a transistor act as a switch?
15. Compare the operations of semiconductor diode and transistor.

Lecture-2A

1. What are the problems of bipolar junction transistor? Compare bipolar junction transistor versus junction field effect transistor.
2. Classify Field effect transistors.
3. Sketch the basic structure of an n-channel field effect transistor.
4. Explain the characteristics of JFET. How does it behave for small V_{DS} and large V_{DS}? How and when it turns from ohomic region to saturation region?
5. Define pinch-off voltage. Sketch the depletion region before and after pinch-off.
6. Explain JFET as amplifier and switch.
7. Explain MOSFET. What are the advantages of MOSFET over JFET?
8. Explain MOSFET with both enhancement and depletion mode.
9. Compare the transfer characteristics in JFET, depletion type MOSFET, enhancement type MOSFET.
10. Explain how the different operating points of JFET, depletion type MOSFET, enhancement type MOSFET change the uses of them.

Lecture-2B

1. Explain the functioning of nMOS inverter considering the load as a) resistor b) enhancement type transistor c) depletion type transistor.
2. What is the problem of the nMOS inverter with pull up as an enhancement type? How is it improved with depletion type pull up?
3. Why is transistor being used in place of the resistor in designing a NOT gate?

4. What are the drawbacks of MOSFETs?
5. What are the advantages of CMOS over MOSFET? What are the disadvantages of CMOS design?
6. How does CMOS work as an inverter?
7. How do you compare FET, enhancement type NMOS, depletion type NMOS with respect to operating point?
8. Explain the output and transfer characteristics enhancement type NMOS, depletion type NMOS, enhancement type PMOS and depletion type PMOS?
9. How is CMOS working as a switch?

LECTURE-3

1. Implement the Boolean function *f= ab + ad+ cd* with the help of nMOS.
2. Implement the Boolean function *f= ab + ad+ ad* with the help of pMOS.
3. Implement the Boolean function *f= ab + ad+ cd* with the help of a) CMOS Nand CMOS Nor.
4. What is single complex cell design in CMOS? What are its advantages and disadvantages of it?
5. Implement the Boolean function *f= ab+ ad +cd* using single complex cell designs in four different ways (consider that for any input, its complement is also available).
6. Implement the Boolean function $\bar{f}$*= ad+ b'd +cd'* using single complex cell designs in four different ways (consider that for any input, its complement is also available).
7. Implement the Boolean function $\bar{f}$*= ad+ b'd +cd'*using NMOS.
8. Implement the Boolean function $\bar{f}$*= ad+ b'd +cd'* using PMOS
9. Implement the Boolean function
   (i) f = (w+ $\bar{x}$ + $\bar{z}$) ($\bar{w}$+y+x) [using n MOS transistors]
   (ii) g = $\bar{A}\bar{C}$ $\bar{D}$ + A $\bar{B}$C [using CMOS transistors]
10. Implement the Boolean function
    i. f = W $\bar{X}$Z + $\bar{W}$ $\bar{Y}$ [using n MOS transistors]
    ii. (ii) g = (A + $\bar{B}$ + D) ($\bar{A}$ + BD) [using CMOS transistors]

Lecture-4

1. What is the significance of stick diagram, as applicable in the design of VLSI? What is its advantage and limitation?
2. Draw the layout of NAND and NOR using CMOS designs.
3. How to reach mask diagram from stick diagram.
4. Draw the coloured stick and mask diagrams for implementing the following Boolean functions :
   i) f = A $\bar{B}$ + $\bar{A}$ $\bar{C}$ [using n MOS transistors]
   ii) g = (w +x + z). ($\bar{w}$ + xz) [using C MOS transistors]
5. Draw the coloured stick and mask diagrams for implementing the following Boolean functions :
   (i) f = W $\bar{X}$Z + $\bar{W}$ $\bar{Y}$ [using n MOS transistors]
   (ii) g = (A + $\bar{B}$ + D) ($\bar{A}$ + BD) [using CMOS transistors]
6. Draw the coloured stick and mask diagrams for implementing the following Boolean functions :
   (i) f = A $\bar{B}$ + $\bar{A}$C + $\bar{C}$D [using n MOS transistors]
   (ii) g = (w + $\bar{x}$) ($\bar{y}$ + z) [using CMOS transistors]
7. Draw the coloured stick and mask diagrams for implementing the following Boolean functions :
   (i) f = (w+ $\bar{x}$ + $\bar{z}$) ($\bar{w}$+y+x) [using n MOS transistors]
   (ii) g = $\bar{A}\bar{C}$ $\bar{D}$ + A $\bar{B}$C [using CMOS transistors]
8. Draw the coloured stick and mask diagrams for implementing the following Boolean functions : (i) f = A $\bar{B}$C + $\bar{A}$B $\bar{C}$ [using n MOS transistors]
   (ii) g = ($\bar{w}$ +x+z) (w+ $\bar{x}$ + $\bar{z}$) [using CMOS transistors]
9. Draw the stick diagram of a shift register cell using a transmission gate followed by a CMOS inverter.
10. Convert the stick diagram obtained in previous question to symbolic form and show an example of optimization in it.

Lecture-5

1. Discus the problems of manufacturing in sizing of the different elements in fabrication.
2. What is design rule? What is the advantage of generalized design rule?
3. What do you mean by λ–based IC design rules?
4. What are the rules of design rules.
5. Explain nMOS design rules.
6. Explain buring contact and butting contact in nMOS design. Compare their merits and demerits.
7. Explain CMOS design rules.
8. Explain the design rules for different contact cuts.
9. Explain the design rules for via and cut.
10. For a CMOS shift register cell (as in question 79 and 80) draw the mask diagram conforming the λ–based design rules.

Lecture-6

1. Compare Silicon versus Germanium in the use of chip designing.
2. How the silicon wafer is prepared from sand? Explain the steps.
3. What is photoresist? Explain its uses in fabrication process.
4. Define lithography.
5. Explain the basic processing steps in fabrication.
6. Describe etching process.
7. What is the role of silicon dioxide in fabrication?
8. Explain the different steps in nMOS fabrication.
9. What is polysilicon? What is its use in fabrication process?
10. Explain the chemical vapour deposition technique.
11. Explain the different fabrication steps in CMOS.
12. Compare the p-well and n-well process in CMOS fabrication

Lecture-7

1. What is partitioning? Why do we need it?
2. What are the different levels of partitioning?
3. Consider a hypergraph H, where each hyperedge interconnects at most three vertices. We model each hyperedge of degree-3 with three edges of weight ½, on the same set of vertices, to obtain a weighted graph G. Prove that an optimal balanced partitioning of G corresponds to an optimal balanced partitioning of H.
4. In refer to Question 3, prove that optimal balanced partitioning of G cannot be done if each edge of H interconnects at most four vertices (i.e., give a counter example).
5. Explain Kernighan-Lin algorithm for partitioning a graph. Find its time complexity.
6. Consider a path graph $v_1, v_2, \ldots, v_n$. That is, v_1 is connected to v_{i+1}, for $1 < i < n-1$. Apply the Kernighan-Lin algorithm to this graph. As the initial partition, let v_a, for all odd values of a be in one set , and v_b, for all even values of b, be in the other set.
7. Consider a complete binary tree with n nodes. Apply Kernighan-Lin algorithm to this graph. As the initial partition, let v_a, for all internal vertices, be in one set and v_b, for all leaves, be in the other set.
8. Show how the Kernighan-Lin Heuristic works on the ladder graph with 2n vertices, starting with initial partition of $V_1 = \{1,2,3,\ldots\ldots,n\}$, and $V_2 = \{n+1,n+2,n+3,\ldots..,2n\}$.

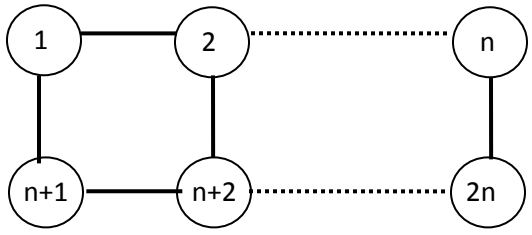

Fig.1

9. What are the drawbacks of Kernighan-Lin algorithm?
10. The following matrix provides 4 modules a,b,c,d with their entries representing the number of connections between the two modules. Apply Kernighan-Lin heuristic to obtain the partitioning.

	a	b	c	d
a	0	1	2	3
b	1	0	1	4
c	2	1	0	3
d	3	4	3	0

Fig.2

Lecture-8

1. What are the advantages of Fiduccia-Mattheyses algorithm over Kernighan-Lin algorithm?
2. What are the similarities between Fiduccia-Mattheyses algorithm and Kernighan-Lin algorithm?
3. Present the Fiduccia-Mattheyses Algorithm. Find out its time complexity.
4. Apply Fiduccia-Mattheyses Algorithm for the problem in question 7 of Lecture-7.
5. Apply Fiduccia-Mattheyses Algorithm for the problem in question 8 of Lecture-7.
6. Apply Fiduccia-Mattheyses Algorithm for the problem in question 10 of Lecture-7.
7. “There is a trade off associated for partitioning with replication.” Is it true or false? Justify.
8. Discuss how Partitioning is affecting overall delay.
9. What do you understand by performance driven partitioning?
10. Discuss the approach of clustering in case of partitioning