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CHAPTER 63

FIELD EFFECT TRANSISTORS

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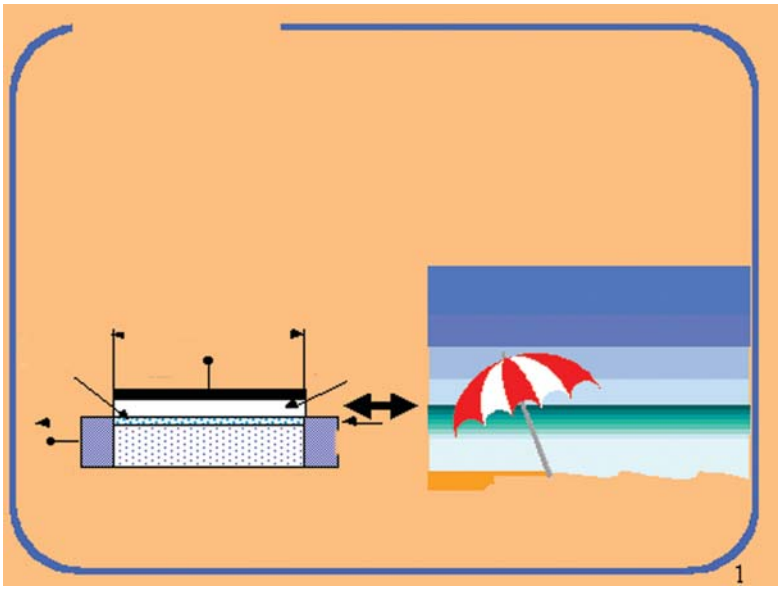

Field Effect Transistor as an Electronic Flute

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63.1. What is a FET ?

The acronym 'FET' stands for **field effect transistor**. It is a three-terminal unipolar solid-state device in which current is controlled ***by an electric field*** as is done in vacuum tubes. Broadly speaking, there are two types of FETs :

(a) junction field effect transistor (JFET)

(b) metal-oxide semiconductor FET (MOSFET)

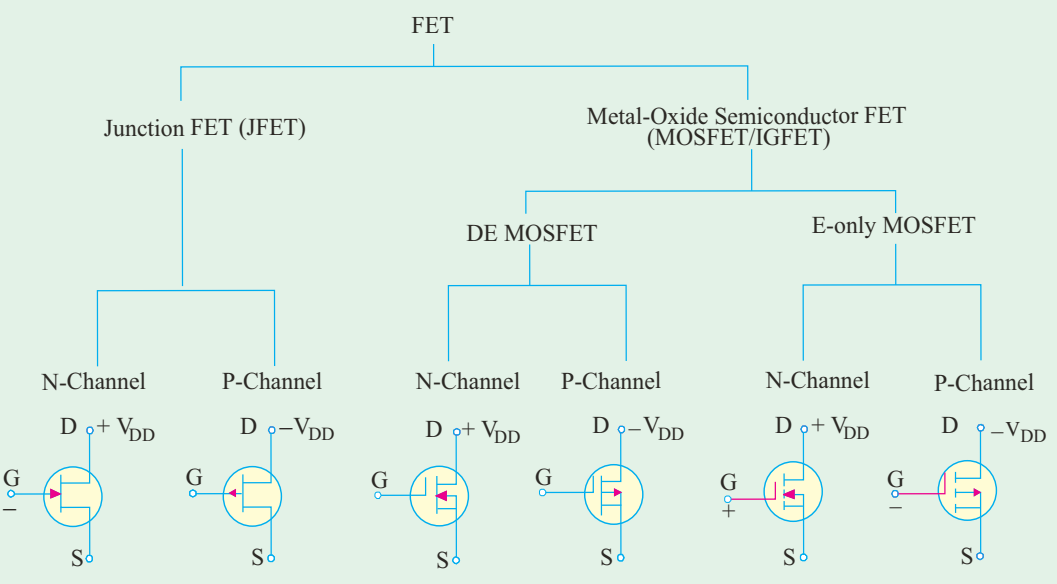
It is also called insulated-gate FET (IGFET). It may be further subdivided into :

(i) depletion-enhancement MOSFET *i.e.* DEMOSFET

(ii) enhancement-only MOSFET *i.e.* E-only MOSFET

Both of these can be either *P*-channel or *N*-channel devices.

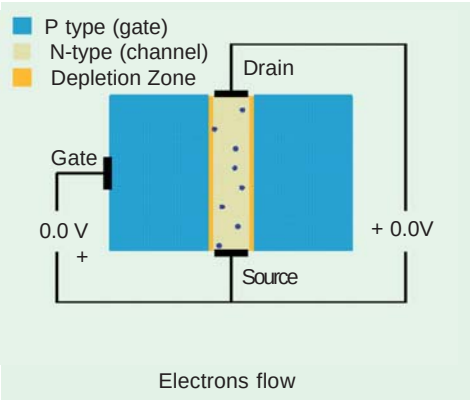
The FET family tree is shown below :



63.2. Junction FET (JFET)

(a) Basic Construction

As shown in Fig. 63.1, it can be fabricated with either an *N*-channel or *P*-channel though *N*-channel is generally preferred. For fabricating an *N*-channel JFET, first a narrow bar of *N*-type semiconductor material is taken and then two *P*-type junctions are diffused on opposite sides of its middle part [Fig. 63.1 (*a*)]. These junctions form two *P*-*N* diodes or **gates** and the area between these gates is called **channel**. The two *P*-regions are internally connected and a single lead is brought out which is called **gate terminal**. Ohmic contacts (direct electrical connections) are made at the two ends of the bar-one lead is called **source terminal** *S* and the other **drain terminal** *D*. When potential difference is established between drain and source, current flows along the length of the 'bar' through the channel located between the two *P*-regions. The current consists of **only majority carriers** which, in the present case, are electrons. *P*-channel JFET is



similar in construction except that it uses *P*-type bar and two *N*-type junctions. The majority carriers are holes which flow through the channel located between the two N-regions or gates.

Following FET notation is worth remembering:

1. **Source.** It is the terminal through which majority carriers enter the bar. Since carriers come from it, it is called the source.
2. **Drain.** It is the terminal through which majority carriers ***leave*** the bar *i.e.* they are drained out from this terminal. The drain-to-source voltage V_{DS} drives the drain current I_D.
3. **Gate.** These are two internally-connected heavily-doped impurity regions which form two *P*-*N* junctions. The gate-source voltage V_{GS} reverse-biases the gates.
4. **Channel.** It is the space between two gates through which majority carriers pass from source-to-drain when V_{DS} is applied.

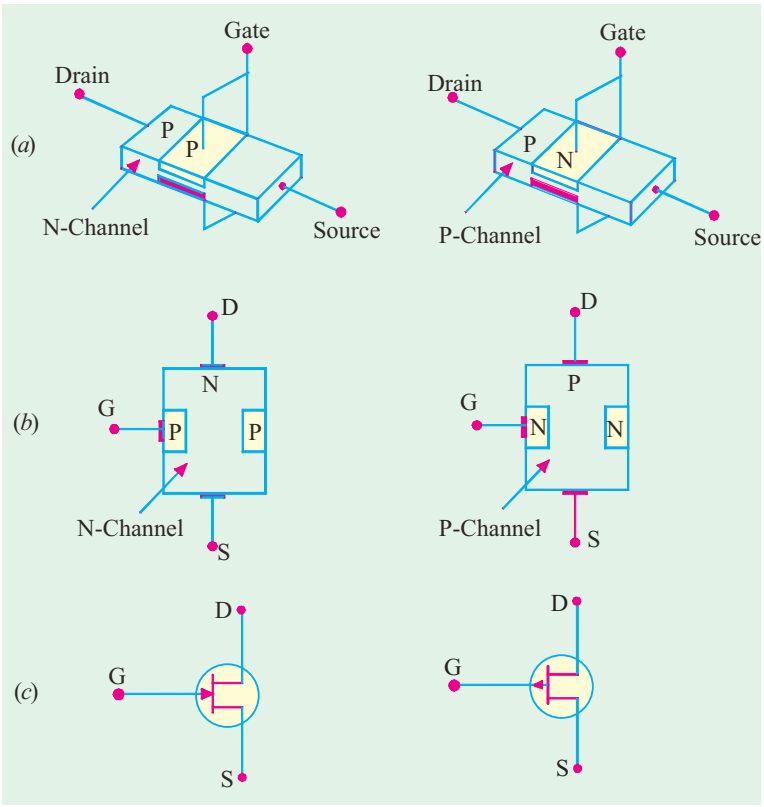


Fig. 63.1

Schematic symbols for *N*-channel and *P*-channel JFET are shown in Fig. 63.1 **(*c*)**. It must be kept in mind that **gate arrow always points to N-type material**.

(*b*) Theory of Operation

While discussing the theory of operation of a JFET, it should be kept in mind that

1. Gates are always reversed-biased. Hence, gate current I_G is practically zero.
2. The source terminal is always connected to that end of the drain supply which provides the necessary charge carriers. In an *N*-channel JFET, source terminal *S* is connected to the negative end of the drain voltage supply (for obtaining electrons). In a *P*-channel JFET, *S* is connected to the positive end of the drain voltage supply for getting holes which flow through the channel.

Let us now consider an ***N-channel*** JFET and discuss its working when either V_{GS} or V_{DS} or both are changed.

(*i*) When $V_{GS} = 0$ and $V_{DS} = 0$

In this case, drain current $I_D = 0$, because $V_{DS} = 0$. The depletion regions around the *P*-*N* junctions are of equal thickness and symmetrical as shown in Fig. 63.2 (*a*)

(*ii*) When $V_{GS} = 0$ and V_{DS} is increased from zero

For this purpose, the JFET is connected to the V_{DD} supply as shown in Fig. 63.2 (*b*). The electrons (which are the majority carriers) flow from *S* to *D* whereas conventional drain current I_D flows through the channel from *D* to *S*. Now, the gate-to-channel bias at any point along the channel is = $|V_{DS}| + |V_{GS}|$ *i.e.* the numerical sum of the two voltages. In the present case, external bias $V_{GS} = 0$.

Hence gate-channel reverse bias is provided by V_{DS} alone. Since the value of V_{DS} keeps decreasing (due to progressive drop along the channel) as we go from D to S, the gate-channel bias also decreases accordingly. It has maximum value in the drain-gate region and minimum in the source-gate region. Hence, depletion regions penetrate more deeply into the channel in the drain-gate region than in the source-gate region. This explains why the depletion regions become wedge shaped when V_{DS} is applied [Fig. 63.2 (*b*)]

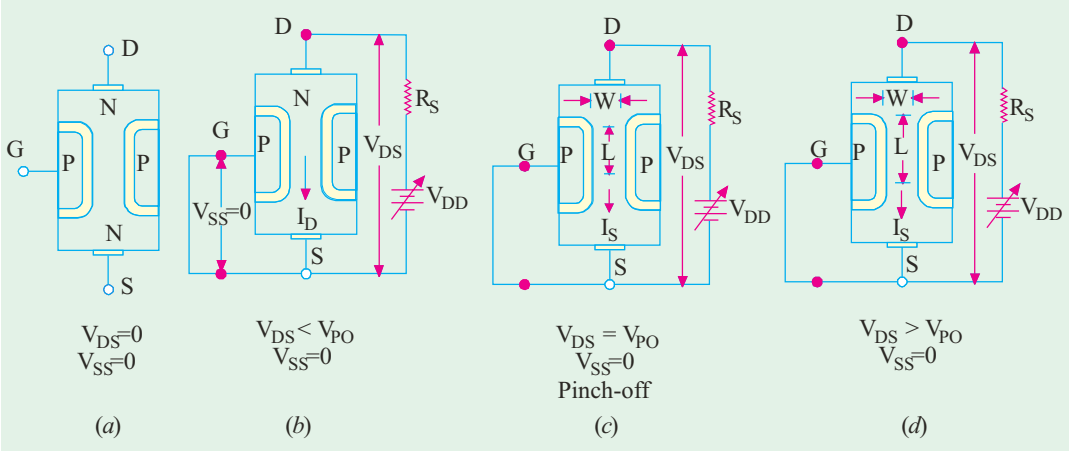


Fig. 63.2

As V_{DS} is gradually increased from zero, I_D increases proportionally as per Ohm's law. It is found that for small initial values of V_{DS}, the N-type channel material acts like a resistor of constant value. It is so because V_{DS} being small, the depletion regions are not large enough to have any significant effect on channel cross-section and, hence, its resistance. Consequently, I_D increases linearly as V_{DS} is increased from zero onwards (Fig. 63.5).

The ohmic relationship between V_{DS} and I_D continues till V_{DS} reaches a certain critical value called ***pinch-off voltage*** V_{PO} when drain current becomes constant at its maximum value called I_{DSS}. The SS in I_{DSS} indicates that the gate is shorted to source to make sure that $V_{GS} = 0$. This current is also known as ***zero-gate-voltage drain current.*** It is seen from Fig. 63.2(*c*) that under pinch-off conditions, separation between the depletion regions near the drain end reaches a minimum value W. It should, however, be carefully noted that ***pinch-off does not mean 'current-off '.*** In fact, I_D is maximum at pinch-off.

When V_{DS} is increased beyond V_{PO}, I_D remains constant at its maximum value I_{DSS} upto a certain point. It is due to the fact that further increase in V_{DS} (beyond V_{PO}) causes more of the channel on the source end to reach the minimum width as shown in Fig. 63.2 (*d*). It means that the channel width does not increase, instead its length L increases. As more of the channel reaches the minimum width, the resistance of the channel increases at the same rate at which V_{DS} increases. In other words, increase in V_{DS} is neutralized by increases in R_{DS}. Consquently, $I_D = (V_{DS} / R_{DS})$ remains unchanged even though V_{DS} is increased. Ultimately, a certain value of V_{DS} (called V_{DSO}) is reached when JFET breaks down and I_D increases to an excessive value as seen from drain characteristic of Fig. 63.5.

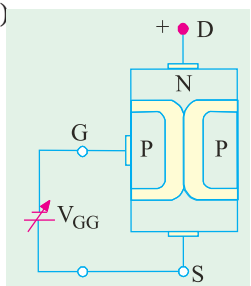


Fig. 63.3

(*iii*) When $V_{DS} = 0$ and V_{GS} is decreased from zero

In this case, as V_{GS} is made more and more negative, the gate reverse bias increases which increases the thickness of the depletion regions. As negative value of V_{GS} is increased, a stage comes when the two depletion regions touch each other as shown in Fig. 63.3. In this condition, the channel is said to be cut-off. This value of V_{GS} which cuts off the channel and

hence the drain current is called $V_{GS(off)}$.*

It may be noted that $V_{GS(off)} = -V_{PO}$ or $|V_{PO}| = |V_{GS(off)}|$. As seen from Fig. 63.6 because $V_{PO} = 4$ V, $V_{GS(off)} = -4$ V. Obviously, their absolute values are equal.

(*iv*) When V_{GS} is negative and V_{DS} is increased

As seen from Fig. 63.6, as V_{GS} is made more and more negative, values of V_P as well as breakdown voltage are decreased.

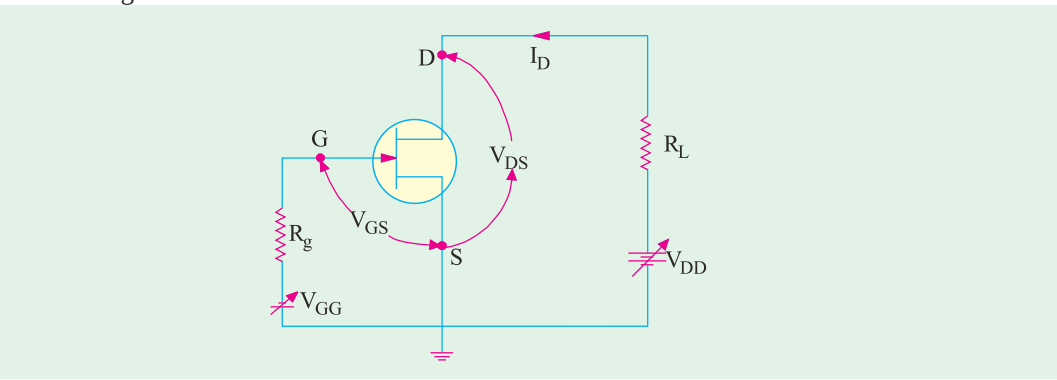


Fig. 63.4

Summary. Summarizing the above, we have that

(*i*) keeping V_{GS} at a fixed value (either zero or negative), as V_{DS} is increased, I_D initially increases till channel pinch-off when it becomes almost constant and finally increases excessively when JFET breaks down under high value of V_{DS}. As V_{GS} is kept fixed at progressively higher negative values, the values of V_P as well as breakdown voltage decrease.

(*ii*) keeping V_{DS} at a fixed value, as V_{GS} is made more and more negative, I_D decreases till it is reduced to zero for a certain value of V_{GS} called $V_{GS(off)}$.

Since gate voltage controls the drain current, JFET is called a ***voltage-controlled*** device. A *P*-channel JFET operates exactly in the same manner as an *N*-channel JFET except that current carriers are holes and polarities of both V_{DD} and V_{GS} are reversed.

Since only one type of majority carrier (either electrons or holes) is used in JFETs, they are called ***unipolar devices*** unlike bipolar junction transistors (*BJTs*) which use both electrons and holes as carriers.

63.3. Static Characteristics of a JFET

We will consider the following two characteristics:

(*i*) drain characteristic

It gives relation between I_D and V_{DS} for different values of V_{GS} (which is called running variable).

(*ii*) transfer characteristic

It gives relation between I_D and V_{GS} for different values of V_{DS}.

We will analyse these characteristics for an *N*-channel JFET connected in the common-source mode as shown in Fig. 63.4. We will first consider the drain characteristic when $V_{GS} = 0$ and then when V_{GS} has any negative value upto $V_{GS(off)}$.

63.4. JFET Drain Characteristic With $V_{GS} = 0$

Such a characteristic is shown in Fig. 63.5 and has been already discussed briefly in Art. 63.2. It can be subdivided into following four regions :

1. Ohmic Region OA

This part of the characteristic is linear indicating that for low values of V_{DS}, current varies directly with voltage following Ohm's Law. It means that JFET behaves ***like an ordinary resistor*** till

* It has negative value for an N-channel JFET but a positive value or a P-channel JFET.

point *A* (called knee) is reached.

2. Curve AB

In this region, I_D increases at reverse square-law rate upto point *B* which is called **pinch-off point**. This progressive decrease in the rate of increase of I_D is caused by the square law increase in the depletion region at each gate upto point *B* where the two regions are closest without touching each other. The drain-to-source voltage V_{DS} corresponding to point *B* is called ***pinch-off voltage Vp*.*** But it is essential to remember that ***"pinch-off "*** does not mean ***"current-off".***

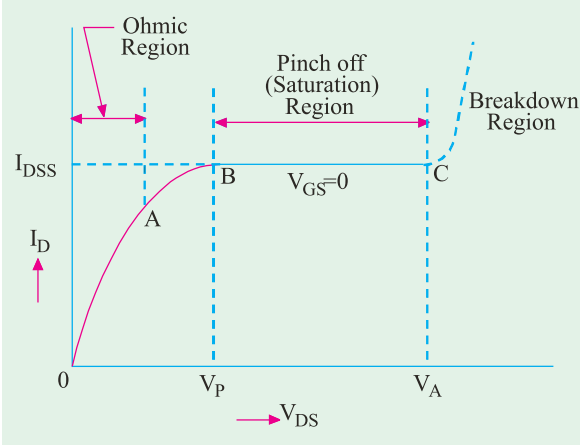


Fig. 63.5

3. Pinch-off Region BC

It is also known as **saturation region** or **'amplified' region**. Here, JFET operates as a constant-current device because I_D is relatively independent of V_{DS}. It is due to the fact that as V_{DS} increases, channel resistance also increases proportionally thereby keeping I_D practically constant at I_{DSS}. It should also be noted that the reverse bias required by the gate-channel junction is supplied entirely by the voltage drop across the channel resistance due to flow of I_{DSS} and none by external bias because $V_{GS} = 0$.

Drain current in this region is given by Shockley's equation

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(I-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$

It is the normal operating region of the JFET when used as an amplifier.

4. Breakdown Region

If V_{DS} is increased beyond its value corresponding to point *C* (called avalanche breakdown voltage), JFET enters the breakdown region where I_D increases to an excessive value. This happens because the reverse-biased gate-channel *P-N* junction undergoes avalanche breakdown when small changes in V_{DS} produce very large changes in I_D.

It is interesting to note that increasing values of V_{DS} make a JFET behave first as a resistor (ohmic region), then as a constant-current source (pinch-off region) and finally, as a constant-voltage source (breakdown region).

63.5. JFET Characteristics With External Bias

Fig. 63.6 shows a family of I_D versus V_{DS} curves for different values of V_{GS}. It is seen that as the negative gate bias voltage is increased

(i) pinch off voltage is reached at a lower value of I_D than when $V_{GS} = 0$.

(ii) value of V_{DS} for breakdown is decreased.

When an external bias of, say, –1V is applied between the gate and source, the *P-N* junctions become reverse-biased even when $I_D = 0$. Hence,

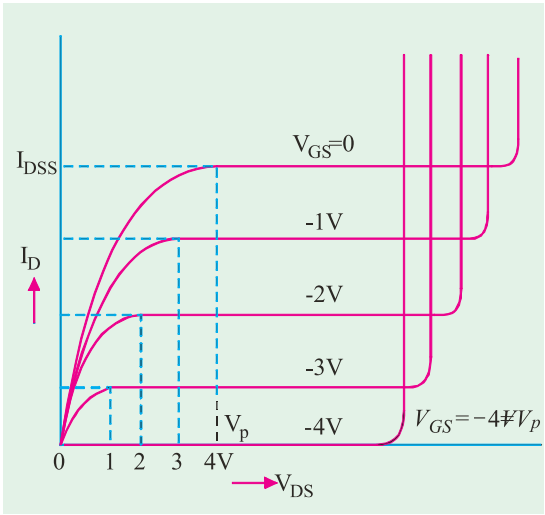


Fig. 63.6

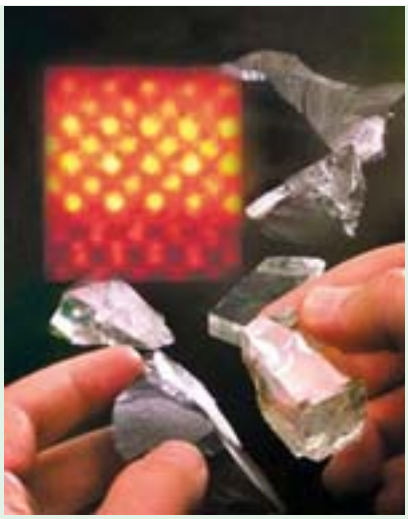
* It is numerically equal to $V_{GS(off)}$ *i.e.* $V_p = / V_{GSC(off)}/$

the depletion regions are already formed which penetrate the channel to a certain extent.

The amount of reverse bias required to be produced by I_D would, obviously, be decreased by 1V. In other words, a smaller voltage drop along the channel (*i.e.* smaller than when $V_{GS} = 0$) will increase the depletion regions to the point where they will pinch off the current. Consequently, V_P is reached at a lower I_D value than when $V_{GS} = 0$.

Now, let us see why value of V_{DS} for breakdown is decreased as the negative gate bias voltage is increased. It is simply due to the fact that V_{GS} keeps adding to the reverse bias at the junction produced by current flow.

It is seen that with $V_{GS} = 0$, I_D saturates at I_{DSS} and the characteristic shows $V_P = 4$V. When an external bias of –1 *V* is applied, gate-channel junctions still require –4 V to achieve pinch-off (remember, $V_{GS} = -V_P$). It means that a 3V drop is now required along the channel instead of the previous 4V. Obviously, this 3V drop can be achieved with a lower value of I_D. Similarly, when V_{GS} is –2V and –3V, pinch-off is achieved with 2 V and 1 V respectively along the channel.



This micrograph shows a mock field effect transistor with a layer of crystalline strontium titanate instead of silicon dioxide as the gate electrode.

These drops of 2 V and 1V are obtained with further-reduced values of I_D. As seen, when $V_{GS} = -4$ V (*i.e.* numerically equal to V_P), no channel drop is required. Hence, I_D is zero.

In general, $V_P = V_{DS(P)} - V_{GS}$ where $V_{DS(P)}$ is the pinch-off value of V_{DS} for a given value of V_{GS}.

63.6. Transfer Characteristic

It is a plot of I_D versus V_{GS} for a constant value of V_{DS} and is shown in Fig. 63.7. It is similar to the transconductance characteristics of a vacuum tube or a transistor. It is seen that when $V_{GS} = 0$, $I_D = I_{DSS}$ and when $I_D = 0$, $V_{GS} = V_P$. The transfer characteristic approximately follows the equation.

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$

The above equation can be written as

$$V_{GS} = V_{GS(off)}\left(1-\sqrt{\frac{I_D}{I_{DSS}}}\right)$$

This characteristic can be obtained from the drain characteristics by reading off V_{GS} and I_{DSS} values for different values of V_{DS}.

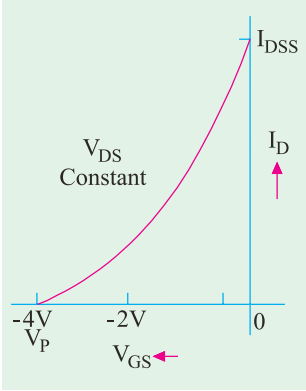


Fig. 63.7

63.7. Small Signal JFET Parameters

The various parameters of a JFET can be obtained from its two characteristics. The main parameters of a JFET when connected in common-source mode are as under :

(*i*) AC Drain Resistance, r_d

It is the ac resistance between drain and source terminals when JFET is operating ***in the pinch-off region.*** It is given by

$$r_d = \frac{\text{change in } V_{DS}}{\text{change in } I_D}\bigg|_{V_{GS}\ \text{constant}} \quad \text{or} \quad r_d = \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{V_{GS}}$$

An alternative name is ***dynamic drain resistance.*** It is given by the slope of the drain characteristic in the pinch-off region. It is sometimes written as r_{ds} emphasizing the fact that it is the resistance from drain to source. Since r_d is usually the output resistance of a JFET, it may also be expressed as an output admittance y_{os}. Obviously, $y_{os} = 1/r_d$. It has a very high value.

(*ii*) Transconductance, g_m

It is simply the slope of transfer characteristic.

$$g_m = \frac{\text{change in } I_D}{\text{change in } V_{GS}} - V_{DS} \text{ constant or } \quad g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Big| V_{DS}$$

Its unit is Siemens (*S*) earlier called ***mho.*** It is also called ***forward transconductance (g_{fs}) or forward transadmittance y_{fs}.***

The transconductance measured at I_{DSS} is written as g_{mo}.

Mathematical Expression for g_m

The Shockley equation* is $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

Differentiating both sides, we have

$$\frac{dI_D}{dI_{DSS}} = 2I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)\left(-\frac{1}{V_P}\right) \quad \text{or} \quad g_m = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right)$$

When $V_{GS} = 0$, $g_m = g_{mo}$ $\therefore$ $g_{mo} = -\frac{2I_{DSS}}{V_P}$

From the above two equations, we have $g_m = g_{mo}\left(1 - \frac{V_{DSS}}{V_P}\right) = g_{mo}\sqrt{\frac{I_D}{I_{DSS}}}$

(*iii*) Amplification Factor, μ

It is given by $\mu = \frac{\text{change in } V_{DS}}{\text{change in } V_{GS}} - I_D$ constant or $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \Big| I_D$

It can be proved from above that $\mu = g_m \times r_d = g_{fs} \times r_d$

(*iv*) DC Drain Resistance, R_{DS}

It is also called the static or ohmic resistance of the channel. It is given by

$$R_{DS} = \frac{V_{DS}}{I_D}$$

Example 63.1. *For an N-channel JFET, $I_{DSS} = 8.7$ mA, $V_P = -3$ V, $V_{GS} = -1$ V. Find the values of (i) I_D (ii) g_{mo} (iii) g_m* **(Basic Electronics, Bombay Univ., 1985)**

Solution. (*i*) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8.7\left(1 - \frac{-1\text{ V}}{-3\text{ V}}\right)^2 =$ **3.87 A**

(*ii*) $g_{mo} = \frac{-2I_{DSS}}{V_P} = \frac{-2 \times 8.7}{-3} =$ **5.8 mS**

(*iii*) $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) = 5.8\left(1 - \frac{-1}{-3}\right) =$ **3.87 mS**

* Because of the squared term in the equation, JFET and MOSFET are referred to as square-law devices.

63.8. DC Biasing of a JFET

A JFET may be biased by using either

1. a separate power source V_{GG} as shown in Fig. 63.8 (*a*),
2. some form of self-bias as shown in Fig. 63.8 (*b*),
3. source bias as in Fig. 63.8 (*c*),
4. voltage divider bias as in Fig. 63.8 **(*d*).**

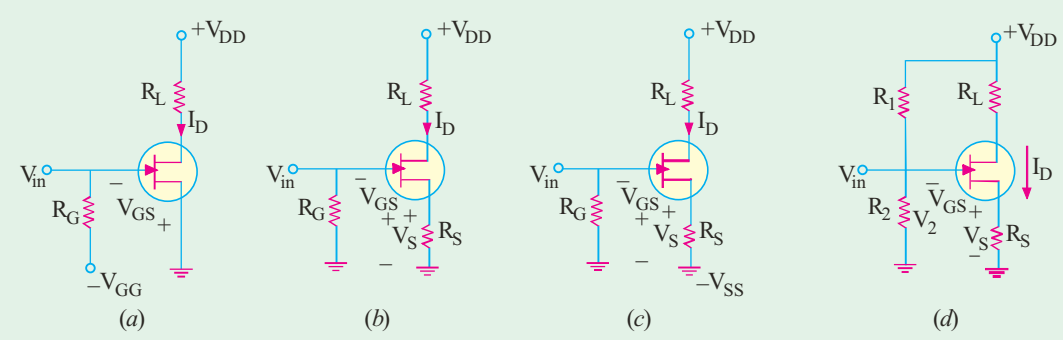


Fig. 63.8

The circuit of Fig. 63.8 (*b*) is called self-bias circuit because the V_{GS} bias is obtained from the flow of JFET's own drawn current I_D through R_S.

$\therefore \qquad V_S = I_D R_S \quad$ and $\quad V_{GS} = - I_D R_S$

The gate is kept at this much negative potential with respect to the ground.

The addition of R_G in Fig. 63.8 (*b*), does not upset this dc bias for the simple reason that no gate current flows through it (the gate leakage current is almost zero). Hence, gate is essentially at ***dc ground***. Without R_G, gate would be kept 'floating' which could collect charge and ultimately cut-off the JFET.

The resistance R_G additionally serves the purpose of avoiding short-circuiting of the ac input voltage, v_{in}. Moreover, in case leakage current is not totally negligible, R_G would provide it an escape route. Otherwise, the leakage current would build up static charge (voltage) at the gate which could change the bias or even destroy the JFET.

Fig. 63.8 (*c*) shows the *source* bias circuit which employs a self-bias resistor R_S to obtain V_{GS}. Here, $V_{SS} = I_D R_S + V_{GS}$ or $V_{GS} = V_{SS} - I_D R_S$.

Fig. 63.8 (*d*) shows the familiar voltage divider bias. In this case, $V_2 = V_{GS} + I_D R_S$ or $V_{GS} = V_2 - I_D R_S$

Since, $\quad V_2 = V_{DD} \dfrac{R_2}{R_1 + R_2}$ $\qquad \therefore \; V_{GS} = V_{DD} \dfrac{R_2}{R_1 + R_2} - I_D R_S$

Example 63.2 . *Find the values of V_{DS} and V_{GS} in Fig. 63.9 for I_D = 4 mA.*
(Applied Electronics-I, Punjab Univ. 1992)

Solution. $\quad V_S = I_D R_S = 4 \times 10^{-3} \times 500 = 2.0$ V

$V_D = V_{DD} - I_D R_L = 12 - 4 \times 1.5 = 6$ V

$\therefore \quad V_{DS} = V_D - V_S = 6 - 2 = 4$ V

Since $\quad V_G = 0, V_{GS} = V_G - V_S = 0 - 2.0 =$ **– 2.0 V**

63.9. DC Load Line

The dc load line for a JFET can be easily drawn by remembering the following two points :

(i) At $\quad I_D = 0, V_{DS} = V_{DD}$

(ii) At $\quad V_{DS} = 0, \quad I_D = \dfrac{V_{DD}}{R_L}$

The *Q*-point is generally situated at the middle point of the load line (for class-A operation) so that

$$V_{DSQ} = \frac{1}{2}V_{DD}$$

$$\text{Also,} \quad I_{DSQ} = \frac{\frac{1}{2}V_{DD}}{R_s + R_L}$$

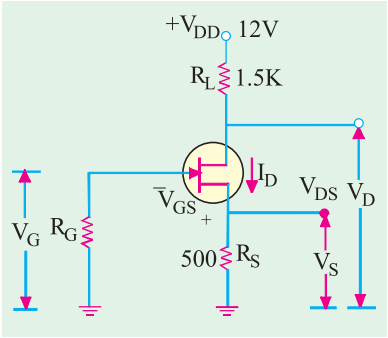


Fig. 63.9

Example 63.3. *For the circuit of Fig. 63.11, find the values of V_{DSQ} and V_{GS} assuming centrally-located Q-point and zero gate current.*

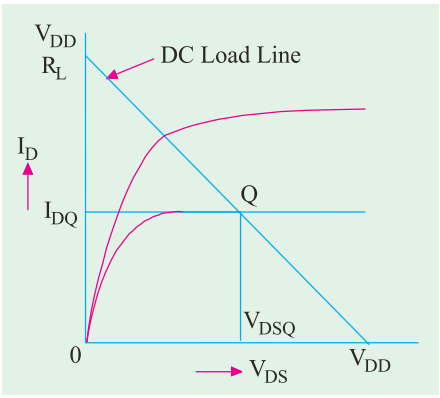


Fig. 63.10

Solution. Since $I_G = 0$, dc circuit is not disturbed.

$$V_{DS} = \frac{1}{2}V_{DD} = \frac{12}{2} = \mathbf{6V}$$

The balance of 6 V drops across series combination of R_L and R_S.

$$\therefore \quad I_D = \frac{6}{150+450} = \mathbf{10\ mA}$$

$$\therefore \quad V_{GS} = -I_D R_S = -10 \times 150 = \mathbf{1.5\ V}$$

It is obvious that gate is 1.5 V negative with respect to the source which is the common point. Incidentally, in common source connection of a JFET, ***gate is the most negative point in the entire circuit.***

Example 63.4. *What values of R_S and R_L are required for the circuit of Fig. 63.12 for setting up an approximate mid-point bias ? The JFET parameters are : $I_{DSS} = 16$ mA, $V_{GS(off)} = -8$ V and $V_D = \frac{1}{2}V_{DD}$.*

Solution. It should be noted that as found from Shockley's equation, for mid-point bias, $I_D \cong I_{DSS}/2$ and $V_{GS} = V_{GS(off)}/4$. Hence, for mid-point bias

$$I_D \cong 16/2 = 8\ \text{mA}$$

$$V_{GS} = \frac{1}{4}V_{GS(off)} = -\frac{8}{4} = -2\text{V}$$

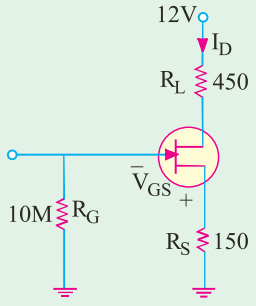


Fig. 63.11

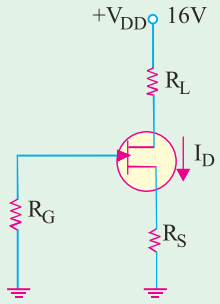


Fig. 63.12

$$R_S = \frac{V_{GS}}{I_D} = \frac{2\text{ V}}{8\,mA} = \mathbf{250\ \Omega}$$

Now, $V_D = V_{DD} - I_D R_L$, $R_L = \dfrac{V_{DD} - V_D}{I_D} = \dfrac{16-8}{8\text{mA}}$

$= \mathbf{1000\ \Omega}$

Example 63.5. *Determine the quiescent value of V_{GS} I_D and V_{DS} for the JFET circuit of Fig. 63.13 given that I_{DSS} = 10 mA, R_S = 5 K and V_P = –5 V.*

(Electronic Devices & Circuits, Pune Univ. 1991)

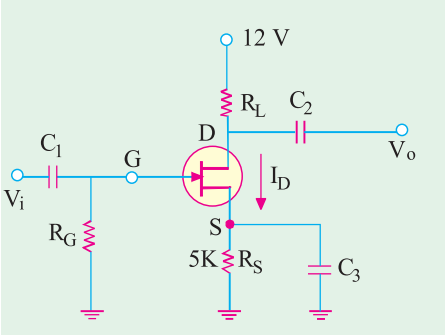


Fig. 63.13

Solution. Since $I_S \cong I_D$, $V_{GS} = -I_D R_S = -5000\ I_D$

Now, $I_D = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2 = 10 \times 10^{-3}\left(1 - \dfrac{V_{GS}}{-5}\right)^2$

$= 10 \times 10^{-3}(1 + 0.2\ V_{GS})^2$

Substituting this value in the above equation, we get

$V_{GS} = -5000(10 \times 10^{-3})(1 + 0.2\ V_{GS})$

Expanding and rearranging the above, we have

$2V_{GS}^2 + 21V_{GS} + 50 = 0$

$\therefore \quad V_{GS} = -3.65\text{ V} \quad \text{or} \quad -6.85\text{ V}$

Rejecting the higher value because it is more than V_P, we have $V_{GS} = \mathbf{-3.65\ V}$

$\therefore \quad -3.65 = -5000\ I_D \quad \therefore \quad I_D = \mathbf{0.73\ mA}$

$V_D = V_{DD} - I_D R_L = 12 - 0.73 \times 2 = \mathbf{1.54\ V}$

$V_S = I_D R_S = 0.73 \times 5 = 3.65\ V \quad \therefore \quad V_{DS} = V_D - V_S = 10.54 - 3.65 = \mathbf{6.89\ V}$

63.10. Common Source JFET Amplifier

A simple circuit for such an amplifier is shown in Fig. 63.14. Here, R_G serves the purpose of providing leakage path to the gate current, R_S develops gate bias, C_3 provides ac ground to the input signal and R_L acts as drain load.

Working

When ***negative-going*** signal is applied to the input

1. gate ***bias is increased,***
2. depletion regions are ***widened,***
3. channel resistance is ***increased,***
4. ***I_D is decreased,***
5. drop across R_L is ***decreased,***
6. Consequently, a ***positive-going*** signal becomes available at the output through C_2 in Fig. 63.14.

When ***positive-going signal*** is applied at the input, then in a similar way, ***a negative-going signal*** becomes available at the output.

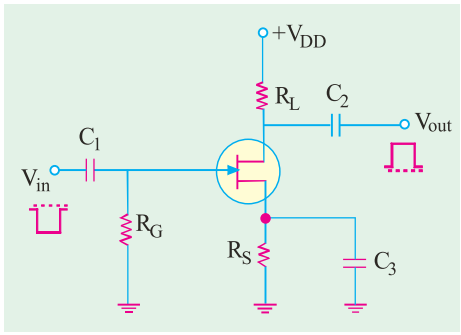


Fig. 63.14

It is seen that there is a ***phase inversion*** between the input signal at the gate and output signal at the drain.

63.11. JFET Amplifier Gains

We will now find the expressions for voltage gain, input resistance, output resistance and input capacitance of a JFET amplifier when connected in different modes. The different capacitance due to *P-N* junction and channel are shown in Fig. 63.15

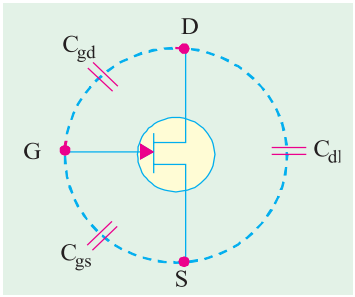


Fig. 63.15

(*a*) Common Source JFET Amplifier (Fig. 63.16)

(*i*) Input Resistance $r'_i = R_G \| R_{GS}$

In an ideal JFET, R_{GS} is infinite because $I_G = 0$. In an actual device, however, R_{GS} is not actually infinite but extremely high (100 M or so) as compared to R_G. Hence, $r_i' \cong R_G$.

(*ii*) Output Resistance $r_o' = r_d \| R_L \cong R_L$ — if $r_d \gg R_L$

(*iii*) Voltage Gain

$$V_o = i_d \times r_d \| R_L \qquad \text{Now,} \quad i_d = -g_m \times v_i$$

$$\therefore \quad V_o = -g_m V_i \times (r_d \| R_L)$$

$$\therefore \quad A_v = \frac{V_o}{V_i} = \frac{-g_m V_i \times (r_d \| R_L)}{V_i} = \frac{-g_m r_d R_L}{r_d + R_L} = \frac{-\mu R_L}{r_d + R_L}$$

Also, $A_v = -g_{fs} \times (r_d \| R_L)$

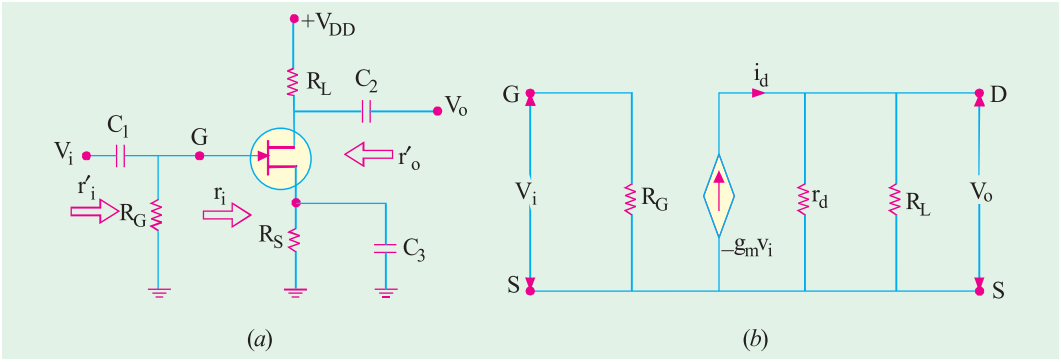


Fig. 63.16

(*iv*) Input Capacitance

The input capacitance is C_{gs} which is increased because of Miller effect.

$$\therefore \quad C_i = C_{gs} + (1 - A_v)\, C_{gd}.$$

It is the large value of C_{gd} which is harmful in high-frequency work.

Example 63.6. *The common-source amplifier of Fig. 63.16 (a) has $r_d = 100$ K, $R_L = 10$ K, $g_m = 3000$ µS, $C_{gs} = 3$ pF and $C_{gd} = 1.5$ pF. Compute its (i) A_v and (ii) C_i.*

Solution. ***(i)*** $$A_v = \frac{-g_m r_d R_L}{r_d + R_L}$$

$$= \frac{-3000 \times 10^{-6} \times 100 \times 10^3 \times 10 \times 10^3}{(100 \times 10^3) + (10 \times 10^3)} = \mathbf{-27.3}$$

(ii) $$C_i = C_{gs} + (1 - A_v)\, C_{gd}$$

$$= 3 + (1 + 27.3) \times 1.5 = \mathbf{45.5\ pF}.$$

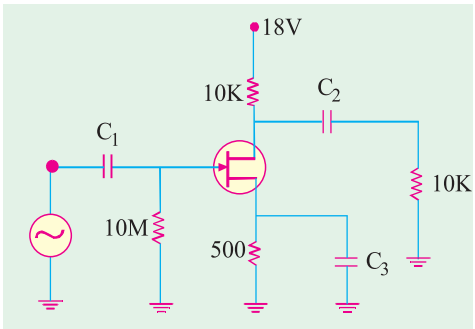


Fig. 63.17

Example 63.7. *The JFET shown in Fig. 63.17 has g_m = 3000 μS and r_{ds} = 100 K. Calculate the voltage gain of the CS amplifier circuit.* **(Basic Electronics, Bombay Univ. 1992)**

Solution. As seen from Art. 63.11 (*a*)

$$A_v = -g_m \times (r_{ds} \| r_L)$$

Now, $r_L = 10\text{ K} \| 10\text{ K} = \mathbf{5\text{ K}}$

$\therefore$ $r_{ds} \| r_L = 100\text{ K} \| 5\text{ K} = \mathbf{4.76\text{ K}}$

$\therefore$ $A_v = -3000 \times 10^{-6} \times 4.76 = \mathbf{-14.3}$

(*b*) Common Drain JFET Amplifier

In the common-drain circuit (also called source follower), the load resistance is in series with the source terminal. There is no drain resistor as shown in Fig. 63.18 (*a*). The input signal is applied to the gate through the capacitor C_1 and the output is taken out from the source *via* C_2. The common-drain equivalent circuit is shown in Fig. 63.18 *(b)*. The current generator is g_m, V_{gs} where $v_{gs} = (V_i - V_o)$. Moreover, $R_G = R_1 \| R_2$.

(*i*) Voltage Gain

$$V_o = i_d \times (r_d \| R_L). \qquad \text{Since,} \quad i_d = g_m V_{gs} = g_m (V_i - V_o),$$

$$\therefore \quad V_o = g_m (V_i - V_o) \times (r_d \| R_L) = g_m (V_i - V_o), \frac{r_d R_L}{r_d + R_L}$$

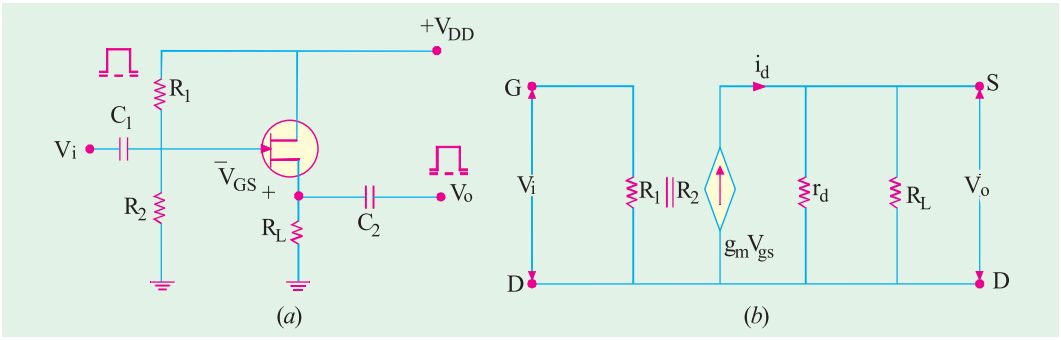


Fig. 63.18

Solving for V_o, we get

$$V_o = g_m V_i \frac{r_d R_L}{r_d + R_L + g_m r_d R_L} \qquad ...(i)$$

$$\therefore \quad A_v = \frac{V_o}{V_i} = \frac{r_d R_L}{r_d + R_L + g_m r_d R_L} \cong 1 \qquad \text{– if } g_m r_d R_L \gg (r_d + R_L)$$

(*ii*) Input Resistance

$r'_{in} = R_1 \| R_2$ – for circuit of Fig. 63.18 (*a*) only.

(*iii*) Output Resistance

In Eq. (*i*) above, $g_m V_i$ is a current which is directly proportional to V_i and $(r_d R_L)/(r_d + R_L + g_m r_d R_L)$ = a resistance, r_o.

$$\therefore \quad r'_o = \frac{r_d R_L}{r_d + R_L (1 + g_m r_d R_L)} = \frac{[r_d / (1 + g_m r_d)] \times R_L}{[r_d / (1 + g_m r_d)] + R_L}$$

$$= \frac{r_d}{1 + g_m r_d} \| R_L \cong \frac{1}{g_m} \| R_L$$

The above result helps us to draw the modified equivalent circuit of Fig. 63.19 for the common-drain amplifier.

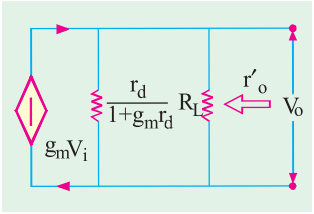


Fig. 63.19

Example 63.8. *The common-drain circuit of Fig. 63.18 (a) uses a JFET having the following parameters :*

$r_d = 100\ K$, $g_m = 3000\ \mu S$ *and* $R_L = 10\ K$

Calculate ***(i)*** A_v *and* ***(ii)*** r'_o.

Solution. ***(i)*** $A_v = g_m \dfrac{r_d R_L}{r_d + R_L + g_m r_d R_L}$

$$= 3000\times10^{-6} \frac{100\times10^3 \times 10\times10^3}{(100\times10^3)+(10\times10^3)+(3000\times10^{-6}\times100\times10^3\times10\times10^3)} = \mathbf{0.965}$$

(ii) $r'_0 = R_L \,\|\, \dfrac{r_d}{1+g_m r_d}$

Now, $\dfrac{r_d}{1+g_m r_d} = \dfrac{100\times10^3}{1+3000\times10^{-6}\times100\times10^3} = \mathbf{330\ \Omega}$

$r'_o = 10\ K \,\|\, 330\ \Omega \cong \mathbf{320\ \Omega}$

(*c*) Common Gate JFET Amplifier

In this amplifier configuration, input signal is applied to the source terminal and output is taken from the drain as shown in Fig. 63.20 (*a*). The gate is grounded, R_L is in series with drain and a source resistance R_S is included in the circuit across which V_i is dropped.

The ac equivalent circuit is shown in Fig. 63.20 (*b*) where current source is connected between the ***drain and the source terminals as always.*** However, since source and drain are the input and output terminals respectively, ($g_m V_{gs}$) appears between the input and the output.

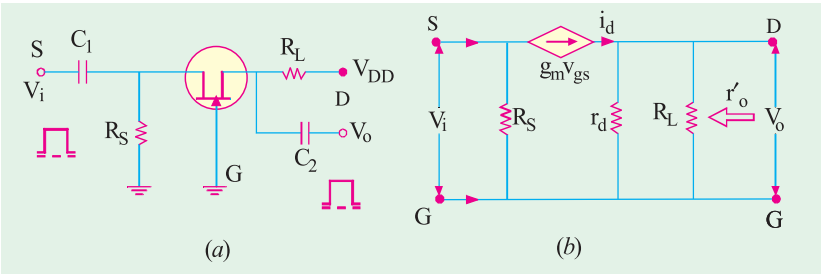


Fig. 63.20

(*i*) Voltage Gain

$$V_o = i_d \times (r_d \,\|\, R_L) = i_d \cdot \frac{r_d R_L}{r_d + R_L}$$

Now, $i_d = g_m V_{gs} = g_m V_i$ $\quad\therefore\quad V_o = g_m V_i \cdot \dfrac{r_d R_L}{r_d + R_L}$ $\quad\therefore\quad A_v = \dfrac{V_o}{V_i} = \dfrac{g_m r_d R_L}{r_d + R_L}$

It is the same as the gain for a common source amplifier except that it is a positive quantity. It means that V_o and V_i are in phase as shown in Fig. 63.20 (*a*).

(*ii*) Input Resistance

If we ignore current through R_S, then as seen from the ac equivalent circuit of Fig. 63.20 (*b*), input current is i_d. Now, $i_d = g_m V_{gs} = g_m V_i$.

The input resistance of the device *i.e.* JFET is $r_i = \dfrac{V_i}{i_d} = \dfrac{V_i}{g_m V_i} = \dfrac{1}{g_m}$

The input resistance of the *circuit* is $r_i' = r_i \| R_S = \dfrac{1}{g_m} \| R_s$

Actually speaking, r_d and R_L are also involved in r_i' but their effect is negligible.

(*iii*) Output Resistance

As seen from the equivalent circuit of Fig. 63.20 (*b*), $r_o' = r_d \| R_L$.

Here, only input capacitance of importance is C_{gs}. Hence, this circuit has low input capacitance as compared to common-source circuit where input capacitance is increased due to Miller effect.*

63.12. Advantages of FETs

FETs combine the many advantages of both BJTs and vacuum tubes. Some of their main advantages are :

1. high input impedance, **2.** small size, **3.** ruggedness, **4.** long life,
5. high frequency response, **6.** low noise,
7. negative temperature coefficient, hence better thermal stability,
8. high power gain,
9. a high immunity to radiations,
10. no offset voltage when used as a switch (or chopper), **11.** square law characteristics.

The only disadvantages are :

1. small gain-bandwidth product,
2. greater susceptibility to damage in handling them.

Tutorial Problems No. 63.1

1. For a particular *N*-channel JFET, $V_{GS(off)} = -4$ V. What would be the value of I_D when $V_{GS} = -6$ V?
[zero]

2. For the *N*-channel JFET shown in Fig. 63.21, $V_P = 8$V and $I_{DSS} = 12$ mA. What would be the value of (*i*) V_{DS} at which pinch-off begins and (*ii*) value of I_D when V_{DS} is above pinch-off but below the breakdown voltage ?
[3V ; 12 mA]

3. The data sheet of a JFET indicates that it has $I_{DSS} = 15$ mA and $V_{GS(off)} = -5$ V. Calculate the value of I_D when V_{GS} is (*i*) 0, (*ii*) –1 V and (*iii*) – 4 V.
[(*i*) 15 mA (*ii*) 9.6 mA (*iii*) 0.6 mA]

4. The data sheet of a JEET gives the following information.
$I_{DSS} = 20$ mA, $V_{GS(off)} = -8$ V. and $g_{mo} = 4000$ µS.
Calculate the value of I_D and g_m for $V_{GS} = -4$ V.
[5 mA ; 2000 µS]

5. For a JEET, I_{DSS} 5 mA and $g_{mo} = 4000$ µS.
Calculate (*i*) $V_{GS(off)}$ and (*ii*) gm at mid-point bias.
[(*i*) –5 V (*ii*) 3000 µS]

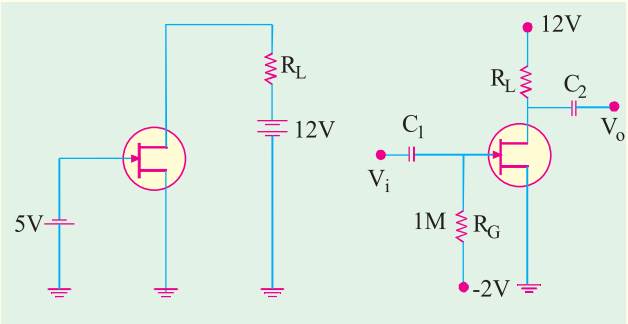


Fig. 63.21

Fig. 63.22

6. At a certain point on the transfer characteristics of an N-channel JFET, following values are read : $I_{DSS} = 8.4$ mA, $V_{GS} = -0.5$ V and $V_P = -3.0$ V.
Calculate (*i*) g_{mo} and (*ii*) g_m at the point.
[(*i*) 5600 µS (*ii*) 4670 µS]

7. For the JFET circuit of Fig. 63.22, $I_{DSS} = 9$ mA and $V_P = -3$ V.
Find the value of R_L for setting the value of V_{DS} at 7 V.
[5 K]
(Hint : $V_{GS} = -2$ V as $I_G = 0$)

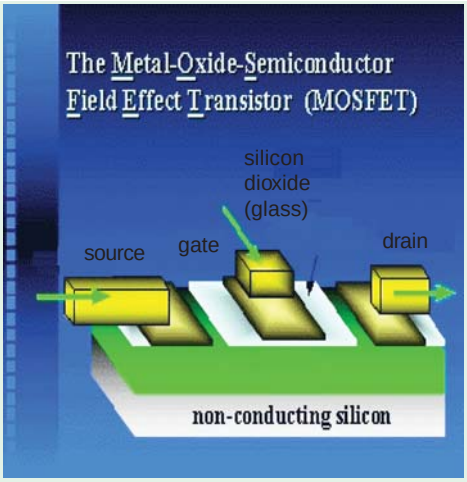
* Miller effect occurs only where output is antiphase with input as *CS* amplifier circuit.

63.13. MOSFET or IGFET

It could be further subdivided as follows :

(*i*) Depletion-enhancement MOSFET or DE MOSFET

This MOSFET is so called because it can be operated in both ***depletion*** mode and ***enhancement*** mode by changing the polarity of V_{GS}. When negative gate-to-source voltage is applied, the *N*-channel DE MOSFET operates in the depletion mode. However, with positive gate voltage, it operates in the enhancement mode. Since a channel exists between drain and source, I_D flows even when $V_{GS} = 0$. That is why DE MOSFET is known as **normally-ON MOSFET.**



Metal-oxide semiconductor field effect transistor

(*ii*) Enhancement-only MOSFET

As its name indicates, this MOSFET operates only in the enhancement mode and has no depletion mode. It works with ***large positive*** gate voltages only. It differs in construction from the DE MOSFET in that structurally ***there exists no channel between the drain and source.*** Hence, it does not conduct when $V_{GS} = 0$. That is why it is called **normally-OFF** MOSFET.

In a DE MOSFET, I_D flows even when $V_{GS} = 0$. It operates in depletion mode with negative values of V_{GS}. As V_{GS} is made more negative, I_D decreases till it ceases when $V_{GS} = V_{GS(off)}$. It works in enhancement mode when V_{GS} is positive as shown in Fig. 63.24 (*b*).

In the case of E-only MOSFET, I_D flows only when V_{GS} exceeds $V_{GS(th)}$ as shown in Fig. 63.30 (*c*).

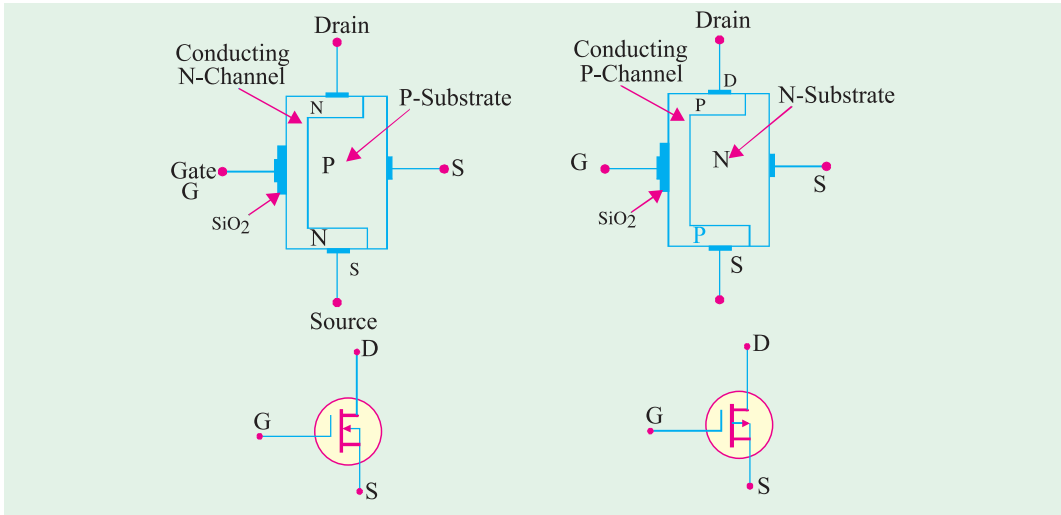


Fig. 63.23

63.14. DE MOSFET

(*a*) Construction

Like JFET, it has source, gate and drain. However, as shown in Fig. 63.23, its gate is insulated from its conducting channel by an ultra-thin metal-oxide insulating film (usually of silicon dioxide SiO_2). Because of this insulating property. MOSFET is alternatively known as insulated-gate field-

effect transistor (IGFET or IGT). Here also, gate voltage controls drain current but main difference between JFET and MOSFET is that, in the latter case, we can apply ***both positive and negative voltages to the gate because it is insulated from the channel.*** Moreover, the gate, SiO_2 insulator and channel from a parallel-plate capacitor. Unlike JFET, a DE MOSFET has only one P-region or N-region called substrate. Normally, it is shorted the ***source internally.*** Fig. 63.23 shows both *P*-channel and *N*-channel DE MOSFETs along with their symbols.

(*b*) Working

(*i*) Depletion Mode of N-channel DE MOSFET

When $V_{GS} = 0$, electrons can flow freely from source to drain through the conducting channel which exists between them. When gate is given negative voltage, it **depletes** the *N*-channel of its

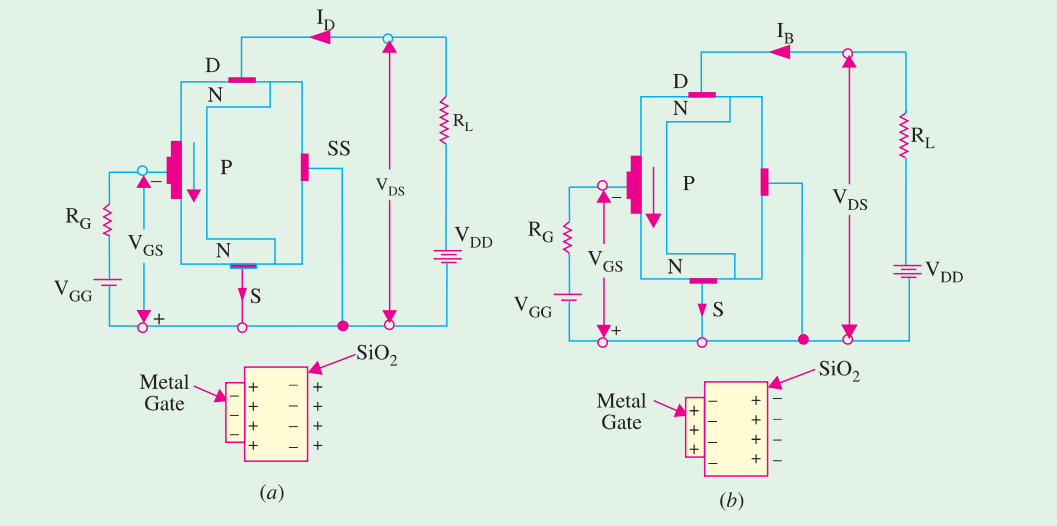


Fig. 63.24

electrons by including positive charge in it as shown in Fig. 63.24 (*a*). Greater the negative voltage on the gate, greater is the reduction in the number of electrons in the channel and, consequently, lesser its conductivity. In fact, too much negative gate voltage called $V_{GS(off)}$ can cut-off the channel. Hence, with negative gate voltage, a DE MOSFET behaves like a JFET.

For obvious reasons, negative-gate operation of a DE MOSFET is called its depletion mode operation.

(*ii*) Enhancement Mode of N-channel DE MOSFET

The circuit connections are shown in Fig. 63.24 (*b*). Again, drain current flows from source to drain even with zero gate bias. When positive voltage is applied to the gate, the input gate capacitor is able to create free electrons in the channel which increases I_D. As seen from the enlarged view of the gate capacitor in Fig. 63.24 (*b*), free electrons are induced in the channel ***by capacitor action.*** These electrons are added to those already existing there. This increased number of electrons ***increases*** or **enhances** the conductivity of the channel. As positive gate voltage is increased, the number of induced electrons is increased, so conductivity of the source-to-drain channel is increased and, consequently, increasing amount of current flows between the terminals. That is why, positive gate operation of a DE MOSFET is known as its **enhancement mode** operation.

Since gate current in both modes is negligibly small, input resistance of a MOSFET is incredibly high varying from $10^{10}\,\Omega$ to $10^{14}\,\Omega$. In fact, MOSFET input current is the leakage current of the capacitor unlike the input current for JFET which is the leakage current of a reverse-biased *P-N* junction.

63.15. Schematic Symbols for a DE MOSFET

Schematic symbol of an *N*-channel normally-ON or DE MOSFET is shown in Fig. 63.25. The gate looks like a metal plate. The arrow is on the substrate and **towards the N-channel.** When *SS* is connected to an external load, we have a 4-terminal device as shown in Fig. 63.25 (*a*) but when it is internally shorted to *S*, we get a 3-terminal device as shown in Fig. 63.25 (*b*). Fig. 63.25 (*c*) shows the symbol for a *P*-channel DE MOSFET.

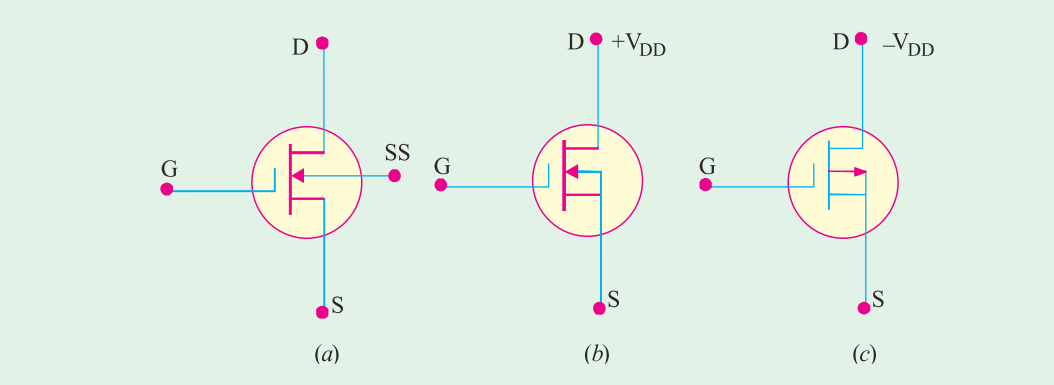


Fig. 63.25

63.16. Static Characteristics of a DE MOSFET

In Fig. 63.26 are shown the drain current and transfer characteristics of a common-source N-channel DE MOSFET for V_{GS} varying from +2 V to $V_{GS(off)}$.

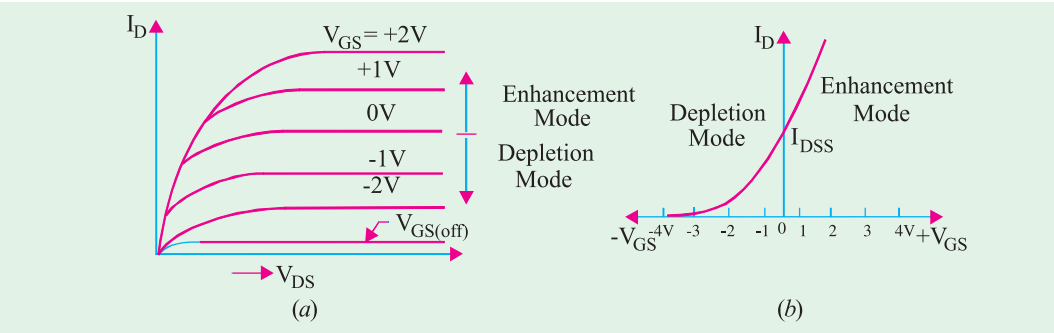


Fig. 63.26

It acts in the enhancement mode when gate is ***positive*** with respect to source and in the depletion mode when gate is ***negative.*** As usual, $V_{GS(off)}$ represents the gate-source voltage which cuts off the source-to-drain current. The transfer characteristic is shown in Fig. 63.26 (*b*). For a given V_{DS}, I_D flows even when $V_{GS} = 0$. However, keeping V_{DS} constant, as V_{GS} is made more negative, I_D keeps decreasing till it becomes zero at $V_{GS} = V_{GS(off)}$. When used in the enhancement mode, I_D increases as V_{DS} is increased positively.

Example 63.9. *For the N-channel zero-biased DE MOSFET circuit of Fig. 63.27, calculate V_{DS} if I_{DSS} = 10 mA and $V_{GS(off)}$ = – 6 V.*

(Electronics-I, Bangalore Univ. 1992)

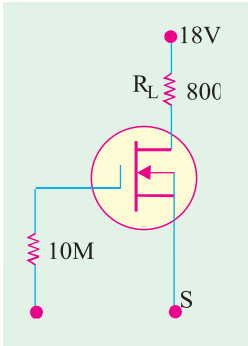


Fig. 63.27

Solution. Since $I_D = I_{DSS}$=10 mA

$\therefore$ $V_{DS} = V_{DD} - I_{DSS} R_L$

$= 18 - 10 \times 10^{-3} \times 800 =$ **10 V**

63.17. Enhancement-only N-Channel MOSFET

This *N*-channel MOSFET (also called NMOS) finds wide application in digital circuitry. As shown in Fig. 63.28 in the NMOS, the *P*-type substrate extends all the way to the metal-oxide layer. Structurally, ***there exists no channel between the source and drain.*** Hence, an NMOS can never operate with a negative gate voltage because it will induce ***positive*** charge in the space between the drain and source which will not allow the passage of electrons between the two. Hence, it operates with ***positive gate voltage only.***

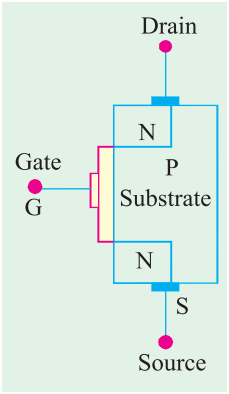


Fig. 63.28

The normal biasing polarities of this *E*-only MOSFET (both *N*-channel and *P*-channel) are shown in Fig. 63.29. With $V_{GS} = 0$, I_D is non-existent even when some positive V_{DD} is applied. It is found that for getting significant amount of drain current, we have to apply sufficiently high positive gate voltage. This voltage is found to produce a thin layer of free electrons very close to the metal-oxide film which stretches all the way from source to drain. The thin layer of *P*-substrate touching the metal-oxide film which provides channel for electrons (and hence acts like *N*-type material) is called ***N*-type *inversion layer* or *virtual*** *N*-channel [Fig. 63.29 (*a*)].

The minimum gate-source voltage which produces this *N*-type inversion layer and hence drain current is called threshold voltage $V_{GS(th)}$ as shown in Fig. 63.30 (*c*). When $V_{GS} < V_{GS(th)}$, $I_D = 0$. Drain current starts only when $V_{GS} > V_{GS(th)}$. For a given V_{DS}, as V_{GS} is increased, virtual channel deepens and I_D increases. The value of I_D is given by $I_D = K(V_{GS} - V_{GS(th)})2$ where K is a constant which depends on the particular MOSFET. Its value can be determined from the data sheet by taking the specified value of I_D called $I_{D(ON)}$ at the given value of V_{GS} and then substituting the values in the above equation. Fig. 63.30 (*a*)

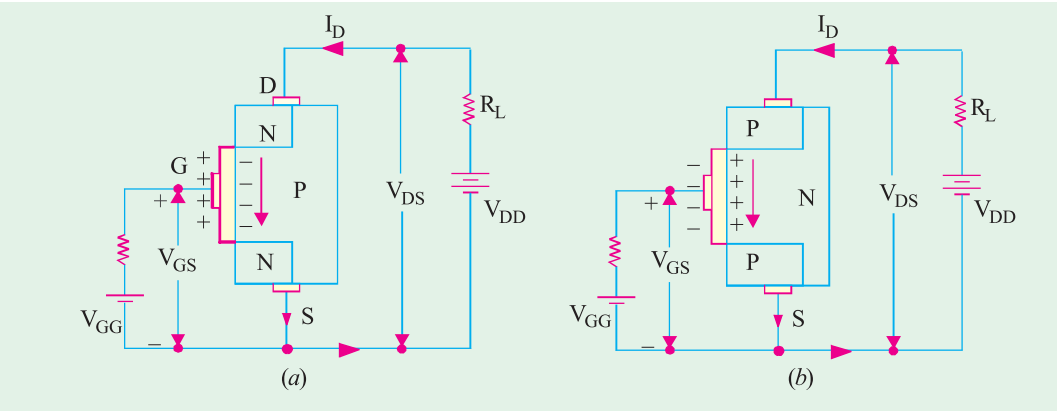


Fig. 63.29

shows the schematic symbol for an *E*-only *N*-channel MOSFET whereas Fig. 63.30 (*b*) shows its typical drain characteristics. As usual, arrow on the substrate points to the *N*-type material and the vertical line (representing-channel) is broken as a reminder of the normally-OFF condition.

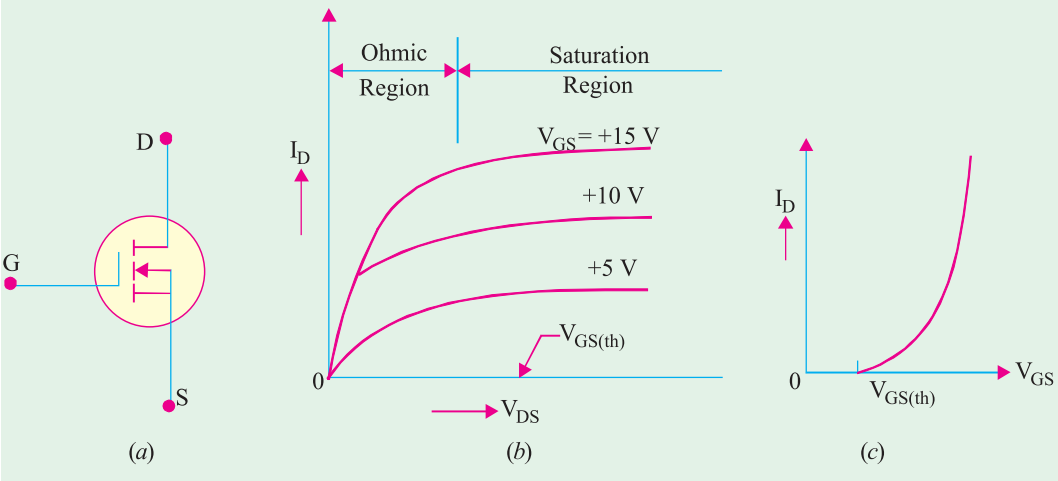


Fig. 63.30

A P-channel E-only MOSFET (PMOS) is constructed like NOMS except that all the *P*– and *N*– regions are interchanged. It operates with ***negative*** gate voltage only.

Differentiating the above-given drain current equation with respect to V_{GS}, we get

$$\frac{dI_D}{dV_{GS}} = g_m = 2K\,(V_{GS} - V_{GS(th)})$$

Transfer Characteristics

It is shown in Fig. 63.30 (*c*). I_D flows only when V_{GS} exceeds threshold voltage $V_{GS(th)}$. This MOSFET does not have an I_{DSS} parameter as do the JFET and DE MOSFET.

63.18. Biasing E-only MOSFET

As stated earlier, enhancement-only MOSFET must have a V_{GS} greater than $V_{GS(th)}$. Fig. 63.31 shows two methods of biasing an *N*-channel E-MOSFET. In either case, the purpose is to make the gate voltage more positive than the source by an amount exceeding $V_{GS(th)}$. Fig. 63.31 (*a*) shows drain-feedback bias whereas Fig. 63.31 (*b*) shows voltage-divider bias.

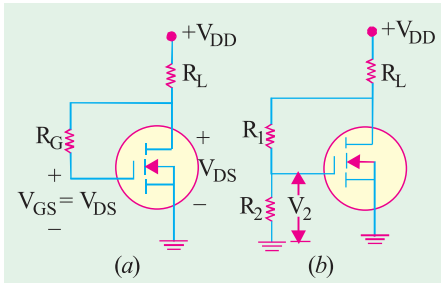


Fig. 63.31

Considering the circuit of Fig. 63.31 (*b*), we have

$$V_{GS} = V_2 = V_{DD}\frac{R_2}{R_1 + R_2}$$

and $$V_{DS} = V_{DD} - I_D R_L$$

where $$I_D = K(V_{GS} - V_{GS(th)})^2.$$

Example 63.10. *The data sheet of the E-MOSFET shown in Fig. 63.32 gives $I_{D(ON)}$ = 4 mA at V_{GS} = 10 V and $V_{GS(th)}$ = 5 V. Calculate V_{GS} and V_{DS} for the circuit.* **(Applied Electronics, Punjab Univ. 1991)**

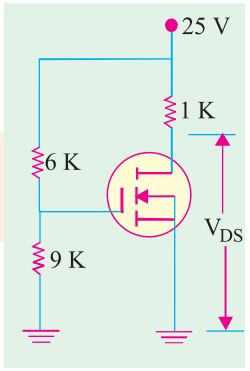


Fig. 63.32

Solution. $V_{GS} = V_2 = 25 \times (9/15) = 15$ V

Let us now find the value of *K*.

$$K = \frac{I_{D(ON)}}{(V_{GS} - V_{GS(th)})^2} = \frac{4}{(10-5)^2} = 0.16\text{mA/V}^2$$

Value of I_D for V_{GS}=15 V is given by

$$I_D = K\,(V_{GS} - V_{GS(th)})^2 = 0.16\,(15 - 5)^2 = 16 \text{ mA}$$

Now, $V_{DS} = V_{DD} - I_D R_L = 25 - 16 \times 1 = \mathbf{9\ V}$

Example 63.11. *An N-channel E-MOSFET has the following parameters:*
$I_{D(ON)} = 4$ *mA at* $V_{GS} = 10$ *V and* $V_{GS(th)} = 5$ *V*
Calculate its drain current for $V_{GS} = 8$ *V.*

Solution. $$K = \frac{I_{D(ON)}}{(V_{GS} - V_{GS(th)})^2} = \frac{4\text{mA}}{(10\,\text{V} - 5\text{V})^2} = 0.16\text{mA/V}^2$$

Now, using this value of K, I_D can be found thus :

$$I_D = K\,(V_{GS} - V_{GS(th)})^2 = 0.16\,(8 - 5)^2 = \mathbf{1.44\ mA}$$

63.19. FET Amplifiers

We will consider the DE MOSFET and E-MOSFET separately.

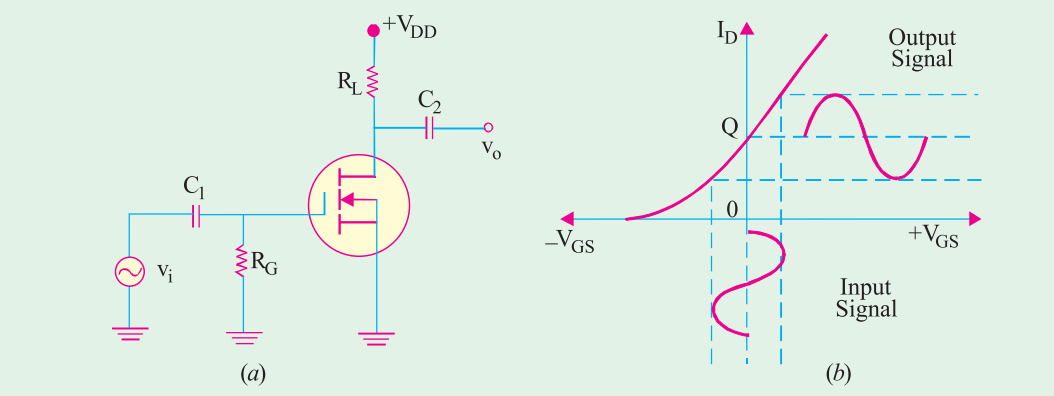


Fig. 63.33

(*i*) DE MOSFET Amplifier

Fig. 63.33 (*a*) shows a zero-biased *N*-channel DE MOSFET with an ac source capacitively-coupled to its gate. Since gate is at 0 volt dc and source is at ground, $V_{GS} = 0$. Fig. 63.33 (*b*) shows the transfer characteristic.

The input ac signal voltage V_i causes V_{GS} to swing above and below its zero value thus producing a swing in I_D as shown in Fig. 63.33 (*b*). The negative swing in V_{GS} produces depletion mode and I_D

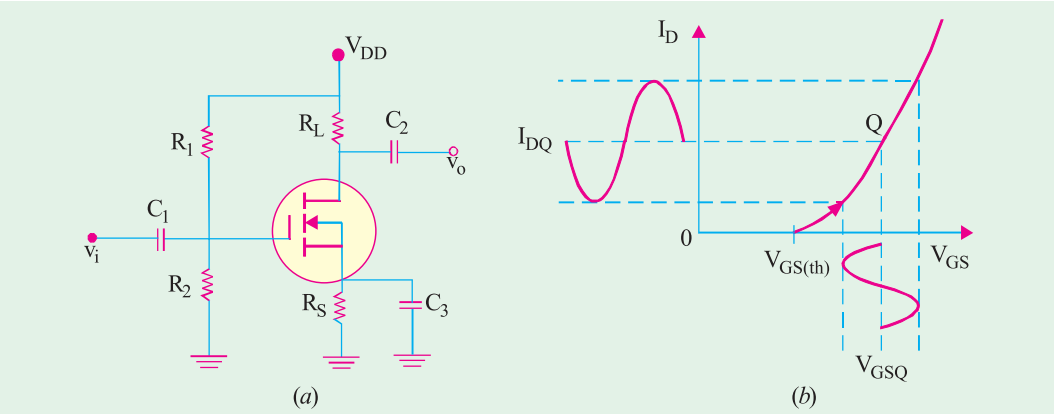


Fig. 63.34

is decreased. A positive swing in V_{GS} produces enhancement mode so that I_D is increased. This leads to a large swing in drop across R_L and can be taken out *via* C_2 as V_o.

(*ii*) E-MOSFET Amplifier

In Fig. 63.34 (*a*) is shown a voltage-divider biased *N*-channel E-MOSFET having an ac signal source coupled to its gate. The gate is biased with a positive voltage such that V_{GS} exceeds $V_{GS(th)}$.

As shown in Fig. 63.34 (*b*), the signal voltage produces a swing in V_{GS} below and above its *Q*-point value. This, in turn, causes a swing in I_D and hence in $I_D R_L$ which gives rise to no.

Example 63.12. *The N-channel E-MOSFET used in the common-source amplifier of Fig. 63.35 has the following parameters :*

$I_{D(ON)} = 4$ mA at $V_{DS} = 10$ V, $V_{GS(th)} = 4$ V and $g_m = 5000$ μS.

Calculate V_{GS}, I_D, V_{GS} *and* v_o. **(Elect. and Electronic Engg., Annamalai Univ. 1992)**

Solution. $V_{GS} = V_{DD}\dfrac{R_2}{R_1+R_2} = 16\times\dfrac{30}{80} = \mathbf{6\ V}$

Now, $K = \dfrac{I_{D(NO)}}{(V_{GS}-V_{GS(th)})^2} = \dfrac{4}{(10-5)^2}$

$= 0.16$ mA/V^2

$\therefore\ I_D = K(V_{GS}-V_{GS(th)})^2 = 0.16(6-4)^2$

$= 0.64$ mA

$\therefore\ V_{DS} = V_{DD} - I_D R_L = 16 - 0.64\times 5 = \mathbf{12.8\ V}$

Now, $A_v = g_m(r_d \| R_L) \cong g_m R_L$

$= 5000\times 10^{-6}\times 5\times 10^3 = 25$

$\therefore\ V_o = A_v v_i = 25\times 100 = 2500$ mV $= \mathbf{2.5\ V}$

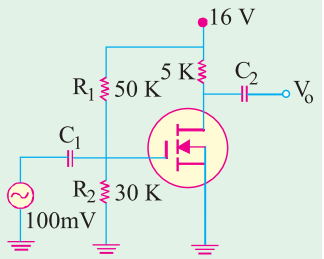


Fig. 63.35

Example 63.13. *The parameters of the enhancement-only NMOS shown in Fig. 63.36 are* $V_{GS(th)} = 2$ *V and* $K = 2\times 10^{-4}$ *A/V*^{2}. *Calculate the values of* I_D *and* V_{DS}.

Solution. Since drain is directly returned to gate, $V_{GS} = V_{DS}$. As seen from the figure

$V_{DS} = V_{DD} - I_D R_L = 12 - 5\times 10^3 I_D$

$\therefore\ I_D = (12 - V_{DS})/5\times 10^3$ A

Now, $I_D = K(V_{GS}-V_{GS(th)})^2 = K(V_{DS}-2)^2$

or $\dfrac{12-V_{DS}}{5\times 10^3} = 2\times 10^{-4}(V_{DS}-2)^2$ or $V_{DS}^2 - 3V_{DS} - 8 = 0$

$\therefore\ V_{DS} = \dfrac{3\pm\sqrt{9+32}}{.2} = \dfrac{3\pm\sqrt{41}}{2} = \mathbf{4.7\ V}$

$\therefore\ I_D = (12-4.7)/5\times 10^3 = \mathbf{1.5\ mA}$

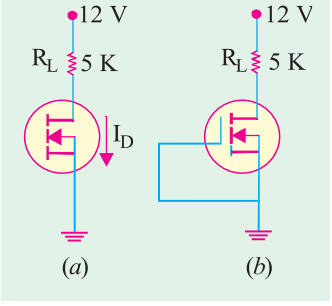


Fig. 63.36

In Fig. 63.36 (*b*), since gate has been directly returned to ground, $V_{GS} = 0$. Hence, $I_D = 0$, because $V_{GS} \ll V_{GS(th)}$. With no current, $V_{DS} = V_{DD} = \mathbf{12\ V}$.

Example 63.14. *A MOSFET has a drain resistance,* R_L *of 44 kΩ and operates at 20 kHz. Calculate the voltage gain of this device as a single stage amplifier. The MOSFET parameters are :*

$g_m = 1.6$ *mA/V,* $r_d = 100$ *k Ω* , $C_{gs} = 3.0$ *pf,* $C_{ds} = 1.0$ *pF and* $C_{gd} = 2.8$ *pF.*

(U.P.S.C. Engg. Services, 1996)

Solution. $A_v = g_m(r_d \| R_L)$

$= 1.6\times 10^{-3}(100\times 10^3 \| 44\times 10^3)$

$= 1.6\times 10^{-3}\times 30.56\times 10^3$

$= \mathbf{48.9}$

63.20. FET Applications

FETs can be used in almost every application in which bipolar transistors can be used. However, they have certain applications which are exclusive to them :

1. As input amplifiers in oscilloscopes, electronic voltmeters and other measuring and testing equipment because their high ***r_{in} reduces loading effect to the minimum.***
2. In logic circuits where it is kept OFF when there is zero input while it is turned ON with very little power input.
3. For mixer operation of *FM* and *TV* receivers.
4. As voltage-variable resistor (*VVR*) in operational amplifiers and tone controls etc.
5. Large-scale integration (*LSI*) and computer memories because of very small size.

63.21. MOSFET Handling

MOSFETs require very careful handling particularly when ***out of circuit.*** In circuit, a MOSFET is as rugged as any other solid-state device of similar construction and size.

It is essential not to permit any stray or static voltage on the gate otherwise the ultra-thin SiO_2 layer between the channel and the gate will get ruptured. Since gate-channel junction looks like a capacitor with extremely high resistance, it requires only a few electrons to produce a high voltage across it. Even ***picking up a*** MOSFET ***by its leads can destroy it.*** Generally, grounding rings are used to short all leads of a MOSFET for avoiding any voltage build up between them. These grounding or shorting rings are removed only after MOSFET is securely wired into the circuit. Sometimes, conducting foam is applied between the leads instead of using shorting rings. As shown in Fig. 13.37, some MOSFETs have back-to-back Zener diodes internally formed to protect them against stray voltages.

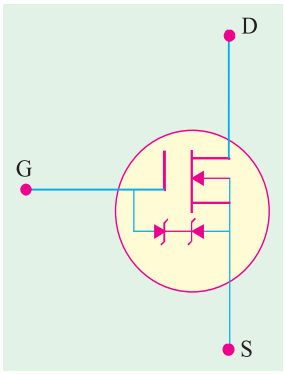


Fig. 63.37

Tutorial Problems No. 63.2

1. For a certain DE MOSFET, $I_{DSS} = 10$ mA and $V_{GS(off)} = -8$V. Calculate I_D when V_{GS} is (*i*) – 4 V and (*ii*) + 4 V. **[(*i*) 2.5 mA (*ii*) 22.5 mA]**
2. The data sheet of a certain zero-biased DE MOSFET gives $I_{DSS} = 15$ mA and $V_{GS(off)} = 5$ V. What is the value of drain current ? **[15 mA]**
3. A certain *E*-only *N*-channel MOSFET has the following parameters :
   $I_{D(on)} = 4$ mA at $V_{GS} = 8$ V and $V_{GS(th)} = 2$ V
   Calculate I_D for $V_{GS} = 6$ V **[1.78 mA]**

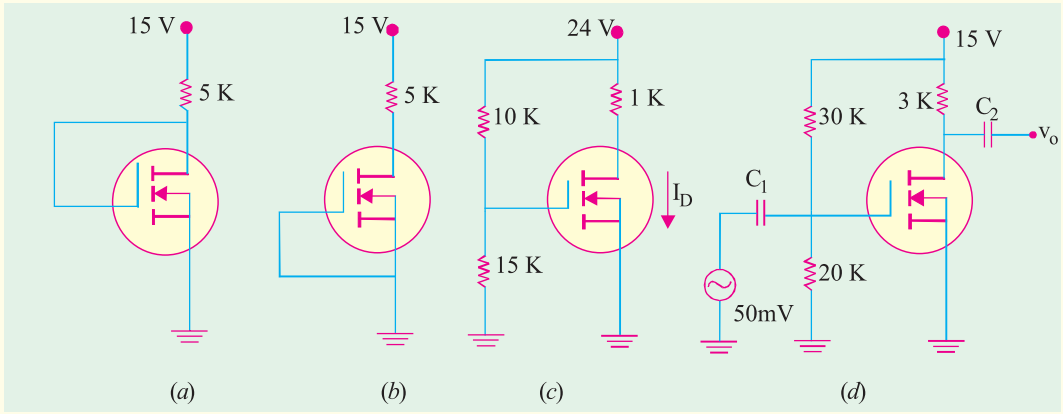


Fig. 63.38

4. The parameters of the *E*-only, *N*-channel MOSFET shown in Fig. 63.38 (*a*) are : $V_{GS(th)} = 2$ V and $K = 0.3$ mA/V^2. Determine the values of I_D and V_{DS}. If the gate is connected as shown in Fig. 63.38 (*b*), what will be the new values of I_D and V_{DS} ? **[(*i*) 2.07 mA (*ii*) 4.63 V ; 0 A, 15 V]**

5. The data sheet for the *E*-only *N*-channel MOSFET of Fig. 63.38 (*c*) gives $I_{D(on)} = 3$ mA at $V_{GS} = 10$ V and $V_{GS(th)} = 5$ V. Calculate the values of V_{GS} and V_{DS}. **[14.4 V ; 13.4 V]**

6. The amplifier circuit of Fig. 63.38 (*d*) used an *E*-only *N*-channel MOSFET having the following parameters : $I_{D(on)} = 5$ mA at $V_{GS} = 10$ V, $V_{GS(th)} = 4$ V, $g_m = 5500$ µS

Calculate V_{GS}, I_D, V_{DS} and v_o. **[6 V ; 0.556 mA ; 12.2 V ; 0.825 V]**

7. A field-effect transistor has a small-signal equivalent circuit with input resistance = 1000 MΩ , forward transfer conductance = 4 m S and output conductance = 100 µS when at the operating point, $V_{DS} = +4$ V, $I_D = 2$ mA, $V_{GS} = -2$ V.

Draw the circuit that you would use for a single-stage voltage amplifier. Describe the use and specify the value of as many components as possible if a 30 V supply was available.

What voltage gain would you expect when the output was unloaded ? Give reasons which might account for not getting this gain exactly.

[Drain load = 12 kΩ, Source Bias Resistor = 1 k Ω, – 21.8]

8. A field-effect transistor is used as a voltage amplifier and with a load resistor of 40 k Ω, a gain of 40 is obtained. If the load resistance is halved, the voltage gain drops to 30. Calculate the output resistance and the mutual conductance of the transistor.

Briefly compare the advantages and limitations of the field-effect transistor with the bipolar transistor. **[20 kΩ, 3 mS]**

OBJECTIVE TESTS – 63

1. A FET consists of a
(*a*) source (*b*) drain
(*c*) gate (*d*) all of the above.

2. FETs have similar properties to
(*a*) *PNP* transistors
(*b*) *NPN* transistors
(*c*) thermonic valves
(*d*) unijunction transistors.

3. For small values of drain-to-source voltage, JFET behaves like a
(*a*) resistor
(*b*) constant-current source
(*c*) constant-voltage source
(*d*) negative resistance

4. In a JFET, the *primary* control on drain current is exerted by
(*a*) channel resistance
(*b*) size of depletion regions
(*c*) voltage drop across channel
(*d*) gate reverse bias.

5. After V_{DS} reaches pinch-off value V_P in a JFET, drain current I_D becomes
(*a*) zero (*b*) low
(*c*) saturated (*d*) reversed.

6. In a JFET, as external bias applied to the gate is increased
(*a*) channel resistance is decreased
(*b*) drain current is increased
(*c*) pinch-off voltage is reached at lower val ues of I_D.
(*d*) size of depletion regions is reduced.

7. In a JFET, drain current is maximum when V_{GS} is
(*a*) zero (*b*) negative
(*c*) positive (*d*) equal to Vp

8. The voltage gain of a given common- source JFET amplifier depends on its
(*a*) input impedance
(*b*) amplification factor
(*c*) dynamic drain resistance
(*d*) drain load resistance.

9. A JFET has the disadvantage of
(*a*) being noisy
(*b*) having small gain-bandwidth product
(*c*) possessing positive temperature coe- fficient
(*d*) having low input impedance.

10. A JFET can be cut-off with the help of
(*a*) V_{GS} (*b*) V_{DS}
(c) V_{DG} (*d*) V_{DD} .

11. The drain source voltage at which drain current becomes nearly constant is called
(*a*) barrier voltage
(*b*) breakdown voltage
(*c*) pick-off voltage
(*d*) pinch-off voltage

12. The transconductance 'g_m' of a JFET is equal to
(*a*) $-\frac{2I_{DSC}}{V_P}$
(*b*) $\frac{2}{|V_P|}\sqrt{I_{DSS}\, I_D}$
(*c*) $-\frac{2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$
(*d*) $\frac{I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$

13. An FET source follower circuit has of 2 millimho and of 50 k Ω. If the source resistance R_S is 1k Ω, the output resistance of the amplifier will be
(*a*) 330 Ω (*b*) 450 Ω
(*c*) 500 Ω (*d*) 1 k Ω

14. A DE MOSFET differs from a JFET in the sense that it has no
(*a*) channel (*b*) gate
(*c*) *P-N* junctions (*d*) substrate.

15. For the operation of enhancement only *N*-channel MOSFET, value of gate voltage has to be
(*a*) high positive (*b*) high negative
(*c*) low positive (*d*) zero.

16. The extremely high input impedance of a MOSFET is primarily due to the
(*a*) absence of its channel
(*b*) negative gate-source voltage
(*c*) depletion of current carriers
(*d*) extremely small leakage current of its gate capacitor

17. The main factor which makes a MOSFET likely to break down during normal hand- ling is its
(*a*) very low gate capacitance
(*b*) high leakage current
(*c*) high input resistance
(*d*) both (a) and (c).

18. The main factor which differentiates a DE MOSFET from an *E*-only MOSFET is the absence of
(*a*) insulated gate (*b*) electrons
(*c*) channel (*d*) *P-N* junctions.

19. The polarity of V_{GS} for *E*-only MOSFET is
(*a*) positive
(*b*) negative
(*c*) zero
(*d*) depends on P-or N-channel.

20. A tranasconductance amplifier has
(*a*) high input impedance and low output impedance
(*b*) low input impedance and high output impedance
(*c*) high input and output impedances
(*d*) low input and output impedances

21. The threshold voltage of an n-channel enhancement mode MOSFET is 0.5 V, when the device is biased at a gate voltage of 3V, pinch-off would occur at a drain voltage of
(*a*) 1.5 V (*b*) 2.5 V
(*c*) 3.5 V (*d*) 4.5 V

22. The zero gate bias channel resistance of a junction field-effect transistor is 750 and the pinch-off voltage is 3V. For a gate bias of 1.5 V and very low drain voltage, the device would behave as a resistance of
(*a*) 320 Ω (*b*) 816 Ω
(*c*) 1000 Ω (*d*) 1270 Ω

23. A MOSFET rated for 15 A, carries a periodic current as shown in Fig. 63.39. the ON state resistance of the MOSFET is 0.15 Ω. The average ON state loss in the MOSFET is

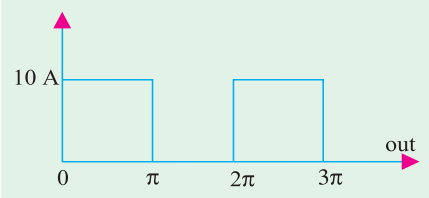


Fig. 63.39

(*a*) 33.8 W (*b*) 15.0 W
(*c*) 7.5 W (*d*) 3.8 W

ANSWERS

1. (*d*) **2.** (*b*) **3.** (*a*) **4.** (*d*) **5.** (*c*) **6.** (*c*) **7.** (*a*) **8.** (*d*) **9.** (*b*) **10.** (*a*) **11.** (*d*)
12. (*c*) **13.** *c* **14.** (*c*) **15.** (*a*) **16.** (*d*). **17.** (*d*) **18.** (*c*) **19.** (*d*) **20.** (*a*) **21.** (*c*) **22.** (*b*)
23. (*c*)

ROUGH WORK

GO To FIRST