High Speed Digital Distance Relaying Scheme Using FPGA and IEC 61850

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Abstract—Full-cycle Fourier and cosine phasor filtering systems are typical implementations of numerical distance relays with a response time of close to one cycle. Fast subcycle numerical distance elements are useful, especially for extra high voltage/UHV transmission systems (400 kV and above). Fast subcycle numerical relaying methods such as half-cycle Fourier method, phaselets, least error squares, traveling wave, and wavelet based methods have been proposed in the literature. In this paper, first improvements to the phaselet-based distance relaying method are proposed by taking the magnitude errors and the phase angle errors into account. An adaptive Mho characteristic based on the phasor estimation errors is used to achieve a fast and secure trip decision. The quality of the estimated values in time domain is analyzed mathematically using a transient monitoring index. Second, the scheme is implemented on a field programmable gate arrays (FPGAs) board, which provides fast computation speeds due to its powerful parallel processing units. The proposed relay is tested using hardware-in-the-loop simulations and a real time digital simulator. Third, the Ethernet-based protocols (IEC 61850 sampled value and generic object oriented substation events protocols) are implemented on the FPGA and used to verify the performance of the proposed relay in digital substation environments.

Index Terms—Sub-cycle algorithms, adaptive protection, FPGAs, IEC 61850, hardware-in-the-loop simulations.

I. INTRODUCTION

HIGH speed protection is desirable for extra high voltage (EHV) transmission lines (400 kV and above). It is reported that for every one millisecond saved in fault clearing time, the stability limit of the transmission system goes up by 15 MW [1].

Full-cycle discrete Fourier transform (FCDFT) needs one complete cycle of samples to exclude pre-fault samples and obtain an accurate fundamental phasor. Some sub-cycle linear numerical filtering methods have been proposed in [2]–[8].

In [2] and [3], half-cycle DFT (HCDFT) is suggested whereby only half-cycle samples are used to estimate the phasors; this makes the convergence speed faster than for the FCDFT method. However, HCDFT is known to lose the ability to reject even harmonics. It also has difficulties removing the decaying DC offset. Half-cycle least error square (HCLES) models the decaying DC component and harmonics using the Taylor series expansion, but the performance depends on the accuracy of the estimated parameters of the decaying DC, especially when the decaying DC rates are fast. In [4] and [5], three off-line look-up tables are added to improve the estimation of the decaying DC parameters. A Clarke transformation based DFT algorithm is proposed in [6]. The main focus is on reducing measurement errors for off-nominal frequency conditions. Another linear filtering method found to be reliable is the Kalman filtering method [7]. The estimation is stable in the presence of noise and harmonics, but takes more than half a cycle to obtain a stable estimation due to the large number of computations needed to find the state variables in each time step. Wavelet transform (WT) techniques have been reported for digital distance protection [8]. Using the WT multiresolution analysis (MRA) described in [8], the fundamental phasor can be extracted faster than FCDFT. However, the performance is affected by the decaying DC component. The response is fast but could be insecure as the impedance trajectories move in and out of the protection zone before settling [8]. To overcome this issue, the data window is reset once a disturbance is detected [8], to give a more stable response. A pre-bandpass filter is used to remove the DC component, but this introduces a time delay. Another type of fault detection is based on artificial intelligence models. In [9], a convolutional sparse autoencoder (CSAE) was used to learn features from voltage/current signals. Fault detection was done by applying a classifier on the feature vectors and the operation time was within one cycle. However, system transients such as CT saturation and CCVT transient errors were not considered, which may affect the classification accuracy and speed.

In this paper, a phaselet-based distance relaying scheme is developed to achieve a fast sub-cycle response. Phaselets are partial integrals of products of the waveform samples and the sinusoidal/cosine coefficients specified by a data window. They can be combined into phasors over a variable length window that is an integer multiple of the basic phaselet. References [10]–[12] describe phaselet scheme and testing using offline computer simulations for transmission line distance and current differential protection.

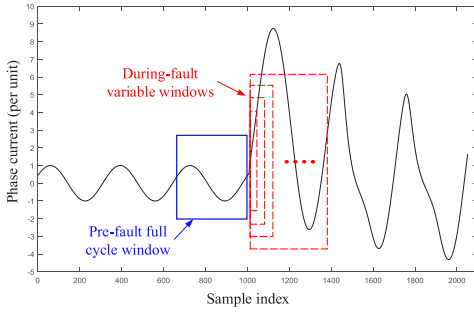IEEE TRANSACTIONS ON SMART GRID, VOL. 9, NO. 5, SEPTEMBER 2018

Fig. 1.   Adaptive filtering window concept.

In this paper, the phaselet method is modified by taking the magnitude errors and the phase angle errors into consideration to obtain a secure trip decision. The probability density functions for the magnitude and phase angle errors are found. The standard deviations are obtained using a mathematical equation for magnitude errors and a numerical solution for phase angle errors. The adaptive Mho reach is set based on the maximum possible errors. The quality of the estimated values in time domain is analyzed mathematically using a transient monitoring index.

The second innovative component of the research work is the hardware implementation of the proposed algorithm described herein on FPGA. The phaselet-based algorithm is parallel in nature and is implemented using the parallel nature of FPGAs. This speeds up the calculations compared to digital signal processor (DSP) implementations.

The third innovative component of this paper is implementing the proposed digital relay using IEC 61850 Sampled Value (SV) and Generic Object Oriented Substation Events (GOOSE) protocols [13]. Testing and the performance of the proposed relay is done using hardware-in-the-loop simulations with a real-time digital simulator (RTDS^{TM}).

II. PHASELET-BASED DISTANCE PROTECTIVE RELAY

The phasor estimation using FCDFT is given as follows:

$$\hat{X}_c = \frac{2}{N} \cdot \sum_{k=0}^{N-1} x(k) \cdot cos\left(2\pi \cdot \frac{k}{N}\right), \tag{1}$$

$$\hat{X}_s = \frac{2}{N} \cdot \sum_{k=0}^{N-1} x(k) \cdot sin\left(2\pi \cdot \frac{k}{N}\right) \tag{2}$$

$$\hat{X} = \hat{X}_c - j\hat{X}_s, \tag{3}$$

When a fault occurs the filter window spans two partial sample sets: pre-fault system measurements and during-fault system measurements. Therefore, phasor estimation using the FCDFT algorithm has an inherent error due to the fixed full-cycle window. To address this issue, a phaselet-based variable window filtering technique is developed. Phaselets are partial integrals of products of the waveform samples and the sinusoidal/cosine coefficients specified by a data window. They are combined into phasors over a set of linearly increasing window sizes, as shown by the dashed line boxes in Figure 1. Each box in the figure represents a filtering window (there would

be 20 of them in one full cycle and each phaselet includes 4 samples). The phaselets are calculated:

$$Pl_c(p) = \sum_{k=p \cdot P}^{p \cdot P + P - 1} x(k) \cdot cos\left(2\pi \cdot \frac{k}{N}\right), \tag{4}$$

$$Pl_s(p) = \sum_{k=p \cdot P}^{p \cdot P + P - 1} x(k) \cdot sin\left(2\pi \cdot \frac{k}{N}\right), \tag{5}$$

where constant P is the number of samples per phaselet and is set to 1/20 of one cycle so that the changes in voltage/current measurements can be captured as early as possible. There are 20 phaselets in one cycle and the phaselet index p ranges from 0 to 19 for the first cycle samples. $Pl_c(p)$ is the cosine part of the p_{th} phaselet and $Pl_s(p)$ is the sine part.

The sum of the phaselets for window $W(n)$ is given by:

$$P_c(n) = \sum_{p=n-\frac{W(n)}{P}+1}^{n} Pl_c(p), \tag{6}$$

$$P_s(n) = \sum_{p=n-\frac{W(n)}{P}+1}^{n} Pl_s(p), \tag{7}$$

where n is the phasor index and $W(n)$ is the adaptive window size which increases in a linear fashion from 1/20 cycle to 1 cycle. $P_c(n)$ is the cosine part of the sum of all the phaselets inside the specified window $W(n)$ and $P_s(n)$ is the sine part. $\hat{X}_c(n)$ and $\hat{X}_s(n)$ can be estimated from $P_c(n)$ and $P_s(n)$ [14], as depicted in:

$$\hat{\mathbf{X}}(n) = \begin{bmatrix} \hat{X}_c(n) \\ \hat{X}_s(n) \end{bmatrix} = \begin{bmatrix} C_1(n) & C_2(n) \\ C_2(n) & C_3(n) \end{bmatrix}^{-1} \begin{bmatrix} P_c(n) \\ P_s(n) \end{bmatrix}, \tag{8}$$

$$C_1(n) = \sum_{k=0}^{W(n)-1} cos^2\left(2\pi \cdot \frac{k}{N}\right), \tag{9}$$

$$C_2(n) = \sum_{k=0}^{W(n)-1} cos\left(2\pi \cdot \frac{k}{N}\right) sin\left(2\pi \cdot \frac{k}{N}\right), \tag{10}$$

$$C_3(n) = \sum_{k=0}^{W(n)-1} sin^2\left(2\pi \cdot \frac{k}{N}\right). \tag{11}$$

When $W(n)$ equals to N, $C_2(n)$ will be zero using the orthogonality principle of sine and cosine terms. $\hat{X}_c(n)$ and $\hat{X}_s(n)$ are orthogonal and Equation (8) will be equivalent to Equations (1), (2). When $W(n)$ is between 0 and N except $N/2$, $C_2(n)$ will not be zero. The precomputed coefficient matrix $\mathbf{C}^{-1}(n)$ in Equation (8) is needed.

Under normal conditions, the phaselets are summed over one cycle and the filter window $W(n)$ is fixed to N, generating an equivalent of FCDFT, as indicated by the solid line box in Figure 1. Once a disturbance is detected (the detection logic is described in the following paragraphs), the filtering window immediately shrinks to P. Because all pre-fault measurements are blocked by the window, the estimated phasor responds more quickly to the change in voltage and current measurements. As new phaselets accumulate, the window size is increased until it reaches one full cycle N, as indicated by
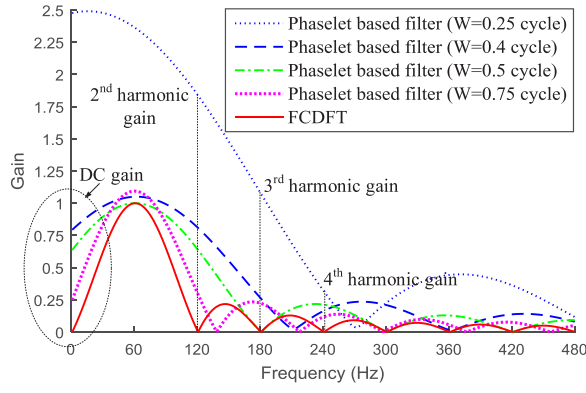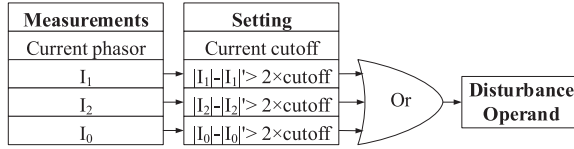
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Fig. 2.   Frequency responses of the phaselet-based filters.

Fig. 3.   Logical implementation of disturbance detector. $|I_1|'$, $|I_2|'$, and $|I_0|'$ are current phasor magnitudes from two cycles before.
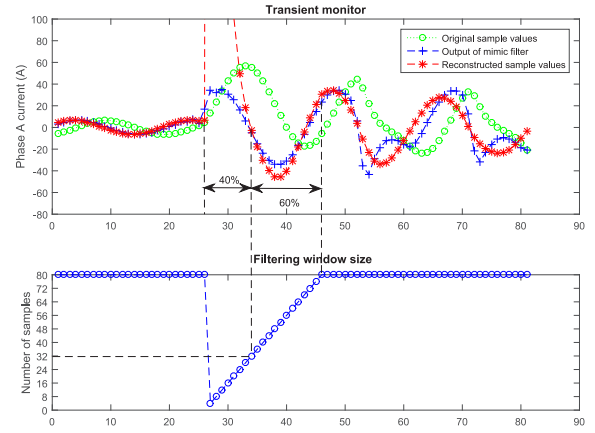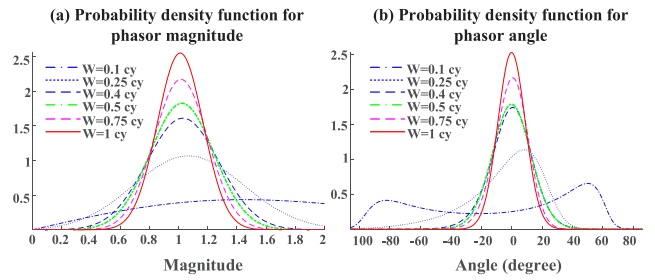

Fig. 4.   Transient monitor.

Fig. 5.   Probability density function for phasor magnitude and angle.

TABLE I
STANDARD DEVIATION & REACH FOR DIFFERENT FILTERING WINDOWS

$w(cy)$	0.45	0.5	0.6	0.7	0.8	0.9	1
$\sigma_r(n)$	22.9%	21.8%	20.3%	19%	17.7%	16.5%	15.6%
$\sigma_\theta(n)$	13.4°	13.1°	12.6°	11.5°	10.2°	9.4°	9.2°
$reach$	70.1%	72.4%	74.2%	74.7%	76.3%	78.4%	80.2%

the dashed line boxes in Figure 1. Unless another new disturbance is detected, phaselets will continue to be combined to form an FCDFT in a recursive manner. The accuracy of the estimated phasor improves as the window expands.

Figure 2 shows the frequency response of the phaselet-based filters with various window sizes. Very small windows (smaller than 0.4 cycles) have little capability to reject harmonics and DC offset but, as the window expands, the harmonic response and DC response improve until they are eventually equivalent to FCDFT. Importantly, the filter loses the ability to reject even harmonics when the window equals to a half cycle (HCDFT). The gain of the filter for DC is 0.64.

In this research, a mimic filter is used to remove the decaying DC component prior to the phaselet calculation. A disturbance detector is used for the purpose of initiating the adaptive phasor estimation. The inputs of the disturbance detector are the present sequence currents and the corresponding measurements from two cycles earlier, as shown in Figure 3. The magnitude of the change in currents are evaluated against two times the cut-off threshold, which is set at 2% [15] of the steady state value. If the change of any sequence current exceeds this limit, a disturbance operand will be sent to the distance element.

A. Transient Monitoring and Error Analysis

If we denote the reconstructed sample as $\check{x}(n)$, then

$$\check{x}(n) = \hat{X}_c(n)cos\left(2\pi \cdot \frac{(n+1)P - 1}{N}\right)$$
$$+ \hat{X}_s(n)sin\left(2\pi \cdot \frac{(n+1)P - 1}{N}\right). \quad (12)$$

Figure 4 compares the original sampled values and the reconstructed values from $\hat{X}_c(n)$ and $\hat{X}_s(n)$. The instantaneous output of the mimic filter is also given to show the phase shift

between them. The window size is dynamically changed from 4 samples to 80 samples upon a fault. The estimation errors are very large, causing large transient overshoots when the filtering window is smaller than 40% of one cycle, which makes the initial phasor estimates unusable. When the filtering window is greater than 40%, the reconstructed values are close to the output of the mimic filter.

The estimation error can be further analysed mathematically for different sizes of filtering windows. It is the fundamental indicator of the level of confidence in the estimated phasors. Assuming that the errors of the relay inputs are uncorrelated and have a constant variance, the probability density function (PDF) of the magnitude and phase angle of the estimated phasor can be obtained [16], [17]. The detailed mathematical analysis is in Appendix A.

Figure 5(a) shows the PDF of the magnitude of the estimated phasor for different filtering window lengths (0.1 cycle ∼ 1 cycle). Table I shows the standard deviation values, $\sigma_r(n)$ for different filtering window lengths.

The phase angle error is very important for a phaselet-based (sub-cycle method in general) distance relay, and has significant impact on the security of the relay. The PDF of the phase angle for different filtering window lengths is shown
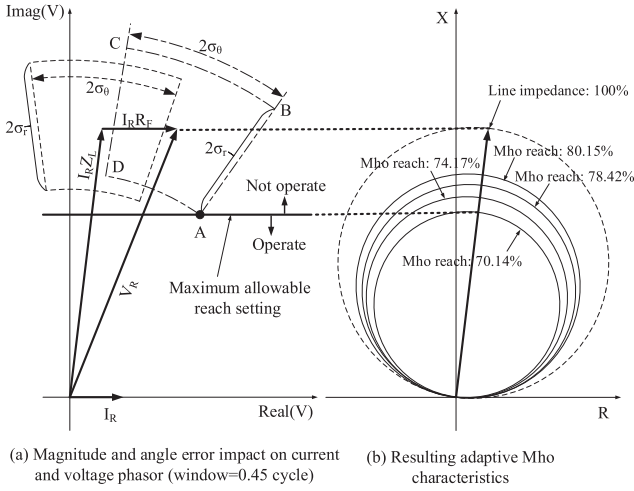
(a) Magnitude and angle error impact on current and voltage phasor (window=0.45 cycle)

(b) Resulting adaptive Mho characteristics

Fig. 6.   Adaptive Mho characteristics.

Fig. 7.   Overall architecture of the proposed distance relaying scheme.

in Figure 5(b). A numerical solution of the standard deviation, $\sigma_\theta(n)$ using Matlab is given in the third row of Table I. When the window lengths are very small, the estimated angle can have a very large error. When the window lengths are between 0.4 cycle $\sim$ 1 cycle, the estimated phasor angles are mainly within $\pm 15^o$ of the expected value. A trip delay routine is used to prevent false trips due to the estimated phase angle errors especially for high source impedance ratios (SIR's).

B. Adaptive Mho Characteristics

The adaptive Mho characteristics is set taking into account both the magnitude and phase angle errors, as shown in Figure 6. The errors reduce as the window expands.

As discussed in Section II-A, the transient overshoots are very large when the filtering window is smaller than 40%. Therefore once a disturbance is detected, the reach is set to zero until the window length > 40% of one cycle so that the transient overshoots are filtered out.

The current and voltage phasor errors that arise can be demonstrated as shown in Figure 6(a). When a fault happens on the remote terminal bus, the measured voltage V_R at the relay location will have both magnitude and phase angle errors. This error has around 70% probability to be inside the sector *ABCD* as shown in the figure. (If the phase angle error is not considered, the sector will become a line segment.) The sector size becomes smaller as the filtering window increases. The sector for the $I_R Z_L$ component is also shown in the figure. In the figure, point '*A*' corresponds to the maximum allowable reach setting. The adaptive reach setting would have to be kept within this value for proper Zone 1 operation. When this is mapped to the impedance plane, as shown in Figure 6(b), the Mho reach will be 70.14% for a filtering window equal to 0.45 cycle. The adaptive Mho characteristics/reaches can be obtained in a similar fashion for the different pairs of $\{\sigma_r(n), \sigma_\theta(n)\}$ from Table I. The last row in Table I lists the adaptive reach setting values corresponding to these magnitude and phase angle errors.
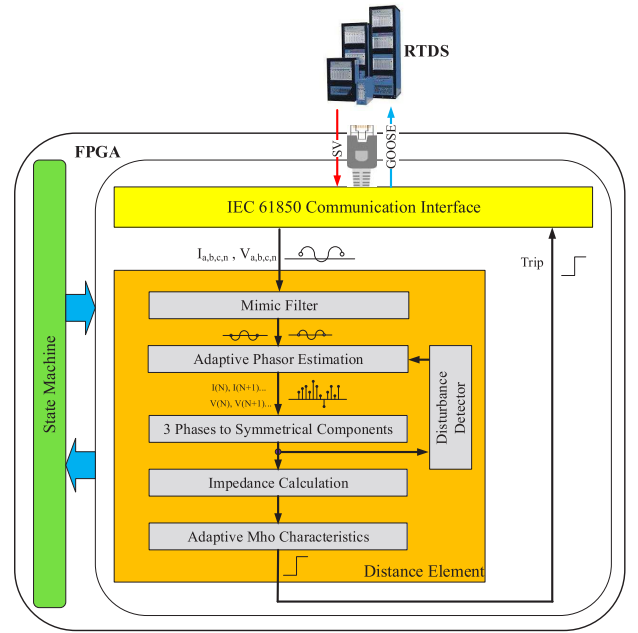
The primary benefit of the adaptive phaselet-based method is that the close-in faults can be detected quickly with a small window, while longer window is used for the Zone 1 boundary to achieve good fault discrimination (trip security). Also high speed tripping is crucial for close-in faults because of the large fault currents involved.

C. Trip Delay Routine

It is activated when the impedance trajectory enters into the adaptive Mho circle for the first time. It then waits for the next couple of phaselets and evaluates if the following consecutive impedances are also located inside the adaptive Mho circle. If so, a trip decision will be made; otherwise, the trip delay routine will be reset to wait for the next activation. Also higher SIR values will need a longer trip delay routine as the voltage at the relay location is going to be lower and will be more prone to magnitude and phase angle errors (relay accuracy is affected by the voltage level). The trip delay settings for different SIRs are listed in Table III.

III. HARDWARE IMPLEMENTATION

The overall architecture of the proposed digital distance relay is shown in Figure 7. It consists of three modules: an IEC 61850 communication interface, a distance element, and a state machine. The IEC 61850 interface implements the SV and GOOSE communication protocols used for the data transfer between the FPGA board and the RTDS, as shown in Figure 8. SV packet format is also demonstrated in Figure 8.

The phaselet-based algorithm proposed in Section II is implemented in the distance element module inside the FPGA. Table II lists the main FPGA hardware usage for the entire design. The available resources of the Xilinx Virtex-6 XC6VLX240T-1FFG1156 FPGA chip are also listed [18].
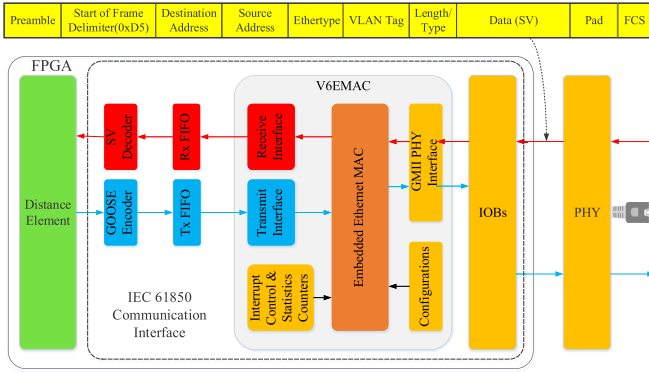
| Preamble | Start of Frame Delimiter(0xD5) | Destination Address | Source Address | Ethertype | VLAN Tag | Length/ Type | Data (SV) | Pad | FCS |

Fig. 8.   FPGA implementation of the IEC 61850 communication interface.
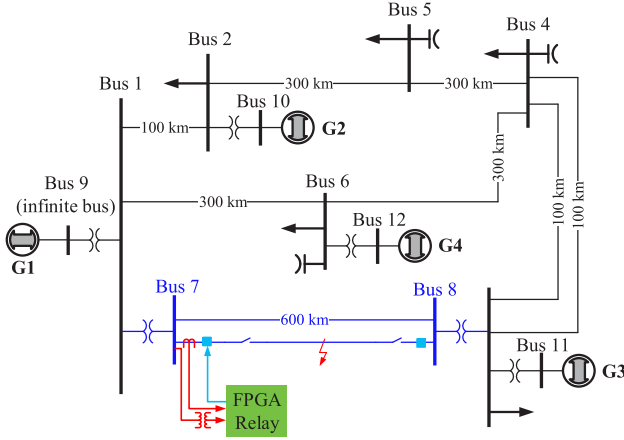

Fig. 9.   IEEE 12-bus system used for testing.

TABLE II
FPGA HARDWARE RESOURCES UTILIZATION

Resources	Slice Registers	Slice LUTs	DSP Blocks
Available	301440	150720	768
Usage	149279 (49.5%)	111258 (73.8%)	526 (68.5%)

50-70% of the resources are used and additional protective elements can be added to expand functionality. The processing time for one SV packet is typically 4.04 μs, which is much less than the sampling interval of 208 μs. This high speed design can be attributed to the massive hardware parallelism and deep pipelining employed in the three modules, especially in the distance element.

IV. HARDWARE-IN-THE-LOOP TESTING AND RESULTS

In the RTDS simulator, the voltages and currents are sampled at 4,800 Hz and then fed into an RTDS Gigabit Transceiver Network Interface (GTNET) card [19] with IEC 61850 SV protocol activated. The encoded packet are sent to the Ethernet switch and further routed to the FPGA. The output trip signal in GOOSE format is sent to another GTNET card with GOOSE protocol enabled. The GOOSE message received is then applied to the dedicated circuit breaker.

Inside the FPGA, a global clock of 125 MHz is used for most computations. A secondary clock of 12.5 MHz is generated to interface with the PHY device

TABLE III
TEST SYSTEM SETTINGS USED IN SIMULATIONS

Phaselet size	4 (samples)
Mimic filter time constant τ	160 (samples)
Zero sequence compensation factor k_0	2.8489
Fault resistance	0.01 Ω
Trip delay setting (SIR=1)	2 (phaselets)
Trip delay setting (SIR=10)	5 (phaselets)
Adaptive Mho characteristics settings	[0 0 0 0 0 0 0 0 0.701 0.724 0.737 0.742 0.744 0.747 0.754 0.763 0.773 0.784 0.794 0.802]
Adaptive Mho settings - no consideration of phase angle error	[0 0 0 0 0 0 0 0 0.770 0.782 0.791 0.797 0.804 0.810 0.817 0.823 0.829 0.835 0.840 0.844]

(12.5 MHz×8 bits/s = 100 Mb/s). The entire design is synthesized using Xilinx ISE Design Suite Version 14.7.

A modified 12-bus test power system reported in [20] (the system is being standardized as an IEEE test system), as shown in Figure 9 is used. This test system is a composite model of Manitoba Hydro, North Dakota, Minnesota, and Chicago area subsystems. The parameters of the IEEE 12-bus test system are given in [20]. The original 345 kV transmission line between Bus 7 and Bus 8 is replaced by two parallel 400 kV transmission lines. The line parameters and the modeled CT [21] and CCVT [22] are provided in Appendix B. Table III lists other settings used in the studies.

A. Operating Time

The operation times of the proposed FPGA relay for various fault types and fault locations are shown in Figure 10. Each point in the figure is obtained from an average of 100 repetitions using the same system parameters except that the fault inception angle is randomly varied. Relay A sub-cycle element refers to GE's sub-cycle distance relay, which uses a time domain algorithm. It utilizes short-window orthogonal filters to calculate direct and quadrature axis quantities for voltage and current in the time domain. A set of comparators are used to shape the impedance zones [23]. The relay B high-speed element refers to SEL's high-speed distance relay. It uses a fixed half-cycle Fourier filter to estimate phasors. A 3 dB low-pass analog filter with cut-off frequency of 3 kHz is used to pre-filter the voltage and current inputs [24]. The operation times of the distance relay A [23] and the distance relay B [24] are also presented as per their data sheet.

For a line-ground fault, the phaselet method performs better than other methods. The tripping times for close-in faults are similar (because the minimum window size chosen is 40% for the trip decision). For remote end fault such as those at 80% of the maximum reach setting, the proposed relay can operate in 0.74 cycles. For three-phase faults, the operating speed will be faster, while for line-line faults, the operating speed will be slower, but still within 0.85 cycles. This is also faster than a FCDFT-based FPGA relay [25], [26] and its operation time for faults happening at 50% of the reach setting is 1.4 cycles, 1.3

(a) Operating times (cycles) for various line to ground fault locations

(b) Operating times (cycles) for various line to line fault locations

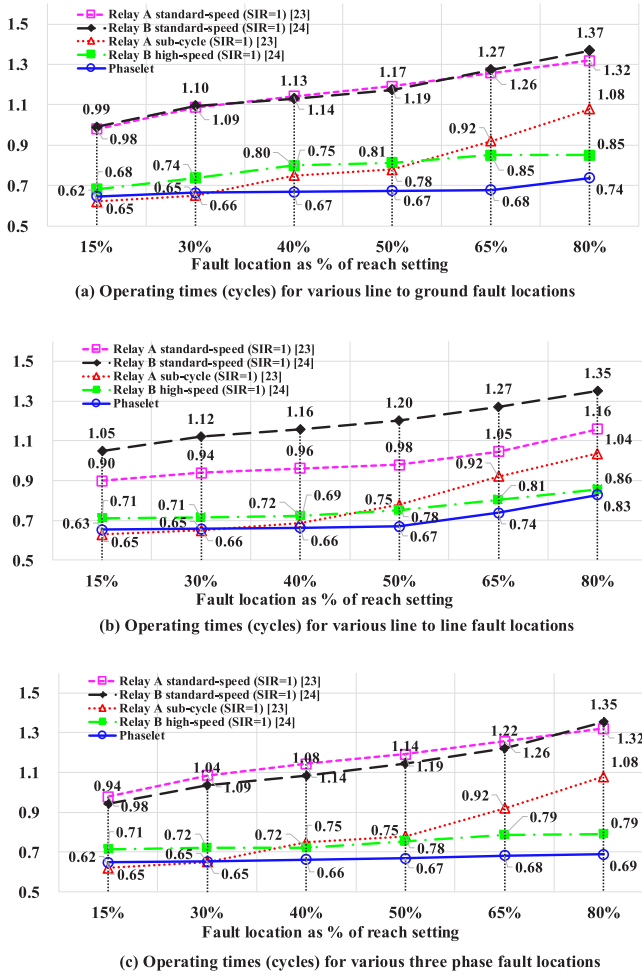(c) Operating times (cycles) for various three phase fault locations

Fig. 10.   The operation times of different distance relays.

cycles and 1.3 cycles for line-ground, line-line and three-phase faults respectively.

Figure 11 shows the waveforms of the current and voltage for a line-ground fault happening at 50% of the maximum reach setting with SIR equals to 1 and the fault inception angle equals to 60°. The associated changes of the disturbance signal, window size, and trip signal are also presented. The disturbance detector can pick up the current change after 0.1 cycles upon fault inception. The filtering window is immediately changed to phaselet size and begins to increase until one full cycle. At 0.45 cycles after the disturbance is picked up, the apparent impedance enters into the adaptive Mho circle (70.1% of the transmission line) and a trip delay routine is started. After evaluating two more phaselets, which equals a 0.1 cycle delay, a trip decision is finally made. In total, the proposed relay can achieve a speed of 0.65 cycles for this case.

The corresponding impedance trajectories is shown in Figure 12. The trajectory enters into the adaptive Mho circle for the first time at 0.3 cycles. The adaptive Mho setting is 0 at this moment since the filtering window is 0.2 cycle, which is less than the threshold of 0.4 cycle. At 0.55 cycle, the Mho setting is increased to 70.1%. The trip delay routine is activated for the security of the trip decision and two more phaselets are delayed. Because after the delay the estimated
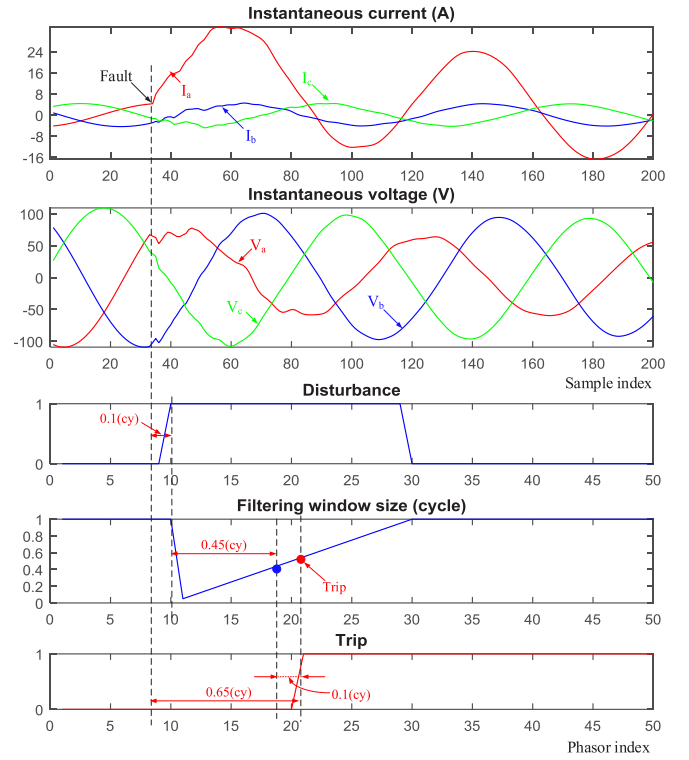

Fig. 11.   Real time fault transients (double line, SIR=1, A-G fault location=50% of maximum reach setting, fault inception angle=60°).
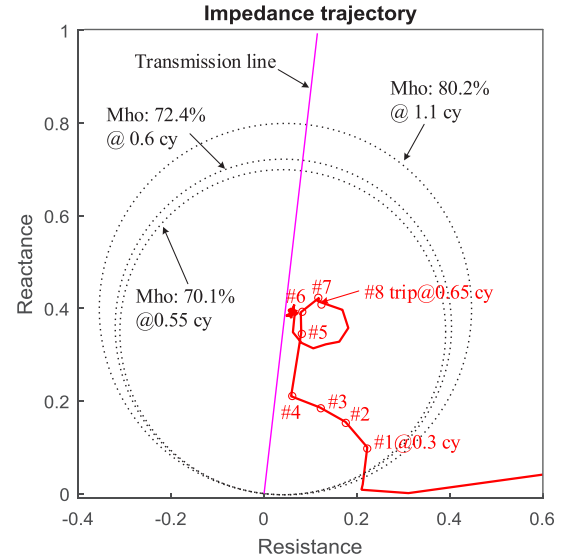

Fig. 12.   Impedance trajectory for the line-ground fault.

impedance still stays inside the adaptive Mho circle, a trip signal is eventually confirmed at 0.65 cycles.

The communication latency (two-way) is about 5.23 ms on average, as shown in Figure 13. The response time performance matches the standard criteria (specified in IEC 61850-5, Type 1A, Class P2/3 messages, 3 ms for one way).

B. Relay Reliability

The security of the proposed relay is tested for faults happening at the remote terminal bus of the line with a SIR equals
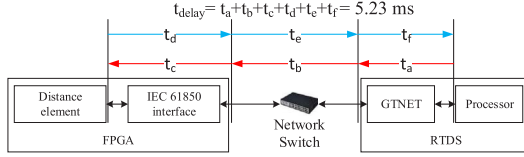
Fig. 13. IEC 61850 communication latency.

TABLE IV
INCORRECT TRIPPING PROBABILITY WITH SIR=10

| # of lines	Single line			2 lines
Method	FCDFT	**Phaselet-no consideration of phase angle error**	**Phaselet**	Phaselet
Line-ground	0%	**8%**	**2%**	0%
Line-line	0%	**8%**	**1%**	0%
Three-phase	0%	**0%**	**0%**	0%

to 10 (line length is changed to 60 km). With a higher SIR, a longer trip delay is required. A 0.25 cycle delay is used for comparing the proposed method and FCDFT according to Table III. The mutual coupling between the parallel lines makes the apparent impedance larger [27] than the actual fault impedance so the relay security is not going to be compromised due to mutual coupling, as shown in the last column of Table IV.

When one of the lines between Bus 7 and Bus 8 is removed, relay over-reach may happen. The left three columns in Table IV give the probability of an incorrect trip when tested with 100 random fault inception angle values with single transmission line setup. FCDFT gives the best results due to the longer one cycle window. Phaselet has good security for three-phase faults, but has a 2% possibility to incorrectly trip for line to ground fault and 1% possibility for line to line fault. A key finding here was that when the phase angle errors are not considered, the incorrect trip probability is 8% for line to ground and line to line faults. The results clearly show that the phase angle errors are an important consideration to improve the trip reliability with the phaselet method.

Figure 14 gives the magnitude and phase angle errors for different SIRs with different line-ground fault locations. With SIR equal to 1, the magnitude and angle errors for FCDFT decrease as the fault location moves farther away. This is because the impedance trajectory for a FCDFT enters into the Mho characteristic from above. For close-in faults, even with an additional 0.1 cycle trip delay, there is going to be a significant difference between the estimated value and the actual value of impedance so the errors are large. As the fault location moves away from the relay location, this gap becomes smaller and will result in a smaller magnitude error. For a fault at 80% of zone 1 boundary, the magnitude error can be as small as 3.6%. For phaselet, the magnitude error will be around 10%, which agrees well with the theoretical calculation given in Table I. This value is lower than FCDFT for close-in faults since no pre-fault values are included. However, the angle error is higher than for FCDFT.
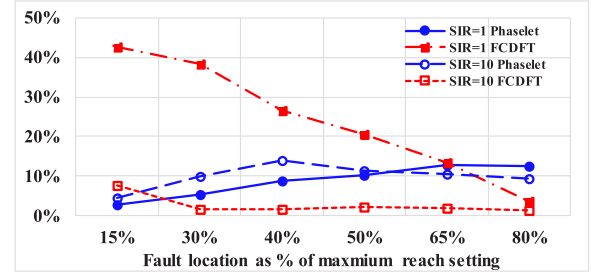
(a) Magnitude error for different fault locations
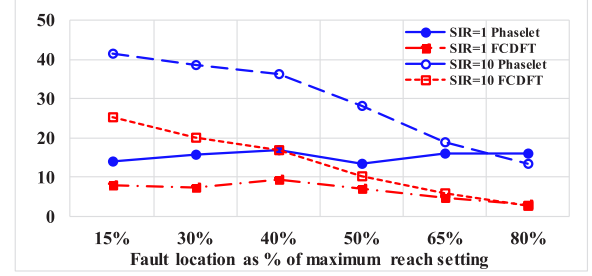
(b) Angle error (degrees) for different fault locations
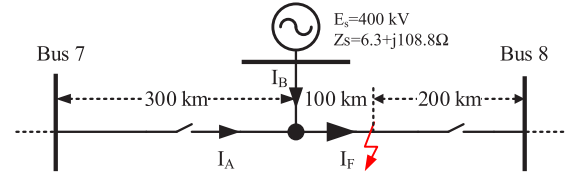
Fig. 14. Magnitude and angle error.

Fig. 15. Test case for line infeed (SIR=1, A-G fault inception angle=60°).

With SIR equal to 10, a longer trip delay is needed (0.25 cycles) for relay security according to Table III. With a high SIR value, FCDFT gives better magnitude accuracy ($<$10% magnitude error). With the proposed phaselet method, the magnitude errors will be higher, but still lower than 15% level. The angle error increases and is between 10°-40°, which is higher than the theoretical values from Table I. This is because the errors of the relay inputs are assumed to be uncorrelated and to have a constant variance. However, in real power systems, the errors are correlated and the variance varies and therefore gives rise to larger angle errors. An appropriate trip delay is used to ensure a secure trip.

C. Effect of Line Infeed

Distance protection with line current infeed requires careful consideration. The test scenario used for the study is shown in Figure 15. The infeed current I_B has the same magnitude as I_A. The impedance seen by the proposed relay at Bus 7 is given by: $0.5 \cdot Z_L + I_F/I_A \cdot 0.17 \cdot Z_L$. The measured result from the test is $0.85 \cdot Z_L$ and the relay would fail to see the fault. One way to address this issue, is sending the voltage and current magnitude/angle from each relay location to each of the other relays. The three-terminal line arrangement is reduced to a two-terminal equivalent and the corrected impedance value is then calculated. For this test case, the corrected impedance value is $0.72 \cdot Z_L$ and the fault could be successfully detected.
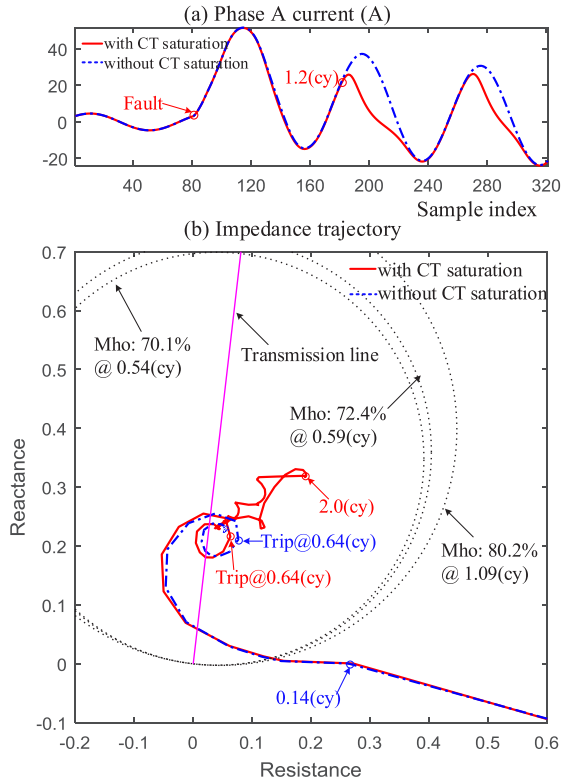
Fig. 16. Effect of CT saturation (double line, SIR=1, A-G fault location=30% of maximum reach setting, fault inception angle=30°).

D. Effect of CT Saturation

The CT ratio is 600 : 5. A line-ground fault is introduced at 30% of the maximum reach setting, where CT saturation has a noticeable effect compared to remote faults. Figure 16(a) shows that CT saturation barely introduces any signal distortion within the first one and quarter cycles after fault inception. In Figure 16(b), the two impedance trajectories overlap during this time. This is also the period when the proposed relay makes its decision. Therefore, we can see that they both initiate a trip signal at 0.64 cycles. After this period, the trajectory will stay at the final steady state if CT saturation is not present; otherwise, it will swing to a larger impedance and then settle back to the same final steady state. This oscillatory behavior is due to the transient distortion introduced in the following cycles, as shown by the solid line in Figure 16(a). In summary, CT saturation does not occur instantly. The sub-cycle relay operation takes place even before severe CT saturation occurs. (Reference [28] also reports a similar finding for high-speed relays.)

E. Effect of CCVT Transient Errors

Effect of CCVT transient response is described in [22]. A system with an SIR = 10 is selected and a line-ground fault is applied at the remote terminal bus. The fault inception angle is 60°. The secondary voltage and its corresponding estimated phasor magnitude are depicted in Figure 17. The dashed line represents the output of an ideal CCVT, while the solid line represents the output of the modeling CCVT. The disturbance detector detects the transient current change in 0.02 cycles,
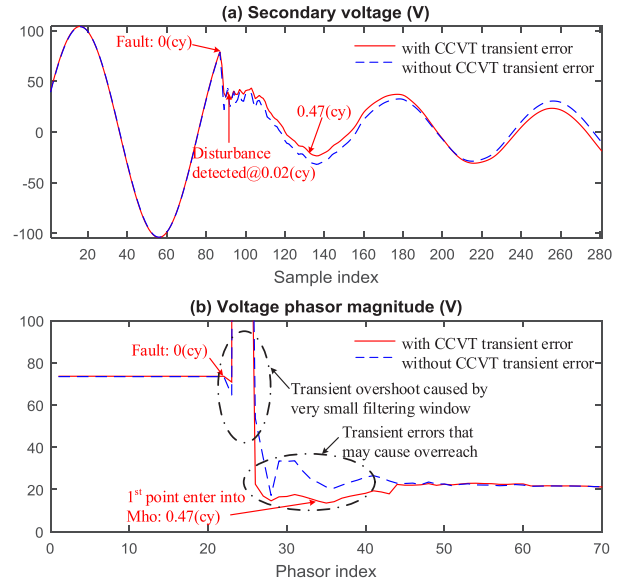

Fig. 17. Secondary voltage and the estimated phasor magnitude (single line, SIR=10, A-G fault location=remote terminal bus, fault inception angle=60°).
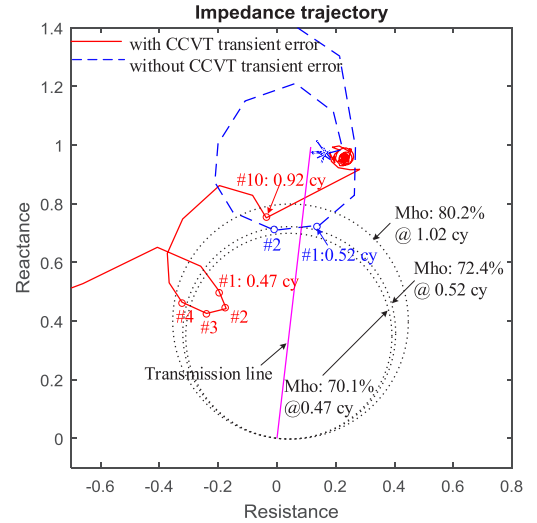

Fig. 18. Impedance trajectory with ideal CCVT and transient error.

and then the filtering window is immediately changed to P. The figure also shows that CCVT transient errors result in a smaller voltage phasor, which further leads to a smaller apparent impedance.

Figure 18 shows the corresponding impedance trajectories. When the CCVT transient error is not present, the impedance trajectory enters into the reach setting at 0.52 cycles but immediately swings out. With the CCVT transient error, the apparent impedance swings into the 70.1% Mho circle at 0.47 cycles. The subsequent three estimates also fall within the Mho circle and potentially can cause a false trip with a trip delay of 0.1 cycle. Since SIR equals 10 for this case, a longer 0.25 cycles trip delay is used to prevent false trip under these conditions.

F. Effect of Shunt Capacitor Energization

When a capacitor bank is energized or de-energized, the initial current and voltage transients produced are quite far
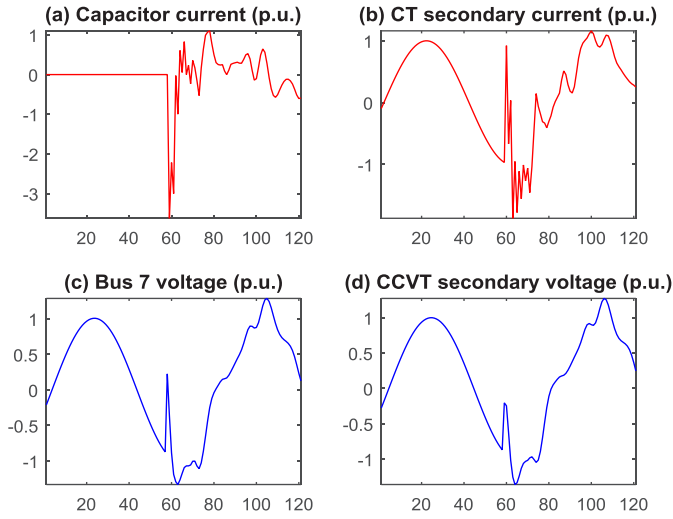
Fig. 19. System transients (phase A) during a shunt capacitor energization (single line, SIR=1, capacitor size: 102 MVar).

from the relay characteristics and would not cause relay mal-operation. Figure. 19(a) shows the capacitor current at the moment that a capacitor bank is connected to Bus 7. A high-frequency, high-magnitude current flows into the capacitor to attempt to maintain the system voltage. The CT secondary current is contaminated by a high frequency transient as shown in Figure 19(b). Figure 19(c,d) shows the transient overvoltages. The disturbance detector pickups the disturbance but the transient impedance never enters the Mho characteristics and therefore the relay would not operate incorrectly for this scenario.

V. CONCLUSION

The phaselet-based distance relaying is improved by taking into account both magnitude and phase angle errors of the voltage and current phasors. A transient monitoring index is also used to check the phasor estimation error and correspondingly adjust the adaptive reach setting. The scheme is implemented on a FPGA board, which achieves speeds similar to solid-state relays (the processing time for each sampled packet is 4.04 μs). The proposed sub-cycle method was tested using hardware-in-the-loop simulations using an RTDS simulator and digital substation communication protocols (IEC 61850 SV and GOOSE) to achieve performance comparisons with current sub-cycle methods in the literature. The experimental test shows that the proposed FPGA relay can make secure trip decision in 0.6~0.8 cycles. Even with large CCVT transient errors (SIR equals to 10) and the fault at the remote bus of the line, the proposed relay could make a secure no trip decision.

APPENDIX A
MAGNITUDE-PHASE ANGLE ERRORS ANALYSIS

If we assume error ε for the input has a covariance matrix:

$$E\left(\varepsilon\varepsilon^T\right) = \sigma_\varepsilon^2 I, \tag{A.1}$$

TABLE B1
TRANSMISSION LINE PARAMETERS

Zero sequence series resistance R_0	$0.208\ \Omega/km$
Zero sequence series inductive reactance X_{l0}	$0.6664\ \Omega/km$
Zero sequence series capacitive reactance X_{c0}	$0.5949\ M\Omega \cdot km$
Positive sequence series resistance R_1	$0.0209\ \Omega/km$
Positive sequence series inductive reactance X_{l1}	$0.1813\ \Omega/km$
Positive sequence series capacitive reactance X_{c1}	$0.3159\ M\Omega \cdot km$

then according to [29], the covariance matrix of $\hat{\mathbf{X}}(n)$ is:

$$Var\left(\hat{\mathbf{X}}(n)\right) = \sigma_\varepsilon^2 C^{-1}(n)$$
$$= \sigma_\varepsilon^2 \begin{bmatrix} a_{11}(n) & a_{12}(n) \\ a_{12}(n) & a_{22}(n) \end{bmatrix}, \tag{A.2}$$

Rewriting Equation 3 in the polar form ($\hat{X} = re^{j\theta}$), then the PDF of the phasor magnitude r [16], [17]:

$$f(r) = \frac{2r}{R} e^{\frac{-(r^2+\bar{r}^2)}{R}} I_0\left(\frac{2\bar{r}r}{R}\right), \tag{A.3}$$

where $\bar{r}$ is the expectation of r; R is different for each n and $R = \sigma_\varepsilon^2[a_{11}(n) + a_{22}(n)]$; and I_0 is the Bessel function. The variance of r is given by:

$$\sigma_r^2 = R + \bar{r}^2 - \frac{\pi R}{4} L_{1/2}^2\left(-\frac{\bar{r}^2}{R}\right), \tag{A.4}$$

where $L_{1/2}$ denotes a Laguerre polynomial function. The PDF of the phase angle θ of phasor is given by:

$$f(\theta) = \frac{e^{-g}\left\{1 + \sqrt{\pi}\xi e^{\xi^2}[1 + erf(\xi)]\right\}}{4\pi\sigma_c\sigma_s\sqrt{1-\rho^2}}$$
$$\times \frac{1}{h + u\cos2\theta + v\sin2\theta}, \tag{A.5}$$

where $erf(\cdot)$ is the error function. The other variables are:

$$\sigma_c = \sqrt{a_{11}}, \sigma_s = \sqrt{a_{22}}, \rho = a_{12}/(\sigma_c\sigma_s), \tag{A.6}$$

$$h = \frac{a_{11} + a_{22}}{4a_{11}a_{22}\left(1-\rho^2\right)}, u = \frac{a_{22} - a_{11}}{4a_{11}a_{22}\left(1-\rho^2\right)}, \tag{A.7}$$

$$v = \frac{-\rho}{2\sigma_c\sigma_s\left(1-\rho^2\right)}, \tag{A.8}$$

$$s = \frac{\bar{X}_c\sigma_s - \rho\bar{X}_s\sigma_c}{a_{11}\sigma_s\left(1-\rho^2\right)}, t = \frac{\bar{X}_s\sigma_c - \rho\bar{X}_c\sigma_s}{a_{22}\sigma_c\left(1-\rho^2\right)}, \tag{A.9}$$

$$g = \frac{\bar{X}_c^2 a_{22} + \bar{X}_s^2 a_{11} - 2\rho\bar{X}_c\bar{X}_s\sigma_c\sigma_s}{2a_{11}a_{22}\left(1-\rho^2\right)}, \tag{A.10}$$

$$\xi = \frac{s\cos\theta + t\sin\theta}{2\sqrt{h + u\cos2\theta + v\sin2\theta}}. \tag{A.11}$$

The postfix (n) in $a_{11}(n)$, $a_{12}(n)$, and $a_{22}(n)$ in Equation (A.6)–(A.11) are not shown but implied for clarity purposes. It is hard to get a closed form solution for equation of $\sigma_\theta^2(n)$ or $\sigma_\theta(n)$. Instead a numerical solution of $\sigma_\theta(n)$ is obtained and is given in the third row of Table I.

TABLE B2
CT PARAMETERS

CT ratio	600 : 5
Burden resistance R_b	1 Ω
Burden reactance X_b	0.175 Ω
Secondary resistance R_s	0.235 Ω
Secondary reactance X_s	0.157 Ω

TABLE B3
CCVT PARAMETERS

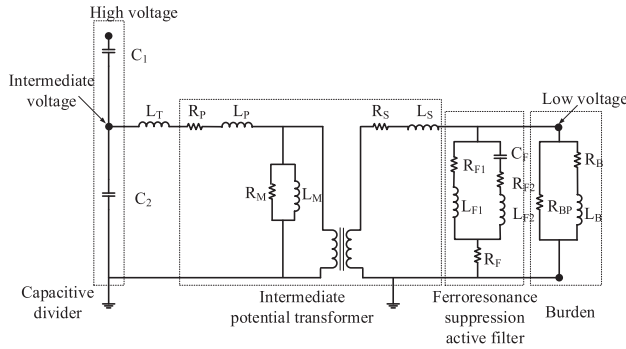| C_1	2.2E-3 μf	R_{F1}	0.5 Ω
C_2	3.78E-2 μf	L_{F1}	1.005 H
L_T	176 H	C_F	9.6 μf
$PT\ ratio$	20000 : 110	R_{F2}	0.5 Ω
R_P	1.4E3 Ω	L_{F2}	0.0001 H
L_P	1.2 H	R_F	37.5 Ω
R_S	0.125 Ω	R_B	14.6 Ω
L_S	1.2E-4 H	L_B	0.0802 H
R_M	1E7 Ω	R_{BP}	1E6 Ω
L_M	5E4 H		

Fig. B1.   CCVT model [22].

APPENDIX B
TEST SYSTEM PARAMETERS

See Tables B1, B2, and B3, and Fig. B1.

ACKNOWLEDGMENT

REFERENCES

[1] E. O. Schweitzer, B. Kasztenny, A. Guzmán, V. Skendzic, and M. V. Mynam, "Speed of line protection—Can we break free of phasor limitations?" in *Proc. 68th Annu. Conf. Protect. Relay Eng.*, College Station, TX, USA, 2015, pp. 448–461.

[2] E. A. Udren and M. Sackin, "Relaying features of an integrated microprocessor-based substation control and protection system," in *Proc. Develop. Power Syst. Protect.*, 1980, pp. 97–101.

[3] C.-S. Yu, Y.-S. Huang, and J.-A. Jiang, "A full- and half-cycle DFT-based technique for fault current filtering," in *Proc. IEEE Int. Conf. Ind. Technol. (ICIT)*, Viña del Mar, Chile, Mar. 2010, pp. 859–864.

[4] T. S. Sidhu, X. Zhang, and V. Balamourougan, "A new half-cycle phasor estimation algorithm," *IEEE Trans. Power Del.*, vol. 20, no. 2, pp. 1299–1305, Apr. 2005.

[5] V. Balamourougan and T. S. Sidhu, "A new filtering technique to eliminate decaying DC and harmonics for power system phasor estimation," in *Proc. IEEE Power India Conf.*, New Delhi, India, 2006, pp. 1–6.

[6] L. Zhan, Y. Liu, and Y. Liu, "A clarke transformation-based DFT phasor and frequency algorithm for wide frequency range," *IEEE Trans. Smart Grid*, vol. PP, no. 99, p. 1, Mar. 22, 2016, doi: 10.1109/TSG.2016.2544947.

[7] H. C. Wood, N. G. Johnson, and M. S. Sachdev, "Kalman filtering applied to power system measurements relaying," *IEEE Trans. Power App. Syst.*, vol. PAS-104, no. 12, pp. 3565–3573, Dec. 1985.

[8] A. H. Osman and O. P. Malik, "Transmission line distance protection based on wavelet transform," *IEEE Trans. Power Del.*, vol. 19, no. 2, pp. 515–523, Apr. 2004.

[9] K. Chen, J. Hu, and J. He, "Detection and classification of transmission line faults based on unsupervised feature learning and convolutional sparse autoencoder," *IEEE Trans. Smart Grid*, vol. PP, no. 99, p. 1, Aug. 10, 2016, doi: 10.1109/TSG.2016.2598881.

[10] M. G. Adamiak, G. E. Alexander, and W. Premerlani, "Advancements in adaptive algorithms for secure high speed distance protection," in *Proc. 23rd Annu. Western Protect. Relay. Conf.*, Spokane, WA, USA, Oct. 1996, pp. 1–10.

[11] M. G. Adamiak and W. Premerlani, "A new approach to current differential protection for transmission lines," presented at the Elect. Council New England Protect. Relaying Committee Meeting, Portsmouth, NH, USA, Oct. 1998, pp. 1–16.

[12] Z. Hao *et al.*, "Anti-saturation algorithm in differential protection based on the phaselet," in *Proc. 5th Int. Conf. Elect. Utility Deregulation Restructuring Power Technol. (DRPT)*, Changsha, China, Nov. 2015, pp. 1030–1035.

[13] *IEC 61850 Communication Networks and Systems in Substations*, Int. Electrotech. Comm., Geneva, Switzerland, 2013.

[14] A. G. Phadke and J. S. Thorp, *Computer Relaying for Power Systems*. Chichester, U.K.: Wiley, 2009.

[15] IEEE Power System Relaying Committee, *Application of Fault and Disturbance Recording Devices for Protective System Analysis*, IEEE special publication 87TH0195-8-PWR, 1987.

[16] K. S. Miller, *Complex Stochastic Processes: An Introduction to Theory and Applications*. Reading, MA, USA: Addison-Wesley, 1974.

[17] K.-H. Ding, M. Rangaswamy, and L. Tsang, "Amplitude and phase distributions for bistatic scattering from pierson-moskowitz sea surfaces," in *Proc. IEEE Radar Conf.*, Rome, Italy, 2008, pp. 1–6.

[18] *ML605 Hardware User Guide*, Xilinx, San Jose, CA, USA, Oct. 2012.

[19] *RTDS GTNET Network Interface Card Manual*, RTDS Technol., Winnipeg, MB, Canada, Jan. 2014.

[20] S. Jiang, U. D. Annakkage, and A. M. Gole, "A platform for validation of FACTS models," *IEEE Trans. Power Del.*, vol. 21, no. 1, pp. 484–491, Jan. 2006.

[21] S. H. Horowitz and A. G. Phadke, *Power System Relaying*. Hoboken, NJ, USA: Wiley, 2013.

[22] E. Pajuelo, G. Ramakrishna, and M. S. Sachdev, "Phasor estimation technique to reduce the impact of coupling capacitor voltage transformer transients," *IET Gener. Transm. Distrib.*, vol. 2, no. 4, pp. 588–599, Jul. 2008.

[23] *D90 Plus Line Distance Protection System Instruction Manual*, GE Multilin Inc., Markham, ON, Canada, Jul. 2015.

[24] *SEL-421-4, -5 Protection and Automation System Data Sheet*, Schweitzer Eng. Lab., Pullman, WA, USA, May 2015.

[25] Y. Wang and V. Dinavahi, "Real-time digital multi-function protection system on reconfigurable hardware," *IET Gener. Transm. Distrib.*, vol. 10, no. 10, pp. 2295–2305, Jul. 2016.

[26] Y. Wang and V. Dinavahi, "Low-latency distance protective relay on FPGA," *IEEE Trans. Smart Grid*, vol. 5, no. 2, pp. 896–905, Mar. 2014.

[27] F. Calero, "Mutual impedance in parallel lines—Protective relaying and fault location considerations," in *Proc. 34th Annu. Western Protect. Relay Conf.*, 2007, pp. 1–15.

[28] J. L. Blackburn and T. J. Domin, *Protective Relaying: Principles and Applications*. Boca Raton, FL, USA: CRC Press, 2006.

[29] T. K. Moon and W. C. Stirling, *Mathematical Methods and Algorithms for Signal Processing*. Upper Saddle River, NJ, USA: Prentice-Hall, 2000.

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