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Protective relaying for power transformers using field programmable gate array

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Abstract: A wavelet-based digital directional relay for power transformer protection, implemented using field programmable gate array. The general purpose SPARTAN3E FPGA kit was employed for developing the prototype relay, with all the coding done using the hardware description language VHDL. The relay logic consists of two parts: disturbance detection based on first-level high-frequency details of the voltage signals and fault discrimination using a power-based directional signal derived from the first-level high-frequency details of both voltage and current signals. The real-time windows target Toolbox of MATLAB was used to apply the current and voltage input signals to the prototype relay in real-time. The logic is deterministic, computationally efficient, fast, secure and highly reliable. The operating time is 6 ms, about one-third of power frequency cycle (20 ms). The scheme uses only the sign of the directional signals, rather than the difference in their magnitudes, hence it can work reliably in the presence of fault resistance and current transformer saturation. The validity of the proposed logic was exhaustively tested by simulating various types of internal and external faults, energisation conditions and load variations on a 132 kV system modelled in EMTP/ATP with a 31.5 MVA, 132/33 kV, Y-Δ transformer. The relay was able to correctly discriminate between internal faults, external faults and non-fault disturbances for the entire 880 test cases.

1 Introduction

The reliable operation of a power transformer is of vital importance in maintaining the continuity of power supply. When transformer internal faults occur, immediate disconnection of the faulted transformer is necessary to avoid extensive damage and/or preserve power system stability and power quality. Any unscheduled outage, especially replacement of a faulty transformer, is very expensive and time consuming [1]. Traditionally, a differential scheme is employed for transformer protection. The performance of simple differential relays is seriously affected by current transformer (CT) saturation. Consequently, a percentage differential scheme was introduced which could avoid the effect of CT saturation to some extent. But these relays are subjected to false tripping because of the inrush current that flows during transformer energisation. Since the inrush current is rich in second-harmonics, a restraint quantity based on second-harmonics, was derived and employed to restrain the relay during energisation. But over the years, the advances in transformer construction and improvements in core materials have brought down the level of second-harmonics during inrush. Also, the second-harmonic component during inrush is very low in the case of transformers connected to long transmission lines. Under these circumstances, the relay using second-harmonic restraint may mal-operate during inrush. On the other hand, the increased concentration of electronic and other nonlinear loads, the widespread use of under ground cables, as well as severe CT saturation can result in a sizeable increase in the second-harmonic components in the event of a fault, delaying the operation of the relay.

Recently, modern protection algorithms based on wavelet transforms (WT), artificial neural networks (ANN), fuzzy logic and multi-channel filtering have been proposed by some authors. Bo *et al.* [2] proposed

a fault-detection technique based on fault generated high-frequency transients extracted using multi-channel filters. Mao and Aggarwal [3] and Ozgonenel [4] used WT to decompose the differential current signals into wavelet components, the spectral energies of which was used to train an ANN to discriminate between magnetising inrush and internal faults. Youssef [5] proposed a wavelet-based technique for transformer protection with second-harmonic component of transformer currents used for blocking false trips during transformer energisation. In another paper [6], Youssef proposed a fuzzy logic-based protection technique with WT pre-processor. Mortazavi and Khorashadi-Zadeh [7] proposed a scheme with a WT-based feature extraction module followed by an ANN classifier stage for deriving restraint signal during magnetising inrush. Saleh and Rahman [8] and Eissa [9] proposed a WT-based algorithm for transformer protection. Sheng and Rovnyak [10] proposed the use of decision trees and wavelet analysis for the protection of large transformers. Most of the above schemes are computationally intensive and requires past information of the system behaviour or expert knowledge and hence are system dependent.

The present work employs a new scheme based on WT to extract high-frequency information in 500–1000 Hz range. The relay logic consists of two parts: disturbance detection and fault discrimination. Disturbance detection is based on first-level high-frequency details of the voltage signals on high-voltage (HV) and low-voltage (LV) windings. A new power differential protection technique based on a directional signal is used for fault discrimination. The directional signal is derived based on the product of high-frequency details of currents and voltages using a WT approach. Since only a single level of decomposition is employed, the computational requirements are reduced considerably when compared with multi-level decomposition applied for differential protection schemes reported in literature. Another important feature is that the scheme is deterministic and not system dependent, unlike the protection algorithms which use the wavelet-based feature extraction for training neural networks or building fuzzy rule base. Also, as the scheme relies on the sign of the directional signals, rather than the difference in their magnitudes, it can work reliably in the presence of fault resistance and CT saturation. The actual hardware implementation of the proposed scheme was realised using field programmable gate array (FPGA).

2 Test system

The proposed scheme was tested on a system modelled in EMTP/ATP by simulating various types of faults, transformer energisation conditions and load variations. The system shown in Fig. 1, consists of a 31.5 MVA, 132/33 kV Y-Δ transformer with star

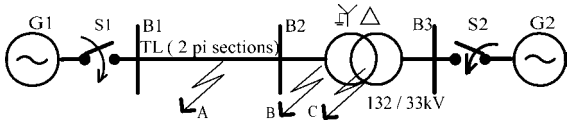

Figure 1 *Test system*

point grounded. It is modelled using the linear RL matrices obtained from BCTRAN routine available in EMTP/ATP [11], with a nonlinear hysteretic reactor (type 96) connected to the LV side to account for transformer nonlinearity. Shunt capacitances of small values were added across the windings to evaluate the behaviour of the transformer during high-frequency transients generated during fault and inrush conditions. The transmission line of 100 km length is modelled as cascaded π consisting of two identical sections. Transformer can be energised from HV side by closing switch S1, from LV side by closing switch S2 and also by simultaneous closing of S1 and S2 in some conditions. Faults anywhere along transmission line, indicated by *A*, are external faults. Faults at positions *B* and *C* are internal faults. The faults can be bolted faults or through fault resistance. Dynamic load variation conditions can be simulated by switching RL loads at buses B1, B2 or B3. System load level can be changed by changing the relative phase angles of equivalent generators G1 and G2.

2.1 Winding model for internal faults

Transformer protection requires accurate representation of the transformer which can model the winding faults also. Bastard *et al.* [12] showed that if a transformer terminal model in terms of winding resistance, self and mutual inductances, that is, 6×6 RL matrices from BCTRAN routine for a three-phase two-winding transformer, are known, then 7×7 and 8×8 RL matrices can be determined for turn-to-ground and turn-to-turn faults, respectively. It is assumed that a turn-to-ground fault divides a winding into two parts resulting in seven windings and a turn-to-turn fault divides the winding into three parts resulting in eight windings. The matrices are calculated by using the principles of consistency, leakage and proportionality. One of the main requirements in this calculation is the value of leakage factor between the sub-windings, details of which is available in [12–15] and hence not repeated here.

3 Proposed relay logic for transformer protection

Any intentional or unintentional change in an electrical network is accompanied by transients, which is a natural process by which the power system moves from one steady-state condition to another. A transformer fault typically causes a low-frequency oscillatory type of transient, the spectral content of which is <5 kHz,

before settling into the post-fault steady-state condition. Typical duration of this transient, which has a wealth of information embedded in it, is 0.3–50 ms and has a magnitude range of 0–4 p.u. WT is used for extracting information from transients, by first-level decomposition of the HV and LV side voltages and current signals. WT is a relatively new tool which is capable of providing both the time and frequency information simultaneously, hence giving a time–frequency representation of the signal [16–18]. Unlike fast Fourier transform (FFT), which works well for signals with smooth or uniform frequencies, WT works better with signals having sharp discontinuities and non-stationary nature. Also, WT is less computationally complex, taking $O(N)$ computations as compared with the $O(N \log N)$ computations required by FFT, where N is the number of samples of the input signal. It expands a signal in terms of a wavelet, generated using translation and dilation of a fixed wavelet function called the 'mother wavelet'. The choice of mother wavelet is important in detecting and localising different types of fault transients. A commonly used mother wavelet suitable for protection applications is Daubechies' wavelet and for this work, the high-pass decomposition filter of 'db-6' wavelet is used. The three-phase current and voltage signals, $v_{(a,b,c)}[n]$ and $i_{(a,b,c)}[n]$ of HV and LV windings are passed through a db-6 high-pass filter. The filter output is down-sampled by 2 to obtain level-1 high-frequency detail coefficients, $v_{\mathrm{hfd}(a,b,c)}[n]$ and $i_{\mathrm{hfd}(a,b,c)}[n]$, in the range of 500–1000 Hz. Wavelet decomposition filter is implemented as an 11th-order finite-impulse response filter.

3.1 Signal pre-processing

The current and voltage signals obtained from the power system are analog signals. In order to make further processing of these signals by digital means possible, they have to be converted into digital signals. Hence, a signal processing unit is the first stage of any digital/numerical relay. The proposed scheme depends on extracting embedded information from the transients generated during faults and disturbances. For 50 Hz systems, the frequency band of 0–1000 Hz is more informative. A sampling frequency of 2 kHz is chosen to extract signals in this band. The signal processing unit should be designed in such a way that this band of frequencies is extracted and converted into digital form. The main components of the signal processing unit are the (i) transducers and isolation, (ii) anti-aliasing filters, (iii) sample and hold, (iv) multiplexer and (v) analog-to-digital converter (ADC). The signal pre-processing stages are shown in Fig. 2.

The currents and voltages in a practical power network are of very high values which cannot be handled by the electronic components and circuitry. It

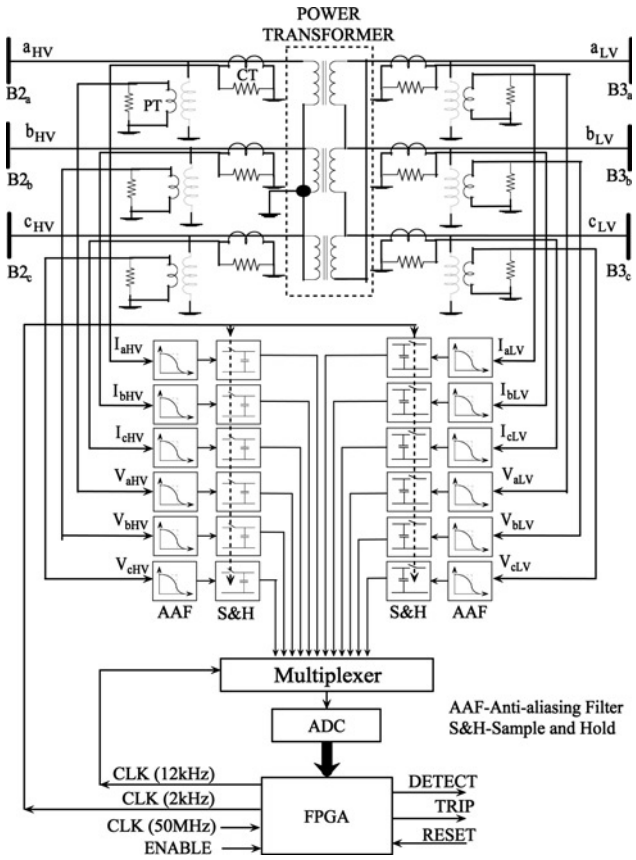

Figure 2 *Signal pre-processing*

is essential to bring down these current and voltage values to levels so that further processing is possible. Since ADC can accept only voltage signals, this module has to convert currents to equivalent voltages. Also, the electronic circuitry and the relay itself have to be isolated from the heavy currents and HVs. These requirements are achieved with the help of potential and CT circuits, which not only step down the voltages and currents but also provide isolation.

Although the power frequency is roughly fixed at 50 or 60 Hz, the frequencies generated because of faults and disturbances cannot be predicted. In other words, the signals from power system cannot be expected to be band-limited. The Nyquist criterion dictates that all signals must be band-limited to less than half the sampling rate of the sampling system. Hence, an analog low-pass filter or anti-aliasing filter must be used to band-limit the signals before converting them to digital form. A sharp frequency response is desirable to completely remove the unwanted harmonics. However, as the frequency response of a filter becomes sharper, the time-domain response becomes worse. So a balance must be achieved between the two. A second order Butterworth filter with a cut-off frequency of 800 Hz is suitable for this work as the detection of the presence of certain frequency components is more important than their

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actual magnitude. Cut-off frequency <1000 Hz ensures that the attenuation is high for frequencies >1000 Hz, thereby avoiding aliasing.

A practical ADC cannot make an instantaneous conversion, the input value must necessarily be held constant during the time that the converter performs the conversion. The purpose of the sample and hold circuitry is to take a snapshot of the analog signal and hold the value. In most relaying applications, a number of analog signals will be monitored. A system can be built with a dedicated ADC channel for each analog signal, but the economical approach is to use an analog multiplexer which has many inputs and one output. The analog multiplexer consists of an array of analog switches controlled with digital logic. It uses the digital control logic to select a specific analog input and direct it to its output. The multiplexed signal is converted into digital form using ADC, the output of which is applied as input to the FPGA. Control signals required by the signal pre-processing circuit are supplied by the FPGA.

3.2 Disturbance detection

The power system is, in general, subjected to a lot of disturbances, which may or may not be a credible fault as far as a particular protection scheme is concerned. The first step is to detect these disturbances. In the proposed relaying scheme, a voltage-based disturbance detection is adopted as the changes are reflected instantaneously in the voltages compared with the current. Disturbance is detected in a phase voltage signal if the absolute value of the first difference of the high-frequency detail coefficients is greater than a threshold value. This logic for phase a of HV side is represented by

$$D_{ah}(n) = \begin{cases} 1 & \text{if } |(v_{\text{hfd}a}[n] - v_{\text{hfd}a}[n-1])| > \text{Th} \\ 0 & \text{otherwise} \end{cases} \quad (1)$$

The Detect signal goes high, if a disturbance is detected in any of the six voltages (three phase HV and three phase LV)

$$\text{Detect}(n) = OR(D_{ah}, D_{bh}, D_{ch}, D_{al}, D_{bl}, D_{cl}) \quad (2)$$

The threshold value, Th, can be fixed based on the maximum expected voltage level (analog input to the signal pre-processor), sampling frequency and the wavelet chosen. For a maximum analog input magnitude of 15 V, sampling frequency of 2 kHz and db-6 wavelet, the maximum value of first difference is 6×10^{-4} (this can be found out by passing the first difference of a sine input of peak value 15 and sampled at 2 kHz, through a db-6 high-pass filter). Choosing a multiplication factor of 3 to detect credible disturbances, the threshold is fixed as $\text{Th} \simeq 2 \times 10^{-3}$. The time required for the disturbance detection is 1 ms.

3.3 Fault discrimination

The transformer protection logic has to act only for faults within the transformer. Hence, it is required to discriminate between the various disturbances that are detected, as internal and external. This is achieved based on a power directional signal. Once Detect(n) goes high, the three-phase voltage and current detail coefficients, $v_{\text{hfd}(a,b,c)}[n]$ and $i_{\text{hfd}(a,b,c)}[n]$ are multiplied to derive high-frequency power signals $P_{a\text{HV}}[n]$, $P_{b\text{HV}}[n]$ and $P_{c\text{HV}}[n]$ for HV and $P_{a\text{LV}}[n]$, $P_{b\text{LV}}[n]$ and $P_{c\text{LV}}[n]$ for LV windings, respectively. Equation (3) represents this calculation for phase a of HV side

$$P_{a\text{HV}}[n] = v_{\text{hfd}a}[n] \times i_{\text{hfd}a}[n] \quad (3)$$

The total instantaneous power of three phases $P_{t\text{HV}}[n]$ and $P_{t\text{LV}}[n]$ are then derived as

$$\begin{aligned} P_{t\text{HV}}[n] &= P_{a\text{HV}}[n] + P_{b\text{HV}}[n] + P_{c\text{HV}}[n] \\ P_{t\text{LV}}[n] &= P_{a\text{LV}}[n] + P_{b\text{LV}}[n] + P_{c\text{LV}}[n] \end{aligned} \quad (4)$$

The direction signals for HV and LV windings is the cumulative sum of these power signals denoted as $P_{\text{HV}}[n]$ and $P_{\text{LV}}[n]$, respectively, and is derived as

$$\begin{aligned} P_{\text{HV}}[n] &= \sum_{i=1}^{n} P_{t\text{HV}}[n] \\ P_{\text{LV}}[n] &= \sum_{i=1}^{n} P_{t\text{LV}}[n] \end{aligned} \quad (5)$$

Pre-fault value of this power signal is negligible as high-frequency power components will be absent. A fault introduces high-frequency oscillations and hence high-frequency power flows. After a delay of 5 ms to allow the signals to reach a steady-state, the direction of P_{HV} and P_{LV} are determined. If the directions of these signals are same, an internal fault is indicated and the Trip signal goes high. This is represented by

$$\text{Trip} = \begin{cases} 1 & \text{if } P_{\text{HV}} \text{ and } P_{\text{LV}} \text{ are both of same sign} \\ 0 & \text{otherwise} \end{cases} \quad (6)$$

The total time between the actual occurrence of a disturbance and the issue of Trip signal (for internal faults) is 6 ms. Fig. 3 shows the functional block diagram of the proposed relaying scheme.

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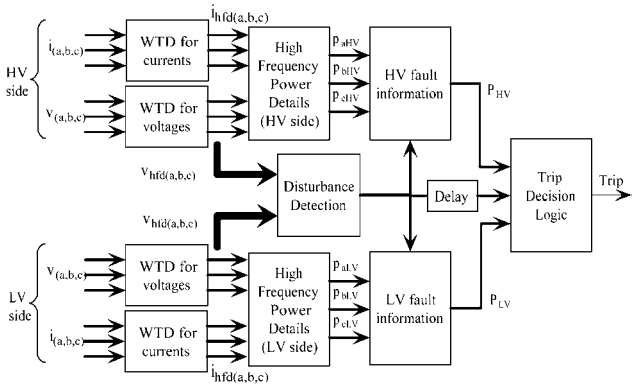

Figure 3 *Functional block diagram for the proposed relaying scheme*

4 FPGA design flow

The hardware realisation of the proposed algorithm was done using FPGA. FPGA contains a matrix of logic elements which can be interconnected in any desired configuration by the user to implement a given application. In this way, one can devise special purpose functional units that are highly efficient for the desired task. As FPGAs can be reconfigured dynamically, it is possible to optimise them for more complex special tasks at speeds that are higher than what can be achieved with general purpose processors. FPGAs come in a wide variety of sizes with advanced features. An FPGA is generally composed of three types of elements [20]: configurable logic blocks (CLB), input/output blocks (IOB) and programmable interconnects (PI). The user can implement logic functions for a given application through CLBs, interface the external package pins to the internal logic using IOBs and routing the paths for connecting the CLBs and IOBs into networks with the PIs.

A typical FPGA design flow consists of design entry, design synthesis, design implementation and FPGA device programming. At the design entry stage, the intended behaviour of the FPGA device is described by means of a hardware description language (HDL) like VHDL [21] or Verilog. The design is synthesised to obtain an intermediate file, called a netlist. The netlist is translated and mapped, which fits the design into the available resources on the target device. Place and route tool, then places and routes the design according to the timing constraints. Programming file generation tool creates a bitstream file, referred as bitmap that can be downloaded to the device. The FPGA design flow is shown in Fig. 4. Design

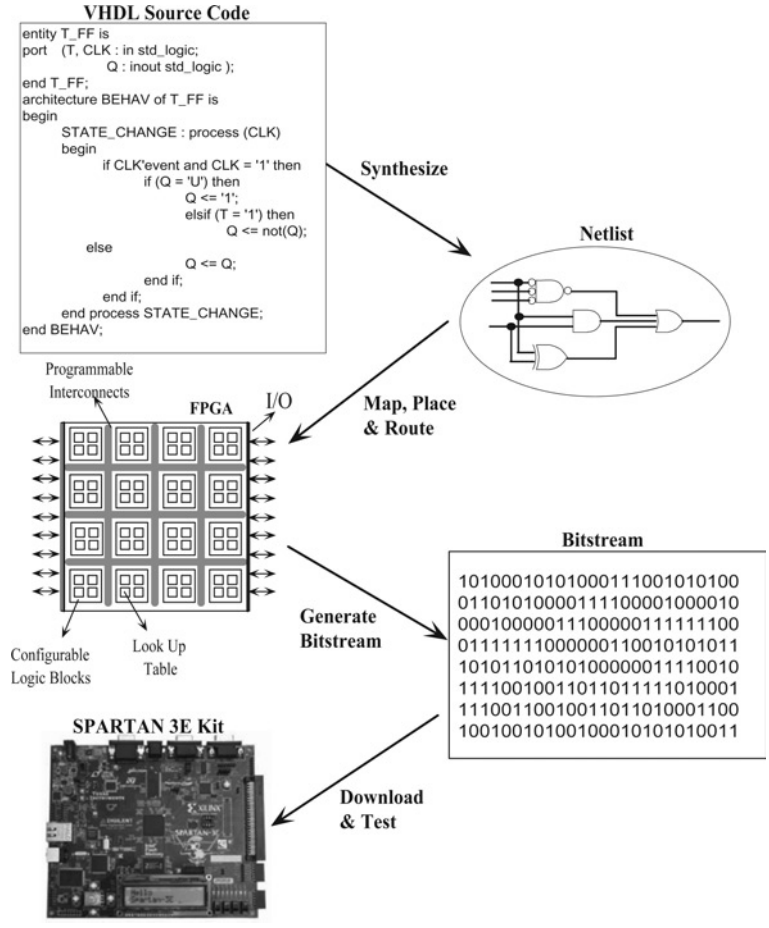

Figure 4 *FPGA design flow*

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verification, which includes both functional verification and timing verification, can be done at different points during the design flow.

Ability to construct highly parallel structures, for processing data, is the main advantage of FPGAs. When compared with a microprocessor or DSP, where performance is tied to the clock rate, FPGA performance is tied to the amount of parallelism that can be brought in the algorithms. Configurability of FPGAs, which allows a design to be modified even after deployment in an end application, is another highlight. FPGA has many degrees of freedom in implementing signal processing functions. The same system can be implemented in different ways to meet the time–resource constraints. An FPGA provides considerable flexibility in defining the arithmetic precision throughout a computation. In comparison, there is a limit on the arithmetic precision and the number of instructions that can be implemented in a microprocessor or a digital signal processor (DSP). The software support for FPGA design tools is another important consideration. Xilinx:ISE WebPACK series provide freely downloadable full-fledged FPGA design environment.

4.1 Simulation results

In order to test and verify the performance of the proposed logic before hardware implementation, the simulation of the logic is carried out using ModelSim SE 6.0D, which gives an idea of internal signals on which the output decisions are based. Fig. 5 shows the multiplexed voltage and current signals and direction signals along with the Detect and Trip outputs for a phase *b* to ground fault on LV winding. The instant of fault is indicated by the vertical cursor. The directional signals are both positive, indicating an internal fault. The corresponding signals during transformer energisation are shown in Fig. 6, where the directional signals are opposite in nature and hence no Trip is issued.

5 Hardware implementation

Xilinx:ISE WebPACK-8.1i was used to synthesise and implement the design into the FPGA chip. The general purpose SPARTAN3E FPGA kit which has an XC3S500E-4-FG320 IC developed by Xilinx Inc. [19], was used for prototype development, because of its cost effectiveness. XC3S500E-4-FG320 chip has over 10 000 logic cells and 232 user I/O pins. It has on-board USB-based FPGA download/debug interface and 50 MHz clock oscillator. The inputs to the FPGA chip for the present application are Clock, Reset, Enable, three-phase current and voltage signals from both windings of the transformer. The main outputs are the Detect and Trip signals. The FPGA device utilisation details for the transformer protection logic are provided in Table 1. It can be observed that only

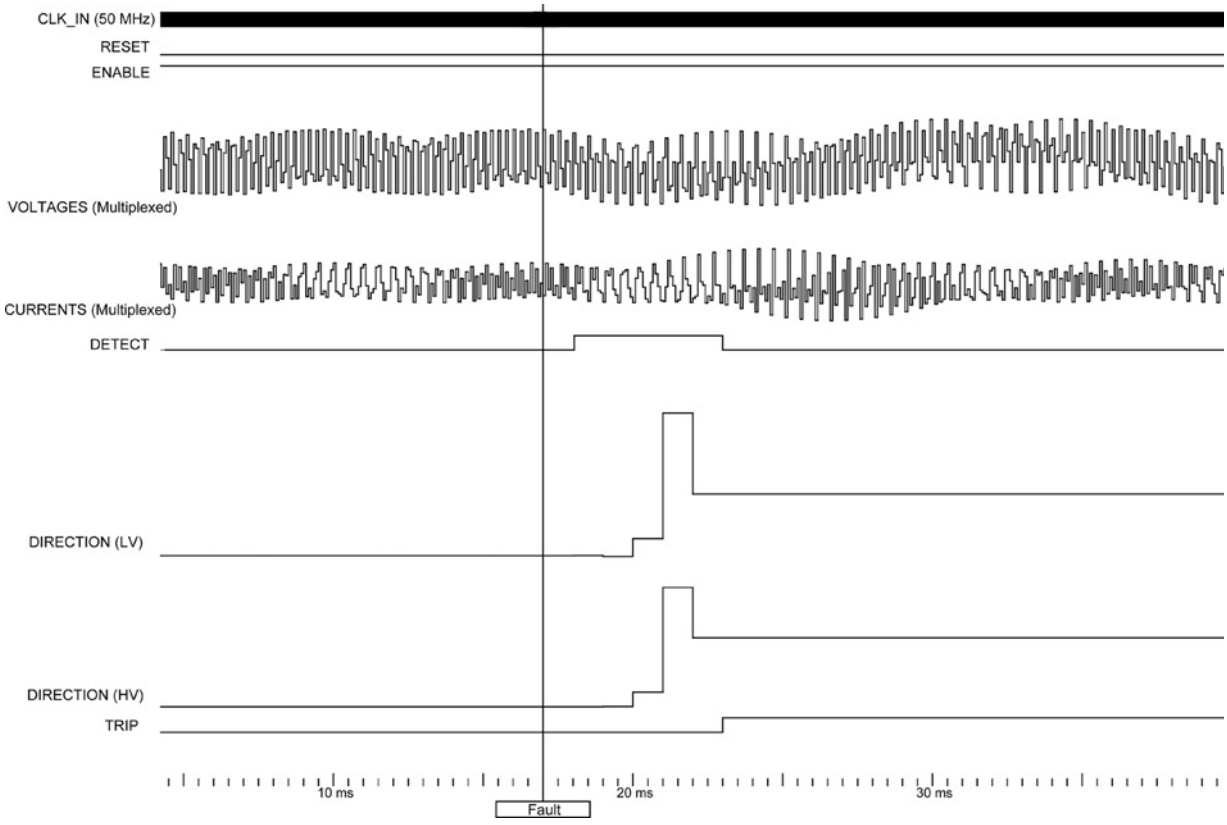

Figure 5 *Simulation result for phase b to ground fault on LV winding*

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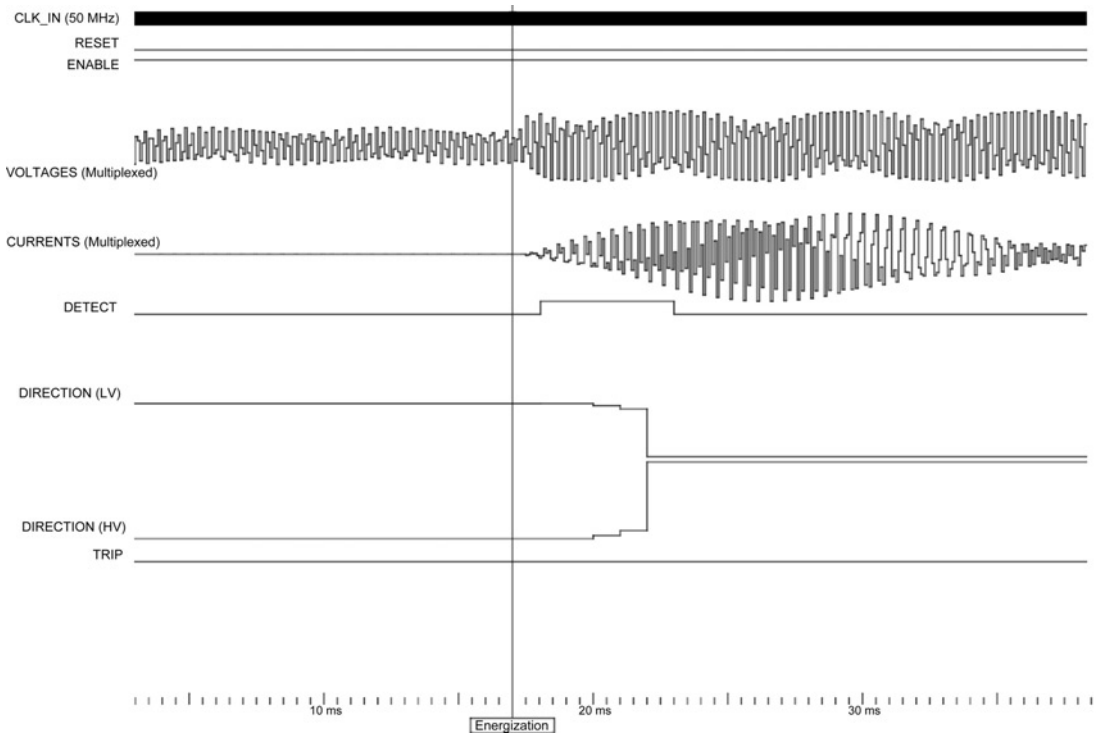

Figure 6 *Simulation result for transformer energisation*

62% of the slices are utilised for this application. Fig. 7*a* shows the logic blocks used and routing between them after the place and route process is completed. The prototype developed for testing the proposed protection scheme is shown in Fig. 7*b*.

The entire power system modelling is done using EMTP/ATP and the waveforms are available as data files in the computer. Since the aim of the prototype development is only to test the performance of the proposed logic in real-time, the analog signal processing which consists of anti-aliasing, sampling, multiplexing and conversion to digital form, was done in MATLAB. The standard parallel port was used for outputting the digital signals from computer to the FPGA kit. The port was accessed using realtime windows target (RTWT) toolbox of MATLAB. The

Table 1 Device utilisation details

Logic utilisation	Used	Available	Utilisation(%)
slice flip flops	927	9312	9
four input LUTs	4486	9312	48
occupied slices	2898	4656	62
bonded IOBs	15	232	6
MULT 18 × 18 s	20	20	100
GCLKs	8	24	33

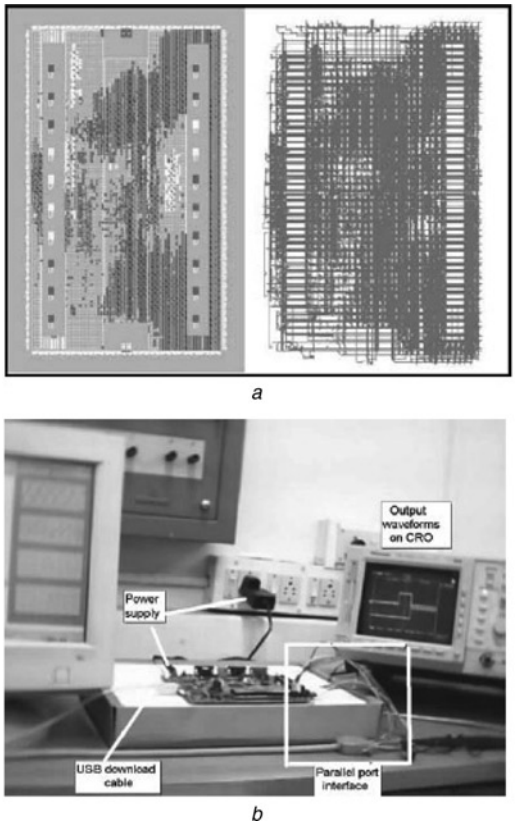

Figure 7 *Placed and routed views of the FPGA and test set-up*

a Placed and routed views of the FPGA
b Test set-up

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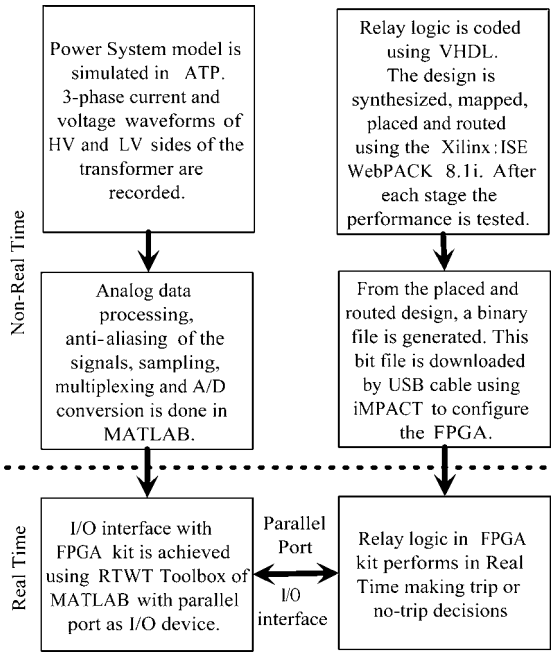

Figure 8 *Flow chart showing stages of work*

RTWT allows the C code generated by real-time workshop to be run on a PC in real-time. The real-time kernel runs at Ring 0 (highest priority) in the Windows environment. The various stages of the work can be divided into non-real-time and real-time operations and are shown in Fig. 8.

Various types of internal and external faults as well as different energisation situations and disturbances were simulated and the test waveforms for the digital relay were obtained. A total of 880 test cases were generated to do a systematic and elaborate evaluation of the proposed relaying scheme. The type of faults considered are single line to ground, double line to ground, line to line and three-phase fault. The transformer energisation types are (i) by closing S1, (ii) by closing S2 and (iii) by simultaneous closing of

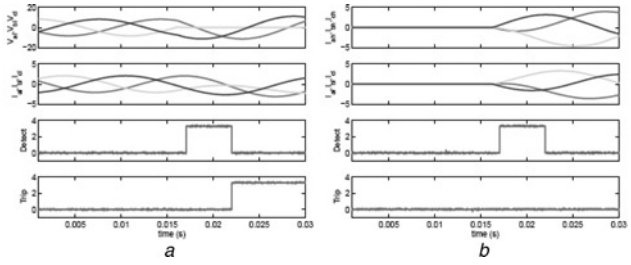

Figure 9 *Output for phase b to ground fault on LV winding and for transformer energisation*

a Output for phase b to ground fault on LV winding
b Output for transformer energisation

S1 and S2 (refer Fig. 1). The performance by the proposed relaying scheme for various types of disturbances is summarised in Table 2. There were no mal-operations in performance of the scheme, that is, there was no trip signal issued for an external fault/disturbance and there was no failure in issuing a trip signal for a valid internal fault.

The output from the prototype for phase *b* to ground fault on LV side is shown in Fig. 9*a*. The 3ϕ voltages and currents for LV windings along with the Detect and Trip signals are presented for a fault which occurs at 16 ms. The disturbance is detected at 17 ms and Detect signal goes high. After 5 ms, the disturbance is discriminated as an internal fault and Trip signal is issued at 22 ms. Fig. 9*b* shows the HV and LV side currents along with Detect and Trip signals for transformer energisation at 16 ms. It can be observed that, although a disturbance is detected at 17 ms, no trip is issued as the directional signals discriminate it as non-fault condition.

6 Conclusions

A novel directional relay for power transformer protection is proposed. The scheme uses WT for extracting information from voltage and current signals

Table 2 Summary of test results

	Type of Disturbance	No. of cases	Output
internal faults	transformer terminal faults	332	TRIP
	transformer winding faults	188	TRIP
	internal faults with CT saturation	10	TRIP
non-fault disturbances	transformer energisation	60	no TRIP
	dynamic load variations	30	no TRIP
external faults	line faults	240	no TRIP
	external faults with CT saturation	20	no TRIP
total number of test cases: 880			

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to detect disturbances and discriminate between internal faults and other disturbances. A high degree of computational efficiency is achieved because of the use of single-level wavelet decomposition. The logic is easily comprehensible, deterministic and is implemented using SPARTAN3E FPGA kit. FPGAs provide an affordable, customised option for testing the performance of new protection techniques. The ability to manipulate the logic at the gate level increases the efficiency of custom processor in implementing the desired function. By simultaneously/parallely performing all the sub-functions, the FPGA can even outperform a DSP, whose performance is limited by the serial instruction stream and limited number of multipliers. The prototype was developed to evaluate the performance of the proposed logic in real-time. Data from various EMTP/ATP simulated fault cases and non-fault disturbances were used to verify that the relay operation is fast, reliable and secure. Since the relay is insensitive to the phase shift caused between HV and LV terminals because of the different types of transformer connections, there is no need to change the CT/PT connections depending on the transformer configuration. The performance of the relay is not affected by the variation in load settings and power flows, thus making it inherently adaptive. It can work reliably in the presence of CT saturation and fault resistances.

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