Embedding Synchronized Measurement Technology for Smart Grid Development

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***Abstract*—Present distribution networks have not been designed to accept extensive Distributed Generation (DG). The present framework may change in the near future impelled by a worldwide increase in DG penetration in distribution grids. The mutual dependency of energy distribution and communications on the same grid requires new means for effectively monitoring and controlling both systems in parallel. Relaying and control IEDs can also serve as measurement units for power quality. Synchronized Measurement Technology (SMT) has the potential of becoming the backbone of this paradigm. By using wide-area information systems, the data can be made available to all involved partners. This paper provides different outlooks about the possibilities of Embedded Systems to integrate the protection, control and monitoring functions in Distribution Automation Systems. To justify the choice of synchronization technology, we have scheduled a complete sequence of synchronism tests and measurement tests based on standard specifications.**

***Index Terms*—Embedded system, field programmable gate array (FPGA), IEC61850, IEEE 1588 v2, intelligent electronics devices (IED), measurement units (PMU), power quality (PQ), smart grid, synchrophasor.**

I. Introduction

TRADITIONALLY, Sustainable Development has been defined as development that meets the requirements of the present generation without compromising the ability of future generations to meet their own needs. Obviously, Sustainable Development not only affects energy, but also all sectors of activity at local as well as at national levels. In recent years, and hand-in-hand with the Sustainable Development initiative, the concept of a "Smart Grid" for the delivery of energy to consumers [1] has emerged. Although there is no standard global definition, the European Smart Grids Technology Platform defines Smart Grids as: "electricity networks that can intelligently integrate the actions of all users connected to it—generators, consumers and those that do both—in order to efficiently deliver sustainable, economic and secure electricity supplies". The nature of the electricity business and of power consumption has changed considerably over the last two decades. Rather than a recipe for specific implementations, the "smartness" provides a conceptual framework that defines new criteria for the design and implementation of a reliable power delivery grid. The constant growth of the electrical network complexity [2] and the need for larger security and reliability levels of the plant infrastructures lead to the need of more detailed contingency analysis in shorter times.

The ability of the electricity system to deliver electric power without interruption is termed 100% reliability. The ability to deliver a clean signal without variations in the nominal voltage or current characteristics is termed high Power Quality (PQ) [3]. As the electric grid is operated under tight power quality and reliability standards, the voltage and frequency provided have to be within certain specified limits, while simultaneously ensuring stable operation. In this context Smart Grid provides a conceptual framework that defines new criteria for the design and implementation of a reliable power delivery grid [5], [6].

Recent interest in distributed electricity generation has emerged in energy markets for economic as well as environmental reasons, such as the shift towards renewable energy sources. The term Distributed Energy Resources (DER) is a catch-all, including wind, solar, biomass, and storage, where power is generated outside the traditional utility framework [5]. However, the integration of DER into existing networks raises several economic, regulatory and technical questions, some of which are closely related to PQ [2]. Elsewhere numerous system issues have been compiled-issues that may be encountered as DER penetration rises. As stated in [3], DER can no longer be treated as negative load; the complete integration of renewable energy sources will require distribution system operators to develop active network management in order to participate in the provision of system security. In this paper we will show the possibilities of Embedded Systems for integrating the protection, control and monitoring functions of Smart Grids within a synchronized framework [7].

The paper is organized as follows: Section II introduces the present Distribution Automation System; Section III analyzes the possibilities and goals for a functional integration of synchronized measurements; Section IV analyzes the experimental

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system while Sections V and VI report the preliminary studies and experimental results.

II. Distribution Automation System Overview

A Distribution Automation System (DAS) can be defined as an integrated system that enables an electricity utility to monitor, coordinate and operate distribution components, in a real-time remote mode [4], [8]. A DAS continuously controls, monitors and protects the network to avoid unplanned network outages. This covers all high-voltage equipment outside the substation (cables, overhead lines etc.) as well as those inside the substation (circuit breakers, transformers, etc.). DAS decisions are generally supported by a Distribution Management System (DMS)—*ad hoc* software which outputs control strategies based on the system's inputs (measurements) and which are in turn provided by a Supervisory Control and Data Acquisition (SCADA) System.

The key component of the DAS infrastructure is the Intelligent Electronic Device (IED) [9]. This device is designed to be intelligent and to be able to communicate with other entities collectively. In other words, some real-time critical functions can be executed autonomously on a single device while other functions are performed in a distributed form over many IEDs.

The basis of these improvements, as part of the Integrated Energy and Communications System Architecture (IECSA), enables four areas of technology to evolve [5], [12]:

- Technologies which allow real time monitoring and control of power systems.
- Those which increase the control and capacity of power delivery systems. Together these developments will transform the functionality of the power delivery infrastructure, enabling such concepts as the "Smart Grid", incorporating self-healing concepts.
- Technologies which enhance the performance of digital devices enabling tomorrow's digital society to be supported.
- Technology which enables connectivity and enhances end-use, thereby revolutionizing the value of electricity services.

Until now, the utilities have used communications schemes in the substations in order to integrate data from relays and IEDs and to capitalize on protection, control, metering and outages recording. With volatile energy rates and a need to control costs, regional agencies and utilities are interested in technologies for metering distribution use and managing utility information. The IECSA requires the integration of customer interaction, power system monitoring and control, energy trading, and business systems.

At the utility grid level, real-time monitoring systems provide up-to-date information on major substation equipment and some transmission line conditions. However, this is not true for most distribution facilities [12].

IECSA will begin to be used in Power Generation and finally in the Smart Grid in general. This will imply the advantage of reusing the infrastructure of existing telecommunications networks. Real-time Ethernet systems now form the new generation of industrial communication systems.

Standardization enables the integration of the equipment and systems for controlling the electric power process into a complete system solution, necessary to support utilities processes. This ensures the interoperability of equipment and systems by providing compatibility between interfaces, protocols and data models. With IEC61850 data acquisition and description methods standardization, integration efforts are reduced.

At the customer level, the transformation of the electricity meter is still in its infancy. In this case, an important link to the consumer to enable demand response functionality is the deployment of AMR Systems that will measure and quantify the load curtailment at the consumer's premises. AMR infrastructure programs are moving forward at a rapid pace with large numbers of pilot and full-scale deployments currently being implemented across the globe [13]. However, the utility industry as a whole has not yet begun to deploy this strategy on a large scale. In addition, technology suppliers have been reluctant to invest in research and development before the market's scope and size is fully understood.

III. Outlooks and Goals

In the previous section we have emphasized the importance of the so-called Distribution Automation System. Its technological development is key to the intelligent management of the network. The need to research and develop models of Intelligent Electronic Devices (IED) with capabilities perfectly adapted to the new demands of the global intelligent network model is therefore justified [10]. Our research group has carefully studied various architectures that have as their central core a Digital Signal Processing (DSP) system or a Field Programmable Gate Array (FPGA) system. To make a proper technical decision, and in order to define our own model, we have carefully studied various standards that are already in force and others that are under development. The study has been divided into two categories:

(A) Study of standards that affect the selection of the measurement system.
(B) Study of standards that impact interoperability between different systems located at industrial facilities.

In the first category we focus on studying the method of capture, synchronization and basic processing [15]. In the second category we focus on the management, monitoring and intelligent control. Therefore, we have to study aspects that refer to real-time communications, distributed synchronization and advanced information processing [4], [11].

A. Standards Defining the Operation of the Measurement System

For this category, we selected the IEEE C37.118 standard for synchrophasors and phasor measurement units (PMUs). This standard possesses very stringent technical requirements. The error in phase measurements is obligatorily less than 32 μs. In its turn, this requirement affects the choice of synchronization technology for the capture and processing of signals.

Furthermore, we selected the IEC61000-4-30 standard for quality-of-supply measurements in order to analyze the computational requirements of the systems that capture steady state parameters to detect deviations from the stable behavior of the

power grid. In addition, this standard also specifies the procedure for the analysis and classification of transient disturbances.

And finally, the IEEE Std. 1588 which describes Precision Time Protocol has been developed for distributed measurements. We have selected it in order to study experimentally their integration into the IED system model [14], [16].

B. Smart Grid Interoperability Standards

In order to extend the IED model to a greater number of applications for Smart Grid [17], we have analyzed some of the regulations that focus on defining an overall architecture such as the IEEE Std 2030-2011 called "IEEE Guide for Smart Grid Interoperability of Energy Technology and Information Technology Operation with the Electric Power System (EPS), End-Use Applications, and Loads" or the standard under development called "Draft NIST Framework and Roadmap for Smart Grid Interoperability Standards, Release 2.0". The target of these guides is to define a model of reference for the interoperability of the systems that wil have to coexist in Smart Grid.

In the same way, we are studying the IEC61850-90-5 standard that establishes a classification based on the synchronization requirements of critical applications. For the first time this standard includes the possibility of using IEEE Std 1588 for power system applications. Its use is subject to further technological development in order to ensure synchronization levels of the standard. Specifically, this trend is clearly described in standard PC37.238, being developed for the implementation of IEEE 1588 in Electric Power control systems.

In addition, the IEEE 1588 Conformity Alliance is an IEEE Conformity Assessment Program (ICAP) with the mission of promoting the IEEE 1588 "Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems". The Alliance Certification Program has been formed to assess the conformity of IEEE 1588 implementations over a wide range of applications such as telecommunications, Smart Grid, manufacturing, and digital audio and video broadcasting. We are following its evolution closely in order gain knowledge of the rules of conformity and how to apply them.

For our purposes, we are interested in the characteristics of the reference model developed in Section V of IEEE Std 2030-2011 guide. Specifically, we define an architecture based on three aspects: functional considerations of power systems, communications technology and technologies for information management. This last point emphasizes the types of parameters to be measured and how to manage its capture and processing.

C. Specifications for Embedded System Selection and Types of Tests to Justify the Choice

All of the studies we performed allow us to define a technological model and its specifications. In this line, we selected the features that we considered essential and which must be included in the platform of an embedded system. The most important aspect is the ability to develop applications in three broad categories such as generation, transmission and energy consumption. The differentiating features are in the 2030 IEEE Smart Grid interoperability reference model (SGIRM) guide.

It is therefore necessary that the system allows us to select different scales in terms of computing power to suit every application while maintaining the same base technology. This allows us to maintain a high degree of compatibility in terms of synchronization technology, capture processing and transmission management and information flow.

Ultimately, the study of standards and requirements of IEEE Std 2030-2011 has led us to define specifications for more critical applications.

- The synchronization subsystem must ensure the simultaneous synchronization of multiple devices to a very high degree of precision ($\leq 1\ \mu$s). The degree of difficulty increases because in many cases devices have to be at a considerable distance, even more than one Km.
- The capture stage of each type of event has to ensure an almost instantaneous response capability, especially when very fast transients occur. This defines a minimum resolution of 16 bits and a minimum sampling of 256 samples per cycle.
- The processing stage should allow us to process and detect multiple disturbances both steady state (Vrms, Irms) and transients. It must have enough computational capability for processing tasks to ensure the trip times of protection systems.
- And finally it is essential to ensure a level of real-time transfer between devices. This requires the use of a technology that allows us to establish secure communication with a high degree of determinism.

These specifications have allowed us to select a platform to carry out all kinds of tests related to the synchronization between devices and related response times during the stages of capture, processing and communications.

Table I illustrates a classification with all scheduled tests. The columns represent the type of tests based on specialized instruments and the rows the standards under test.

In the first step, tests are designed to check if our source of synchronization guarantees the stability of each of the slaves on the basis of standard specifications. This corresponds to column (A) of Table I and determines:

- Row (1): The stability of the clocks in each of the slave based on master PPS, at short, medium and long term.
- Row (2): The alignment error between PPS slave clock and sampling clock.
- Row (3): The error associated with the alignment of the windows of 10 cycles with respect to the PPS of the slave.
- Row (4): The error associated with the alignment of the PPS with respect to a transient less than one cycle.

The first test (A,1) enables us to determine the quality and stability of synchronization of the slaves under test, the second test (A,2) enables us to determine the effect on the Time Stamp quality of samples and third test enables us to determine the effect concerning the synchronism of the analysis window. These first tests are very important because these errors affect the quality of the measurements of all kinds of electric parameters, such as those programmed in columns (B) and (C), and they correspond to more complex tests for estimating the response times of the stages of capture, and the processing and classification of power grid disturbances [18].

TABLE I
TYPES OF TESTS FOR EMBEDDED SYSTEMS

Types of standards for testing	Types of tests based on specialized instruments.					
	(A) GrandMaster XLI 1588		**(B) C.I. Tree-phase Power**		**(C) C.I. 3091LD Load.**	
	Internal Slave: NI-RIO	External Slave: ARM and PCI.	Transients with external trigger	Transients with internal trigger	Variation of load with external trigger	Variation of load with internal trigger
(1) To Sync with IEEE 1588 V2	Slave PPS	Slave PPS	CLK OUT	CLK INT	CLK OUT	CLK INT
	Measurement of stability with respect to Master PPS		Measurement of stability of sync pulse		Measurement of stability of sync pulse.	
(2) For Phasors Measurement (IEEE C37.118)	Sampling clock		Voltage measurement		Current measurement	
	Measurement of shift and stability with resmpect to Slave PPS		Measurement and Time Stamp of Frequency and Phasors.		Measurement and Time Stamp, of Frequency and Phasors	
(3) For Power Quality (IEC61000-4-30)	Start Windows with 256 SPCycle.		Voltage measurement		Current measurement	
	Measurement of shift and stability with respect to Slave.		Measurement and Time Stamp, of voltage sags, surges, etc.		Measurement and Time Stamp of, Current Harmonics.	
(4) For very fast transient (Standards for protections)	Start Windows with 1024 SPCycle		Voltage measurement		Current measurement	
	Measurement of shift and stability with respect to Slave.		Detection and Time Stamp of Transient in less than half cycle.		Detection and Time Stamp of Gradients and short-circuit current.	

The second phase of testing is divided into two categories: external and internal sync. With the external sync, the system under test triggers a sync signal to enable the generator to reproduce the transient. This approach allows us to assess the measurement system response with great accuracy. The internal sync reproduced a real situation. The measurement system under test does not know the time when the transition occurs. With this method we evaluate the actual response of our system.

To perform all these tests our research group has defined a special type of laboratory with highly specialized equipment to calibrate and certify the results. We have three main instruments that will allow us to define each trial: a Grand Master XLI acting as Master of PTP synchronization, a three-phase fully programmable 9 KVA power supply that can generate all kinds of disturbances at low voltage and a programmable 3091LD load to emulate different types of behaviors of a three-phase load. The three instruments include a measurement system that enables any type of test to be certified.

In particular, the test allowed us to calculate synchronization errors with two slaves simultaneously. In this part of the research we do not include results of the capture and processing of the phasors. We have only estimated the influence of the synchronization error in the phasor measurements.

In columns (A) and (B) and row (4), we have scheduled a series of tests to estimate the sensitivity of the measurement system. These are the most critical tests. The goal is to detect transient changes very quickly.

Section IV explains the method for evaluating the quality of the PTP slaves. The tests included in V are scheduled in the first phase (A). As the standard for synchrophasors requires a very high level of synchronism, this has allowed us to define a maximum threshold for the embedded system.

TABLE II
TEST RESULTS FOR PTP SLAVE

Standard under Test.	Alternatives as PTP slaves			
	External slave		Integrated slave	
	LM3S8962	PCI-1588	SbRIO	CRIO 9074
IEEE 1588 v1. Router and Switch of 100Mbit	12us	150ns	Not feasible	Not feasible
IEEE 1588 v2. Router and Switch of 100Mbit	In progress	100ns	75us	75us
IEEE 1588 v2. Industrial Switch of 1Gbyte and integrated PTP v2.	Planned	Planned	Planned	Planned

Table II includes the tests we have performed to date. The tests on the third row are in progress and correspond to the connection of a specialized industrial Switch (Moxa PT-7710) that manages the IEEE 1588 V2. The results should be even more successful.

D. Procedure for Synchronization of the Sampling

As explained in the previous section, our main goal is to use a method of data synchronization and correlation between separate systems with errors less than those specified by the standard for synchrophasors [21].

Timing and synchronization technologies allow the correlation or coordination of events in time and maximize the value the system provides. The tests in Table II are designed to ensure the correct selection of the technology for synchronization.

To estimate the quality of synchrophasors, the most important tests are indicated in Table I, specifically in (A,2). This test cor-

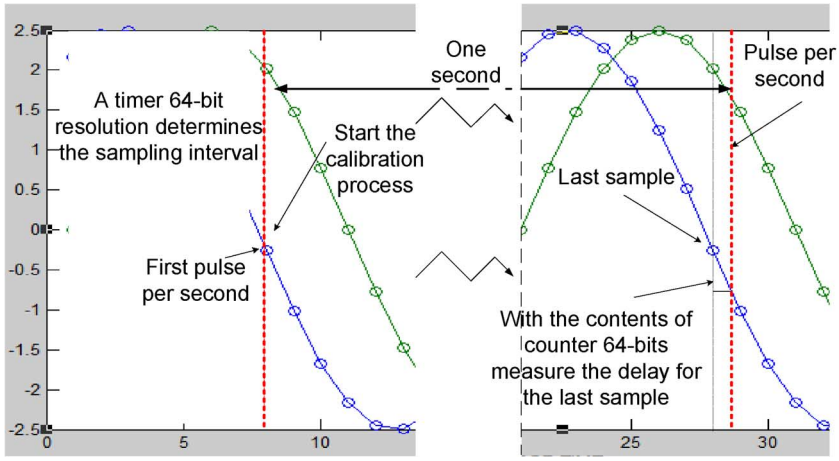

Fig. 1. Synchronism method for capture process.

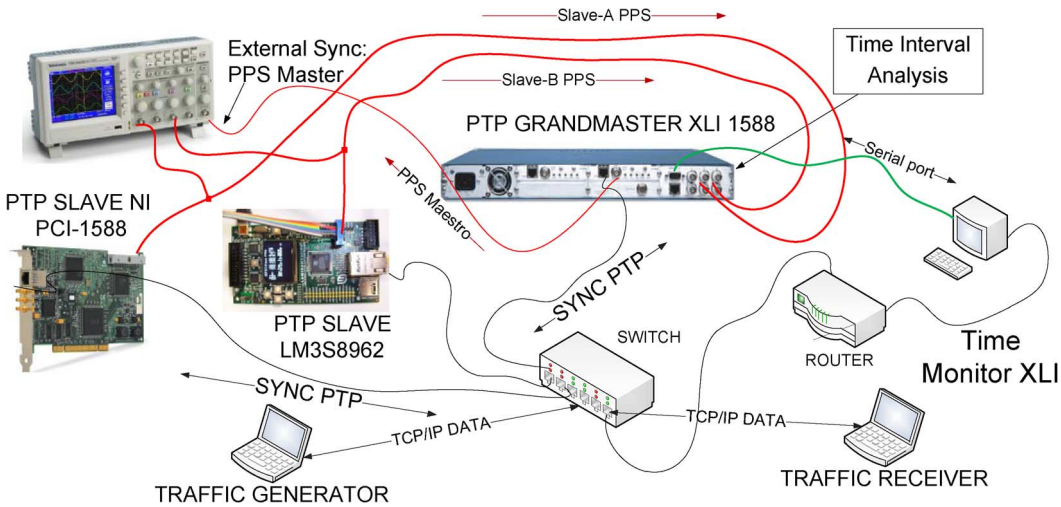

Fig. 2. Slave measurement test set-up.

responds with the estimated error between the PTP Slave synchronization and sampling clock.

The NI-RIO works as a PTP-Slave and provides a PPS signal with high stability. This signal starts the capture process and enables us to re-synchronize sampling (see Fig. 1). The NI-RIO CLK module provides a real-time clock. This clock can be used to measure the passage of time, as well as to add timestamp messages to event logs. A high-resolution counter determines the sampling intervals. The 64-bit counter (FPGA I/O functions) is implemented in the FPGA. We use a Single-Cycle Timed Loop (SCTL) which guarantees that all operations will be executed in one clock pulse at 40 MHz internal time-base. It is worth emphasizing, therefore, that with this system we appraise in nanoseconds the deviation between the pulse per second and the last sample for the second (see Fig. 1). The process is repeated for several seconds to adjust the counter and reduce the maximum drift.

Therefore, we establish a process of resynchronization between the PPS and the oscillator responsible for maintaining the sampling frequency. This process is repeated every time the system reboots. Once the capture process is started, it continuously measures the drift and stores it in a register along with the drift. This information should be stored in the frame with the captured parameters. When the deviation exceeds a threshold, the system can adjust the beginning of the capture process in the following PPS in real time. Short-term stability depends on the local oscillator.

IV. Procedures for Synchronism Test

The first procedure allows us to evaluate the quality of the slaves and the master individually. This test is essential in order to compare the precision and stability of the clocks of all architectures. The method consists in detecting the deviation of the PPS with respect to a time of a higher quality. In Fig. 2 we have highlighted in red the PPS output of the PTP-Master and of the two PTP-Slaves under test. The PTP-Master synchronizes the oscilloscope to display the correct moment of onset of PPS for each slave. This signal is also connected to the inputs for analyzing long-term stability. We use specialized software called Time Monitor.

A second procedure allows us to determine the stability of a PTP integrated into an embedded system. NI CompactRIO combines an embedded floating point processor (PowerPC) with real-time operating system VxWorks, a high-performance

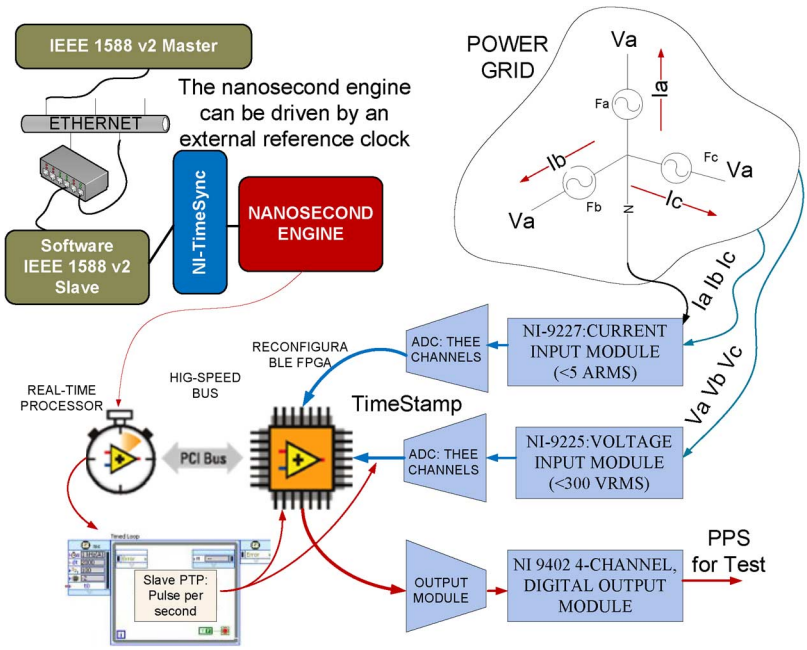

Fig. 3. Basic measurement time interval for processing and TimeStamp with IEEE 1588 v2.

FPGA and hot-swappable I/O modules (see Fig. 3). This architecture provides a high level of determinism and is suitable for aligning the samples during the capture process with the PPS.

A. Experimental System for External PTP-Slave

In the Appendix we have included the technical details of the two slaves under test (PCI-1588 and LM3S8962).

The method is to check if traffic data for synchronization and communication traffic can be shared in the same Ethernet network. The standard for synchrophasors [25] clearly specifies the volume data exchange between PMU and the data concentrator. The transmitted frame has the size specified by the standard and the transmission rate equals the speed of system response. Fig. 2 shows the simultaneous connection of PTP-Slaves and PC to simulate traffic. A similar method is used in [16].We use an ordinary switch Fast Ethernet 100Base-Tx.

The XLi's Time Interval/Event Time (TIET) feature can be used to measure PTP synchronization across timing networks and the Time Monitor analyzer application provides the capability to measure and analyze Packet and Synchronization networks to ensure timing and frequency stability (see Fig. 2).

Synchronization performance depends on several factors, including, but not limited to, Slave oscillator quality and PLL control, networking equipment, network traffic levels, network topology and the transient deterioration of synchronization accuracy during a recovery from a master failure [7].

The measuring of slave PPS time error from the hardware-generated PPS signals provides direct observation of master-slave end-to-end synchronization. Errors can be viewed using a frequency counter, oscilloscope or a grandmaster equipped with an integrated time interval measurement input "XLI IEEE 1588".

B. Experimental System for Internal PTP-Slave

In the Appendix we have included the architecture details of the slave under test (NI-RIO).

For distributed synchronization (see Fig. 3) the NI-TimeSync provides a clock reference with IEEE 1588 v2. Accessing these resources, it can run an IEEE1588 synchronism-based Time loop. This Time loop is executed in a real-time processor with the highest priority. At the beginning of each second, the time loop sends a pulse to the FPGA (PPS internally). To measure the quality of the sync use one digital output NI-9402.

Our experimental system uses one NI cRIO-9074 chassis and one NI Single-Board-RIO working as an IEEE1588 slave for synchronism Test. For this type of essays we use one NI PCI-1588 working as Master. This card incorporates one Real Time System Integration (RTSI).

All modules, connected via an RTSI cable, receive the same RTSI signals. This feature makes the RTSI lines useful in situations where you want, for example, to start an acquisition on several devices at the same time, because all modules will receive the same signal. To use RTSI signals to communicate with other NI PCI modules, RTSI cabling to connect the signals between the boards is needed.

In this project we have chosen to use them as output PPS for comparison with the PPS generator NI cRIO-9074.

V. Experimental Test Result

This type of test corresponds with Table I (A,1) and with tests scheduled in the Table II. Three different technologies are evaluated. The technical specifications are described in the Appendix.

A. Experimental Test Results for External PTP-Slave

The TDS2024B oscilloscope visualizes the delay of two slaves with respect to PPS Master XLI. (See Fig. 4).

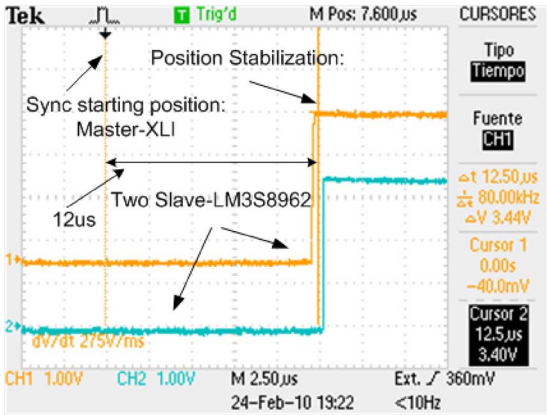

Fig. 4. Delay slave-master after 10 minutes.

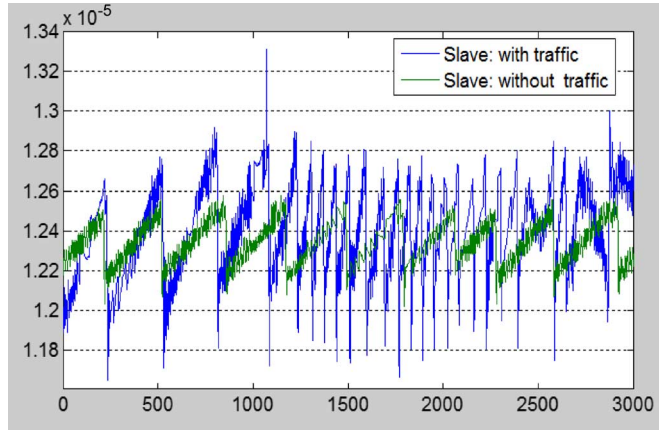

Fig. 5. PTP slave PPS M3S8962 PPS error (phase delay) under traffic and non-traffic conditions.

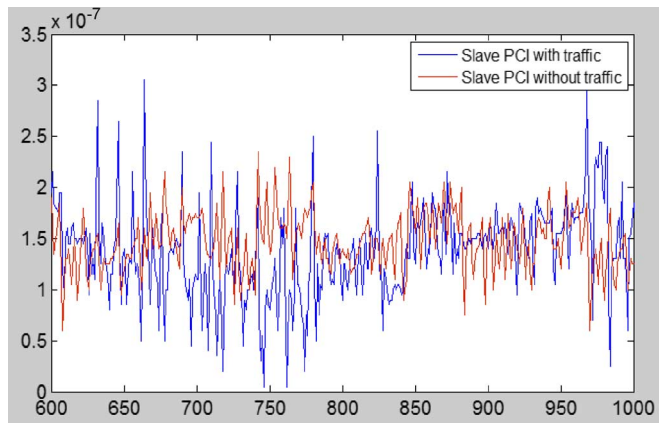

Fig. 6. PTP slave PCI-1588 error (phase delay) under traffic and non-traffic conditions.

Traffic volume is moderate because it simulates the exchange of frames generated by the PMU with the data concentrator equipment. There is extensive literature which studies the effect on the PTP synchronization with conventional network traffic.

Therefore, we performed several tests with a moderate data transfer:

Slave1.Test A: The first prototype analysis is shown in Fig. 2. The expected performance of both PTP system (XLI-IEEE1588 MASTER and LM3S8962-PTPd SLAVE) was tested with Symmetricom and Texas Instruments with the following conditions: synchronization was performed for 10 minutes; test durations were 2 hours; sync intervals of 2 second were used for all tests, and all Ethernet connections were of 100 Mbps; for the switch test, non-1588 Ethernet traffic was present on the switch. The information was transmitted by a second UDP Unicast socket for the same RJ45 channel used for the PTP synchronism. A central instrument receives the frames.

We use two methods:

— *Method-1*: both RJ-45 PMU lines were connected to an ordinary switch Fast Ethernet 100Base-Tx (CenTreCom FS709FC). A moderated amount of Ethernet traffic was generated between both PMU devices. Every PMU generates traffic at 10 data frames ($10 * 100$ bytes) per second sending rates

— *Methods-2*: both RJ-45 PMU lines connected to an ordinary switch Fast Ethernet 100Base-Tx (CenTreCom FS709FC). Every PMU generates traffic at 100 data frames ($100 * 100$ bytes) per second sending rates.

Results: The slave synchronization error has been measured with relation to its PPS output (see Fig. 5). Maximum peak value is about 1.26×10^{-5}. Additional traffic generates "*sync*" and "*Delay_rep*" packets delays, so that the slave clock oscillator increasingly accumulates stability errors. Maximum peak value is about 1.33×10^{-5}.

Slave2.Test B: Second prototype analysis. The expected performance of both PTP system (XLI-MASTER and PCI-1588 SLAVE) was tested with Symmetricom and National Instrument with the same conditions and methods: synchronization was performed for 10 minutes before testing began; test durations were 2 hours; sync interval of 2 second were used for all tests, and all Ethernet connections were 100 Mbps.

TABLE III
DELAY PHASE

Test	1PPS error:Delay Phase		Estimated Phase deviation of the synchrophasor	
	Mean	S. Dev.	Mean	S.Dev.
TA.M-1	1.23E-5	1.1E-7	0.222º	1.9mº
TA.M-2	1.24E-5	2.2E-7	0.223º	4.0mº
TB.M-1	1.45E-7	2.7E-8	0.003º	0.5mº
TB.M-2	1.48E-7	3.9E-8	0.003º	0.7mº

Results: The slave synchronization error has been measured with relation to its PPS output under the same conditions (see Fig. 6). Maximum peak value is about 2.35x10-7. Additional traffic generates "*sync*" and "*Delay_rep*" packets delays, so that the slave clock oscillator increasingly accumulates stability errors. Maximum peak value is about 3.1×10^{-7}.

The differences between the quantities measured by the master and by the slave have been evaluated and statistically analyzed (Table III).

With the experimental PTP-based system, the events can be well-synchronized within 12 μs. Requirements IEEE 37.118-2005 standard [21] limit time error to be lower than 31 μs. Nevertheless, with a slave PCI-1588 for test recovers its stability around 150 ns.

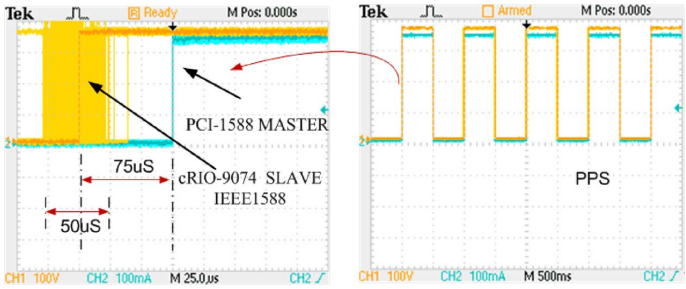

Fig. 7. Level of synchronization IEEE1588 V2.

For a prototype reaching nanoseconds error and for future test users XLI IEEE-1588 Grandmaster Clock supports PTP version 2, Slave LM3S8962 with PTPv2.

The use of ordinary switches or routers should be avoided in critical timing applications where sub-microseconds or a greater accuracy are needed. In these cases Transparent Clocks (TCs) and Boundary Clocks (BCs) should be utilized. In [22] advantages of using devices compliant with IEEE 1588-2008 standard are investigated.

B. Experimental Test Result for Internal PTP-Slave

The results correspond to the synchronization of an NI cRIO-9074 chassis working as IEEE1588 Slaves.

The external sync signal is connected to the PPS of the PTP-Master. In the oscilloscope image (Fig. 7) we can observe the level of synchronization achieved between the master and one slave for 30 minutes. The average error is 75 us with a variance about of 50 us.

VI. Conclusions

Table I has been defined in order to analyze if the embedded system meets the specifications of several Smart Grid standards. The standard for synchrophasors represents the highest level of demand for synchronization.

The tests in this work represent a first phase corresponding to the analysis of the synchronous system, as we can see in the first column of Table II. We verified that the ARM and PCI slave comply with the requirements of synchronism and stability, remembering that the maximum allowable error is 32 μs. It is comparable to the method used in [16], [25].

Moreover, the PCI-1588 card oscillator's quality is sufficient for it to work as a Master PTP in an industrial environment. We must emphasize that the tests have been performed with the standard IEEE-1588 v2 2008. This standard has been imposed definitively and is incompatible with the IEEE 1588 v1 2003 version. This has forced us to redefine our tests to be applied only to the new standard. Table II illustrates the error of synchronization in relation to other devices. The average error is 150 ns. This quality justifies its use as a PTP master. Table II specifies tests that are in progress.

Tests with the slave integrated into the architecture of the NI-CompactRIO reach a level below the synchronization required by the standard. The result is 75 μs. We hope that through the use of an industrial switch (e.g. Moxa PT-7710) the required level is achieved. This IEEE-1588 v2 switch is to eliminate the latency associated with the conventional router and switch.

However, external synchronization is the best solution (this is implemented in our research with ARM technology). The processor is dedicated to the capture, processing and communication tasks and does not have to run a critical timing loop. Tests with the slave ARM and IEEE 1588 v2 are in progress.

Finally, it is quite notable the integration process of this type of synchronization, in industrial protocols as EtherCAT [24].

Appendix

Synchronization precision and the distance between the system nodes are the two parameters we have to take into account when designing a timing and synchronization scheme. System designers must take into account the limitations created by these variables because as transmission distance increases it is more difficult to share signals between systems in order to keep them synchronized.

To achieve a high degree of synchronization precision, we must have a highly accurate, high-frequency. This accuracy, however, can degrade as the distance between the chassis, or nodes, increases. The IEEE 1588 standard achieves the highest levels of precision timing systems over one km. Only GPS synchronization is better. Distance does not affect the synchronization quality because a GPS must be installed in each measuring point.

A. Technical Specifications of PCI1588-Master

This device is able to work as either a PTP slave or master and has been tested to determine its stability with respect to XLI GrandMaster. In the future we will be able to use it for field measurements outside the laboratory. The PCI card can be inserted into an industrial computer.

This latter is equipped with a standard RJ-45 connection for Ethernet communication (up to 100 Mbps), with PFI terminals and with a 10 MHz TCXO. TCXO is characterized by an initial accuracy of ± 1.5 PPM, temperature stability (0° to 55°C) of ± 2 PPM and an aging per year of ± 1 PPM.

This Master oversees and manages the synchronism of a set of PTP slaves connected to a standard Ethernet network. The PTP Master sends multicast synchronism "sync and Delay_req" packets to every slave unit in order to synchronize their local clocks with the master unit clock.

B. Technical Specifications of ARM-Slave

The slave is developed using a Stellaris LM3S8962 Evaluation Board Layout. The LM3S8962 microcontroller is based on the ARM Cortex-M3 controller core operating at 50 MHz and also features hardware-assisted support for synchronized industrial networks utilizing the IEEE 1588 Precision Time Protocol (PTP) [20]. High-precision time stamps can be achieved with the support of specialized hardware interfaces in the physical layer of the network.

The software integrating the Precision Time Protocol daemon (PTPd) is a complete implementation of the IEEE 1588 specification for a standard non-boundary clock.

The above software was developed by two engineering students at Case Western Reserve University over a period of approximately six months as part of an undergraduate senior project [19].

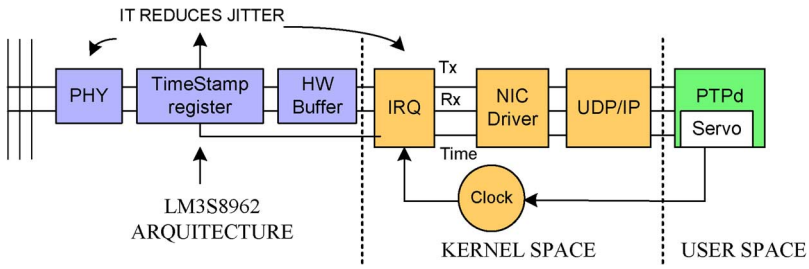

Fig. 8. LM3S8962 (arquitecture for IEEE1588).

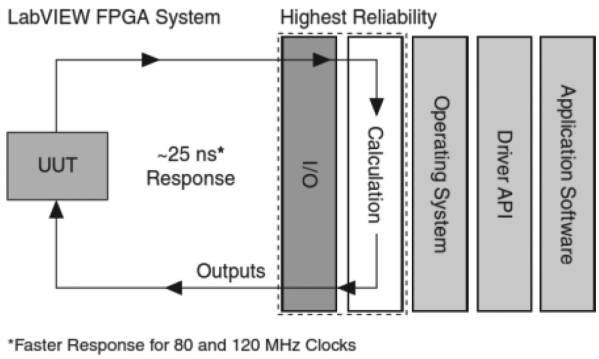

Fig. 9. FPGA software and hardware layers.

Fig. 8 illustrates the message send and receive paths in an LM3S8962 microcontroller system running the Precision Time Protocol daemon PTPd. For applications requiring very high-precision synchronization packets, the Ethernet Controller provides a means of generating precision timestamps in support of the IEEE Precision Time Protocol IEEE-1588 [20]. This feature is enabled by setting the TSEN bit in the Ethernet MAC Timer Support (MATCS) register. The General-Purpose Timer must be dedicated to the Ethernet Controller for storing the received time, and it stores the transmission time.

C. Technical Specifications of NI RIO-Slave

The embedded system selected is an NI CompactRIO running LabVIEW Real-Time, with the reconfigurable FPGA chassis as the center of the embedded system architecture. The FPGA is directly connected to the I/O modules for high-performance access to each module's I/O circuitry and for unlimited flexibility in timing, triggering, and synchronization. Because each module is connected directly to the FPGA rather than through a BUS, almost no control latency for system response when compared to other industrial controllers is experienced.

Additionally, a software-based system poses added vulnerability because a crash that interferes with the response of the system can occur at multiple levels. When executing calculations in hardware, as with FPGA, software from the required response to the UUT can be removed. In the configuration shown in Fig. 9, the LabVIEW FPGA system can respond to digital signals within a single clock cycle. With a default clock rate of 40 MHz, the LabVIEW FPGA system can respond to a digital signal within 25 ns. In some cases, we can compile LabVIEW FPGA code at higher rates.

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