LimeMicro LMS8001 PLL-Sim Handbook

Lime Microsystems

July 1, 2016

Contents

Abstract

This document presents the quick-guide to LMS8001 PLL-Sim software tool. The LMS8001 PLL-Sim's basic purpose is to ease the PLL configuration to the end-user of LMS8001 IC and to suitably illustrate the influence of many programmable parameters on the LMS8001 PLL performance. The most important functions of the LMS8001 PLL-Sim are described in this document.

Chapter 1

Introduction

Lime-Micro LMS8001 PLL-Sim software is intended to provide the user deeper insight into the operation of PLL frequency synthesizer inside the LMS8001 frequency conversion IC. There are many ways to confugure LMS8001 PLL Core. In order to somewhat facilitate getting optimal configuration of PLL core for targeted input parameters such as VCO (or LO) frequency, loop crossover frequency, phase margin etc, many functions are implemented to automate the whole optimization process.

One can use Lime-Micro LMS8001 PLL-Sim to configure all eight PLL profiles available in LMS8001 IC and save INI (*.ini) file for *lms8suite* GUI that can be used to configure the LMS8001 IC on evaluation board designed by Lime Microsystems. Also, INI files generated by *lms8suite* GUI can be opened using LMS8001 PLL-Sim to check PLL-LODIST performance for settings provided in the PLL profiles of INI file.

Most important parts of LMS8001 PLL-Sim tool are described in this document as well as basic steps in common usage scenarios.

- Basic info about Lime-Micro LMS8001 PLL-Sim software can be found in chapter 2
- Very brief and quick quide to LMS8001 PLL-Sim is given in chapter 3.
- LMS8001 PLL-Sim main window is described in more detail in chapter 4.
- As stated above, LMS8001 PLL-Sim offers the user also the possibilty to configure complete PLL-LODIST subsystem of LMS8001 chip and store that configuration in INI file for *lms8suite* GUI tool which can further be used to program chip samples on Lime-Micro LMS8001 evaluation boards (LMS8001-EVB). Also, user has the possibility to open INI files and analyze settings related to PLL-LODIST subsystems stored in that file. This and more can be found in 5
- In chapter 6 are given block diagrams of PLL Core and LO distribution network implemented in LMS8001 IC as a remainder for the user to better understand different functions implemented in LMS8001 PLL-Sim.

Chapter 2

Basic Info

Lime-Microsystems' LMS8001 PLL-Sim software is free, open-source tool completely developed in Python (`http://ww.python.org`) programming language.

The 32b and 64b installers for Windows operating system are available and generated using pynsist tool (`https://pypi.python.org/pypi/pynsist`).

Packages for different linux distributions are still not available. On linux, user can start the LMS8001 PLL-Sim using the source code. Python source modules should be extracted in the desired location, and user should type in the terminal: **% python LMS8001_PLLSim.py**, to start the software.

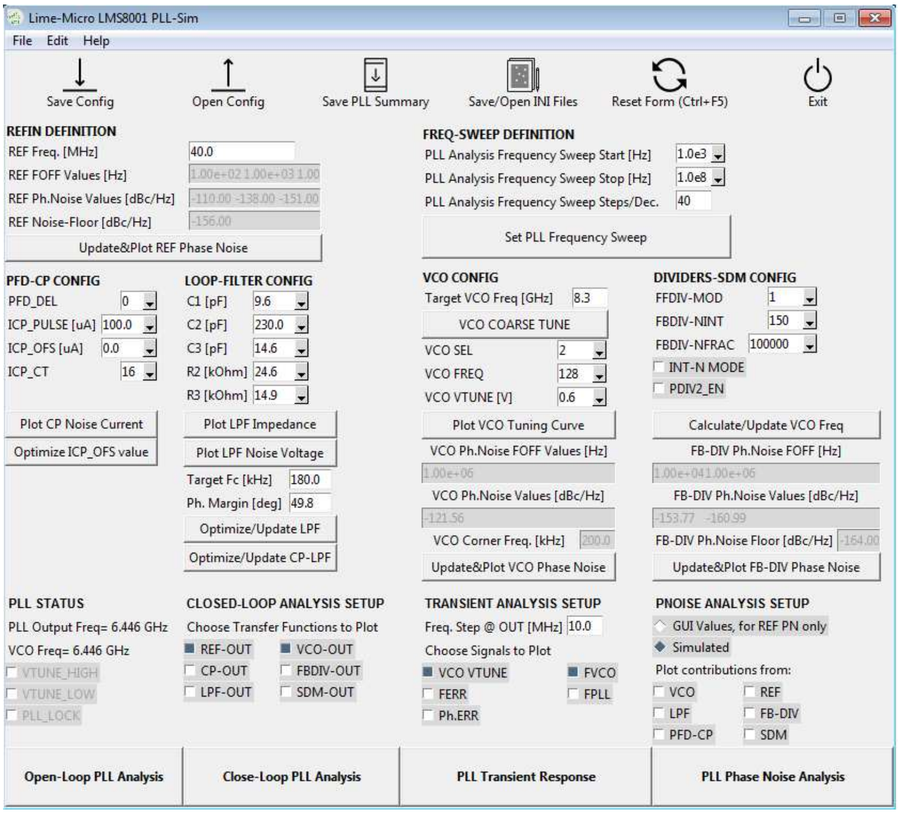
In the cases when user wants to run LMS8001 PLL-Sim's source code, the list of all required Python modules can be very handy and it's given bellow:

os
pyparsing
pylab
numpy
scipy
pandas
pytz
matplotlib
cycler
six
dateutil
Tkinter
ttk
tkFileDialog
tkMessageBox
PIL
webbrowser
tkFont
copy

Chapter 3

Quick Usage Guide

Lime-Micro LMS8001 PLL-Sim's main purpose is to provide to the user of LMS8001 IC a simple tool to model, analyze the performance and optimize the configuration of chip's internal frequency synthesizer. On a startup, LMS8001 PLL-Sim's main window appears as shown in fig.3.1. Main window with all the implemented important functionalities inside it is described in chapter 4.



REFIN DEFINITION
REF Freq. [MHz] 40.0
REF FOFF Values [Hz] 1.00e+02 1.00e+03 1.00
REF Ph.Noise Values [dBc/Hz] -110.00 -138.00 -151.00
REF Noise-Floor [dBc/Hz] -156.00

FREQ-SWEEP DEFINITION
PLL Analysis Frequency Sweep Start [Hz] 1.0e3
PLL Analysis Frequency Sweep Stop [Hz] 1.0e8
PLL Analysis Frequency Sweep Steps/Dec. 40

PFD-CP CONFIG
PFD_DEL 0
ICP_PULSE [uA] 100.0
ICP_OFS [uA] 0.0
ICP_CT 16

LOOP-FILTER CONFIG
C1 [pF] 9.6
C2 [pF] 230.0
C3 [pF] 14.6
R2 [kOhm] 24.6
R3 [kOhm] 14.9
Target Fc [kHz] 180.0
Ph. Margin [deg] 49.8

VCO CONFIG
Target VCO Freq [GHz] 8.3
VCO SEL 2
VCO FREQ 128
VCO VTUNE [V] 0.6
VCO Ph.Noise FOFF Values [Hz] 1.00e+06
VCO Ph.Noise Values [dBc/Hz] -121.56
VCO Corner Freq. [kHz] 200.0

DIVIDERS-SDM CONFIG
FFDIV-MOD 1
FBDIV-NINT 150
FBDIV-NFRAC 100000
☐ INT-N MODE
☐ PDIV2_EN
FB-DIV Ph.Noise FOFF [Hz] 1.00e+041.00e+06
FB-DIV Ph.Noise Values [dBc/Hz] -153.77 -160.99
FB-DIV Ph.Noise Floor [dBc/Hz] -164.00

PLL STATUS
PLL Output Freq= 6.446 GHz
VCO Freq= 6.446 GHz
☐ VTUNE_HIGH
☐ VTUNE_LOW
☐ PLL_LOCK

CLOSED-LOOP ANALYSIS SETUP
Choose Transfer Functions to Plot
■ REF-OUT ■ VCO-OUT
☐ CP-OUT ☐ FBDIV-OUT
☐ LPF-OUT ☐ SDM-OUT

TRANSIENT ANALYSIS SETUP
Freq. Step @ OUT [MHz] 10.0
Choose Signals to Plot
■ VCO VTUNE ■ FVCO
☐ FERR ☐ FPLL
☐ Ph.ERR

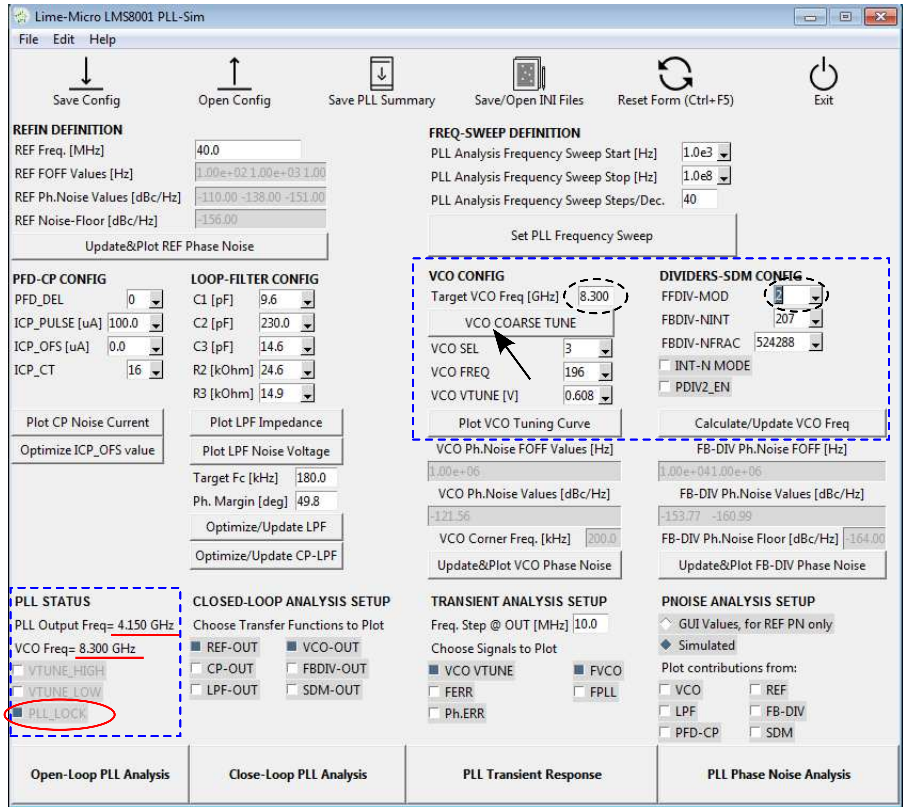
PNOISE ANALYSIS SETUP
◇ GUI Values, for REF PN only
◆ Simulated
Plot contributions from:
☐ VCO ☐ REF
☐ LPF ☐ FB-DIV
☐ PFD-CP ☐ SDM

Figure 3.1: LMS8001 PLL-Sim's Main Window

In LMS8001 PLL-Sim, all the main constituting blocks of the PLL Core inside LMS8001 IC are modeled on the basis of data gathered from real measurements of LMS8001 samples and circuit simulations, in order to provide to the user possibility to estimate the influence of various PLL settings to the overall performance of LMS8001 frequency synthesizer.

Prior to any kind of analysis, user should first define targeted VCO frequency inside the 'VCO CONFIG' frame and press 'VCO COARSE TUNE' button. The reader is reffered to section 4.5 to find out more about this function.

After pressing 'VCO COARSE TUNE' button, for desired VCO frequency of 8.3 GHz, LMS8001 PLL-Sim's main window looks like in fig.3.2. Division modulus of feedforward divider ('FFDIV-MOD' combobox) was manualy set to 2. As it can be seen, VCO configuration was changed compared to the situation in fig.3.1. This function also calculates and configures feedback-divider integer and fractional division modulus settings inside the dedicated GUI frame of main window, based on the inputs provided by the user (target VCO frequency, reference frequency, INTMOD_EN and PDIV2_EN checkbutton values). State of PLL-Core loop configured in main window of LMS8001 PLL-Sim is briefly summarized in 'PLL STATUS' frame. 'PLL Output Freq' is the frequency at the output of feedforward frequency divider. More about 'PLL STATUS' frame user can find in section 4.7.



REFIN DEFINITION
REF Freq. [MHz] 40.0
REF FOFF Values [Hz] 1.00e+02 1.00e+03 1.00
REF Ph.Noise Values [dBc/Hz] -110.00 -138.00 -151.00
REF Noise-Floor [dBc/Hz] -156.00

FREQ-SWEEP DEFINITION
PLL Analysis Frequency Sweep Start [Hz] 1.0e3
PLL Analysis Frequency Sweep Stop [Hz] 1.0e8
PLL Analysis Frequency Sweep Steps/Dec. 40

PFD-CP CONFIG
PFD_DEL 0
ICP_PULSE [uA] 100.0
ICP_OFS [uA] 0.0
ICP_CT 16

LOOP-FILTER CONFIG
C1 [pF] 9.6
C2 [pF] 230.0
C3 [pF] 14.6
R2 [kOhm] 24.6
R3 [kOhm] 14.9
Target Fc [kHz] 180.0
Ph. Margin [deg] 49.8

VCO CONFIG
Target VCO Freq [GHz] 8.300
VCO SEL 3
VCO FREQ 196
VCO VTUNE [V] 0.608

DIVIDERS-SDM CONFIG
FFDIV-MOD 2
FBDIV-NINT 207
FBDIV-NFRAC 524288
□ INT-N MODE
□ PDIV2_EN

VCO Ph.Noise FOFF Values [Hz] 1.00e+06
VCO Ph.Noise Values [dBc/Hz] -121.56
VCO Corner Freq. [kHz] 200.0

FB-DIV Ph.Noise FOFF [Hz] 1.00e+041.00e+06
FB-DIV Ph.Noise Values [dBc/Hz] -153.77 -160.99
FB-DIV Ph.Noise Floor [dBc/Hz] -164.00

PLL STATUS
PLL Output Freq= 4.150 GHz
VCO Freq= 8.300 GHz
□ VTUNE_HIGH
□ VTUNE_LOW
■ PLL_LOCK

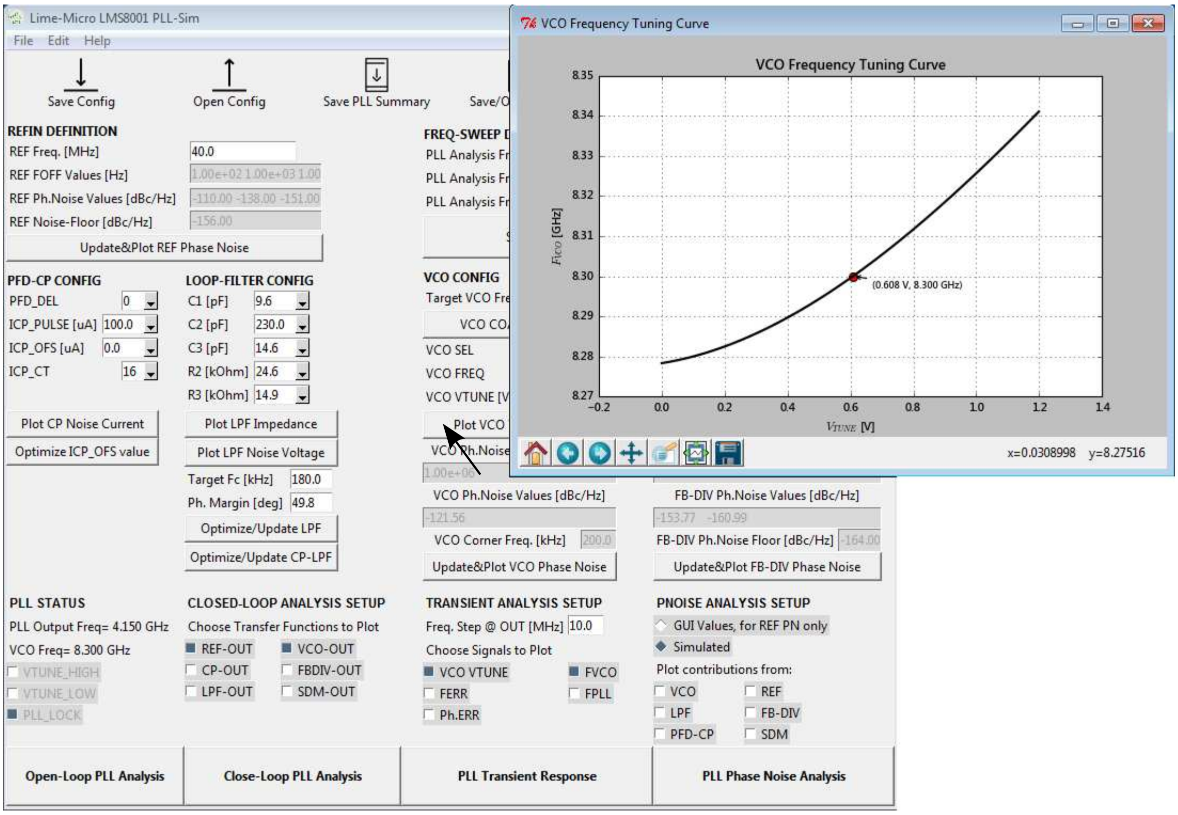
CLOSED-LOOP ANALYSIS SETUP
Choose Transfer Functions to Plot
■ REF-OUT ■ VCO-OUT
□ CP-OUT □ FBDIV-OUT
□ LPF-OUT □ SDM-OUT

TRANSIENT ANALYSIS SETUP
Freq. Step @ OUT [MHz] 10.0
Choose Signals to Plot
■ VCO VTUNE ■ FVCO
□ FERR □ FPLL
□ Ph.ERR

PNOISE ANALYSIS SETUP
◇ GUI Values, for REF PN only
◆ Simulated
Plot contributions from:
□ VCO □ REF
□ LPF □ FB-DIV
□ PFD-CP □ SDM

Figure 3.2: LMS8001 PLL-Sim's Main Window after pressing 'VCO COARSE TUNE' button for $F_{VCO} = 8.3GHz$

Main window offers many options to the user to plot different kind of performance parameters for different circuits, such as impedance of loop-filter or VCO frequency tuning curve. When user presses the 'Plot VCO Tuning Curve' button inside the 'VCO CONFIG' frame, new window pops-up containg graph that illustrates the dependence of VCO frequency on tuning voltage for the programmed VCO configuration, as shown in 3.3. This is only a rough estimation, since this VCO characteristic varies with PVT, and from sample to sample. Marker on the graph points the location estimated by LMS8001 PLL-Sim on VCO characteristics where targeted VCO frequency will be generated.



REFIN DEFINITION
REF Freq. [MHz] 40.0
REF FOFF Values [Hz] 1.00e+02 1.00e+03 1.00
REF Ph.Noise Values [dBc/Hz] -110.00 -138.00 -151.00
REF Noise-Floor [dBc/Hz] -156.00

PFD-CP CONFIG
PFD_DEL 0
ICP_PULSE [uA] 100.0
ICP_OFS [uA] 0.0
ICP_CT 16

LOOP-FILTER CONFIG
C1 [pF] 9.6
C2 [pF] 230.0
C3 [pF] 14.6
R2 [kOhm] 24.6
R3 [kOhm] 14.9
Target Fc [kHz] 180.0
Ph. Margin [deg] 49.8

FREQ-SWEEP D
PLL Analysis Fr
PLL Analysis Fr
PLL Analysis Fr

VCO CONFIG
Target VCO Fre
VCO SEL
VCO FREQ
VCO VTUNE [V
VCO Ph.Noise
1.00e+06
VCO Ph.Noise Values [dBc/Hz]
-121.56
VCO Corner Freq. [kHz] 200.0

FB-DIV Ph.Noise Values [dBc/Hz]
-153.77 -160.99
FB-DIV Ph.Noise Floor [dBc/Hz] -164.00

PLL STATUS
PLL Output Freq= 4.150 GHz
VCO Freq= 8.300 GHz
□ VTUNE_HIGH
□ VTUNE_LOW
■ PLL_LOCK

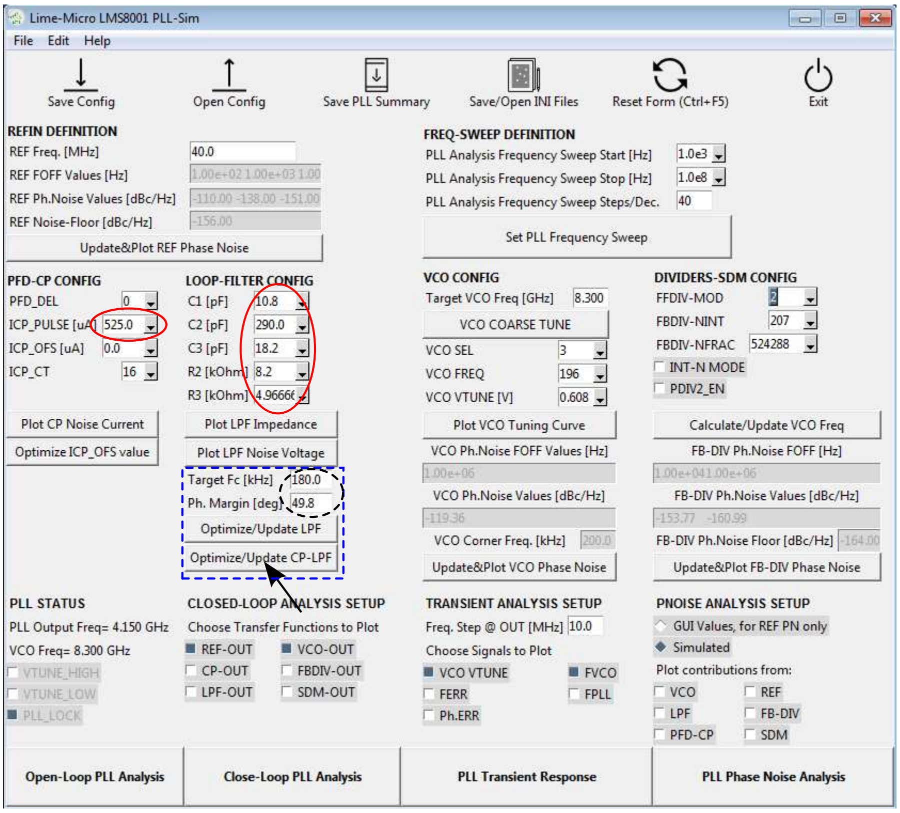
CLOSED-LOOP ANALYSIS SETUP
Choose Transfer Functions to Plot
■ REF-OUT ■ VCO-OUT
□ CP-OUT □ FBDIV-OUT
□ LPF-OUT □ SDM-OUT

TRANSIENT ANALYSIS SETUP
Freq. Step @ OUT [MHz] 10.0
Choose Signals to Plot
■ VCO VTUNE ■ FVCO
□ FERR □ FPLL
□ Ph.ERR

PNOISE ANALYSIS SETUP
◇ GUI Values, for REF PN only
◆ Simulated
Plot contributions from:
□ VCO □ REF
□ LPF □ FB-DIV
□ PFD-CP □ SDM

Figure 3.3: LMS8001 PLL-Sim's Main Window after pressing 'Plot VCO Tuning Curve' button

After setting the VCO to the specified frequency, next step is often to set the PFD-CP and Loop-Filter parameters in order to achieve desired dynamics of the loop. Dynamics of the loop can be specified in terms of open-loop crossover frequency 'Target Fc [kHz]' and phase margin 'Phase Margin [deg]' inside the 'LOOP-FILTER CONFIG' frame. Built-in function that implements PLL Loop BW optimization method is available to the users and can be called by pressing the 'Optimize/Update CP-LPF' button. LMS8001 PLL-Sim automaticaly sets the CP pulse current and Loop-Filter component values to achieve targeted PLL dynamics, if possible. New state of main window after this step is shown in fig. 3.4.



REFIN DEFINITION

REF Freq. [MHz] 40.0

REF FOFF Values [Hz] 1.00e+02 1.00e+03 1.00

REF Ph.Noise Values [dBc/Hz] -110.00 -138.00 -151.00

REF Noise-Floor [dBc/Hz] -156.00

FREQ-SWEEP DEFINITION

PLL Analysis Frequency Sweep Start [Hz] 1.0e3

PLL Analysis Frequency Sweep Stop [Hz] 1.0e8

PLL Analysis Frequency Sweep Steps/Dec. 40

PFD-CP CONFIG

PFD_DEL 0

ICP_PULSE [uA] 525.0

ICP_OFS [uA] 0.0

ICP_CT 16

LOOP-FILTER CONFIG

C1 [pF] 10.8

C2 [pF] 290.0

C3 [pF] 18.2

R2 [kOhm] 8.2

R3 [kOhm] 4.96666

Target Fc [kHz] 180.0

Ph. Margin [deg] 49.8

VCO CONFIG

Target VCO Freq [GHz] 8.300

VCO SEL 3

VCO FREQ 196

VCO VTUNE [V] 0.608

VCO Ph.Noise FOFF Values [Hz] 1.00e+06

VCO Ph.Noise Values [dBc/Hz] -119.36

VCO Corner Freq. [kHz] 200.0

DIVIDERS-SDM CONFIG

FFDIV-MOD 2

FBDIV-NINT 207

FBDIV-NFRAC 524288

□ INT-N MODE

□ PDIV2_EN

FB-DIV Ph.Noise FOFF [Hz] 1.00e+041.00e+06

FB-DIV Ph.Noise Values [dBc/Hz] -153.77 -160.99

FB-DIV Ph.Noise Floor [dBc/Hz] -164.00

PLL STATUS

PLL Output Freq= 4.150 GHz

VCO Freq= 8.300 GHz

□ VTUNE_HIGH

□ VTUNE_LOW

■ PLL_LOCK

CLOSED-LOOP ANALYSIS SETUP

Choose Transfer Functions to Plot

■ REF-OUT ■ VCO-OUT

□ CP-OUT □ FBDIV-OUT

□ LPF-OUT □ SDM-OUT

TRANSIENT ANALYSIS SETUP

Freq. Step @ OUT [MHz] 10.0

Choose Signals to Plot

■ VCO VTUNE ■ FVCO

□ FERR □ FPLL

□ Ph.ERR

PNOISE ANALYSIS SETUP

◇ GUI Values, for REF PN only

◆ Simulated

Plot contributions from:

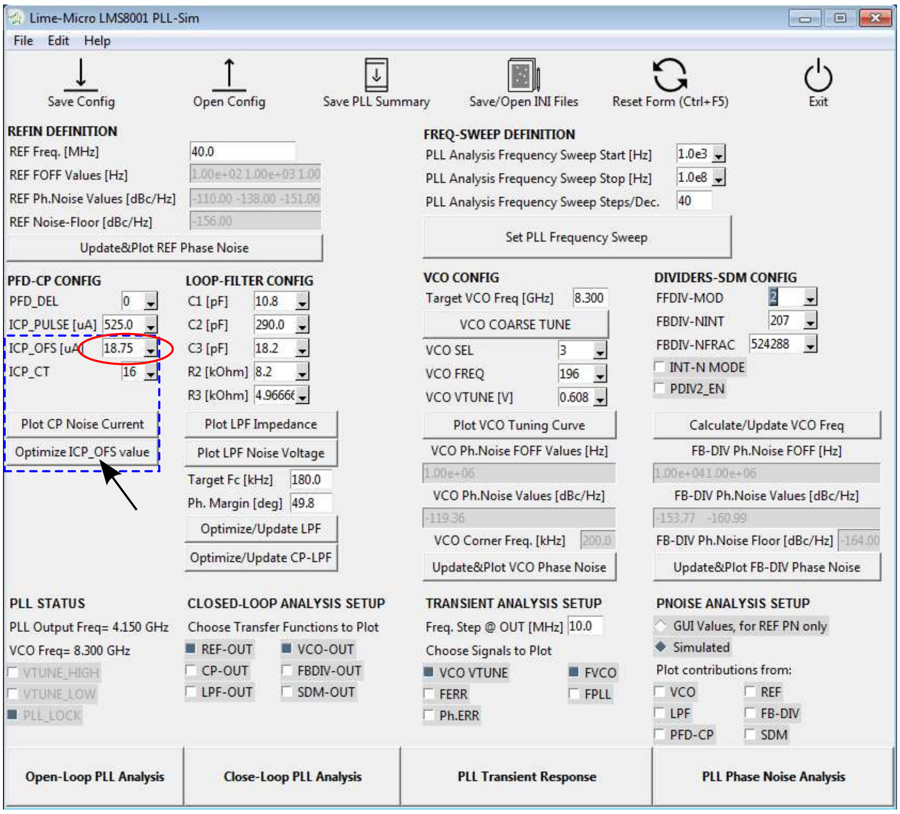
□ VCO □ REF

□ LPF □ FB-DIV

□ PFD-CP □ SDM

Figure 3.4: LMS8001 PLL-Sim's Main Window after pressing 'Optimize/Update CP-LPF' button

As the last step in PLL core optimization, user might want to get optimal value for CP offset current. This function is called by pressing 'Optimize ICP_OFS value' button in 'PFD-CP CONFIG' frame. Method updates 'ICP_OFS' value when PLL works in fractional-N mode, as illustrated in fig.3.5. User can find more info about this functionality in section 4.3.



REFIN DEFINITION
REF Freq. [MHz] 40.0
REF FOFF Values [Hz] 1.00e+02 1.00e+03 1.00
REF Ph.Noise Values [dBc/Hz] -110.00 -138.00 -151.00
REF Noise-Floor [dBc/Hz] -156.00

FREQ-SWEEP DEFINITION
PLL Analysis Frequency Sweep Start [Hz] 1.0e3
PLL Analysis Frequency Sweep Stop [Hz] 1.0e8
PLL Analysis Frequency Sweep Steps/Dec. 40

PFD-CP CONFIG
PFD_DEL 0
ICP_PULSE [uA] 525.0
ICP_OFS [uA] 18.75
ICP_CT 16

LOOP-FILTER CONFIG
C1 [pF] 10.8
C2 [pF] 290.0
C3 [pF] 18.2
R2 [kOhm] 8.2
R3 [kOhm] 4.96666
Target Fc [kHz] 180.0
Ph. Margin [deg] 49.8

VCO CONFIG
Target VCO Freq [GHz] 8.300
VCO SEL 3
VCO FREQ 196
VCO VTUNE [V] 0.608
VCO Ph.Noise FOFF Values [Hz] 1.00e+06
VCO Ph.Noise Values [dBc/Hz] -119.36
VCO Corner Freq. [kHz] 200.0

DIVIDERS-SDM CONFIG
FFDIV-MOD 2
FBDIV-NINT 207
FBDIV-NFRAC 524288
☐ INT-N MODE
☐ PDIV2_EN
FB-DIV Ph.Noise FOFF [Hz] 1.00e+041.00e+06
FB-DIV Ph.Noise Values [dBc/Hz] -153.77 -160.99
FB-DIV Ph.Noise Floor [dBc/Hz] -164.00

PLL STATUS
PLL Output Freq= 4.150 GHz
VCO Freq= 8.300 GHz
☐ VTUNE_HIGH
☐ VTUNE_LOW
■ PLL_LOCK

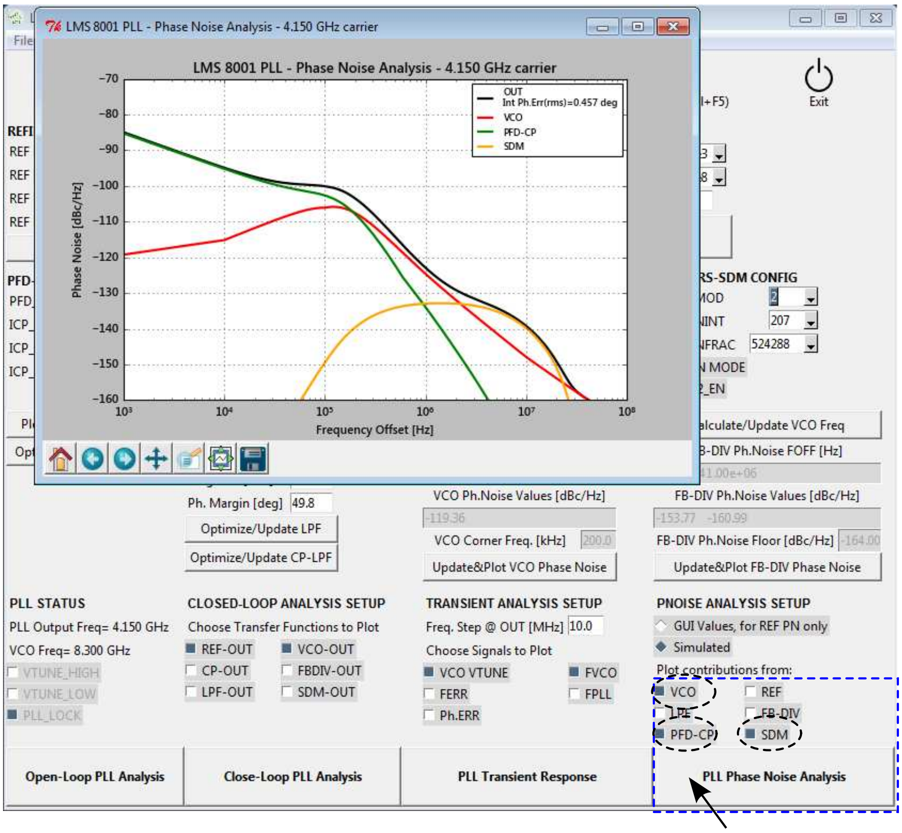
CLOSED-LOOP ANALYSIS SETUP
Choose Transfer Functions to Plot
■ REF-OUT ■ VCO-OUT
☐ CP-OUT ☐ FBDIV-OUT
☐ LPF-OUT ☐ SDM-OUT

TRANSIENT ANALYSIS SETUP
Freq. Step @ OUT [MHz] 10.0
Choose Signals to Plot
■ VCO VTUNE ■ FVCO
☐ FERR ☐ FPLL
☐ Ph.ERR

PNOISE ANALYSIS SETUP
○ GUI Values, for REF PN only
● Simulated
Plot contributions from:
☐ VCO ☐ REF
☐ LPF ☐ FB-DIV
☐ PFD-CP ☐ SDM

Figure 3.5: LMS8001 PLL-Sim's Main Window after pressing 'Optimize ICP_OFS value' button

At this point, PLL core is configured and ready for performing different analysis. For example, fig.3.6 presents main window after performing 'PLL Phase Noise Analysis' by pressing the button in last row with this name. Main phase noise contributors in various regions are presented beside the total phase noise curve. Which contributions will be ploted can be selected using available checkbuttons in the 'PNOISE ANALYSIS SETUP' frame.



MOD 2
NINT 207
NFRAC 524288
FB-DIV Ph.Noise FOFF [Hz] 1.00e+06
Ph. Margin [deg] 49.8
VCO Ph.Noise Values [dBc/Hz] -119.36
VCO Corner Freq. [kHz] 200.0
FB-DIV Ph.Noise Values [dBc/Hz] -153.77 -160.99
FB-DIV Ph.Noise Floor [dBc/Hz] -164.00

PLL Output Freq= 4.150 GHz
VCO Freq= 8.300 GHz
□ VTUNE_HIGH
□ VTUNE_LOW
■ PLL_LOCK

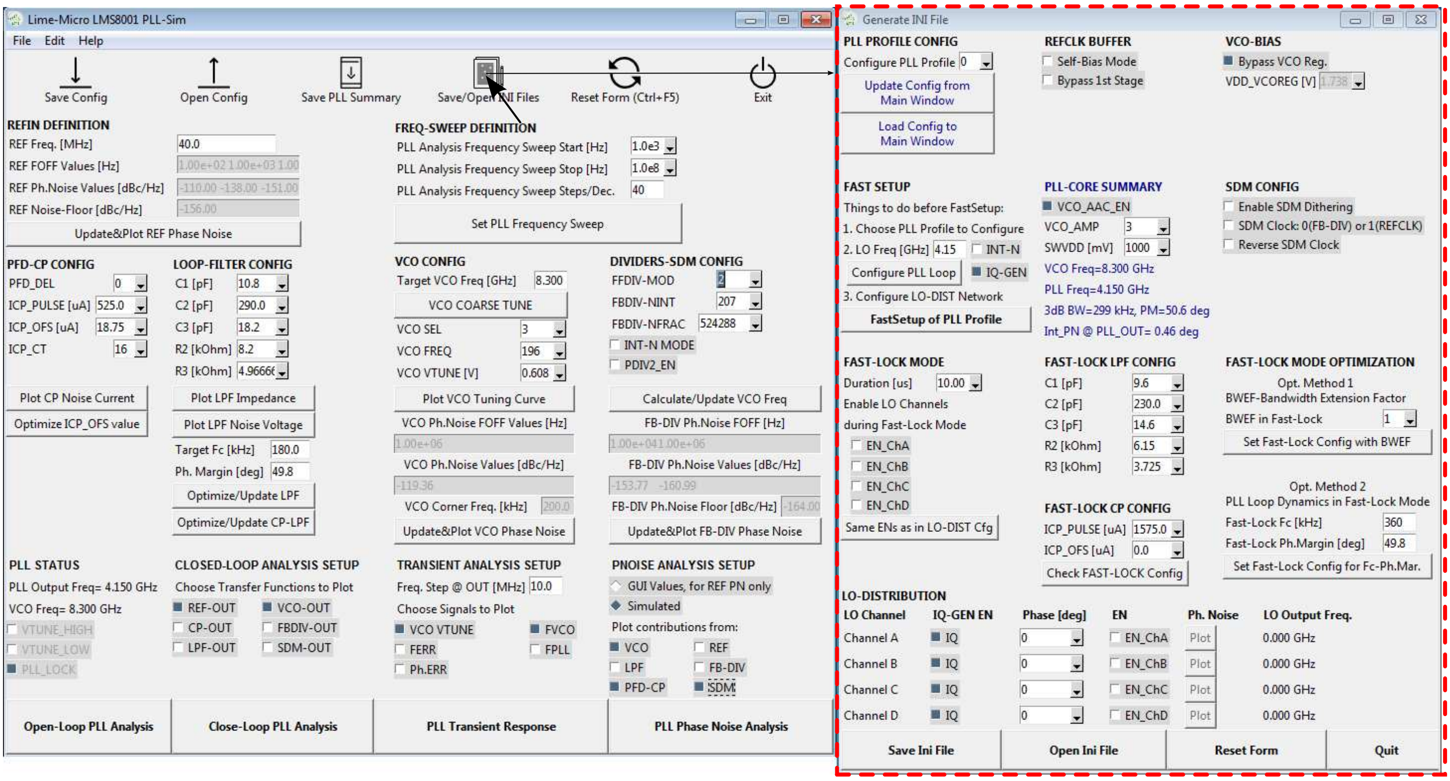
Choose Transfer Functions to Plot
■ REF-OUT ■ VCO-OUT
□ CP-OUT □ FBDIV-OUT
□ LPF-OUT □ SDM-OUT

Freq. Step @ OUT [MHz] 10.0
Choose Signals to Plot
■ VCO VTUNE ■ FVCO
□ FERR □ FPLL
□ Ph.ERR

○ GUI Values, for REF PN only
● Simulated
Plot contributions from:
■ VCO □ REF
□ LPF □ FB-DIV
■ PFD-CP ■ SDM

Figure 3.6: LMS8001 PLL-Sim's Main Window after pressing 'PLL Phase Noise Analysis' button

Beside defining and analysis of PLL core configuration, LMS8001 PLL-Sim software provides to the user the possibility to also define most important parameters of LMS8001 LO distribution network, to configure PLL Core settings in fast-lock mode, and to check phase noise performance of final LO carrier signals which are driving LMS8001 mixers. All of these features are available in new window which opens up after pressing the 'Save/Open INI Files' button in main window toolbar, as shown in fig.3.7. More info about functions and settings available in this window user can find in chapter 5. Beside this, the user has also the possibility to define settings for all eight PLL profile register banks available in LMS8001 IC and to save them in INI file for *lms8suite* GUI control software. User can also use feature to open *lms8suite* INI file, load settings from desired PLL profile into LMS8001 PLL-Sim GUI and analyze the performance of PLL-LODIST subsystem with a given configuration.



REFIN DEFINITION

REF Freq. [MHz] 40.0
REF FOFF Values [Hz] 1.00e+02 1.00e+03 1.00
REF Ph.Noise Values [dBc/Hz] -110.00 -138.00 -151.00
REF Noise-Floor [dBc/Hz] -156.00

FREQ-SWEEP DEFINITION

PLL Analysis Frequency Sweep Start [Hz] 1.0e3
PLL Analysis Frequency Sweep Stop [Hz] 1.0e8
PLL Analysis Frequency Sweep Steps/Dec. 40

PFD-CP CONFIG

PFD_DEL 0
ICP_PULSE [uA] 525.0
ICP_OFS [uA] 18.75
ICP_CT 16

LOOP-FILTER CONFIG

C1 [pF] 10.8
C2 [pF] 290.0
C3 [pF] 18.2
R2 [kOhm] 8.2
R3 [kOhm] 4.9666(
Target Fc [kHz] 180.0
Ph. Margin [deg] 49.8

VCO CONFIG

Target VCO Freq [GHz] 8.300
VCO SEL 3
VCO FREQ 196
VCO VTUNE [V] 0.608
VCO Ph.Noise FOFF Values [Hz] 1.00e+06
VCO Ph.Noise Values [dBc/Hz] -119.36
VCO Corner Freq. [kHz] 200.0

DIVIDERS-SDM CONFIG

FFDIV-MOD 2
FBDIV-NINT 207
FBDIV-NFRAC 524288
☐ INT-N MODE
☐ PDIV2_EN
FB-DIV Ph.Noise FOFF [Hz] 1.00e+041.00e+06
FB-DIV Ph.Noise Values [dBc/Hz] -153.77 -160.99
FB-DIV Ph.Noise Floor [dBc/Hz] -164.00

PLL STATUS

PLL Output Freq= 4.150 GHz
VCO Freq= 8.300 GHz
☐ VTUNE_HIGH
☐ VTUNE_LOW
■ PLL_LOCK

CLOSED-LOOP ANALYSIS SETUP

Choose Transfer Functions to Plot
■ REF-OUT ■ VCO-OUT
☐ CP-OUT ☐ FBDIV-OUT
☐ LPF-OUT ☐ SDM-OUT

TRANSIENT ANALYSIS SETUP

Freq. Step @ OUT [MHz] 10.0
Choose Signals to Plot
■ VCO VTUNE ■ FVCO
☐ FERR ☐ FPLL
☐ Ph.ERR

PNOISE ANALYSIS SETUP

○ GUI Values, for REF PN only
◆ Simulated
Plot contributions from:
■ VCO ☐ REF
☐ LPF ☐ FB-DIV
■ PFD-CP ■ SDM

PLL PROFILE CONFIG

Configure PLL Profile 0

REFCLK BUFFER

☐ Self-Bias Mode
☐ Bypass 1st Stage

VCO-BIAS

■ Bypass VCO Reg.
VDD_VCOREG [V] 1.738

FAST SETUP

Things to do before FastSetup:
1. Choose PLL Profile to Configure
2. LO Freq [GHz] 4.15 ☐ INT-N
■ IQ-GEN
3. Configure LO-DIST Network

PLL-CORE SUMMARY

■ VCO_AAC_EN
VCO_AMP 3
SWVDD [mV] 1000
VCO Freq=8.300 GHz
PLL Freq=4.150 GHz
3dB BW=299 kHz, PM=50.6 deg
Int_PN @ PLL_OUT= 0.46 deg

SDM CONFIG

☐ Enable SDM Dithering
☐ SDM Clock: 0(FB-DIV) or 1(REFCLK)
☐ Reverse SDM Clock

FAST-LOCK MODE

Duration [us] 10.00
Enable LO Channels during Fast-Lock Mode
☐ EN_ChA
☐ EN_ChB
☐ EN_ChC
☐ EN_ChD

FAST-LOCK LPF CONFIG

C1 [pF] 9.6
C2 [pF] 230.0
C3 [pF] 14.6
R2 [kOhm] 6.15
R3 [kOhm] 3.725

FAST-LOCK CP CONFIG

ICP_PULSE [uA] 1575.0
ICP_OFS [uA] 0.0

FAST-LOCK MODE OPTIMIZATION

Opt. Method 1
BWEF-Bandwidth Extension Factor
BWEF in Fast-Lock 1

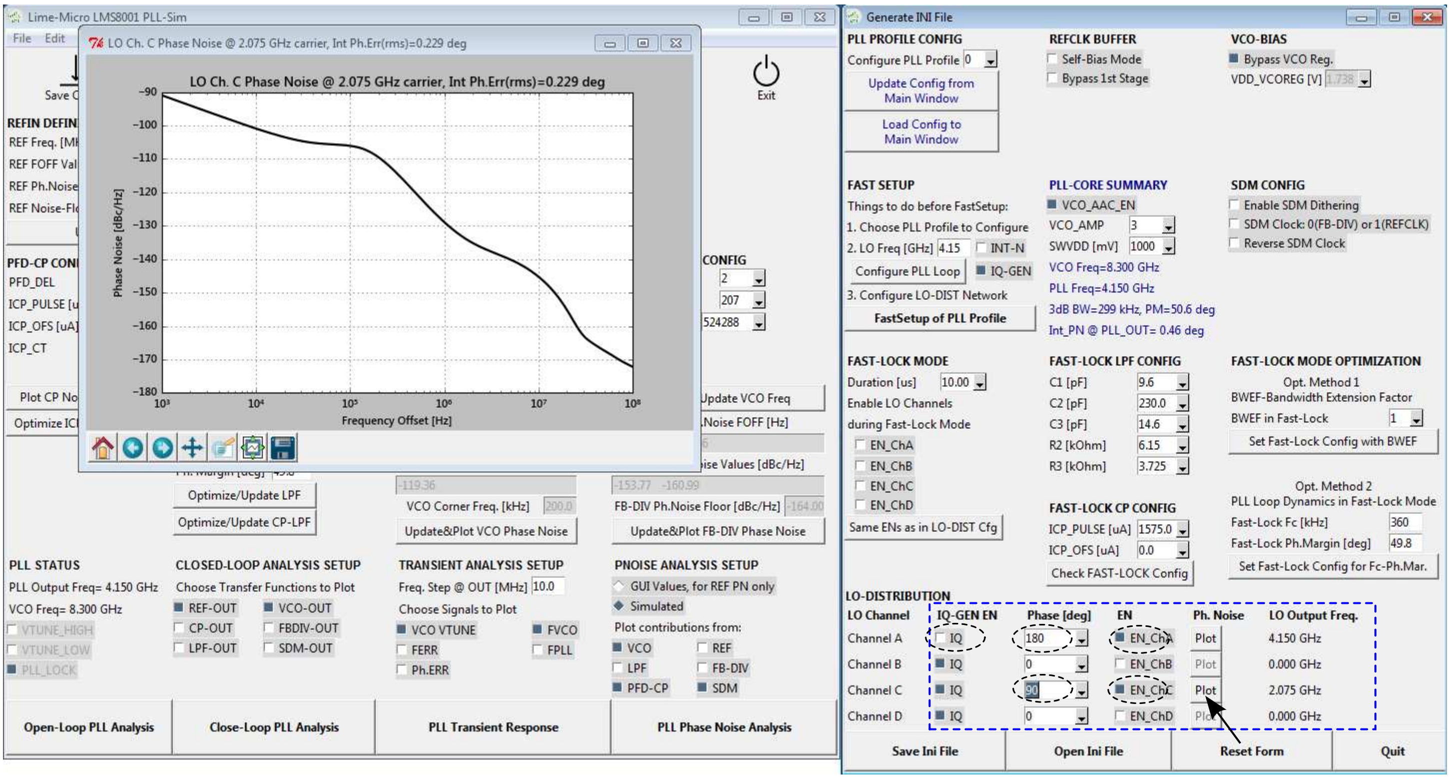
Opt. Method 2
PLL Loop Dynamics in Fast-Lock Mode
Fast-Lock Fc [kHz] 360
Fast-Lock Ph.Margin [deg] 49.8

LO-DISTRIBUTION

LO Channel	IQ-GEN EN	Phase [deg]	EN	Ph. Noise	LO Output Freq.
Channel A	■ IQ	0	☐ EN_ChA	Plot	0.000 GHz
Channel B	■ IQ	0	☐ EN_ChB	Plot	0.000 GHz
Channel C	■ IQ	0	☐ EN_ChC	Plot	0.000 GHz
Channel D	■ IQ	0	☐ EN_ChD	Plot	0.000 GHz

Figure 3.7: LMS8001 PLL-Sim's Main Window + Additional Settings (Save/Open INI Files)

After defining settings available in 'LO-DISTRIBUTION' frame, user can see exact LO frequency and plot expected phase noise performance for enabled LO channels in distribution network. This is presented in fig.3.8.



LO Ch. C Phase Noise @ 2.075 GHz carrier, Int Ph.Err(rms)=0.229 deg

REFIN DEFIN
REF Freq. [MH
REF FOFF Val
REF Ph.Noise
REF Noise-Fl

PFD-CP CON
PFD_DEL
ICP_PULSE [u
ICP_OFS [uA]
ICP_CT

Plot CP No
Optimize ICI

CONFIG
2
207
524288

Update VCO Freq
Noise FOFF [Hz]
ise Values [dBc/Hz]

-119.36
VCO Corner Freq. [kHz] 200.0
Update&Plot VCO Phase Noise

-153.77 -160.99
FB-DIV Ph.Noise Floor [dBc/Hz] -164.00
Update&Plot FB-DIV Phase Noise

Optimize/Update LPF
Optimize/Update CP-LPF

PLL STATUS
PLL Output Freq= 4.150 GHz
VCO Freq= 8.300 GHz
□ VTUNE_HIGH
□ VTUNE_LOW
■ PLL_LOCK

CLOSED-LOOP ANALYSIS SETUP
Choose Transfer Functions to Plot
■ REF-OUT ■ VCO-OUT
□ CP-OUT □ FBDIV-OUT
□ LPF-OUT □ SDM-OUT

TRANSIENT ANALYSIS SETUP
Freq. Step @ OUT [MHz] 10.0
Choose Signals to Plot
■ VCO VTUNE ■ FVCO
□ FERR □ FPLL
□ Ph.ERR

PNOISE ANALYSIS SETUP
◇ GUI Values, for REF PN only
◆ Simulated
Plot contributions from:
■ VCO □ REF
□ LPF □ FB-DIV
■ PFD-CP ■ SDM

Open-Loop PLL Analysis | Close-Loop PLL Analysis | PLL Transient Response | PLL Phase Noise Analysis

PLL PROFILE CONFIG
Configure PLL Profile 0
Update Config from Main Window
Load Config to Main Window

REFCLK BUFFER
□ Self-Bias Mode
□ Bypass 1st Stage

VCO-BIAS
■ Bypass VCO Reg.
VDD_VCOREG [V] 1.738

FAST SETUP
Things to do before FastSetup:
1. Choose PLL Profile to Configure
2. LO Freq [GHz] 4.15 □ INT-N
Configure PLL Loop ■ IQ-GEN
3. Configure LO-DIST Network
FastSetup of PLL Profile

PLL-CORE SUMMARY
■ VCO_AAC_EN
VCO_AMP 3
SWVDD [mV] 1000
VCO Freq=8.300 GHz
PLL Freq=4.150 GHz
3dB BW=299 kHz, PM=50.6 deg
Int_PN @ PLL_OUT= 0.46 deg

SDM CONFIG
□ Enable SDM Dithering
□ SDM Clock: 0(FB-DIV) or 1(REFCLK)
□ Reverse SDM Clock

FAST-LOCK MODE
Duration [us] 10.00
Enable LO Channels during Fast-Lock Mode
□ EN_ChA
□ EN_ChB
□ EN_ChC
□ EN_ChD
Same ENs as in LO-DIST Cfg

FAST-LOCK LPF CONFIG
C1 [pF] 9.6
C2 [pF] 230.0
C3 [pF] 14.6
R2 [kOhm] 6.15
R3 [kOhm] 3.725

FAST-LOCK CP CONFIG
ICP_PULSE [uA] 1575.0
ICP_OFS [uA] 0.0
Check FAST-LOCK Config

FAST-LOCK MODE OPTIMIZATION
Opt. Method 1
BWEF-Bandwidth Extension Factor
BWEF in Fast-Lock 1
Set Fast-Lock Config with BWEF

Opt. Method 2
PLL Loop Dynamics in Fast-Lock Mode
Fast-Lock Fc [kHz] 360
Fast-Lock Ph.Margin [deg] 49.8
Set Fast-Lock Config for Fc-Ph.Mar.

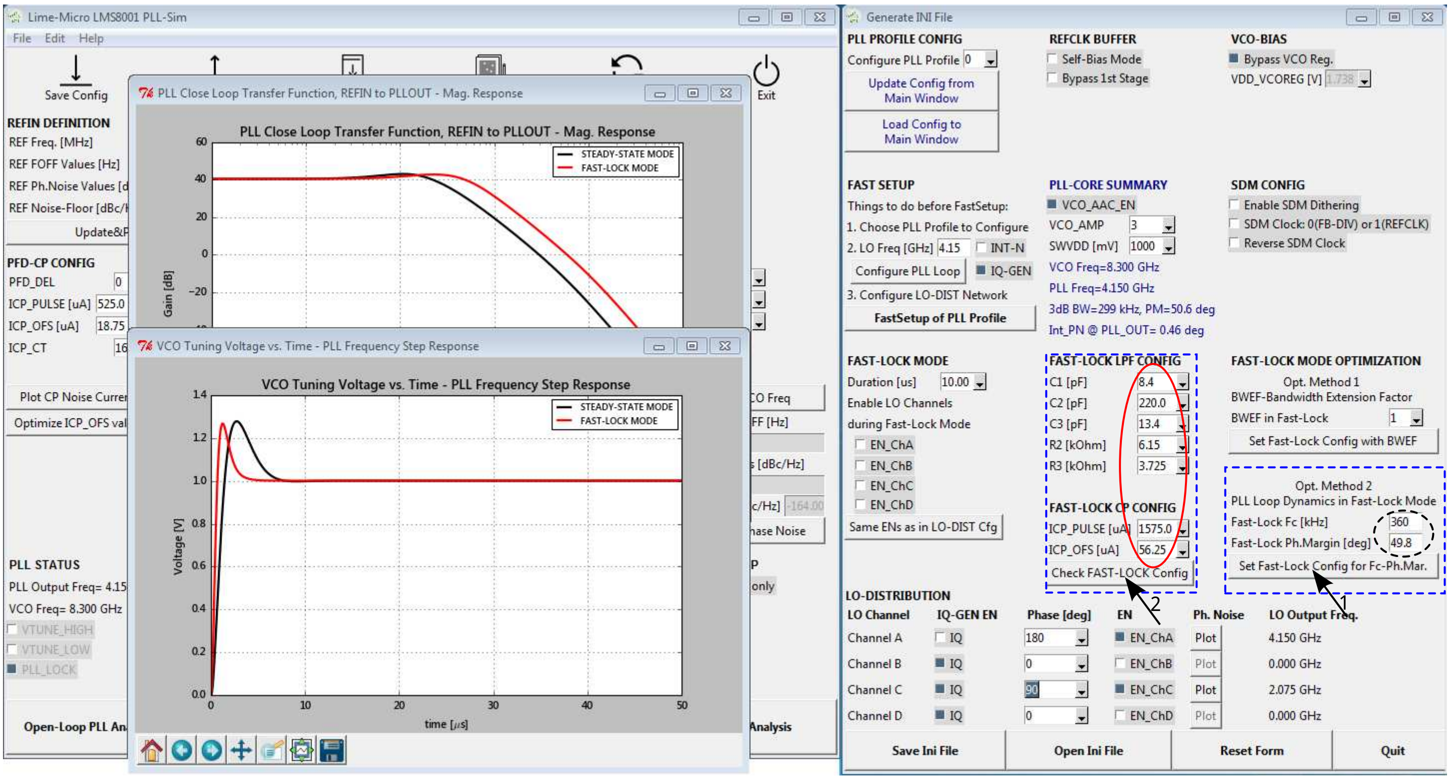
LO-DISTRIBUTION

LO Channel	IQ-GEN EN	Phase [deg]	EN	Ph. Noise	LO Output Freq.
Channel A	□ IQ	180	■ EN_ChA	Plot	4.150 GHz
Channel B	■ IQ	0	□ EN_ChB	Plot	0.000 GHz
Channel C	■ IQ	90	■ EN_ChC	Plot	2.075 GHz
Channel D	■ IQ	0	□ EN_ChD	Plot	0.000 GHz

Save Ini File | Open Ini File | Reset Form | Quit

Figure 3.8: LMS8001 PLL-Sim - Estimated Phase Noise Performance of the LMS8001's LO Channel C

There are two optimization methods available for fast definition of Fast-Lock operation mode in the frame titled with 'FAST-LOCK MODE OPTIMIZATION'. With 'Check FAST-LOCK Config' button, user can easy compare loop bandwidths and settling times of PLL Core for normal (steady-state) and fast-lock settings. This is shown in fig.3.9. More about fast-lock mode optimizations can be found in section 5.7.



PLL PROFILE CONFIG
Configure PLL Profile 0
Update Config from Main Window
Load Config to Main Window

REFCLK BUFFER
☐ Self-Bias Mode
☐ Bypass 1st Stage

VCO-BIAS
■ Bypass VCO Reg.
VDD_VCOREG [V] 1.738

FAST SETUP
Things to do before FastSetup:
1. Choose PLL Profile to Configure
2. LO Freq [GHz] 4.15 ☐ INT-N
Configure PLL Loop ■ IQ-GEN
3. Configure LO-DIST Network
FastSetup of PLL Profile

PLL-CORE SUMMARY
■ VCO_AAC_EN
VCO_AMP 3
SWVDD [mV] 1000
VCO Freq=8.300 GHz
PLL Freq=4.150 GHz
3dB BW=299 kHz, PM=50.6 deg
Int_PN @ PLL_OUT= 0.46 deg

SDM CONFIG
☐ Enable SDM Dithering
☐ SDM Clock: 0(FB-DIV) or 1(REFCLK)
☐ Reverse SDM Clock

FAST-LOCK MODE
Duration [us] 10.00
Enable LO Channels during Fast-Lock Mode
☐ EN_ChA
☐ EN_ChB
☐ EN_ChC
☐ EN_ChD
Same ENs as in LO-DIST Cfg

FAST-LOCK LPF CONFIG
C1 [pF] 8.4
C2 [pF] 220.0
C3 [pF] 13.4
R2 [kOhm] 6.15
R3 [kOhm] 3.725

FAST-LOCK CP CONFIG
ICP_PULSE [uA] 1575.0
ICP_OFS [uA] 56.25
Check FAST-LOCK Config

FAST-LOCK MODE OPTIMIZATION
Opt. Method 1
BWEF-Bandwidth Extension Factor
BWEF in Fast-Lock 1
Set Fast-Lock Config with BWEF

Opt. Method 2
PLL Loop Dynamics in Fast-Lock Mode
Fast-Lock Fc [kHz] 360
Fast-Lock Ph.Margin [deg] 49.8
Set Fast-Lock Config for Fc-Ph.Mar.

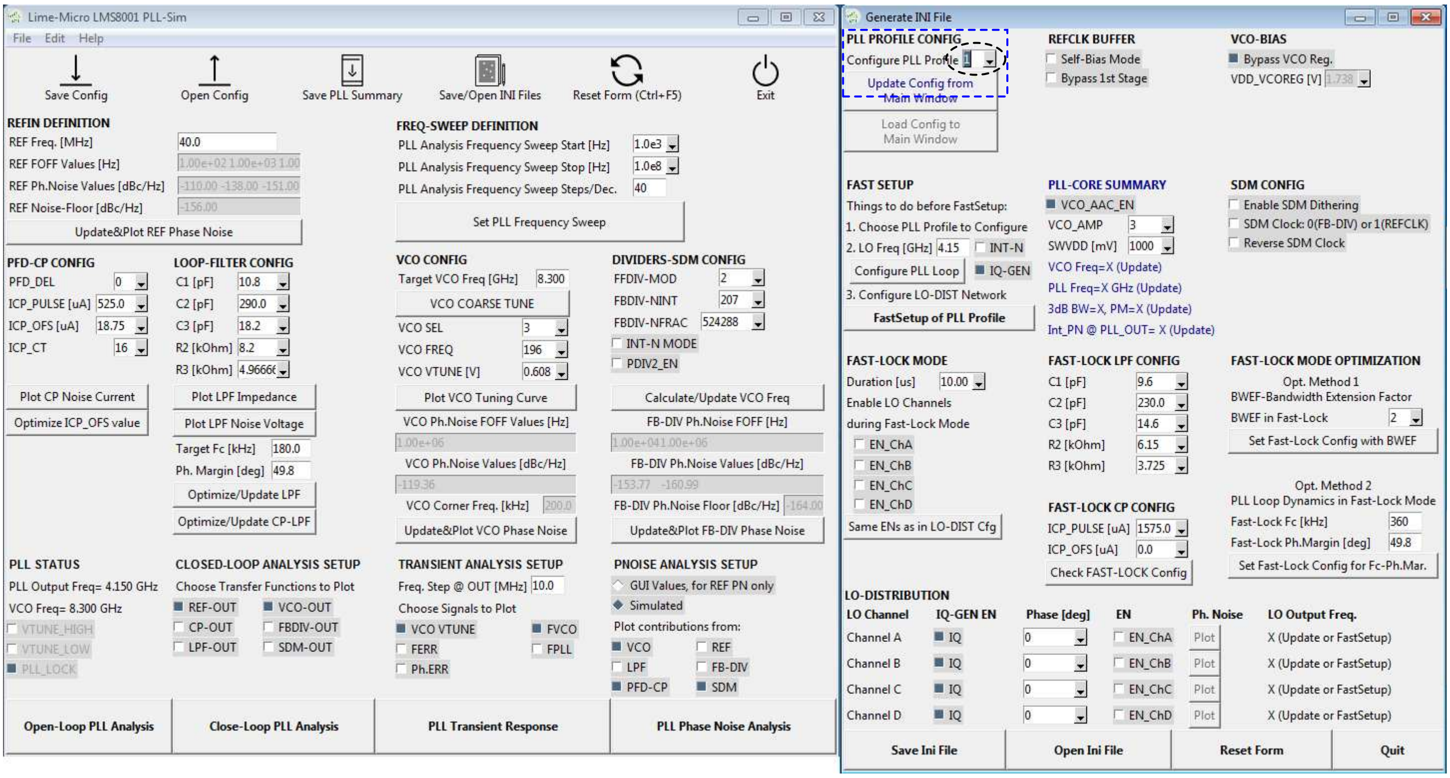
LO-DISTRIBUTION

LO Channel	IQ-GEN EN	Phase [deg]	EN	Ph. Noise	LO Output Freq.
Channel A	☐ IQ	180	■ EN_ChA	Plot	4.150 GHz
Channel B	■ IQ	0	☐ EN_ChB	Plot	0.000 GHz
Channel C	■ IQ	90	■ EN_ChC	Plot	2.075 GHz
Channel D	■ IQ	0	☐ EN_ChD	Plot	0.000 GHz

Save Ini File | Open Ini File | Reset Form | Quit

Figure 3.9: LMS8001 PLL-Sim - Optimization of Fast-Lock Mode Config

If user changes active PLL profile using combobox inside 'PLL PROFILE CONFIG' frame at the top of 'Generate INI File' window, all the windows are automaticaly updated if this profile is in the list of configured PLL profiles. When the new PLL profile is not configured yet, all the settings in 'Generate INI File' window are set to default values, main window settings are not changed and user is informed that PLL profile needs to be configured. This is presented in fig.3.10.



REFIN DEFINITION
REF Freq. [MHz] 40.0
REF FOFF Values [Hz] 1.00e+02 1.00e+03 1.00
REF Ph.Noise Values [dBc/Hz] -110.00 -138.00 -151.00
REF Noise-Floor [dBc/Hz] -156.00

FREQ-SWEEP DEFINITION
PLL Analysis Frequency Sweep Start [Hz] 1.0e3
PLL Analysis Frequency Sweep Stop [Hz] 1.0e8
PLL Analysis Frequency Sweep Steps/Dec. 40

PFD-CP CONFIG
PFD_DEL 0
ICP_PULSE [uA] 525.0
ICP_OFS [uA] 18.75
ICP_CT 16

LOOP-FILTER CONFIG
C1 [pF] 10.8
C2 [pF] 290.0
C3 [pF] 18.2
R2 [kOhm] 8.2
R3 [kOhm] 4.96666
Target Fc [kHz] 180.0
Ph. Margin [deg] 49.8

VCO CONFIG
Target VCO Freq [GHz] 8.300
VCO SEL 3
VCO FREQ 196
VCO VTUNE [V] 0.608
VCO Ph.Noise FOFF Values [Hz] 1.00e+06
VCO Ph.Noise Values [dBc/Hz] -119.36
VCO Corner Freq. [kHz] 200.0

DIVIDERS-SDM CONFIG
FFDIV-MOD 2
FBDIV-NINT 207
FBDIV-NFRAC 524288
□ INT-N MODE
□ PDIV2_EN
FB-DIV Ph.Noise FOFF [Hz] 1.00e+041.00e+06
FB-DIV Ph.Noise Values [dBc/Hz] -153.77 -160.99
FB-DIV Ph.Noise Floor [dBc/Hz] -164.00

PLL STATUS
PLL Output Freq= 4.150 GHz
VCO Freq= 8.300 GHz
□ VTUNE_HIGH
□ VTUNE_LOW
■ PLL_LOCK

CLOSED-LOOP ANALYSIS SETUP
Choose Transfer Functions to Plot
■ REF-OUT ■ VCO-OUT
□ CP-OUT □ FBDIV-OUT
□ LPF-OUT □ SDM-OUT

TRANSIENT ANALYSIS SETUP
Freq. Step @ OUT [MHz] 10.0
Choose Signals to Plot
■ VCO VTUNE ■ FVCO
□ FERR □ FPLL
□ Ph.ERR

PNOISE ANALYSIS SETUP
○ GUI Values, for REF PN only
● Simulated
Plot contributions from:
■ VCO □ REF
□ LPF □ FB-DIV
■ PFD-CP ■ SDM

PLL PROFILE CONFIG
Configure PLL Profile 1

REFCLK BUFFER
□ Self-Bias Mode
□ Bypass 1st Stage

VCO-BIAS
■ Bypass VCO Reg.
VDD_VCOREG [V] 1.738

FAST SETUP
Things to do before FastSetup:
1. Choose PLL Profile to Configure
2. LO Freq [GHz] 4.15 □ INT-N
■ IQ-GEN
3. Configure LO-DIST Network

PLL-CORE SUMMARY
■ VCO_AAC_EN
VCO_AMP 3
SWVDD [mV] 1000
VCO Freq=X (Update)
PLL Freq=X GHz (Update)
3dB BW=X, PM=X (Update)
Int_PN @ PLL_OUT= X (Update)

SDM CONFIG
□ Enable SDM Dithering
□ SDM Clock: 0(FB-DIV) or 1(REFCLK)
□ Reverse SDM Clock

FAST-LOCK MODE
Duration [us] 10.00
Enable LO Channels
during Fast-Lock Mode
□ EN_ChA
□ EN_ChB
□ EN_ChC
□ EN_ChD

FAST-LOCK LPF CONFIG
C1 [pF] 9.6
C2 [pF] 230.0
C3 [pF] 14.6
R2 [kOhm] 6.15
R3 [kOhm] 3.725

FAST-LOCK CP CONFIG
ICP_PULSE [uA] 1575.0
ICP_OFS [uA] 0.0

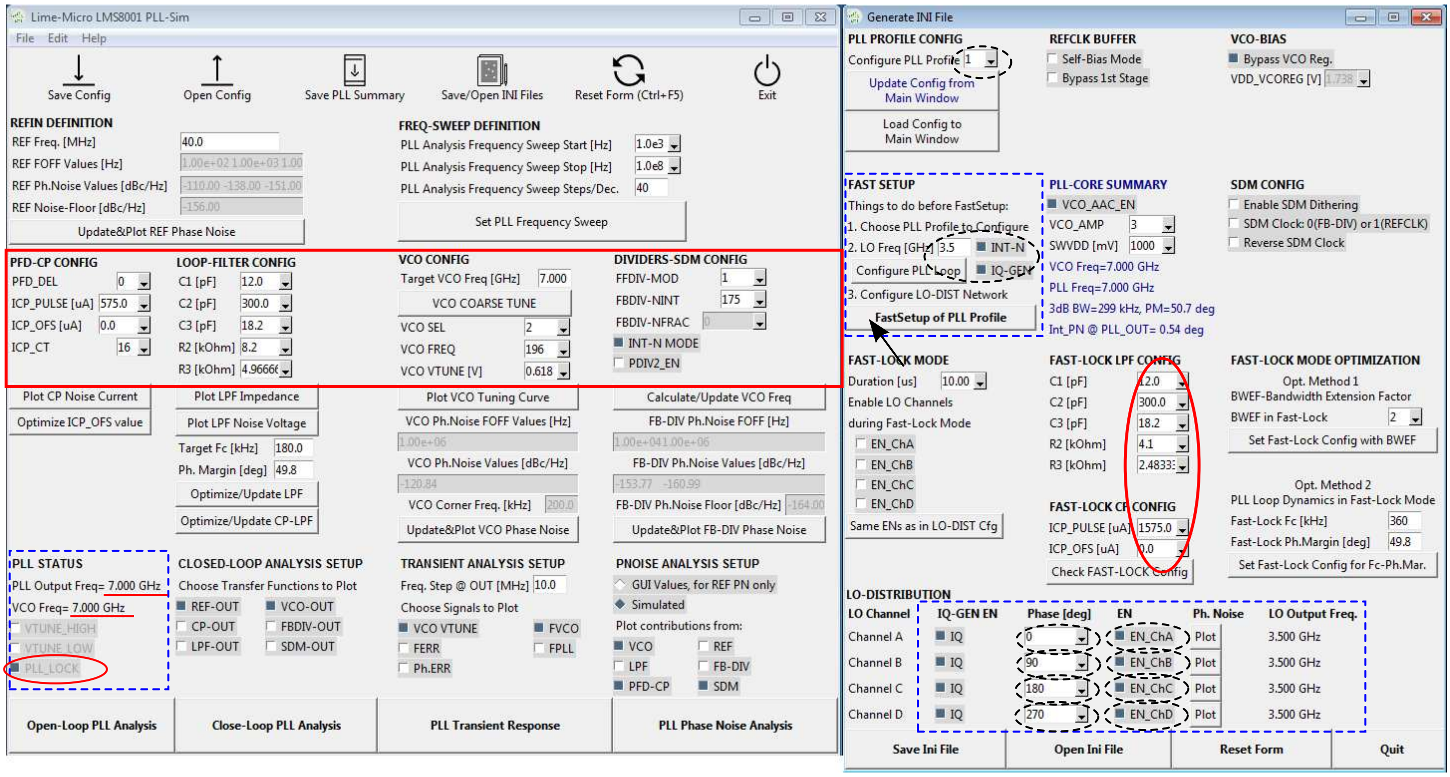
FAST-LOCK MODE OPTIMIZATION
Opt. Method 1
BWEF-Bandwidth Extension Factor
BWEF in Fast-Lock 2
Opt. Method 2
PLL Loop Dynamics in Fast-Lock Mode
Fast-Lock Fc [kHz] 360
Fast-Lock Ph.Margin [deg] 49.8

LO-DISTRIBUTION

LO Channel	IQ-GEN EN	Phase [deg]	EN	Ph. Noise	LO Output Freq.
Channel A	■ IQ	0	□ EN_ChA	Plot	X (Update or FastSetup)
Channel B	■ IQ	0	□ EN_ChB	Plot	X (Update or FastSetup)
Channel C	■ IQ	0	□ EN_ChC	Plot	X (Update or FastSetup)
Channel D	■ IQ	0	□ EN_ChD	Plot	X (Update or FastSetup)

Figure 3.10: LMS8001 PLL-Sim - Selection on new unconfigured PLL Profile

Easy and fast way to configure settings for new PLL profile is given and briefly described in 'FAST SETUP' frame. The user should enter desired LO frequency, check if operation in integer-N mode is required, check if quadrature LO phases are necessary and press 'FastSetup of PLL Profile' button. This button calls a method which performs full algorithm which includes optimizing PLL-Core settings and defining loop dynamics in Fast-Lock mode. For more info, user is reffered to section 5.4. Fast Setup of PLL Profile 1 for LO frequency of 3.5 GHz in integer-N mode with IQ generator enabled, is presented in fig.3.11.



REFIN DEFINITION
REF Freq. [MHz] 40.0
REF FOFF Values [Hz] 1.00e+02 1.00e+03 1.00
REF Ph.Noise Values [dBc/Hz] -110.00 -138.00 -151.00
REF Noise-Floor [dBc/Hz] -156.00

FREQ-SWEEP DEFINITION
PLL Analysis Frequency Sweep Start [Hz] 1.0e3
PLL Analysis Frequency Sweep Stop [Hz] 1.0e8
PLL Analysis Frequency Sweep Steps/Dec. 40

PFD-CP CONFIG
PFD_DEL 0
ICP_PULSE [uA] 575.0
ICP_OFS [uA] 0.0
ICP_CT 16

LOOP-FILTER CONFIG
C1 [pF] 12.0
C2 [pF] 300.0
C3 [pF] 18.2
R2 [kOhm] 8.2
R3 [kOhm] 4.96666
Target Fc [kHz] 180.0
Ph. Margin [deg] 49.8

VCO CONFIG
Target VCO Freq [GHz] 7.000
VCO SEL 2
VCO FREQ 196
VCO VTUNE [V] 0.618
VCO Ph.Noise FOFF Values [Hz] 1.00e+06
VCO Ph.Noise Values [dBc/Hz] -120.84
VCO Corner Freq. [kHz] 200.0

DIVIDERS-SDM CONFIG
FFDIV-MOD 1
FBDIV-NINT 175
FBDIV-NFRAC 0
■ INT-N MODE
□ PDIV2_EN
FB-DIV Ph.Noise FOFF [Hz] 1.00e+041.00e+06
FB-DIV Ph.Noise Values [dBc/Hz] -153.77 -160.99
FB-DIV Ph.Noise Floor [dBc/Hz] -164.00

PLL STATUS
PLL Output Freq= 7.000 GHz
VCO Freq= 7.000 GHz
□ VTUNE_HIGH
□ VTUNE_LOW
■ PLL_LOCK

CLOSED-LOOP ANALYSIS SETUP
Choose Transfer Functions to Plot
■ REF-OUT ■ VCO-OUT
□ CP-OUT □ FBDIV-OUT
□ LPF-OUT □ SDM-OUT

TRANSIENT ANALYSIS SETUP
Freq. Step @ OUT [MHz] 10.0
Choose Signals to Plot
■ VCO VTUNE ■ FVCO
□ FERR □ FPLL
□ Ph.ERR

PNOISE ANALYSIS SETUP
○ GUI Values, for REF PN only
● Simulated
Plot contributions from:
■ VCO □ REF
□ LPF □ FB-DIV
■ PFD-CP ■ SDM

PLL PROFILE CONFIG
Configure PLL Profile 1

REFCLK BUFFER
□ Self-Bias Mode
□ Bypass 1st Stage

VCO-BIAS
■ Bypass VCO Reg.
VDD_VCOREG [V] 1.738

FAST SETUP
Things to do before FastSetup:
1. Choose PLL Profile to Configure
2. LO Freq [GHz] 3.5 ■ INT-N ■ IQ-GEN
3. Configure LO-DIST Network

PLL-CORE SUMMARY
■ VCO_AAC_EN
VCO_AMP 3
SWVDD [mV] 1000
VCO Freq=7.000 GHz
PLL Freq=7.000 GHz
3dB BW=299 kHz, PM=50.7 deg
Int_PN @ PLL_OUT= 0.54 deg

SDM CONFIG
□ Enable SDM Dithering
□ SDM Clock: 0(FB-DIV) or 1(REFCLK)
□ Reverse SDM Clock

FAST-LOCK MODE
Duration [us] 10.00
Enable LO Channels during Fast-Lock Mode
□ EN_ChA
□ EN_ChB
□ EN_ChC
□ EN_ChD

FAST-LOCK LPF CONFIG
C1 [pF] 12.0
C2 [pF] 300.0
C3 [pF] 18.2
R2 [kOhm] 4.1
R3 [kOhm] 2.48333

FAST-LOCK CP CONFIG
ICP_PULSE [uA] 1575.0
ICP_OFS [uA] 0.0

FAST-LOCK MODE OPTIMIZATION
Opt. Method 1
BWEF-Bandwidth Extension Factor
BWEF in Fast-Lock 2
Opt. Method 2
PLL Loop Dynamics in Fast-Lock Mode
Fast-Lock Fc [kHz] 360
Fast-Lock Ph.Margin [deg] 49.8

LO-DISTRIBUTION

LO Channel	IQ-GEN EN	Phase [deg]	EN	Ph. Noise	LO Output Freq.
Channel A	■ IQ	0	■ EN_ChA	Plot	3.500 GHz
Channel B	■ IQ	90	■ EN_ChB	Plot	3.500 GHz
Channel C	■ IQ	180	■ EN_ChC	Plot	3.500 GHz
Channel D	■ IQ	270	■ EN_ChD	Plot	3.500 GHz

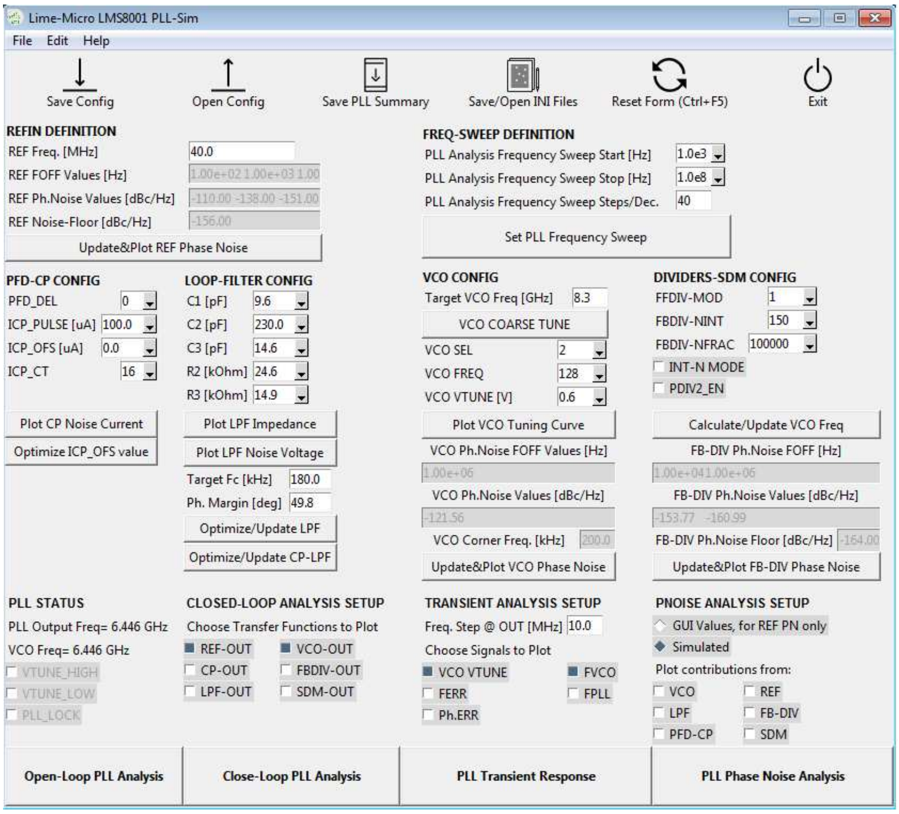
Figure 3.11: LMS8001 PLL-Sim - FastSetup of PLL Profile 1 Config

When all of the work is done, user can save the settings for configured PLL profiles in INI file. Pressing 'Save INI File' button opens File Dialog window that can be used to navigate to the location where INI file is going to be saved. This INI file can further be used to configure LMS8001 IC using *lms8suite* GUI for LMS8001 EVB control.

Chapter 4

Main Window Functions

Main window of LMS8001 PLL-Sim is shown in fig.4.1. GUI elements are logically grouped in several frames. Frames that represent PLL-Core subcircuits inside LMS8001 PLL, contain programmable parameters of subcircuits that influence the most the total PLL performance. First row of LMS8001 PLL-Sim main window contains frame for definition of reference clock frequency source and frequency offset sweep for various PLL analysis. Buttons for starting four available types of PLL analysis are placed in the last row of main window. Toolbar with most useful functions is available at the top. Some additional functions and informations are also available in the drop-down menu at the top of the main window.



REFIN DEFINITION

REF Freq. [MHz] 40.0

REF FOFF Values [Hz] 1.00e+02 1.00e+03 1.00

REF Ph.Noise Values [dBc/Hz] -110.00 -138.00 -151.00

REF Noise-Floor [dBc/Hz] -156.00

FREQ-SWEEP DEFINITION

PLL Analysis Frequency Sweep Start [Hz] 1.0e3

PLL Analysis Frequency Sweep Stop [Hz] 1.0e8

PLL Analysis Frequency Sweep Steps/Dec. 40

PFD-CP CONFIG

PFD_DEL 0

ICP_PULSE [uA] 100.0

ICP_OFS [uA] 0.0

ICP_CT 16

LOOP-FILTER CONFIG

C1 [pF] 9.6

C2 [pF] 230.0

C3 [pF] 14.6

R2 [kOhm] 24.6

R3 [kOhm] 14.9

Target Fc [kHz] 180.0

Ph. Margin [deg] 49.8

VCO CONFIG

Target VCO Freq [GHz] 8.3

VCO SEL 2

VCO FREQ 128

VCO VTUNE [V] 0.6

VCO Ph.Noise FOFF Values [Hz] 1.00e+06

VCO Ph.Noise Values [dBc/Hz] -121.56

VCO Corner Freq. [kHz] 200.0

DIVIDERS-SDM CONFIG

FFDIV-MOD 1

FBDIV-NINT 150

FBDIV-NFRAC 100000

□ INT-N MODE

□ PDIV2_EN

FB-DIV Ph.Noise FOFF [Hz] 1.00e+041.00e+06

FB-DIV Ph.Noise Values [dBc/Hz] -153.77 -160.99

FB-DIV Ph.Noise Floor [dBc/Hz] -164.00

PLL STATUS

PLL Output Freq= 6.446 GHz

VCO Freq= 6.446 GHz

□ VTUNE_HIGH

□ VTUNE_LOW

□ PLL_LOCK

CLOSED-LOOP ANALYSIS SETUP

Choose Transfer Functions to Plot

■ REF-OUT ■ VCO-OUT

□ CP-OUT □ FBDIV-OUT

□ LPF-OUT □ SDM-OUT

TRANSIENT ANALYSIS SETUP

Freq. Step @ OUT [MHz] 10.0

Choose Signals to Plot

■ VCO VTUNE ■ FVCO

□ FERR □ FPLL

□ Ph.ERR

PNOISE ANALYSIS SETUP

◇ GUI Values, for REF PN only

◆ Simulated

Plot contributions from:

□ VCO □ REF

□ LPF □ FB-DIV

□ PFD-CP □ SDM

Figure 4.1: LMS8001 PLL-Sim Main Window

4.1 Definition of Reference Frequency Source

In frame titled 'REFIN DEFINITION', the user can define the value of the input reference frequency for LMS8001 PLL. Default value for reference frequency is 40 MHz. Fields that define the phase noise performance of reference frequency source are disabled by default. Default phase noise profile is taken from the datasheet of clipped-sine wave, 40 MHz TCXO from Rakon, RTX5032A. This TCXO is used on the LMS8001 evaluation board (LMS8001 EVB). The user can enable fields for reference source phase noise definition by checking 'GUI Values, for REF PN only' checkbox inside the 'PNOISE ANALYSIS SETUP' frame in the lower right corner of main window. Field with offset frequency values and field with corresponding phase noise values should have equal number of elements separated with space characters. It is recommended to specify (frequency offset, phase noise) pairs inside the defined frequency offset sweep range.

Phase noise performance of reference frequency source can be ploted using 'Update&Plot REF Phase Noise' button.

4.2 Frequency Offset Sweep Definition

'FREQ-SWEEP DEFINITION' frame contains GUI widgets that can be used to define frequency offset sweep for PLL performance analysis. User can choose start and stop values and number of points per decade, since log-sweep can only be used. After choosing desired values, user should press 'Set PLL frequency sweep' button in order for changes to take place.

4.3 PFD-CP Settings

'PFD-CP' frame contains most important settings for PFD-CP (Phase-Frequency Detector and Charge-Pump) circuit inside PLL core of LMS8001. User can define following parameters:

- PFD-DEL - Reset path delay of PFD
- ICP_PULSE - Pulse current of CP
- ICP_OFS - Offset current of CP
- ICT_CP - CP bias current control word

User can see how different settings affect output steady-state noise current of CP around DC, by pressing 'Plot CP Noise Current' button.

Button labeled as 'Optimize ICP_OFS value' calls the function that implements simple method for calculating optimal offset current value. Offset current value is especially important in PLLs working in fractional-N mode. It was shown in practice, that CP offset current can decrease the effect of in-band phase noise folding due to CP nonlinearities in fractional-N operation mode. This effect is nonlinear and it is not modeled in LMS8001 PLL-Sim's simulations, but optimization function is implemented based on conclusions derived from practice and phase noise measurements. In integer-N operation mode, it is usually not required. Therefore, function first checks if PLL operates in integer-N mode. If so, it sets ICP_OFS field to 0. If contrary, offset current value is set to around 3% of programmed pulse current value.

4.4 Loop-Filter Settings

Third-order passive loop-filter is integrated inside the LMS8001 PLL core. All components inside loop-filter (three capacitors and two resistors) are 4-bit programmable. The schematic is shown in fig.4.2. Component values can be set using comboboxes inside 'LOOP-FILTER CONFIG' frame of main window.

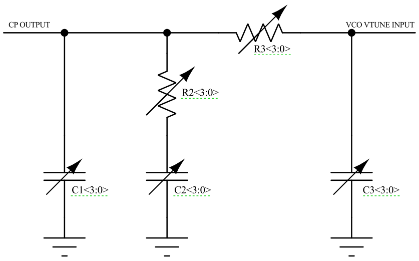


Figure 4.2: LMS8001 PLL - Loop Filter Schematic

There are options to plot loop filter impedance and output noise voltage using buttons labeled as 'Plot LPF Impedance' and 'Plot LPF Noise Voltage'. Loop-Filter component is quite important since it's configuration affects the dynamics of PLL-Core loop a lot. Therefore, two methods for optimization of loop-filter configuration are provided. Both methods take as input arguments desired open-loop crossover frequency and phase margin of the PLL loop. These two parameters user can set in text fields placed above 'Optimize/Update LPF' and 'Optimize/Update CP-LPF' buttons. These two buttons call mentioned PLL loop BW optimization methods.

- 'Optimize/Update LPF' button calls method that calculates Loop-Filter element values in order to achieve PLL loop dynamics as defined by the user, if that's possible with the chosen value for CP pulse current and VCO frequency.
- 'Optimize/Update CP-LPF' button calls method that calculates Loop-Filter element values and CP pulse current value in order to achieve PLL loop dynamics as defined by the user, if possible for a given VCO frequency. The algorithm chooses the maximum possible CP pulse current value for targeted PLL loop bandwidth that results with implementable values for Loop-Filter elements. This would lead to minimum phase noise plateau level for targeted loop bandwidth, since phase-noise of PLL in plateau region is usually inversely proportional to CP pulse current value.

Important: It's recommended to perform one of described PLL loop BW optimization methods after tuning VCO to the targeted VCO frequency. State of PLL core can be checked in 'PLL-STATUS' frame, which is placed in low-left corner of main window above 'Open-Loop PLL Analysis' button. More info is given in following sections.

4.5 VCO Settings

Most important VCO settings are provided in 'VCO CONFIG' frame. These are:

- 'VCO SEL' combobox defines active VCO core inside LMS8001 PLL. Oscillation frequency increases from core 1 to core 3.
- 'VCO FREQ' combobox defines capacitor bank configuration for selected VCO core. Oscillation frequency increases with increasing the value of 'VCO FREQ'
- 'VCO VTUNE' combobox defines tuning voltage value for selected VCO core.

Possibility to plot VCO tuning curve for given configuration is given with 'Plot VCO Tuning Curve' button. Estimated phase noise performance of VCO for given configuration can be seen

by pressing 'Update&Plot VCO Phase Noise' button. This also updates phase noise values of VCO model used in LMS8001 PLL-Sim tool that are shown in the appropriate text fields of 'VCO CONFIG' frame.
User can automatically set VCO and feedback-divider confiurations for desired VCO frequency by pressing 'VCO COARSE TUNE' button. Text field for setting target VCO frequency is placed in a row above this button. VCO coarse tuning algorithm implemented in LMS8001 PLL-Sim software, can be further defined in more details using separate window which can be called using drop-down menu sequence, Edit->Configure->VCO->Coarse Tune Algo.

4.6 Feedback and Feedforward divider settings

Feedback and feedforward divider settings are grouped inside the frame titled as 'DIVIDERS-SDM CONFIG'. The total frequency division ratio inside the feedback path of LMS8001 PLL is given with:

$$N_{DIV} = 2^{PDIV2\_EN}(FBDIV\_INT + FBDIV\_FRAC/2^{20})$$

Button labeled with 'Calculate/Update VCO Freq', when pressed, updates 'Target VCO Freq' text field with value equal to $\mathrm{N_{DIV}F_{REF}}$. Expected phase noise profile at the output of feedback-divider inside LMS8001 PLL can be ploted using 'Update&Plot FB-DIV Phase Noise'.

4.7 PLL Status Frame

Frame titled as 'PLL STATUS' is placed in the lower-left corner of LMS8001 PLL-Sim's main window, above 'Open-Loop PLL Analysis' button. 'PLL Output Freq' is the frequency at the output of feedforward frequency divider. Labels containing VCO oscillation frequency and PLL output frequency are continuously updated as the user changes VCO and feedforward divider settings inside the appropriate frames. These two frequencies are related with following equation:

$$F_{PLL} = F_{VCO}/FFDIV\_MOD$$

Checkbuttons, VTUNE_HIGH and VTUNE_LOW, are indicators that are simulating the behavior of VTUNE monitoring circuit that sets the values for these bits inside the real LMS8001 IC. 'VTUNE_HIGH' indicator is True when VCO VTUNE voltage is higher than 0.9 V. 'VTUNE_LOW' indicator is True when VCO VTUNE voltage is lower than 0.3 V. Checkbutton 'PLL_LOCK' corresponds to the real indicator generated by the analog lock detector circuit inside LMS8001 IC. 'PLL LOCK' indicator is active if calculated frequency at the output of feedback frequency divider is close enough to the specified reference frequency of the PLL.

Important: User is advised to check if 'PLL_LOCK' indicator is True before performing any type of PLL analysis and loop bandwidth optimizations. If not, user should configure VCO and Feedback-Divider for targeted PLL (VCO) frequency with 'PLL_LOCK' indicator in ON (True) state.

4.8 PLL-Core Performance Analysis

There are four types of PLL performance analysis available to the user of LMS8001 PLL-Sim tool. These are:

- Open-Loop PLL Analysis

- Close-Loop PLL Analysis
- PLL Transient Response
- PLL Phase Noise Analysis

Four buttons that can be used to run above-mentioned simulations are placed in the last row LMS8001 PLL-Sim main window. It is recommended that user, prior to starting any kind of analysis, checks if PLL is configured properly ('PLL_LOCK' checkbutton should be in True state). Above each button for starting simulation, there are usually some GUI widgets that provide to the user possibility to setup the analysis in more detail and to choose which outputs to plot.

All the simulations are based on linear models of PLL-Core subcicuits, so nonlinear effects in PLL, as for example noise folding, spurs, cycle slipping etc., are not taken into account.

4.9 Save/Open Config (*.cfg) Files

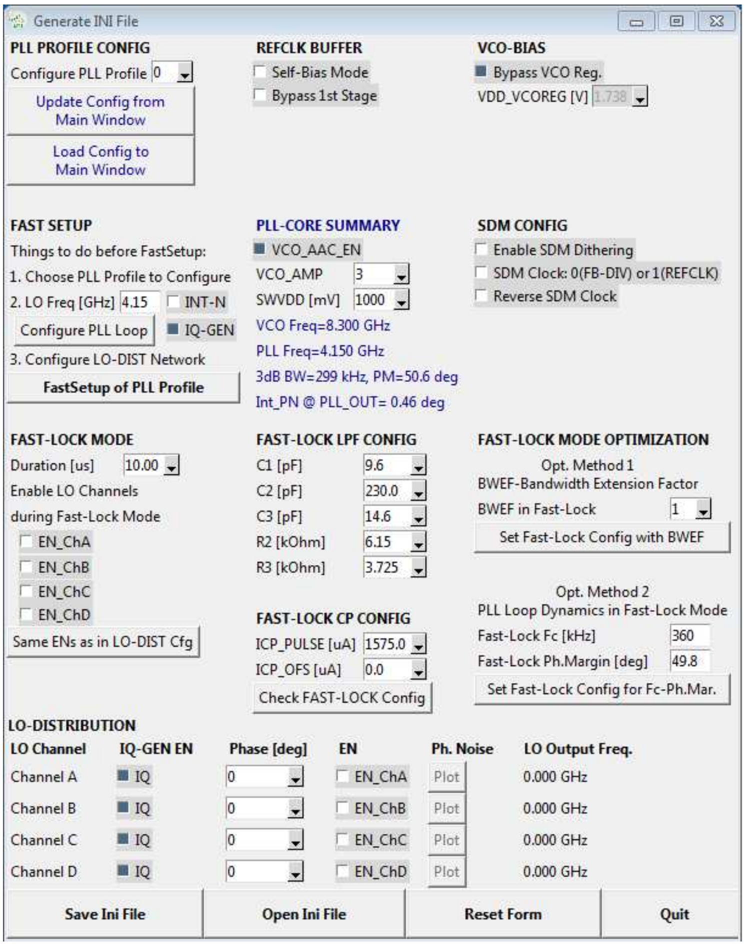
If user wants to save complete configuration of LMS8001 PLL-Sim's main window to use it again later, there is possibility to store it in a file with *.cfg extension, using 'Save Config' button in toolbar. File-Dialog window appears when this button is pressed, and the user can navigate to the location where the config file will be stored. When user wants to load specific configuration into main window, 'Open Config' toolbar button should be used.

'Open Config' and 'Save Config' functions can also be accessed from the 'File' drop-down menu at the top of the root window.

Chapter 5

Save/Open Ini File (*.ini) for LMS8001 GUI

The user of LMS8001 PLL-Sim has the possibility to generate INI files for LMS8001-EVB control software. The child window (shown in fig.5.1) for that purpose can be called from LMS8001 PLL-Sim's main window using 'Save/Open INI Files' button in toolbar or using 'Edit->Save/Open INI Files' in drop-down menu. As in the case of main window, different settings are logically grouped into several frames. The functions embedded in each frame will be described in the following sections of this chapter.



Generate INI File

PLL PROFILE CONFIG
Configure PLL Profile 0

REFCLK BUFFER
□ Self-Bias Mode
□ Bypass 1st Stage

VCO-BIAS
☒ Bypass VCO Reg.
VDD_VCOREG [V] 1.738

FAST SETUP
Things to do before FastSetup:
1. Choose PLL Profile to Configure
2. LO Freq [GHz] 4.15 □ INT-N

☒ IQ-GEN
3. Configure LO-DIST Network

PLL-CORE SUMMARY
☒ VCO_AAC_EN
VCO_AMP 3
SWVDD [mV] 1000
VCO Freq=8.300 GHz
PLL Freq=4.150 GHz
3dB BW=299 kHz, PM=50.6 deg
Int_PN @ PLL_OUT= 0.46 deg

SDM CONFIG
□ Enable SDM Dithering
□ SDM Clock: 0(FB-DIV) or 1(REFCLK)
□ Reverse SDM Clock

FAST-LOCK MODE
Duration [us] 10.00
Enable LO Channels during Fast-Lock Mode
□ EN_ChA
□ EN_ChB
□ EN_ChC
□ EN_ChD

FAST-LOCK LPF CONFIG
C1 [pF] 9.6
C2 [pF] 230.0
C3 [pF] 14.6
R2 [kOhm] 6.15
R3 [kOhm] 3.725

FAST-LOCK CP CONFIG
ICP_PULSE [uA] 1575.0
ICP_OFS [uA] 0.0

FAST-LOCK MODE OPTIMIZATION
Opt. Method 1
BWEF-Bandwidth Extension Factor
BWEF in Fast-Lock 1

Opt. Method 2
PLL Loop Dynamics in Fast-Lock Mode
Fast-Lock Fc [kHz] 360
Fast-Lock Ph.Margin [deg] 49.8

LO-DISTRIBUTION

LO Channel	IQ-GEN EN	Phase [deg]	EN	Ph. Noise	LO Output Freq.
Channel A	☒ IQ	0	□ EN_ChA	Plot	0.000 GHz
Channel B	☒ IQ	0	□ EN_ChB	Plot	0.000 GHz
Channel C	☒ IQ	0	□ EN_ChC	Plot	0.000 GHz
Channel D	☒ IQ	0	□ EN_ChD	Plot	0.000 GHz

Figure 5.1: LMS8001 PLL-Sim - Save/Open INI Files Window

5.1 Choosing the PLL Profile

LMS8001 PLL-Sim's user can choose which PLL profile of LMS8001 to configure, using combobox GUI widget inside the frame titled with 'PLL PROFILE CONFIG'. Two buttons are also available in this frame. Button 'Update Config from Main Window' copies the current settings of PLL core in main window to the memory reserved for the selected PLL Profile and adds the PLL profile to the list of configured PLL profiles. PLL Profile 0 is automatically configured on start-up. PLL-Core settings in configured PLL profiles can be loaded back to LMS8001 PLL-Sim's main window, using 'Load Config to Main Window' button.

5.2 REFCLK Buffer Settings

Settings in frame 'REFCLK BUFFER' are common for all PLL profiles and their influence is not modeled in the available PLL performance simulations in LMS8001 PLL-Sim. These settings define the configuration of reference clock buffer circtuit inside the LMS8001 IC.

5.3 VCO-BIAS Settings

Settings in frame 'VCO BIAS' are common for all PLL profiles and their influence is not modeled in available PLL performance simulations in LMS8001 PLL-Sim. These settings define the configuration of internal on-chip low-noise LDO for supplying LMS8001 VCO. When internal LDO is not bypassed, combobox that define the level of internal LDO's output voltage is activated.

5.4 FastSetup of PLL Profile

In 'FAST SETUP' frame there is brief description of several steps for fast configuration of the PLL Profile settings for the desired LO frequency. First user should choose the PLL profile that needs to be configured using combobox inside the 'PLL PROFILE CONFIG' frame.

After that, in the 'FAST SETUP' frame, there is entry widget for defining the targeted LO frequency and two checkboxes. Checkbox 'INT-N' tells to the LMS8001 PLL-Sim tool that user prefers PLL operation in integer-N mode. In integer-N mode, VCO will be configured to generate frequency equal to the integer multiple of reference frequency that is closest to the ideal value of VCO frequency in given scenario. Checkbox 'IQ-GEN' indicates that targeted LO frequency should be synthesized using the last frequency divide by 2 stage inside LO-Distribution network and that quadrature LO phases should be available for selection. User can use 'Configure PLL Loop' button to automatically configure PLL-core settings in main window for targeted LO frequency. This button when pressed does not save main window settings in the chosen PLL profile or in other words does not add the selected PLL profiles to the list of configured PLL profiles. 'Configure PLL Loop' button can be used when user wants to make sure that PLL core configuration for targeted LO frequency is OK before saving it in the selected PLL profile memory. User can save the PLL Core configuration in the memory for chosen PLL profile, by pressing the 'Update Config from Main Window' button located in the 'PLL PROFILE CONFIG' frame or by pressing 'FastSetup' button.

Configuring the PLL loop, using 'FastSetup' button, for targeted LO frequency consists of three basic steps. First step is to calculate the target VCO frequency, feedforward and feedback divider modulus words and to configure the VCO setttings to generate desired frequency (for more, see section 4.5). This calculations are based on the inputs that user provides in the

’FAST SETUP’ frame. When the first step is done, optimization of PLL core loop bandwidth is performed based on the algorithm described in section 4.4 (’Optimize/Update CP-LPF’ button method). Targeted loop dynamics specifications are taken from the designated entry elements in main window. The last step is optimization of CP offset current value which is described in section 4.3.

User can also configure the LO distribution network settings before pressing the ’FastSetup’ button. Under configuring LO distribution network, it’s meant mainly on enabling the LO channels that user wants to use and selection of desired LO signal phases for those channels (for more info, see section 5.8). This can also be done and after pressing the ’FastSetup’ button. Each action on GUI widgets available in window shown in fig. 5.1 will be automaticaly updated to the memory reserved for the selected PLL profile, if this profile is in the list of configured PLL profiles.

Pressing ’FastSetup’ button configures the PLL loop and LO distribution network for targeted LO frequency value, saves settings to the memory for the selected PLL profile and adds this profile to the list of configured PLL profiles. Beside this, ’FastSetup’ method optimizes the Fast-Lock mode configuration of the PLL loop, by choosing the BWEF value of 2 (for more, see section 5.7).

5.5 PLL Core Summary

User can find summarized performance of PLL core settings for the selected PLL Profile inside the ’PLL CORE SUMMARY’ frame. This frame is automatically updated when user change active PLL profile number in ’PLL PROFILE CONFIG’ frame. Also, in this frame, options to make more detailed configuration of VCO core for the selected PLL profile are available. For example, ’VCO_AAC_EN’ checkbutton enables/disables the automatic amplitude control of VCO core. ’VCO_AMP’ combo defines bias current value for selected VCO core. ’VDIV_SWVDD’ combo defines value of internal bias voltage for switches inside the capacitor bank of VCO core’s LC tank. These options does not affect the circuit models used in LMS8001 PLL-Sim to estimate the PLL performance for defined configuration of LMS8001 PLL.

5.6 ΣΔ Modulator Settings

Few ΣΔ modulator settings are grouped inside the ’SDM CONFIG’ frame. User can enable additional dithering in ΣΔ modulator of LMS8001 PLL to further spread the quantization noise energy, can select clock source for ΣΔ modulator circuit and inverse the polarity of clock signal. These options does not affect the circuit models used in LMS8001 PLL-Sim to estimate the PLL performance for defined configuration of LMS8001 PLL.

5.7 Fast-Lock Mode Settings

As already said, LMS8001 IC has eight separate register banks for eight different PLL profile configurations. The idea is that the user of LMS8001 IC can, prior to normal operation while performing system calibrations, configure PLL profiles intended for use, with appropriate PLL settings. Then, in normal operation mode, user can use PLL profiles and several options to make a fast selection of active PLL profile to make fast frequency jumps from channel to channel. In order to furhter improve the system settling time while jumping from one to another PLL configuration and LO frequency, the user has an option to configure Fast-Lock mode settings of PFD-CP and Loop filter circuits for each PLL profile. Fast-Lock mode should last for certain, user defined, amount of time when the PLL profile is selected, to speed-up settling time of VCO core to the new frequency. When fast-lock mode duration time expires, the PLL core loop is automaticaly switched to the PFD-CP and loop filter settings for steady state configuration.

Fast-Lock mode settings are grouped in the 'FAST-LOCK MODE' frame. In first column, user can select the duration of Fast-Lock mode for selected PLL profile in μs. Also, if user wants to enable some of LO channels during the Fast-Lock mode, four checkboxes for four LO channels can be used for that purpose. By default, all LO channels are disabled during the fast-lock mode. Button 'Same ENs as in LO-DIST Cfg' performs an action and enables same LO channels in fast-lock as in steady-state mode.

The second column provides comboboxes that user can use to manualy define settings for loop-filter elements and CP offset and pulse current values during the operation of PLL core in Fast-Lock mode. User can check the Fast-Lock mode configuration of PLL loop using 'Check FAST-LOCK Config' button. When pressed, this button generates two plots showing the comparement of close loop transfer function and VCO VTUNE settling for steady-state and fast-lock mode configurations of the PLL loop.

The last column in 'FAST-LOCK CONFIG' frame, provides the user possibility to automaticaly setup the PLL loop dynamics during the Fast-Lock operation mode. First optimization method, takes only one input argument, marked as 'BWEF' which is taken as abbreviation from 'BandWidth Extension Factor'. User can choose from designated combobox values 1,2,3 and 4 for BWEF parameter. The basic idea behind the method is to make PLL loop bandwidth in fast-lock mode BWEF times wider than that in steady-state. This can be achieved by setting the loop-filter element values and CP pulse current during the fast-lock mode using following equations:

$$FLOCK\_C_1 = C_1$$

$$FLOCK\_C_2 = C_2$$

$$FLOCK\_C_3 = C_3$$

$$FLOCK\_R_2 = R_2/BWEF$$

$$FLOCK\_R_3 = R_3/BWEF$$

$$FLOCK\_I_{CP,PULSE} = I_{CP,PULSE} \times BWEF^2$$

If some of the parameters exceed its minimum or maximum achievable value inside the LMS8001 IC, optimization method sets it to the appropriate boundary value.

The second optimization method performs same routine as in the case described in section 4.4 for 'Optimize/Update CP-LPF' button in LMS8001 PLL-Sim's main window, except that in this case, targeted PLL loop dynamics for fast-lock mode are defined using the fields above 'Set Fast-Lock Config for Fc-Ph.Mar.' button.

5.8 LO Distribution Network Settings

The 'LO-DISTRIBUTION' frame contains basic settings user can use to make a desired configuration of LO distribution network inside the LMS8001 IC. Since LMS8001 IC has four separate RF channels each driven by separate LO signal whose phase can be independently set, user of LMS8001 PLL-Sim has the option to choose the value of phase for each LO channel. For each LO channel, user can choose wheater or not quadrature phases of LO signal should be available at the output of that channel. If this option is enabled, possible LO signal phase values are 0°, 90°, 180° and 270°. Also, in that case LO frequency is two times lower than the output frequency of PLL core which enters the LO-DIST network since quadrature phases are generated using frequency divider by 2 circuit. Each LO channel can be enabled by its own checkbox defining the state of its enable signal. For enabled LO channels, user has an option to plot the estimated phase noise performance of LO signal at the output of the selected channel by pressing the appropriate 'Plot' button in this GUI block. Also, for each enabled LO channel exact value of frequency of the LO signal at the output of that LO channel is printed in the column 'LO Output Freq.' inside the 'LO-DISTRIBUTION' frame.

Chapter 6

Frequency Synthesis in LMS8001 IC

In this short chapter, two important figures are given. First, fig. 6.1, presents block diagram of PLL-Core inside LMS8001 IC, with most important constituting subcircuits and its control signals.

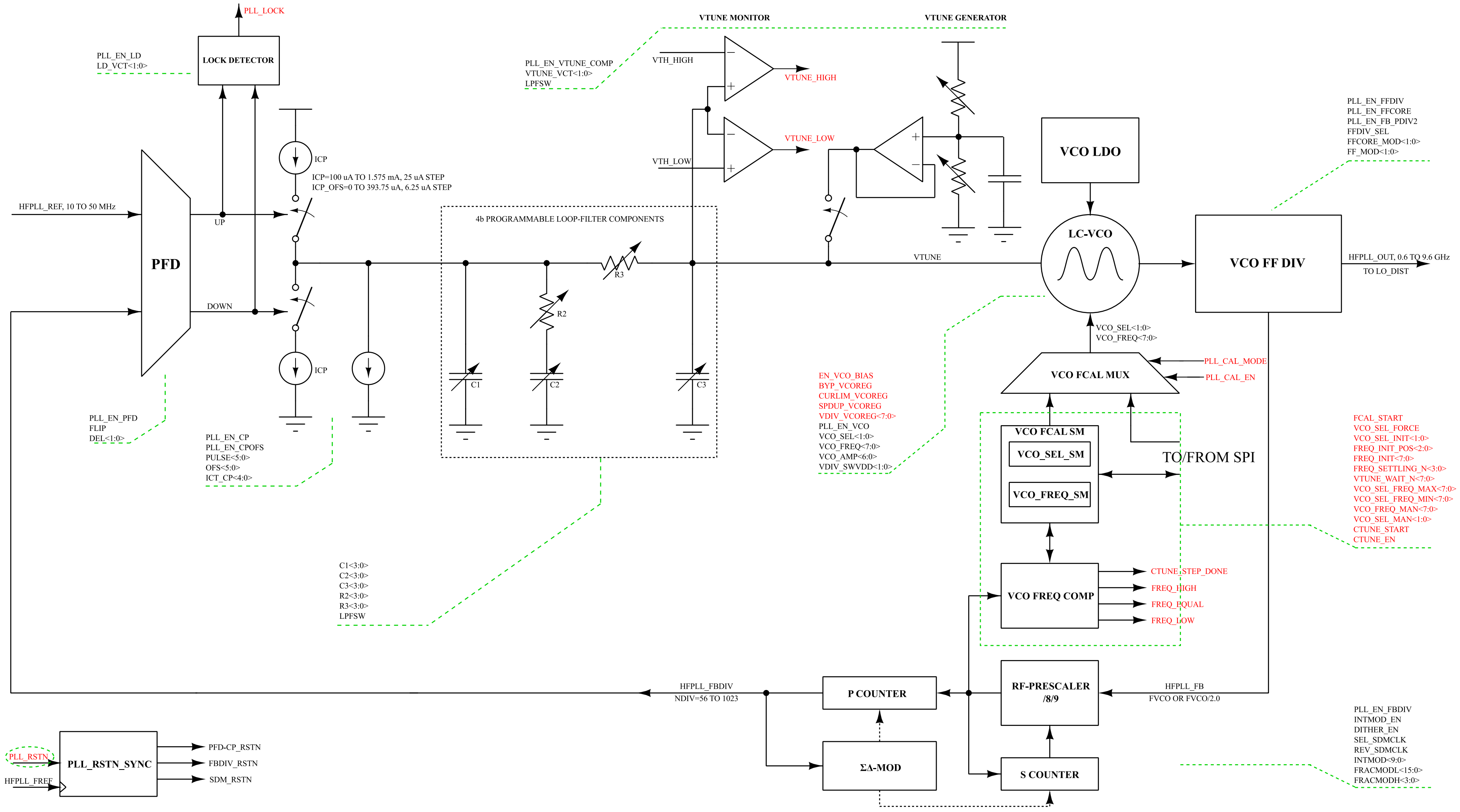


Figure 6.1: PLL Core inside LMS8001 IC

Second figure, fig. 6.2, presents LO distribution network inside the LMS8001 chip along with the digital signals for configuration of LO-DIST subsystem.

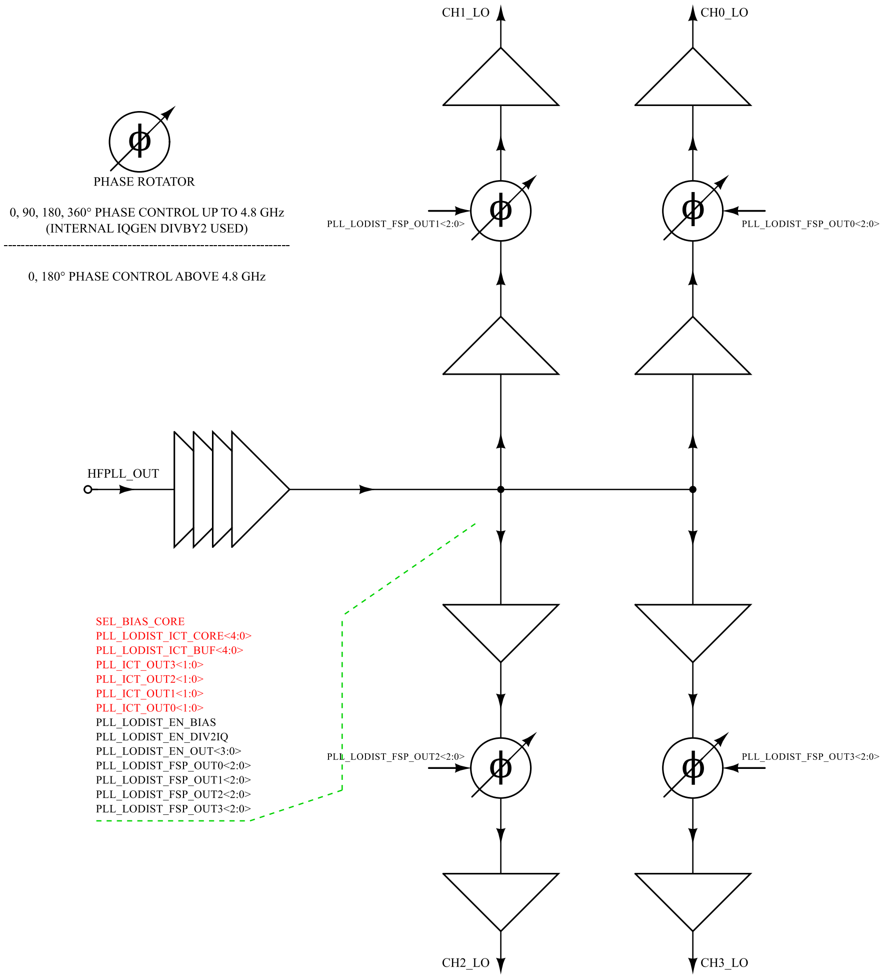


Figure 6.2: LMS8001 LO Distribution Network Block Diagram

These figures are given as a brief remainder to all users of LMS8001 IC and Lime-Micro LMS8001 PLL-Sim software tool, about the architecture of frequency synthesis subsystem inside the chip in order to better understand functions implemented in LMS8001 PLL-Sim.