Lab 2 report

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1. **Basic Questions**
2. **(Gate Level) 8-bit ripple carry adder (RCA)**
3. **(Gate Level) Decode and execute**
4. **(Gate Level) 8-bit carry-lookahead (CLA) Adder**
5. **(Gate Level) 4-bit multiplier**
6. **An exhaustive testbench design**
7. **FPGA: (Gate Level) Decode and execute**
8. **Summary**
9. **Contributions**

* **Code:**

**(Gate Level) 8-bit ripple carry adder (RCA)** by 李品萱

**(Gate Level) Decode and execute** by 李品萱

**(Gate Level) 8-bit carry-lookahead (CLA) Adder** by 唐翊雯

**(Gate Level) 4-bit multiplier** by 唐翊雯

**An exhaustive testbench design** by 唐翊雯

**FPGA: (Gate Level) Decode and execute** by李品萱

* **Report:**