5 BOOLEAN LOGIC

5.1 PURPOSE

The goal for this lab is to design circuits when given a Boolean expression. This is normally called "realizing" a circuit; that is, making a real circuit from a Boolean expression.

The *Logisim-Evolution* starter for this lab includes a `main` circuit and one subcircuit, named `Equation_1`. The starter subcircuit is used to practice creating a circuit from a Boolean expression and then a new subcircuit is added and a second Boolean expression is used to build that circuit.

5.2 PROCEDURE

5.2.1 *Subcircuit: Equation 1*

The starter circuit includes a subcircuit named `Equation_1`. Double-click that circuit in the Explorer Pane to activate it. The drawing canvas for this subcircuit is mostly blank except for a Boolean expression: $(A'BC') + (AB'C') + (ABC)$. Before starting to design a circuit, it is helpful to take a minute to analyze the expression.

- There are only three variables used in the entire expression: *A*, *B*, and *C*. Therefore, there would be three inputs into the circuit.
- There are three groups of variables and within each group the variables are joined with an `AND`. Therefore, the circuit must include three `AND` gates with three inputs for each gate.
- The three groups of variables are joined with an `OR`. Therefore, the circuit must include an `OR` gate with three inputs.
- While the expression does not name an output variable, it is reasonable to assume that the circuit would output a logic 1 or 0. Therefore, a one-bit output variable must be specified.

Start by placing three inputs and an output on the drawing canvas. Inputs are indicated by a green icon with *I->* on the tool bar above the drawing canvas. Click that tool and place three input pins named *In1A*, *In1B*, and *In1C* —that means "Input for Equation One, variable A" and so forth.

Outputs are indicated by a white icon with *->O* found on the tool bar above the drawing canvas. Click that tool and place an output named *Out1*. The circuit should look like Figure 5.1.

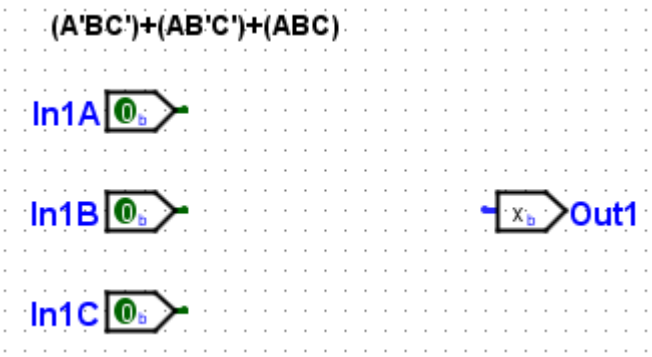

Figure 5.1: Equation 1 Inputs-Outputs

Next, the gates should be added. Place three `AND` gates on the circuit. Click each gate and in its properties panel set the *Number of Inputs* to 3.

Place an `OR` gate on the circuit. Click that gate and in its properties panel set the *Number of Inputs* to 3.

The circuit should look like Figure 5.2.

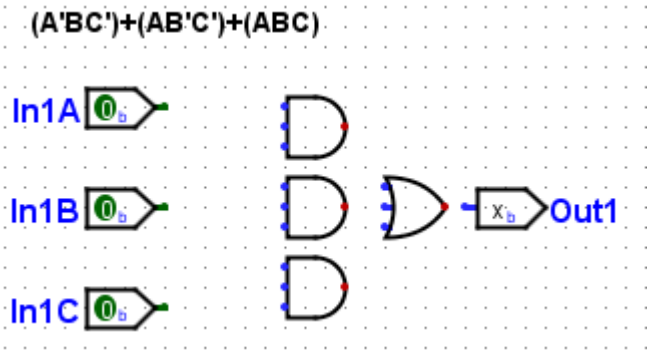

Figure 5.2: Equation 1 And-Or Gates

Next, the inputs for the `AND` gates should be set to match the Boolean expression. The top `AND` gate will match the first group of inputs, $(A'BC')$, so inputs A and C should be negated. To negate those two inputs, click the `AND` gate and in the properties panel set the *Negate* item for the top and bottom input to "Yes." When that is done, the two inputs on the `AND` gate should include a small "negate" circle.

In the same way, the middle and bottom input for the second `AND` gate should also be negated. The circuit should look like Figure 5.3.

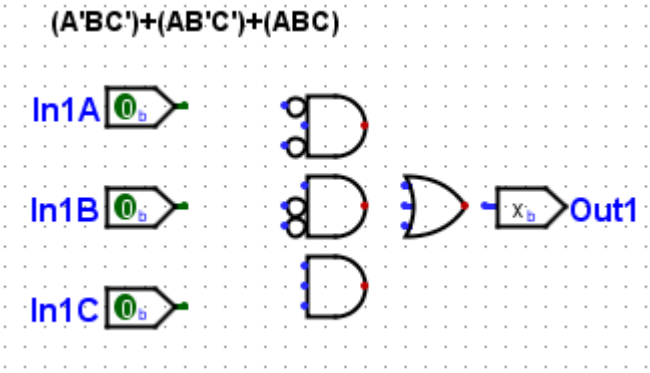

Figure 5.3: Equation 1 And Gate Inputs Set

Finally, connect all gates with wires, like Figure 5.4.

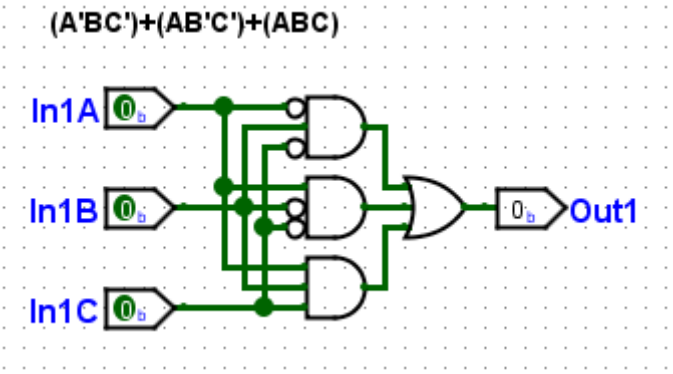

Figure 5.4: Equation 1 Circuit Completed

Test the circuit by selecting the *poke* tool in the tool bar (it looks like a pointing finger) and setting various combinations of 1 and 0 on the three inputs. The output pin should go high only when the inputs are set to $(A'BC')$, $(AB'C')$, or (ABC).

5.2.2 *Subcircuit: Equation 2*

A new subcircuit can be added to a circuit by clicking PROJECT -> ADD CIRCUIT. Name the new circuit `Equation_2`. Open the new subcircuit by double-clicking its name in the Explorer Pane.

Because this is a new subcircuit, the drawing canvas is blank. To start this subcircuit, write the equation for the circuit near the top of the drawing canvas by clicking the "A" button on the Toolbar and then clicking near the top of the drawing canvas and typing the following:

$$(A'B'CD') + (A'BCD) + (AB'CD') + (ABCD')$$

It will save time to take a few minutes and analyze the expression.

- There are only four variables used in the entire expression: *A*, *B*, *C*, and *D*. Therefore, there would be four inputs into the circuit.
- There are four groups of variables and within each group the variables are joined with an `AND`. Therefore, the circuit must include four `AND` gates with four inputs for each gate.
- The four groups of variables are joined with an `OR`. Therefore, the circuit must include an `OR` gate with four inputs.
- While the expression does not name an output variable, it is reasonable to assume that the circuit would output a logic 1 or 0. Therefore, a one-bit output variable must be specified.

Design the subcircuit using these names for the inputs: *In2A*, *In2B*, *In2C*, and *In2D*. Also include an output named *Out2*. Set the `AND` gates so the their inputs are negated properly and then wire the entire subcircuit. Finally, test the circuit to ensure the output goes high only when the four specified combinations of inputs are present.

5.2.3 *Main Circuit*

Make the `main` circuit active by double-clicking its name in the Explorer Panel. Click once on the `Equation_1` circuit and the cursor will change into an image of that circuit as it will appear on the drawing canvas. Click on the drawing canvas to drop that subcircuit. The circuit can later be moved by clicking it and dragging it to a new location. Wire the three inputs and output as shown in Figure 5.5. Notice that the input/output pins do not need to be named the same as in the subcircuit; for example, the output for `Equation_1` is labeled *Out1* but it is connected to an output pin labeled *True1*.

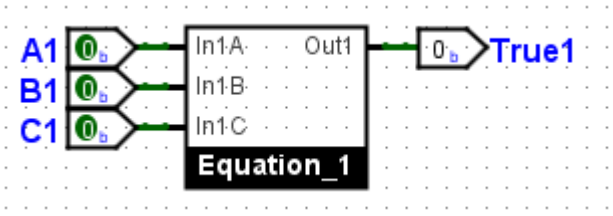

Figure 5.5: Main Circuit

Add the `Equation_2` circuit in the same way and wire four inputs and one output to that circuit. The inputs should be labeled *A2*, *B2*, *C2*, and *D2* and the output labeled *True2*.

5.3 DELIVERABLE

To receive a grade for this lab, complete the `main` circuit and both subcircuits. Be sure the standard identifying information is at the top left of the `main` circuit, similar to:

```
George Self
Lab 05: Boolean Equations
February 18, 2018
```

Save the file with this name: *`Lab05_Bool`* and submit that file for grading.

It is important to name all inputs and outputs as specified in the lab since they are checked with a Test Vector file that depends on those names.