6 PROGRAMMABLE LOGIC ARRAY

6.1 PURPOSE

This lab explores using a Programmable Logic Array (PLA) to simplify circuits that are designed for Boolean operations. A PLA is an Integrated Circuit (IC) that contains an array of `AND` and `OR` gates that can be linked in whatever way the circuit designer needs. A single PLA can replace dozens of other gates and greatly simplify circuit design.

6.2 PROCEDURE

6.2.1 *Equation One*

$$(A'BC') + (AB'C') + (ABC) \tag{6.1}$$

In Lab 5 the circuit in Figure 6.1 was developed to realize a Boolean expression.

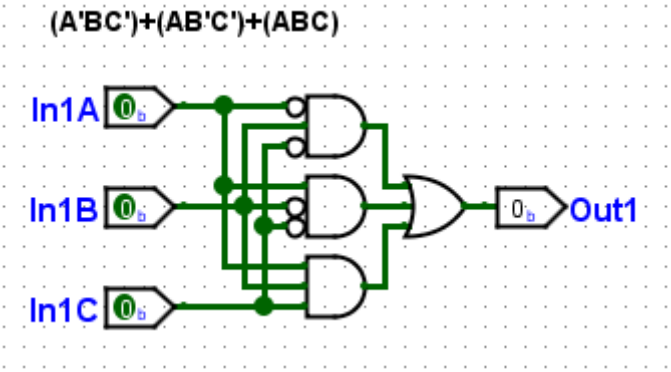

Figure 6.1: Boolean Expression Realized

This entire circuit can be realized in a single PLA saving the cost of redundant `NOT/AND/OR` gates and improving the reaction time for the circuit while reducing the heat it generates.

The *Logisim-Evolution* PLA component is a single box, as illustrated in 6.2. This PLA has a 3-bit input attached, for inputs *A*, *B*, and *C*, and a 1-bit output. The input is labeled *ABC1* to indicate this is the input for equation one.

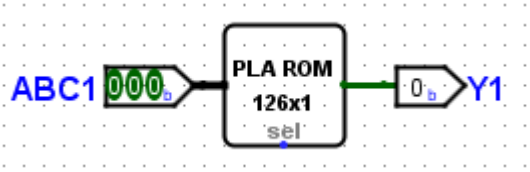

Figure 6.2: Equation One

Internally, a PLA contains a matrix of NOT/AND/OR gates that are connected by the circuit designer. Figure 6.3 illustrates the internal connections for the Equation One PLA.

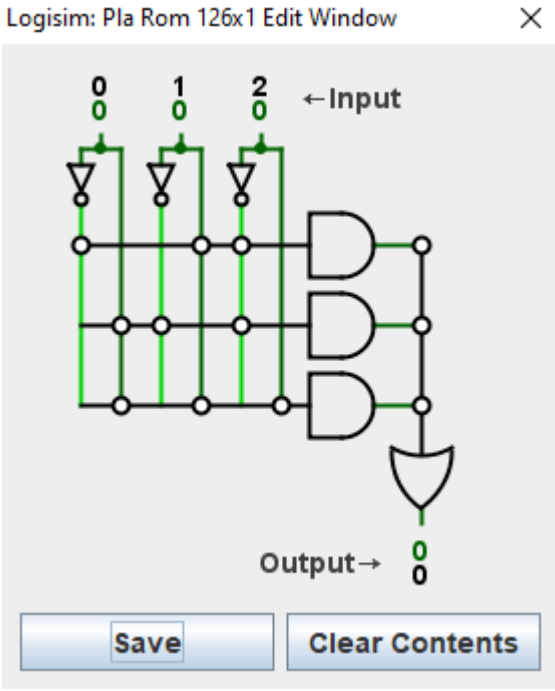

Figure 6.3: PLA Internal Connections

The three inputs are at the top of the PLA and are labeled input 0, 1, and 2. Also, the values of those inputs is indicated immediately under the input number. At this time, all three are inputting a zero.

Notice that all three inputs are split and a NOT gate is inserted in one of the two split lines. By doing this, both A and A' are available on PLA input zero.

To the right of the grid is a column of three AND gates. These gates look a bit odd since there is only one input for each gate. This, though, simply represents that the AND gate has a variable number of inputs, depending on how the designer wired the circuit. For example, the top row has three connections to the top AND gate so it is a 3-input gate. The gate sizing happens automatically within the PLA so the designer does not have to worry about it.

In the same way, there is a single OR gate near the bottom of the PLA. While the diagram indicates that the OR gate has a single input,

that gate actually has a variable input and will expand as necessary to support the circuit design. In this case, three separate rows are connected to the OR gate so it is a 3-input gate.

The very bottom of the PLA is the output. It is numbered as output zero and its current value is zero.

To wire the PLA device, the designer clicks on the wire intersections to place a connector (the small circle). Thus, row one of this device is connecting A', B, and C' to the top AND gate, which is then connected to the output OR gate.

Inspecting the connections for each row in this device should reveal that the top row is $(A'BC')$, the second row is $(AB'C')$ and the third row is (ABC), which are the three gates in the Boolean expression. The outputs from all three of those gates goes through an OR gate to the output.

Thus, this one PLA replaces all of the circuitry found in Figure 6.1.

Before moving on to the second equation, it will be helpful to take a look at the properties for a PLA.

VHDL	Verilog
Number Of Inputs	3
PlaANDAttr	3
PlaOutputsAttr	1
Label	
Label Font	SansSerif Bold 16
Label Visible	Yes
Contents	(click to edit)
ramSelAttr	Low Level

Figure 6.4: PLA Properties

The first property sets the number of inputs for the PLA, the second property, *PalANDAttr*, sets the number of AND gates and the third property, *PlaOutputsAttr*, sets the number of outputs. These three properties ensure that the PLA device can be used for many different applications. The three label properties are the same as found in most *Logisim-Evolution* components. Clicking the *Contents* property will open the PLA editor as illustrated in Figure 6.3[1]. Finally, the *ramSelAttr* determines whether the *Select* port, on the south edge of the PLA is enabled on a high or low signal. The enable port is not used in this lab.

1 Important! The *Logisim-Evolution* PLA seems to have a minor bug and the Contents editor will not always open. However, if the *ramSelAttr* is clicked so its drop-down list is visible then the Contents *(click to edit)* link will function properly. This is odd, but it will hopefully be corrected in a future iteration of *Logisim-Evolution* .

6.2.2 *Equation Two*

$$(BCD') + (A'B'C) + (A'BCD') + (ABCD) \tag{6.2}$$

The subcircuit for Equation Two is very similar to that for Equation One, but the PLA has different internal connections.

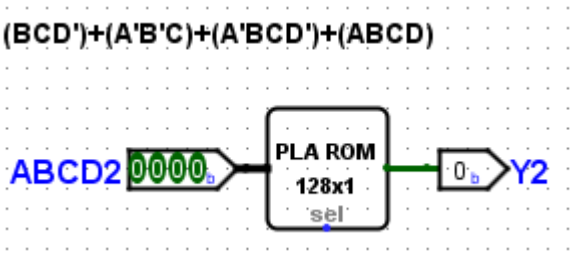

Figure 6.5: Equation Two

Notice that the input has four bits since the equation includes inputs *A*, *B*, *C*, and *D*. Also, the inputs and outputs include the number 2 to differentiate this subcircuit from the others.

When building this subcircuit be sure to use a PLA device from the library instead of copy/paste from the subcircuit for Equation One. The internal connections for Equation Two are illustrated in Figure 6.6.

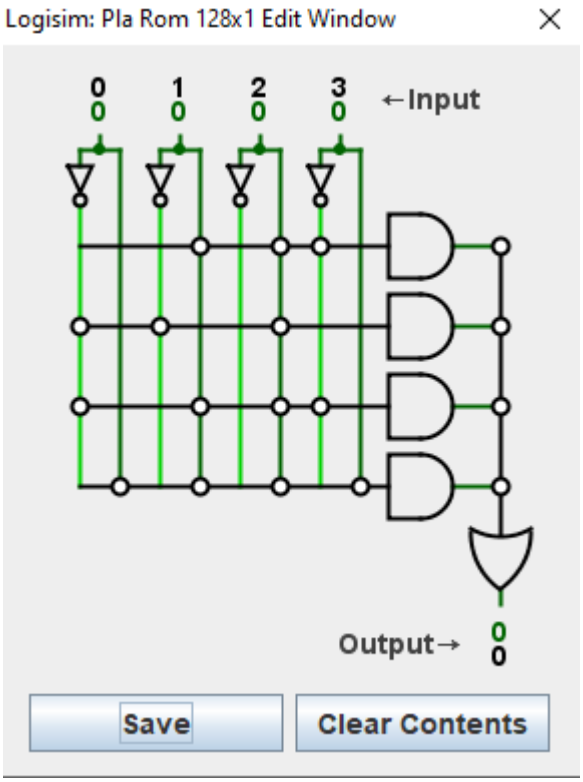

Figure 6.6: Connections for Equation Two

Notice that this equation includes two terms that have only three variables instead of four: (BCD′) and (A′B′C). It does not cause a problem when a term in incomplete, only the variables present in the term are connected and the missing variable is ignored.

6.2.3 *Equation Three*

$$(A'BC') + (AB'C') + (ABC) \qquad (6.3)$$
$$(A'B'CD') + (A'BCD) + (AB'CD') + (ABCD')$$

The subcircuit for Equation Three is very similar to that for Equation Two, but the PLA has different internal connections.

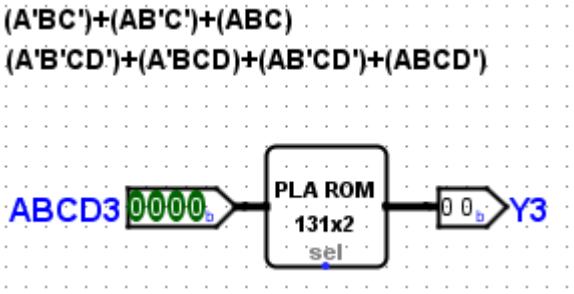

Figure 6.7: Equation Three

The major difference in Equation Three is that there are two outputs, so the PLA must have two outputs specified and each equation is connected to the correct output.

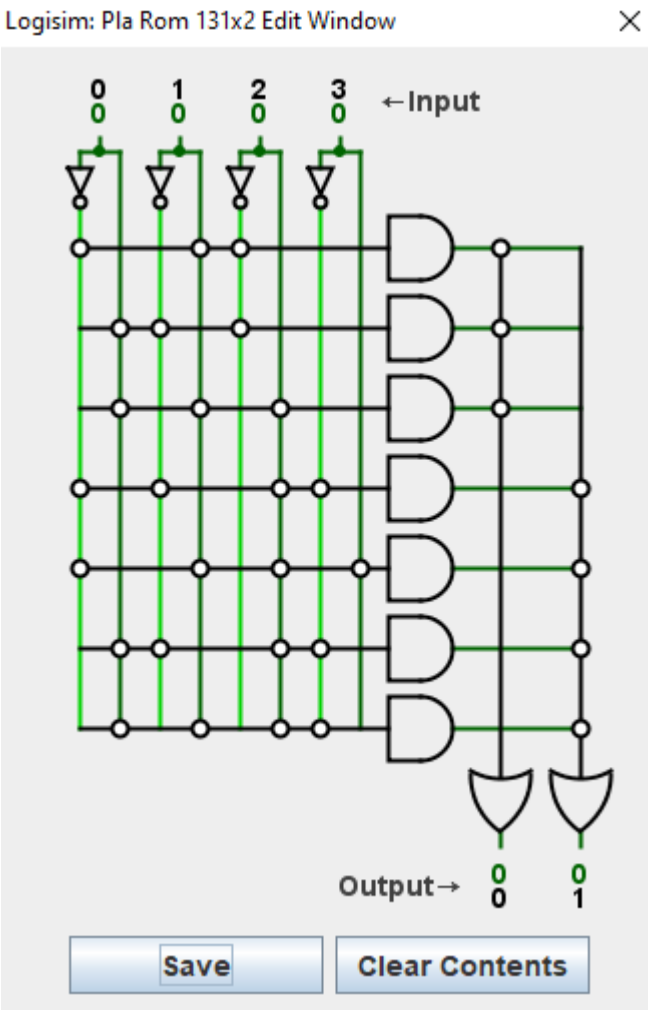

Figure 6.8: Connections for Equation Three

6.3 CHALLENGE

On the `main` circuit, wire a PLA device using the same procedure that was used for circuits one, two, and three. That PLA should display the correct outputs for equations 6.4.

$$(A'BC) + (ABC'D) + (A'B'CD) \tag{6.4}$$
$$(BCD') + (A'B'C) + (A'BCD') + (ABCD)$$

The main circuit can be tested with the test vector provided with the lab starter circuit.

6.4 DELIVERABLE

To receive a grade for this lab, complete the circuit. Be sure the standard identifying information is at the top left of the `main` circuit, similar to:

```
George Self
Lab 06: PLA
September 17, 2019
```

Save the file with this name: *Lab06_PLA* and submit that file for grading.