4 LOGIC OPERATIONS

4.1 PURPOSE

This lab develops a logic unit that includes eight different logic functions using *Logisim-Evolution* library components. This device will eventually be used as part of the Arithmetic Logic Unit (ALU) in Lab 8. This device will have two inputs, labeled *A* and *B*, and will output the following logic values.

1. AB
2. $(AB)'$
3. $A + B$
4. $(A + B)'$
5. AXorB
6. AB'
7. $A + B'$
8. A'

4.2 PROCEDURE

This circuit is very similar to the arithmetic circuit developed in Lab 3. However, the logic circuit is much simpler than the arithmetic circuit since there is not carry in/out bit and no comparator output.

To complete the lab, start a new circuit in *Logisim-Evolution* and create a subcircuit named `logic`. Place appropriate devices from the *Gates* library in the `logic` subcircuit such that it can produce the required output. Connect each of the devices to inputs *A* and *B* and then wire the outputs from each device to *LoOut* through a multiplexer. The exact design of the `logic` subcircuit is left to the student.

> Tip: the value *(AB)'* is a `NAND` gate and $(A + B)'$ is a `NOR` gate. To negate input *B* for AB' set the *Negate* property in the properties panel for the `AND` gate to "Yes." When that is done, the *B* input on the `AND` gate should include a small "negate" circle.

Drop the logic subcircuit on the main circuit and wire the various inputs and outputs, as shown in Figure 4.1.

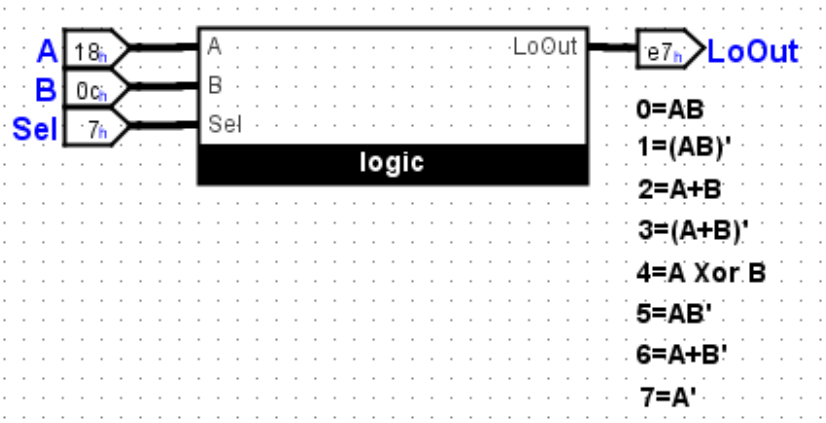

Figure 4.1: The Main Logic Circuit

The circuit can be tested by using the *poke* tool and entering various inputs and then checking to see that the output is correct. A test vector file has been provided for this lab so all of the logic functions can be exercised.

As a last step, the main circuit must be renamed since this circuit will be reused in Lab 8. Click one time on the main circuit to activate it and in the properties panel change its label to logic_main.

4.3 DELIVERABLE

To receive a grade for this lab, complete the circuit. Be sure the standard identifying information is at the top left of the logic_main circuit, similar to:

```
George Self
Lab 04: Logic Operations
September 17, 2019
```

Save the file with this name: *Lab04_Logic* and submit that file for grading.