Class	CS147, Sec 01
Homework	I
Due Date	Feb 23, 2017 11:59 PM PST

Instructions

1. There are 10 questions with total 10 points. Each question carries 1 point.
2. Please create electronic document with your answer.
3. There is no need to include the question itself. However, you **MUST** include question number and sub-part index if any. Example: 9(b)
4. Please create a PDF document **hw1.pdf** and ***upload that in Canvas*** assignment page by the due date.
5. **NO** handwritten + scanned document is accepted.
6. **NO LATE SUBMISSION.**

1. Convert the following 'CS147DV' assembly instructions in 'Result Table' into corresponding machine code. Show the operation performed (e.g. r3 = r8 + 0xFFFF92AB for an I-type instruction) by the instruction. Assume 'don't care' value is all 0. Fill out all the required information of each instructions in 'Calculation Table' . Put 'N/A' if some field is not applicable for that particular type of instruction.

Table 1.1: Result Table

Code	Binary	Hex	Operation
muli r6, r3, 0x8FA7			
add r3, r3, r1			
nor r2, r3, r5			
jal 0x34F832			

Table 1.2: Calculation Table

Code	Type	RS	RT	RD	SHAMT	FUNCT	IMM	ADDR
muli r6, r3, 0x8FA7	I							
add r3, r3, r1	R							
nor r2, r3, r5	R							
jal 0x34F832	J							

2. The following assembly program is written using 'CS147DV' instruction set. Once converted into machine code by assembler, the code is loaded into the memory from address 0x00001000. What is the memory content from start address after loading the program? Assume that the memory is 'word' (32-bit) addressable memory. Also assume that before loading content of entire memory and registers were all 0 except from address 0x01008000 on wards, which contains array of numbers (in decimal) as following – 10, 11, 12, 13, 14, 15, 16, 17, 18, 19. Also program counter (PC) is initialized with 0x00001000. Also write down all the dynamic data memory locations (includes stack and heap) with non-zero content once processor completes execution of the last instruction in the program (you may or may not need all the rows in the Data address column).

Table 2.1: Machine code and execution result table

Code	Program Address	Content	Data Address	Content
`addi r0, r0, 0x1008`	0x0000 1000			
`sll r0, r0, 0xC`	0x0000 1001			
`addi r2, r2, 0x9`				
`LOOP: beq r1, r2, END`	0x0000 1002			

`lw r3, r0, 0x0`
`lw r4, r0, 0x1`
`add r5, r3, r4`
`sw r5, r0, 0x0`
`addi r0, r0, 0x1`
`addi r1, r1, 0x1`
`jmp LOOP`
`END: sw r5, r0, 0x0`
	0x0000 1003			

	0x0000 1004			
	0x0000 1005			
	0x0000 1006			
	0x0000 1007			
	0x0000 1008			
	0x0000 1009			
	0x0000 100A			
	0x0000 100B			
	0x0000 100C			
	0x0000 100D			
	0x0000 100E			
	0x0000 100F			
	0x0000 1010			
	0x0000 1011			

3. A small 12-bit synchronous computer (uses clock signal to synchronize operation) system has 4K word (12-bit consists of an word) addressable memory and 16 registers. It supports 24 mathematical operations which include only binary operators. All the storage element (memory and registers) has reset pin to reset the stored data to 0x0.

   The memory supports read and write operation and uses common data bus for taking in data for write operation and giving out data for read operation. If 'read' and 'write' are OFF or ON at the same time, the data bus goes in circuit isolation state or HighZ state. It performs read operation if 'read' is ON (logic high or 1) and 'write' is OFF (logic low or 0). Similarly it performs write operation if 'write' is ON (logic high or 1) and 'read' is OFF (logic low or 0). All the memory operations are done in positive edge of the clock and both read and write takes 2 clock cycle to complete.

   Draw complete schematic diagram of the input-output connection of the proposed computer involving memory, ALU, register file and control unit.

4. Suppose that the computer described on #3 runs on a clock with 2.5GHz clock with 40% duty cycle. The rise and fall time of the clock is 10ps. The memory used in the design takes 2 clock cycle time to complete a write and 1 clock cycle to complete a read operation. Draw the timing diagram of the memory for one read followed by one write operation at address 0x23EA8 (You do not need to show the rise time and fall time of the clock signal in the clock signal diagram). Also answer the following questions.

   (a) What is the Time period of this clock in picosecond unit?

   (b) How much time in picosecond unit the clock signal is at logic low?

5. Fill in the empty slots in the table by converting numbers into different representations. All numbers are 8 bits in length. Use 2's compliment representation in binary and hexadecimal numbers.

Binary	Hex	Octal	Unsigned Decimal	Signed Decimal
1101 0011				
		213		
	AF			
				-83

6. Using 2's complement binary arithmetic
   (a) Convert numbers a = 6_{10} and b = -4_{10} into 4-bit two's compliment binaries.
   (b) Perform (i) zero-extension and (ii) sign-extension of numbers a and b to get 8-bit binaries. You should report 4 numbers.

7. Derive truth tables for the following Boolean functions.

   (a) F(x, y, z) = x'y + z

   (b) F(x, y, z) = (xyz') + (x'y'z)

8. Prove by Boolean algebraic manipulation that the following expressions are valid.

   (a) a+b+ (ab)' = 1

   (b) w'.(wxyz)' = w'

9. Using K-Map technique perform the following.
   (a) Simplify the following function:

   f (A, B, C, D) = ΠM(1, 3, 12, 13)

   Show all the "prime-implicants" and "Essential prime implicants"

   (b) Find a minimum SOP expression for:

   f (w, x, y, z) = ∑ m (5, 7, 12, 14) + d(0, 2, 13, 15)

   Show all the "prime-implicants" and "Essential prime implicants"

10. Design and implement a digital circuit which takes decimal values in range [-7,7] in form of 4-bit 2's complement binary and output negative of that value as 4-bit 2's complement binary. For example if input is 4, output is -4. Similarly if input is -6, output is 6. Show every steps in that design process (e.g. truth table generation, SOP equation formation, K-map reduction (and further reduction using Boolean identity if any), optimized logic equation formation). Draw the logic schematic diagram of this logic circuit.