Time		10 ns	20 ns	30 ns	40 ns	50 ns
clk						
set						
sig_in0[3:0]	1010					
sig_out0[3:0]	xxxx	1010	0101	1010	1101	0110
sig_in1[3:0]	0011					
sig_out1[3:0]	xxxx	0011	1001	0100	1010	1101
sig_in2[3:0]	1000					
sig_out2[3:0]	xxxx	1000	0100	0010	0001	1000
sig_in3[3:0]	0110					
sig_out3[3:0]	xxxx	0110	0011	1001	0100	1010
sig_in4[3:0]	0010					
sig_out4[3:0]	xxxx	0010	0001	1000	1100	1110