Homework 3

Andrei Tumbar

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a)

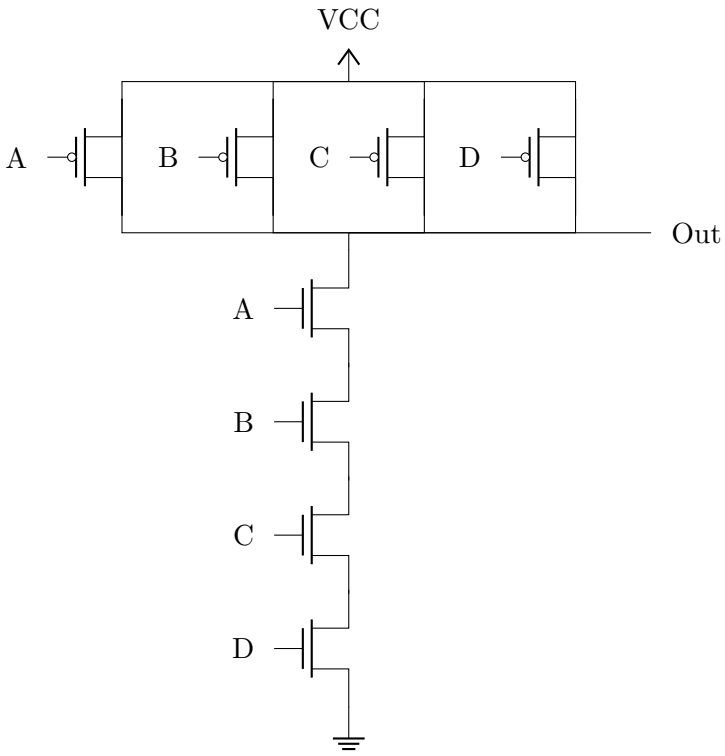

Figure 1: Four-input NAND gate

b)

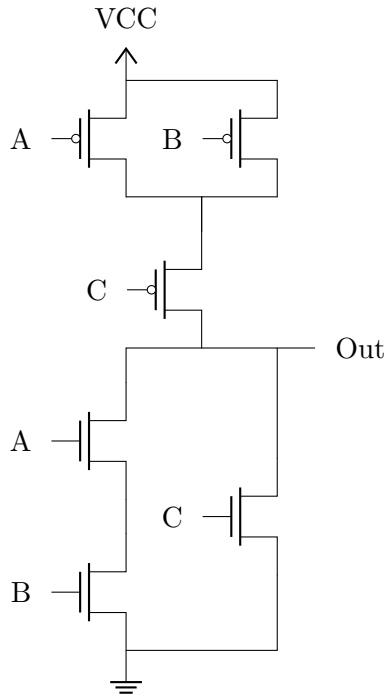

Figure 2: Three-input OR-AND-INVERT gate

c)

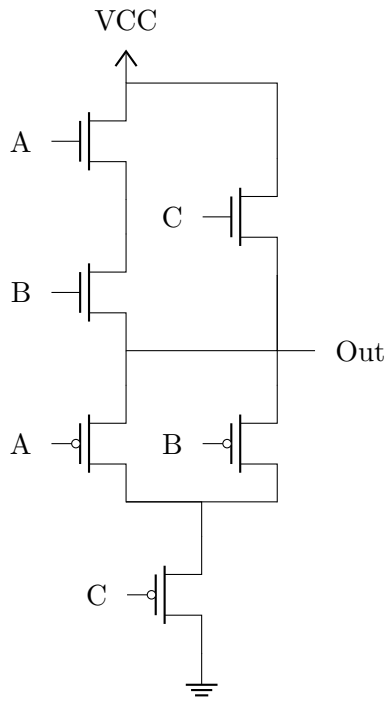

Figure 3: Three input AND-OR gate

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Sketch a transistor-level circuit for the following CMOS gates. Use the minimum number of transistors.

a)

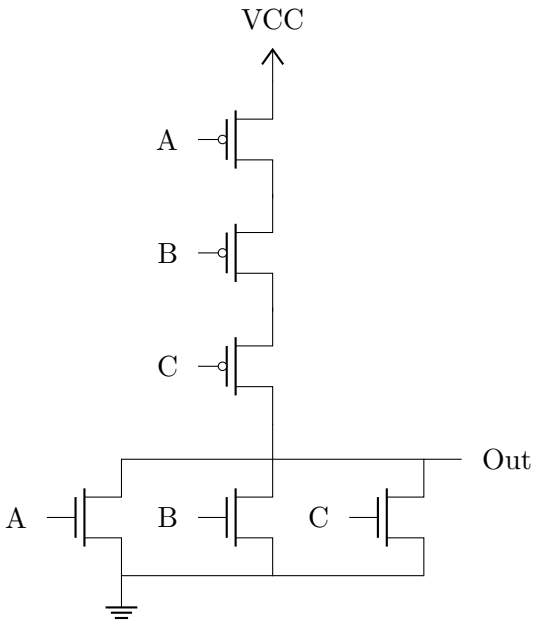

Figure 4: Three-input NOR gate.

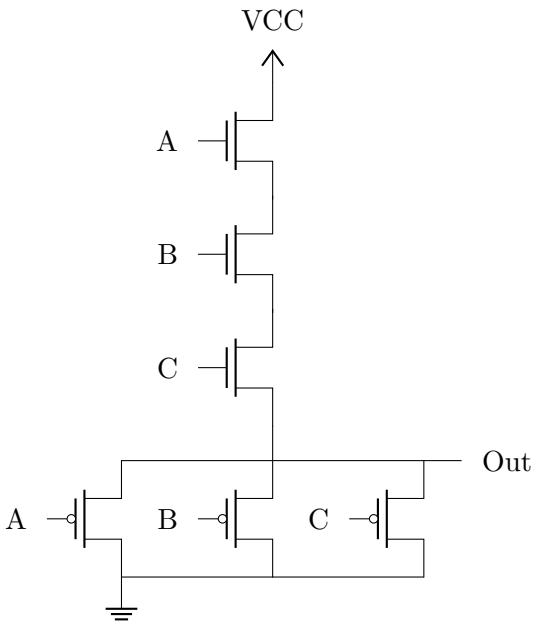

Figure 5: Three-input AND gate

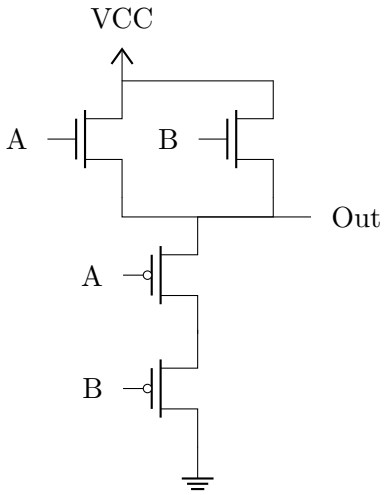

Figure 6: Two-input OR gate

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Table 1: Truth table for Figure 1.50

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

This is an XOR gate.

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Table 2: Truth table for equation 1

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Interview Question

Sketch a transistor-level circuit for a CMOS four-input NOR gate.

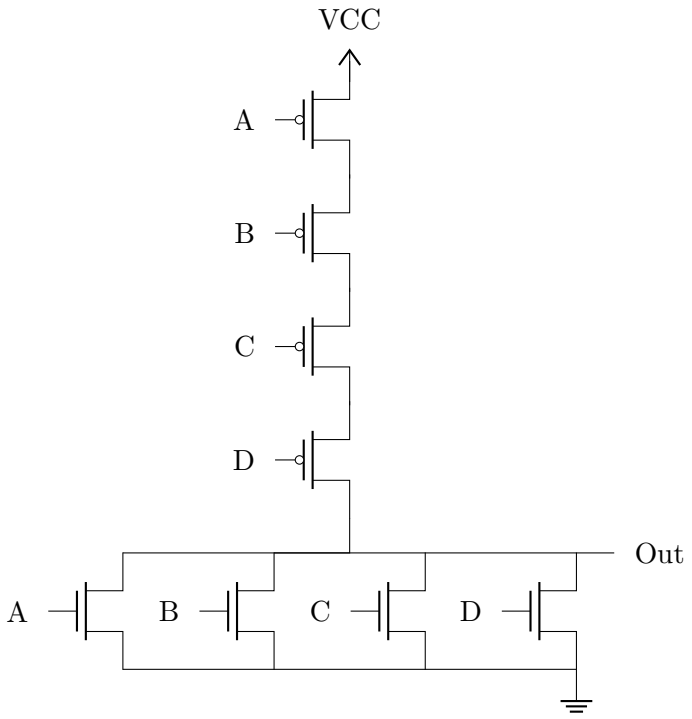

Figure 7: Four-input NOR gate