CMPE 260 Laboratory Exercise 7

Project 2 - Processor Timing

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Performed: May 1st
Submitted: May 3rd

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Your Signature: _____

Introduction

A flip-flop needs a certain amount of time before and after the active clock edge where the input signal must be stable. If the signal is not stable during this period of time the state of the flip-flop may become metastable where the input could be either `0` or `1`. The time before the clock edge where the signal must stay constant is called the setup time whereas the time after the clock edge is called the hold time. Violating these two times is usually caused by propagation delays and contamination delays in the logic between flip-flops. The hold time on a flip-flop is usually designed to be near zero so that the circuit designer need not worry about too little logic between registers. The contamination delay on the Baysis 3 board is longer than the hold time meaning that a hold time violation cannot be obtained. The setup time, however, can be violated. If the clock period is too short and the propagation delay in the logic is too high, the setup time will be violated.

Results

To test the clocking limits of the MIPS processor, repeatedly incrementing the clock frequency by 5Mhz was implemented. The starting frequency was 10 MHz.

A table of results was generated to show the success and failure during testing of each clock frequency.

Table 1: Results of MIPS Processor at different clock frequencies

Frequency (MHz)	Result
10	Pass
15	Pass
20	Pass
25	Pass
30	Pass
35	Pass
40	Pass
45	Pass
50	Fail

A post-implementation timing waveform was generated for each of the tested frequencies. The Part A test from Project 1 was used to verify all instruction types.

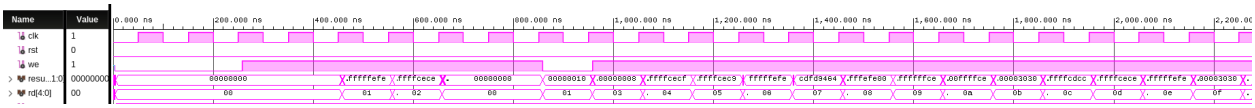

Figure 1: Timing simulation at 10Mhz - Pass

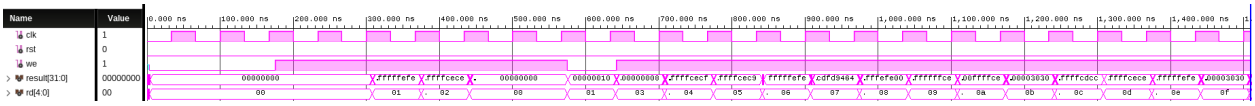

Figure 2: Timing simulation at 15Mhz - Pass

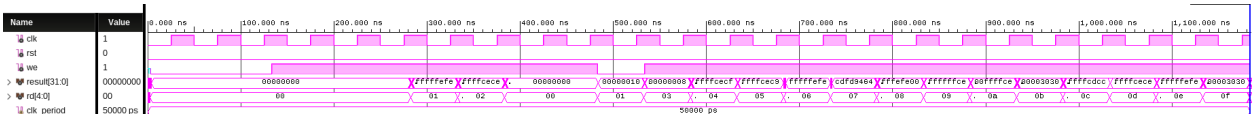

Figure 3: Timing simulation at 20Mhz - Pass

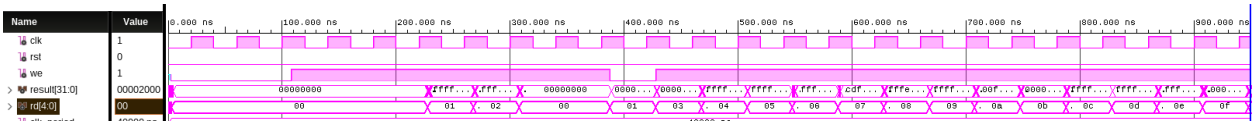

Figure 4: Timing simulation at 25Mhz - Pass

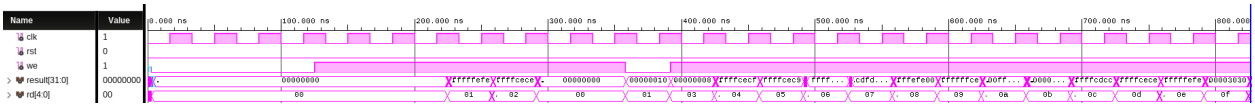

Figure 5: Timing simulation at 30Mhz - Pass

Figure 6: Timing simulation at 35Mhz - Pass

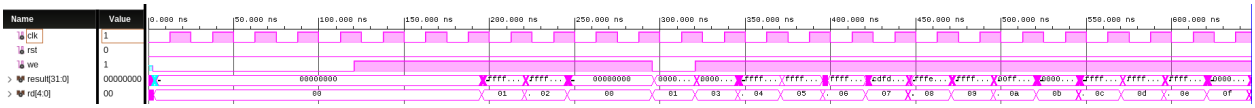

Figure 7: Timing simulation at 40Mhz - Pass

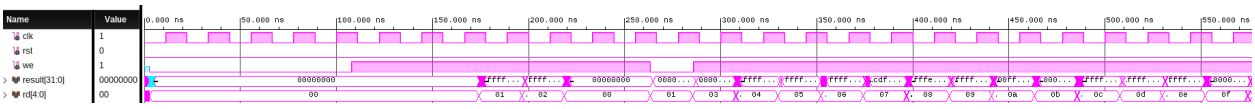

Figure 8: Timing simulation at 45Mhz - Pass

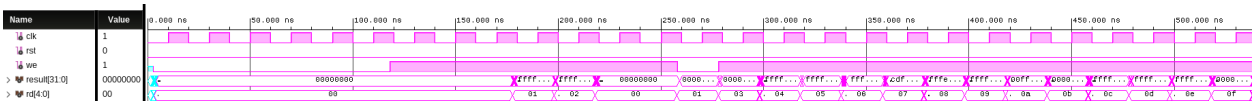

Figure 9: Timing simulation at 50Mhz - Fail