Homework 11

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Exercise 34

a

The critical path on this circuit is from A or B on the first adder to C_{out} followed by C_{in} to S on the second adder. The propagation delay of the flip-flops as well as their hold times are also taken into account.

$$\begin{aligned} T_c &= 35 + 30 + 25 + 20 \\ &= 35ps + 25ps + 20ps + 10ps = 110ps \\ F &= 9.09GHz \end{aligned}$$

b

$$\begin{aligned} T_c &= 35 + 30 + 25 + 20 + t_{skew} \\ 1/8GHz &= 125ps \\ t_{skew} &= 125ps - 110ps = 15ps \end{aligned}$$

b

The flip flops have a minimum hold time of 10ps. The earliest the output can begin to change is the sum of the FF_{cd} and the $Adder_{min-cd}$ which is:

$$CD_{min} = 21ps + 15ps = 35ps$$

Therefore the max skew for a holdtime violation is:

$$Skew_{max} = 35ps - 10ps = 25ps$$

Exercise 35

a

$$\begin{aligned} 40MHz &= 25ns \\ 25ns &= 0.61x + 0.72ns + 0.53ns \\ x &= 38.93 = 38CLBs \end{aligned}$$

b

The hold time is 0ns so the maximum clock skew is the clock period of 25ns.

Exercise 40

Given that the metastablity detector M has a low enough propagation time, this circuit would never produce a metastable result. This setup time would need to be low enough to satify this equation:

$$T_c \geq FF_{setup} + 2 * FF_{prop} + M_{prop}$$

The FF propagation time must be multiplied by 2 so that the D2 signal has time to reset when the metastable detector asynchronously resets the first flip-flop.