Homework 7

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Problem 9

Create a circuit that outputs 1 if four consecutive inputs are equal.

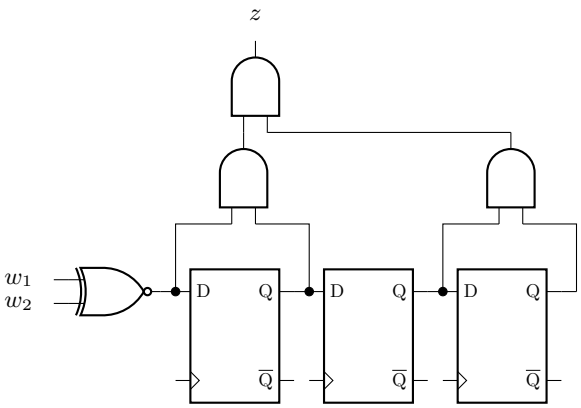

Figure 1: Circuit which compares two numbers and outputs a 1 if they are equal for four consecutive clocks.

The comparison is done via a `XNOR` gate which will output a 1 if the two inputs are equal. The previous 3 comparisons will be held in the D-flip-flop. All of the previous comparisons as well as the current comparison must be true in order to produce a high output.

Problem 10

(See VHDL file)

Exercise 22

This FSM will output a `1` if the sequence `AB` is seen in the input. It will always output `0` otherwise.

Table 1: State-transistion and output table

Input	State	Next State	Output
A	`00`	`01`	`0`
$\bar{A}$	`00`	`00`	`0`
B	`01`	`10`	`0`
$\bar{B}$	`01`	`00`	`0`
	`10`	`00`	`1`

AB \ Q_1Q_0	00	01	11	10
00	0	0	0	0
01	0	1	0	0
11	0	1	0	0
10	0	0	0	0

(a) K-map for $Q_1{}'$

AB \ Q_1Q_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	0	0	0
10	1	0	0	0

(b) K-map for $Q_0{}'$

Figure 2: K-Map for Exercise-22 state machine

$$Y = Q_1\overline{Q_0}$$
$$Q_1{}' = \overline{Q_1}Q_0B$$
$$Q_0{}' = \overline{Q_0}\overline{Q_0}A$$