CMPE 460 Laboratory Exercise 8

Heartbeat Monitor

Andrei Tumbar
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Lab Section: 2
Instructor: Beato
TA: Xavier Brooks
Diana Yakobchuk
Charles Poliwoda

Lecture Section: 1
Professor: Beato

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Abstract

In this laboratory exercise a simple heartbeat monitor circuit was modeled and constructed on a breadboard. The heartbeat monitor operated on a signal from an optoisolator circuit or a signal generator mimicking this sensor. The purpose of the circuit was to filter a desired signal from a noisy input. Choosing the appropriate frequency ranges to filter out of an input signal with the goal of sending a measurable analog signal to the MSP432 microcontroller. Finally a PCB was designed and laid out as well as an order made to a manufacturer.

Design Methodology

The heart rate monitor circuit is able to measure a low frequency periodic signal in the presence of noise. An optoisolator circuit is used to detect a heart beat in the neck or wrist. Small variations in the reflection of light against the OBP745 can be detected in the generated signal of the optoisolator.

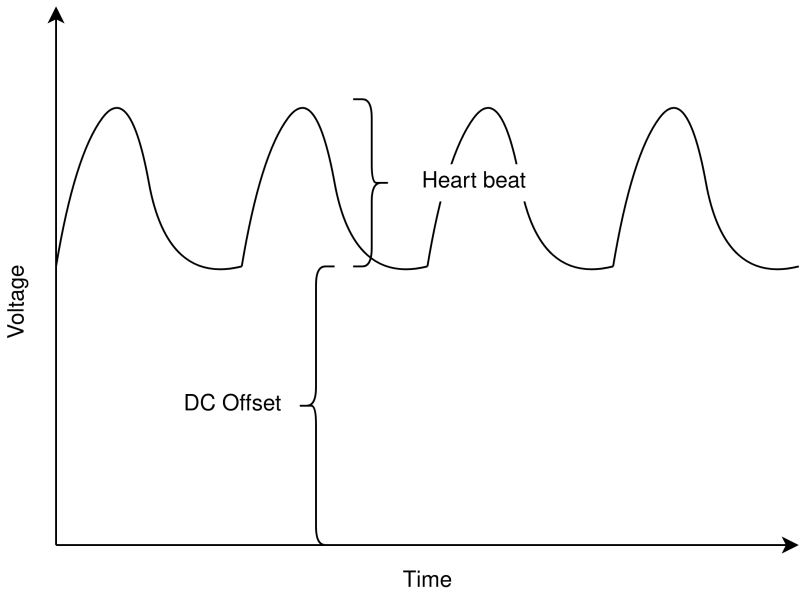

Figure 1: Example heartbeat signal from an optoisolator circuit.

Figure 1 shows an example of the signal generated by an optoisolator circuit if it were to be held up to the neck or wrist. Notice that the signal has a DC offset which comes from the fact that the heart beat signal will only vary the base voltage being output from the optoisolator. Figure 1 also does not show the noise from the optoisolator which would show up as higher frequency signals. High amount of noise will make the signal undetectable if it were directly fed into the microcontroller. Another challenge from the raw signal of the optoisolator is the amplitude of the wave itself. At an amplitude of about 35 mV, the signal is very

difficult to detect on the microcontroller which accepts signals from 0 V to its 2.5 V reference.

All of these problems may be solved by filtering the signal generated by the optoisolator. The DC offset is in fact a 0 Hz signal and may be filtered out with a high-pass filter. The signal after a high pass filter with a relatively small cut-off frequency will look similar to the signal shown in Figure 1, however it will not include the DC offset. The next issue is static noise. Static noise can be characterized as a signal with constant magnitude across all frequencies. Because our desired signal is of relatively low frequency when comparing the the frequency spectrum of static noise, the higher frequency noise will cause the signal to appear "fuzzy". To filter out this feature from the signal, a low-pass filter may be used. Choosing the correct cut-off frequencies for both the low-pass and the high-pass is key in designing the heartbeat monitor circuit.

Low pass filter

While the average beats-per-minute of the heart may vary from person to person [1], the maximum heart rate of humans is usually based on age. The older a person gets, the lower their maximum heartrate. At 20 years of age, the maximum heartrate is about 200 bpm [2]. While this number influences the cutoff frequency of the low-pass filter, 200 bpm (3.33 Hz) should not be directly used as the cut off frequency. Firstly, the cut-off frequency is simply the -3 dB point of the transfer function. This means that frequencies above this range will not be completely cut off. Another thing to consider is the fact that after the two filters, we must apply a voltage gain to scale the signal to a voltage range that is detectable by the microcontroller. Ideally, frequencies out of the range of the human heartbeat should not be amplified. For this reason, a lower frequency of 2 Hz was chosen as a low-pass cut-off frequency.

High pass filter

The cutoff frequency of the high pass filter should be low enough to not cut off the desired signal, but also high enough to to properly filter out the DC offset. A frequency of 0.5 Hz was chosen for this purpose.

Schematic & Simulation

As previously discussed, the heartbeat monitor circuit consists of a high-pass filter, followed by a low-pass filter, followed by a gain stage. The circuit for the optoisolator is discussed in [3] and will be used as the input into our filter stages.

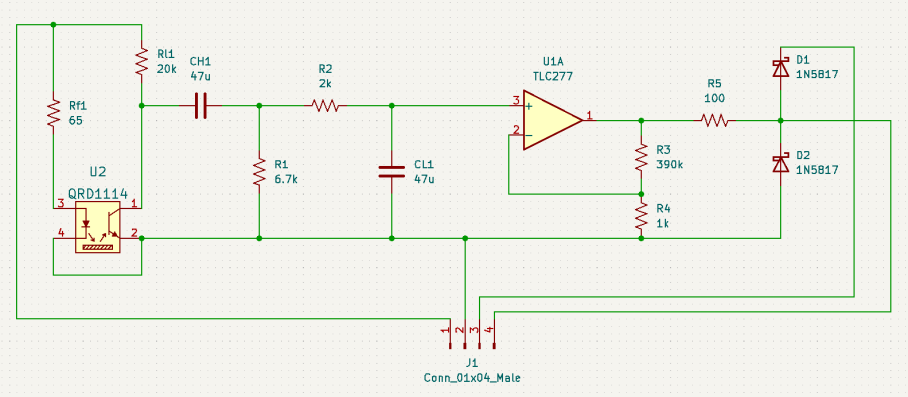

Figure 2: Schematic layout of heartbeat monitor.

As seen in Figure 2, the values chosen for the resistors and capacitors in high and low pass filters will yield cutoff frequencies of 0.505 Hz and 1.693 Hz respectively. These numbers are slightly off from the chosen cutoff frequencies due to resistor and capacitor availability in the lab. Finally, the gain stage is meant gain the filtered optoisolator signal from 35 mV to about 3 V. This schematic layout was simulated in LTSpice to find the ideal gain of the signal across frequencies ranging from 10 mHz to 20 Hz.

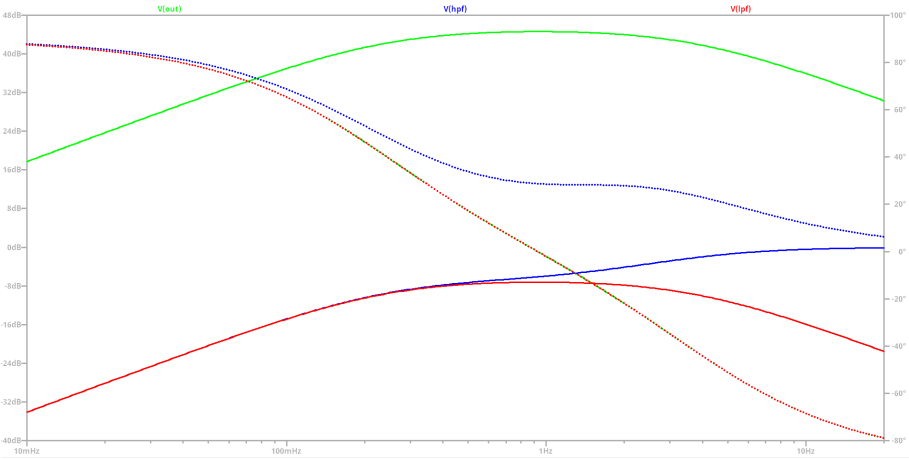

Figure 3: Transfer function of heartbeat monitor circuit from 10 mHz to 20 Hz between all filter stages.

Figure 3 shows the transfer function of the heartbeat sensor plotted across relevant frequencies. The plot shows the transfer function for the output of each individual filter stage as well as for the overall circuit including the gain stage. We can see that at about 1 Hz, the circuit is applying about 44 dB gain on the signal. If we convert that to linear gain, we find that this op-amp configuration will multiple the voltage by about 158 times.

$$44\,\text{dB} = 20log(A_{linear}) \tag{1}$$
$$A_{linear} \approx 158 \tag{2}$$
$$V_{in} = 35\,\text{mV} \tag{3}$$
$$V_{out} \approx 2.5\,\text{V} \tag{4}$$
$$\frac{V_{out}}{V_{in}} = 72 \neq 158 \tag{5}$$

Looking at the equations above, the expected signal magnitude from the optoisolator is about 35 mV and the desired voltage should be amplified to use a good portion of the range of the analog to digital converter (ADC). The MSP432's ADC has a reference voltage of 2.5 V meaning any voltage above this range will be cut off to the maximum digital output of the ADC. The theoretical gain required to amplify a 35 mV signal to 2.5 V is 72 (linear). However, because in reality we are not using ideal components, we will see a decrease in amplification as tolerance variations will cause a delta compared to simulation. A linear gain of 158 is used in this circuit as it showed great results.

Results & Analysis

To test the functionality of the circuit, an oscilloscope capture was taken on the output node following each of the three stages (high-pass, low-pass, gain). A sinusoidal input signal from the signal generator was used with a 500 mV DC offset and 35 mV amplitude.

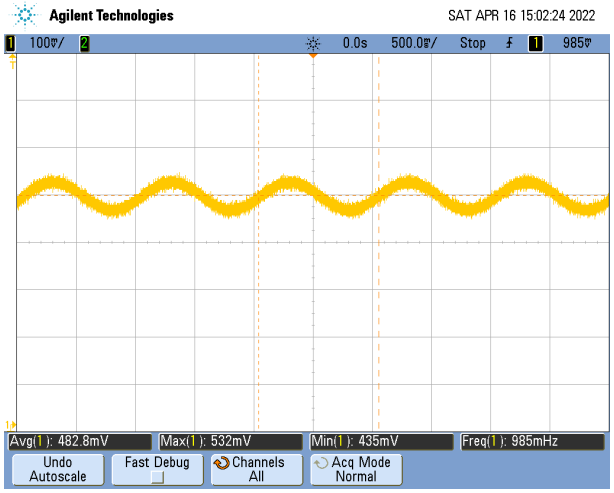

Figure 4: Input signal 482.8 mV DC offset and 35 mV amplitude.

We can see the input signal from the signal generator in Figure 4 is about what we would expect out of the OPB745. The signal is quite noisy which manifests as "fuzz" on the oscilloscope capture. The next step is to apply a high pass filter to this signal to filter out the DC offset.

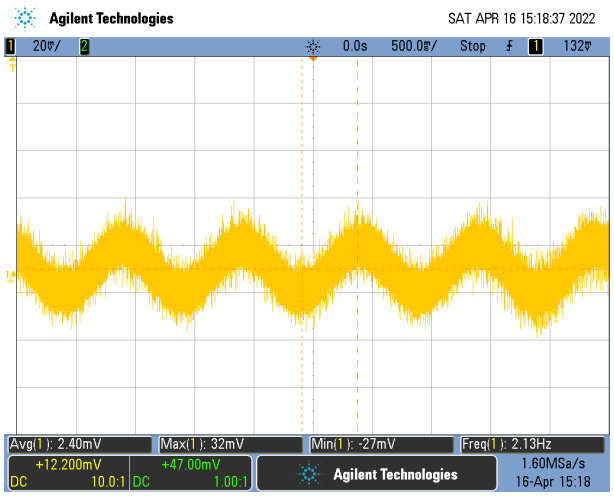

Figure 5: Signal with high-pass filter applied.

After applying a high pass filter, Figure 5 shows the signal is now centered at 0 V as expected. There is also a noticeable amplitude reduction to about 20 mV. This feature will become important later on. Notice that the frequency detected by the oscilloscope is also incorrect at this stage because the presence of high amounts of noise will trip the trigger more. The next filter we must apply to this signal is a low pass to filter out the higher frequencies.

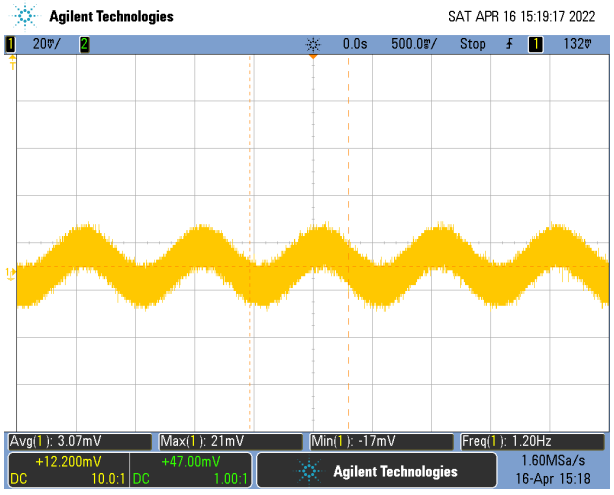

Figure 6: Signal with high-pass and low-pass filters applied.

Figure 6 shows the signal with the high-pass and low-pass filters applied. We can see an improvement in the quality of the signal when comparing to Figure 5. The remaining fuzz is caused by the sampling error from the oscilloscope due to the a low signal amplitude. This will no longer be visible when the gain stage is applied.

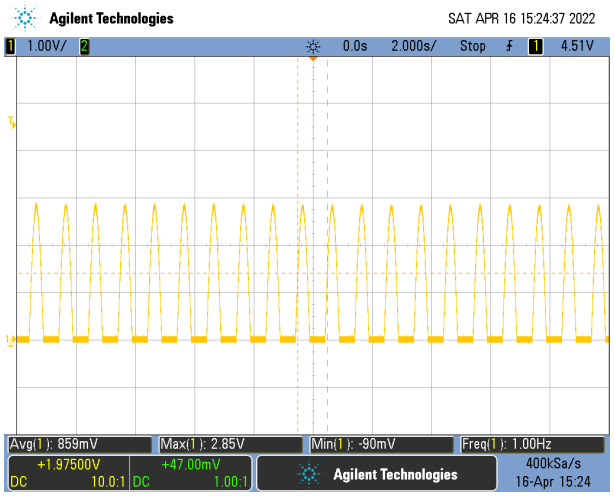

Figure 7: Signal with high-pass, low-pass and gain stages applied.

The generated signal shown in Figure 7 is the ideal output to send to a micro-controller. There are some important features to note in the final signal. The simulation shows that the output of the circuit should have a gain of about 44 dB. At an output amplitude of 2.85 V and an input amplitude of 35 mV, the actual gain about 38.2 dB. This may be due to dampening in low pass and high pass stages which is not modeled by the ideal components in the LT-spice simulation. Another feature of this wave when comparing it to the output of the low pass filter is the voltage cut off in the negative range. This occurs because the negative terminal on the op-amp is 0 V and therefore cannot provide an output beyond this voltage. However, this characteristic of the signal will not effect the measurements discussed in the next section, as the micro-controller doesn't need both halves of the sine wave to estimate the frequency.

There is one final step to protect the input pin on the ADC from being damaged. Too much current as well as voltage beyond the limits on the micro-controller will cause damage to the ADC peripheral. To avoid these two hazards, a 100 Ω resistor and two diodes are placed on the output node. The diodes are used to direct current to V_{cc} or ground in case of a voltage surge or high amplitude input. The resistor is used to limit the current flow to the micro-controller and not overdrive the ADC peripheral. Figure 8 shows the Shotkey protection circuit on the output of the gain stage.
The circuit shown in Figure 8 is able to drive the circuit output to either 0 V or 3.3 V if the gain stage outputs beyond this range.

Software

Once the circuit was constructed and verified to generate a clean signal, the next step was to use the micro-controller to measure the input frequency. To do this, the Analog-To-Digital converter (ADC) must be used to digitize the signal. The ADC driver written in [4] is used to perform this task. A simple way to find the frequency of a signal is to measure the time between rising edges. A rising edge can be classified as a transition from a low state to a high state. The simplest possible way to classify low states and high states is to provide a

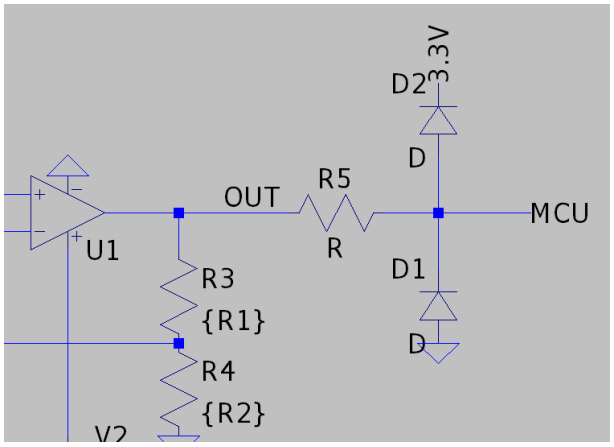

Figure 8: Shotkey protection circuit for heartbeat sensor.

single threshold between low and high states. The issue with this approach in this application is that an extra rising edge may be detected if the signal were to jump slightly at the threshold due to noise. A single threshold is therefore extremely sensitive to noise and signal imperfections for this application.

A more noise tolerant design is to use a Schmitt-trigger. The Schmitt trigger instead uses two thresholds. The upper threshold will send the system into a high state while the lower threshold will transition the system into a low state. The space in-between the two thresholds will hold the system state constant. This method is far more tolerant to small jumps and noise from the input signal and was used to find the rising edges while reading ADC values.

To implement the actual data collection, a timer is used to trigger an ADC capture at a configurable frequency for a configurable length of time. Once enough data is collected, the timer is switched off and the system will average the distances between rising edges. Pressing one of the switches on the MSP432 will trigger the data collection cycle again.

The software was tested using an upper threshold of 1.5 V and a lower threshold of 0.5 V. Input frequencies of 3 Hz, 2 Hz, 1 Hz, and 0.5 Hz were tested to obtain an accurate set of readings over the full spectrum of heart rates we are interested in.

```
Average frequency is 2.985074 Hz (179.104477 bpm)
Sampling for 5 seconds...
Found 9 edges in 5 seconds
Average frequency is 1.991150 Hz (119.469026 bpm)
Sampling for 5 seconds...
Found 4 edges in 5 seconds
Average frequency is 0.995024 Hz (59.701492 bpm)
Sampling for 5 seconds...
Found 1 edges in 5 seconds
Average frequency is 0.500000 Hz (30.000000 bpm)
```

Figure 9: UART capture of software for 3 Hz, 2 Hz, 1 Hz, and 0.5 Hz input signals.

Figure 9 shows the system responding to various input signals with the correct output. The output of the heartbeat monitor software proves the system has a fairly high degree of accuracy as it correctly displays the signal frequencies displayed on the signal generator.

PCB

The final step of this lab exercise was to realize the schematic designed in PSpice as a printed circuit board (PCB) design in KiCAD. This process is fairly straight forward. The first step is to redraw the circuit schematic in KiCAD and assign part footprints to each component. The footprints will tell KiCAD the shapes and sizes of the terminals on the components in question. The next step is to layout the circuit components on the physical PCB. This can be tedious as avoiding crossing tracks can sometimes be problematic.

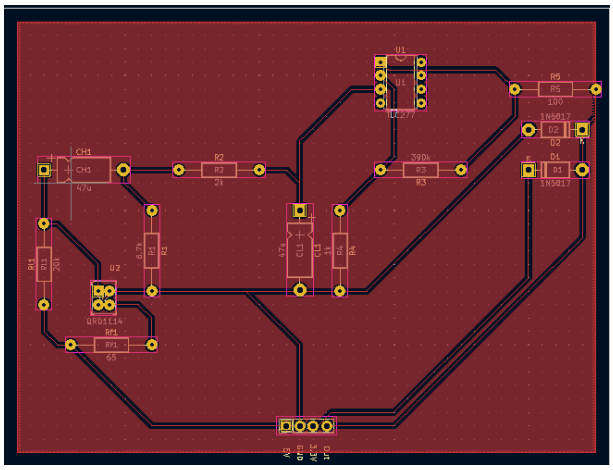

Figure 10: Physical layout of the heartbeat monitor circuit.

Figure 10 shows the physical layout of the PCB with all the relevant components in place. Although greater care could have been taken to constrain the overall size of the board, the main effort here was to attempt to match the layout of the schematic to the layout of the PCB. This would improve readability of the PCB itself even though not strictly required. We can see there are four pin headers exposed at the bottom of the PCB. These pins will interface with ground, 5 V, 3.3 V and the ADC input pin on the micro controller.
Figure 11 shows a 3D view of the PCB with the components in place as well as labels for each of the four pin headers.

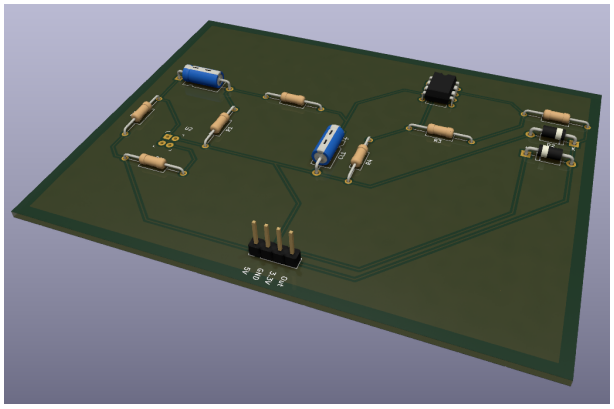

Figure 11: 3d rendering of the heartbeat monitor PCB.

The final step after designing and laying out the PCB is to place an order to the manufacturer. Most manufacturers accept a zip file containing a set of Gerber files and drill files describing the construction process of the PCB. KiCAD can generate these files once the design rules check has passed.

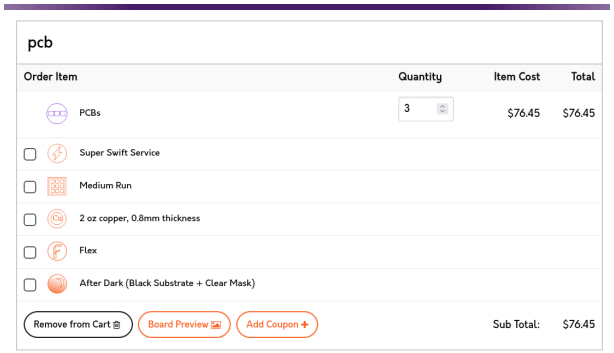

Figure 12: 3d rendering of the heartbeat monitor PCB.

Figure 12 shows an order ready to be placed for this PCB. This order is of course only for the PCB itself and not the components shown in the 3D view. These components must be ordered separately and soldered onto the PCB. A parts list was generated for the entire heartbeat monitor circuit.

Table 1: Heartrate monitor parts list

Part	Quantity	Purpose
65 Ω Resistor	1	Optoisolator input resistor
20 kΩ Resistor	1	Optoisolator output resistor
OPB745	1	Optoisolator sensor
47 µF Capacitor	2	High pass and low pass filters
6.7 kΩ Resistor	1	High pass filter
2 kΩ Resistor	1	Low pass filter
390 kΩ Resistor	1	Gain stage
1 kΩ Resistor	1	Gain stage
TLC277	1	Op-amp for gain stage
100 Ω Resistor	1	Microcontroller current protection
1N5817 Diode	2	Microcontroller voltage protection

Questions

1. The electrical rules check (ERC) and design rules check (DRC) are tools native to KiCAD that are meant to check certain characteristics of the schematic and PCB layout respectively. For example, the ERC will warn the designer of an unconnected terminal or component that is missing a footprint. The DRC will check physical design constraints such as a right angle track or a component being placed in close proximity to another component. These automated checks are not a "catch-all" for design mistakes but rather provide valuable insight to the designer on common issues.

2. I originally designed the low pass filter with a cut-off frequency of 7 Hz. When I tested the signal on the breadboard, I found that the signal was still fairly noisy due to the low pass filter failing to filter out enough frequencies. I decided to drop the cutoff frequency to 1.7 Hz. Even though the upper limit of possible human heart rates are slightly above this frequency, the amplitude drop at the upper limit was low enough that the microcontroller did not experience any issues detecting rising edges in these signals.

3. Interestingly, the gain did *not* match the theoretical values. Specific values are discussed at length above. The main cause of this is that small variations in resistor and capacitor tolerance may have caused a negative gain in the filter stages. This negative gain would differ from the simulated circuit which would explain the discrepancy.

Conclusion

This lab looked at filter design both in simulation as well as in reality on a physical breadboard. The passive components of the filter caused some issues in varying the gain slightly when comparing to the simulation. That was determined to be a tolerance related issue. This small variation in amplitude meant that the active gain stage needed to be adjusted to work properly with the physical components of the circuit. Once a clean signal with the proper characteristics was filtered and amplified, the microcontroller could detect a periodic signal using a noise tolerant Schmitt trigger design implemented in software. The Schmitt trigger worked very well as it correctly calculated the frequency of the input signal with a high degree of accuracy. Finally, the circuit was laid out on a PCB and a

References

[1] F. Arvin, S. Doraisamy, and E. Safar Khorasani, "Frequency shifting approach towards textual transcription of Heartbeat sounds," Biological procedures online, 04-Oct-2011. [Online]. Available: https://www.ncbi.nlm.nih.gov/pmc/articles/PMC3396354/. [Accessed: 16-Apr-2022].

[2] B. Gholipour, "What is a normal heart rate?," LiveScience, 13-Dec-2021. [Online]. Available: https://www.livescience.com/42081-normal-heart-rate.html. [Accessed: 16-Apr-2022].

[3] A. Tumbar, "Characterization of OPB745" Rochester Institute of Technology, 4-Feb-2022.

[4] A. Tumbar, "MSP432 Timers, Interrupts, and Analog-to-Digital Converter" Rochester Institute of Technology, 12-Feb-2022.

Exercise 8: Heartrate Monitor

Student's Name: Andrei Tumbar Section: 2

Demo		Point Value	Points Earned	Date
Demo	Pre-Lab (Individual)	10	10	CP 3/25
	LTspice and Plots for HRM	10	10	CP 3/25
	Completed HRM	20	20	XB 3/28/22
	PCB Design and Layout (Individual)	10	10	DJ 4/14

Bonus: Working HRM with OPB745 (10 pts) _____

To receive any grading credit students must earn points for both the demonstration and the report.