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edit - Using_Universal.vhd
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100 ns
V:/HPModelSim_Projects/Using_Universal.vhd

1 library ieee;
2 use ieee.std_logic_1164.all;
3 entity with_universal is
4 port(A: in std_logic;
5      B: in std_logic;
6      andwithnand: out std_logic;
7      andwithnor: out std_logic;
8      orwithnand: out std_logic;
9      orwithnor: out std_logic;
10     notwithnand: out std_logic;
11     notwithnor: out std_logic;
12     exorwithnand: out std_logic;
13     exorwithnor: out std_logic;
14     exnorwithnand: out std_logic;
15     exnorwithnor: out std_logic);
16 end with_universal;
17
18 architecture universal_arch of with_universal is
19 begin
20 andwithnand<=(A nand B)nand(A nand B);
21 andwithnor<=(A nor A)nor(B nor B);
22 orwithnand<=(A nand A)nand(B nand B);
23 orwithnor<=(A nor B)nor(A nor B);
24 notwithnand<=(A nand A);
25 notwithnor<=(A nor A);
26 exorwithnand<=((A nand (A nand B))nand(B nand (A nand B)));
27 exorwithnor<=((A nor A) nor (B nor B))nor(A nor B);
28 exnorwithnand<=((A nand (A nand B))nand(B nand (A nand B)))nand((A nand (A nand B))nand(B nand (A nand B)));
29 exnorwithnor<=((A nor B) nor A) nor (B nor (A nor B));
30 end universal_arch;
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