MICROPROCESSOR I/O DEVICES – DETAILED NOTES (8259, 8255, 8279, 8253/8254, 8251)

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8259 – PROGRAMMABLE INTERRUPT CONTROLLER (PIC)

Introduction:

The 8259 PIC is used to expand and manage hardware interrupts for microprocessors such as 8085/8086. It supports 8 vectored interrupts, expandable to 64 using cascading.

Internal Architecture:

• Data Bus Buffer – Transfers data/control words between CPU and PIC.

• Read/Write Control Logic – Controls read/write operations.

• IRR (Interrupt Request Register) – Stores incoming interrupt requests.

• ISR (In-Service Register) – Tracks interrupts currently being serviced.

• IMR (Interrupt Mask Register) – Masks unwanted interrupts.

• Priority Resolver – Determines highest priority among active interrupts.

• Cascade Buffer/Comparator – Supports master-slave configurations.

Interrupt Sequence:

1. Device sends request → IR line.

2. IRR stores request.

3. Priority resolver picks highest priority.

4. INT sent to CPU.

5. CPU responds with INTA.

6. ISR bit set.

7. Vector address sent to CPU.

8. CPU executes ISR.

9. EOI command clears ISR bit.

Priority Modes:

• Fully Nested Mode – IR0 highest.

• Rotating Priority – Priority rotates.

• Special Mask Mode – Masking independent of priority.

• Automatic EOI – ISR automatically cleared.

ICWs and OCWs explained:

• ICW1 – Basic configuration.

• ICW2 – Vector address.

• ICW3 – Slave/master connections.

• ICW4 – Mode configuration.

• OCW1 – Mask register.

• OCW2 – Priority control + EOI.

• OCW3 – Polling + masking.

8255 – PROGRAMMABLE PERIPHERAL INTERFACE (PPI)

Introduction:

The 8255 provides 24 programmable I/O lines (Port A, B, C). Used for keyboards, displays, ADC/DAC, etc.

Operating Modes:

Mode 0 – Simple I/O:

- No handshaking; direct input/output.
- Ports A, B, C can be programmed independently.

Mode 1 – Strobed I/O (Handshake Mode):

- Used when external device is slower.
- Signals: STB, IBF, INTR for input; OBF, ACK for output.

Mode 2 – Bidirectional Mode:

- Only Port A.
- Bidirectional data transfer with handshake via Port C.

BSR Mode:

- Controls individual bit of Port C.
- Useful for relays, LEDs.

8279 – KEYBOARD/DISPLAY CONTROLLER

Introduction:

The 8279 handles keyboard scanning and display refreshing. Used in calculator-type interfaces.

Keyboard Features:

• 8×8 matrix support.

• Debouncing logic.

• Two-key lockout mode.

• N-key rollover mode.

• FIFO buffer (8-byte) to store keycodes.

Display Features:

• Supports 16×7-segment displays.

• Display RAM for automatic refreshing.

• Left-entry and Right-entry modes.

Commands:

• Keyboard/Display Mode Set.

• Read FIFO.

• Write Display RAM.

• Clear Display.

• Clear FIFO.

8253 / 8254 – PROGRAMMABLE INTERVAL TIMER

Introduction:

Programmable timers used to generate delays, waveforms, frequency division, and rate generation.

Contains three 16-bit counters, each with:

- CLK input.
- GATE input.
- OUT output.

Modes of Operation:

Mode 0 – Interrupt on Terminal Count

Mode 1 – One Shot

Mode 2 – Rate Generator

Mode 3 – Square Wave Generator

Mode 4 – Software Triggered Strobe

Mode 5 – Hardware Triggered Strobe

Difference Between 8253 & 8254:

- 8254 supports higher frequencies (10 MHz).
- BCD mode supported by 8254.

8251 – USART (Universal Synchronous/Asynchronous Receiver/Transmitter)

Introduction:

Used for serial communication. Converts parallel data ↔ serial data.

Modes:

Asynchronous Mode:

• Start/stop bits.

• Baud rate from clock generator.

Synchronous Mode:

• Clock shared between sender and receiver.

• No start/stop bits; faster.

Transmitter Operation:

• CPU writes data → transmitter buffer.

• Data serialized and transmitted.

Receiver Operation:

• Detects start bit.

• Shifts bits.

• Stores parallel byte.

• Sets Data Ready flag.

Registers:

• Mode Word

• Command Word

• Status Register