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DCF77-BASED DIGITAL CLOCK

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Abstract

The aim of the lab project was to build a clock synchronized with the Physikalisch-Technische Bundesanstalt atomic clock in Mainflinen via a DCF77 receiver. The objective was achieved by creating a finite state machine that, as soon as it is turned on, starts synchronizing with the signal. Once synchronized it starts listening to the time data transmitted by the radio station. Finally, when all the necessary data has been gathered, the machine waits for the end of the current minute and then it goes on by itself as a standard clock.

1 Introduction

The DCF77 is a type of time-signal related to the atomic clock managed by the Physikalisch-Technische Bundesanstalt. Its antennas are located at N 50°1′ E 9°0′ in Mainflinen [1], 25 Km southeast of Frankfurt, and they emit an amplitude modulated signal at a constant frequency of 77.5kHz [2]. The signal is characterized by steep drops in its power (15% of the high-state) that can last 100 or 200 ms and they encode respectively for binary 0 and 1. The time interval between each negative edge is exactly 1 s, in this way the signal can transmit also a clock information to the eventual receivers [3, 4].

The first 20 bits of signal encode for various information slightly related to time itself, for instance weather report, civil warning, abnormal transmitter operation, summer time and eventual leap seconds. The 21^{st} bit marks the beginning of the encoded time and it is always set to 1. After that, there follow a sequence with 8 bits assigned to minutes, 7 bits assigned to hours and 23 bits assigned to date. The last bit of each sub-sequence it is used for parity check and every decimal digit is encoded independently from the others, this implies that, for instance, the bits encoding for minutes data are not weighted as (1, 2, 4, 8, 16, 32, 64) but as (1, 2, 4, 8, 10, 20, 40) [4]. The 60^{th} bit, the last one, is always suppressed, this means that there is no actual signal drop-down and, therefore, it can be used as a syncing reference [3].

2 Experimental setup

The main device used during the realization of the project was an Altera DE2 development and educational board [5] mounting a Cyclone II FPGA 2C35 chip [6]. To receive the signal a BN 641138 receiver was used. This particular component provides already a signal converted from analog to digital and offers two output possibilities: a standard one, with the PWM 1 and 0 on the high state, and an inverted one [7]. The power, ground and standard output pins of the receiver were connected to the GPIO array 1 to the Altera DE2 via a bus connector and a breadboard, as shown in figures 1 and 2. A 100kΩ pull-up resistor was introduced, as suggested by the manual [7], and a Tektronix TBS1102B-EDU oscilloscope was used for troubleshooting.

3 Troubleshooting

During the assembly phase of the experimental setup, several sources of noise and problems were encountered.
The first one to be noticed was the strong dependency of the strength and the quality of the output on the orientation of the antenna. This can be explained by the fact that, since the receiver is sensitive to magnetic field oscillations rather than electric field ones, it must be set parallel to the direction of the signal oscillating magnetic field and, therefore, perpendicular to the direction pointing towards N 50°1′ E 9°0′.
An additional source was identified in other radio devices such as mobile phones. A picture of noise

generated from such devices is shown in figure 3. Finally, the last noise source was traced back to the GPIO pins themselves. It was noticed that when they are not declared in the header of the verilog HDL file, their state is uncertain and it can influence the one of the output pin conductor. This was fixed by simply enabling the used GPIO array.

4 Code explanation

The first section of the program is entirely dedicated to the variables declaration. Here the 50 MHz clock is passed to the `freqdivider` module in order to get a 100 Hz signal. The newly generated clock is used as the base clock for the state machine. Moreover, since the signal posedges seem to be not well detected, here a debounced signal is generated as well but only to be used with the ticks counting `always` block.

The second section is occupied by the main `always` block and the `case` responsible for the state changing. Since the necessary states are 3, they must be encoded with at least a 2 bits word. In the sync state (`00`) the machine looks for the 2 seconds low pattern in the signal at the end of each minute. To do so it counts up from 0 whenever the 100 Hz clock is ticking and when the counter reaches the value `1001 0110` (150 in decimal), it means that around 1.5 seconds have passed from the previous low state and, therefore the state is changed to `01`. The number of tickings N in a time interval T is evalueted as $N = f_{clock}T$. Whenever the signal is high, the counter is reset.
In the listen state (`01`) the machine decodes the signal and each time add the gathered value to the relevant `reg` variables (`min` or `hour`). Since the signal is pulse width modulated, whenever it is high, starting from 0, a counter increases by 1 at each clock cycle. When the signal gets down again, the counter is compared to different values. If it is grater than 15 (`0000 1111`), then it corresponds to a 1 and an addition is performed, the corresponding time multiplier factor is doubled and the counter is reset. If it is just grater than 7 (`0000 0111`), then it corresponds to a 0 and only the multiplication and the reset operations are performed. If none of the previous condition is satisfied, then probably it is just noise and the counter is reset to 0. Furthermore, there is only interest in specific bits, namely the ones (starting from 1 not from 0) from 22 (`0001 0110`) to 28 (`0001 1100`) and the ones from 30 (`0001 1110`) to 35 (`0010 0011`).
In the clock state (`10`) the board just works as a standard clock.

Finally, in the third section there is another `always` block that counts the ticks of the signal, but only if the machine is in the listen state, and in the fourth section the time data is displayed on the hex-displays.

5 Conclusions

The project has been completed with excellent results. All the adjustments made to prevent errors have proven to be effective and, if attention is payed to avoid interference from radio devices during the syncing and listening states, the clock works as intended.

References

[1] Physikalisch-Technische Bundesanstalt. *DCF77 location*.

[2] Physikalisch-Technische Bundesanstalt. *DCF77 carrier frequency*.

[3] Physikalisch-Technische Bundesanstalt. *DCF77 amplitude modulation*.

[4] Physikalisch-Technische Bundesanstalt. *DCF77 time code*.

[5] School of Electrical and Computer Engineering. *DE2 Hardware Reference Manual*.

[6] School of Electrical and Computer Engineering. *DE2 FPGA Chip Datasheet*.

[7] Conrad. Receiver BN 641138

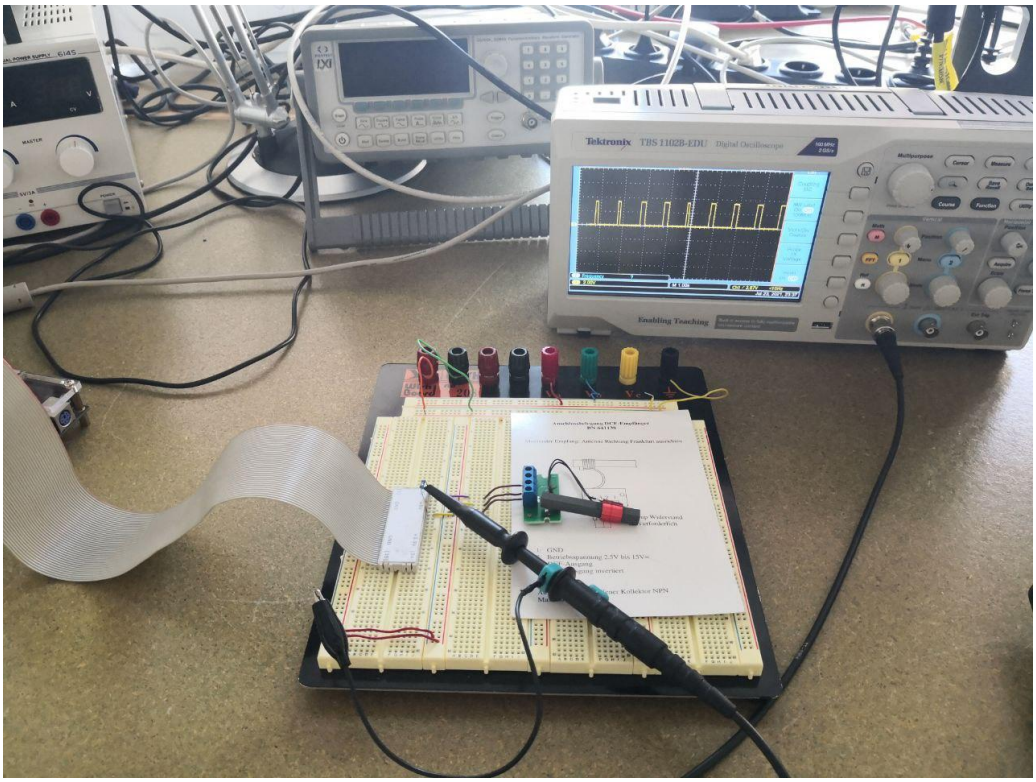

Figure 1: Picture of the experimental setup

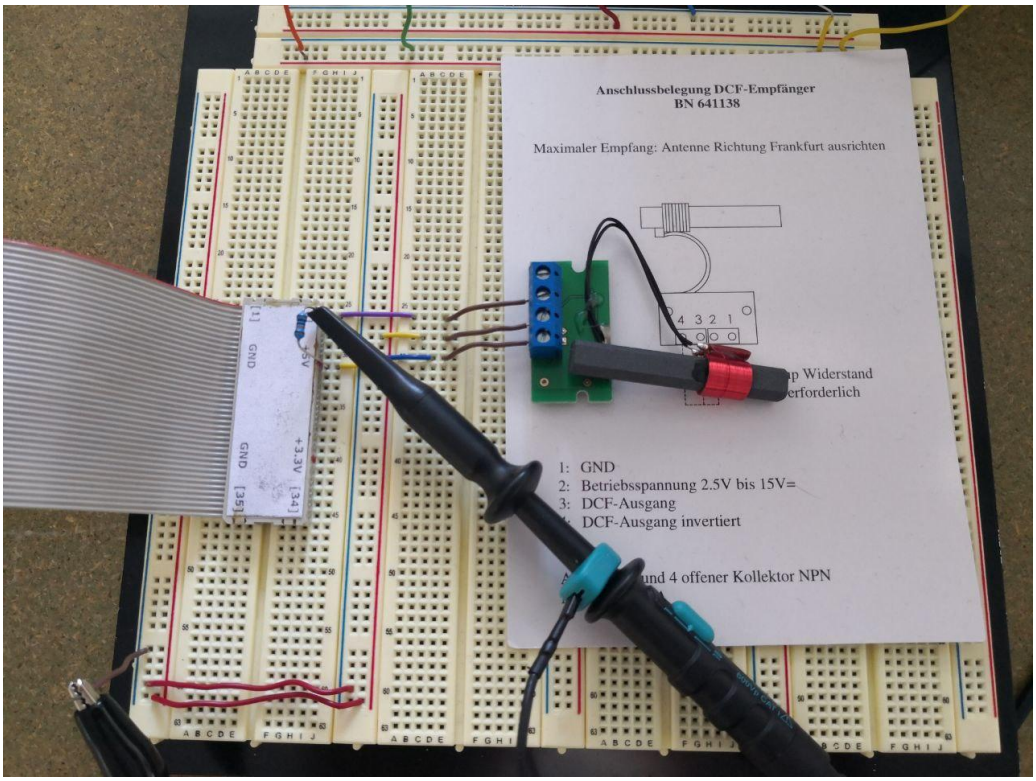

Figure 2: Close-up picture of the breadboard

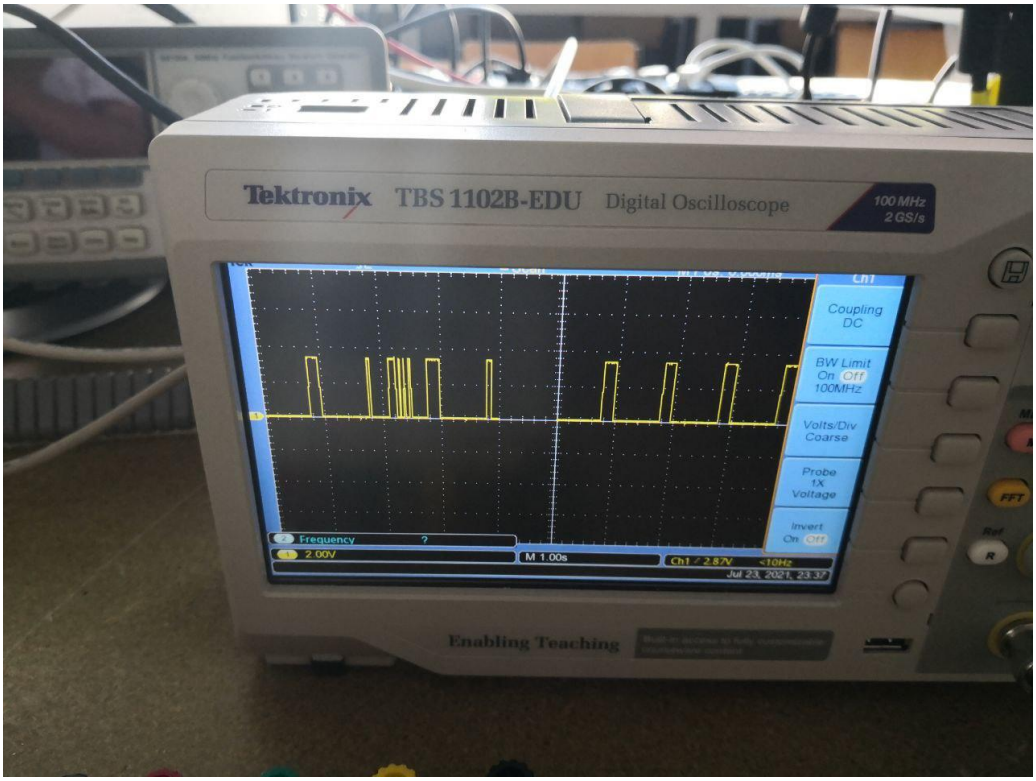

Figure 3: Picture of noise generated by a radio device

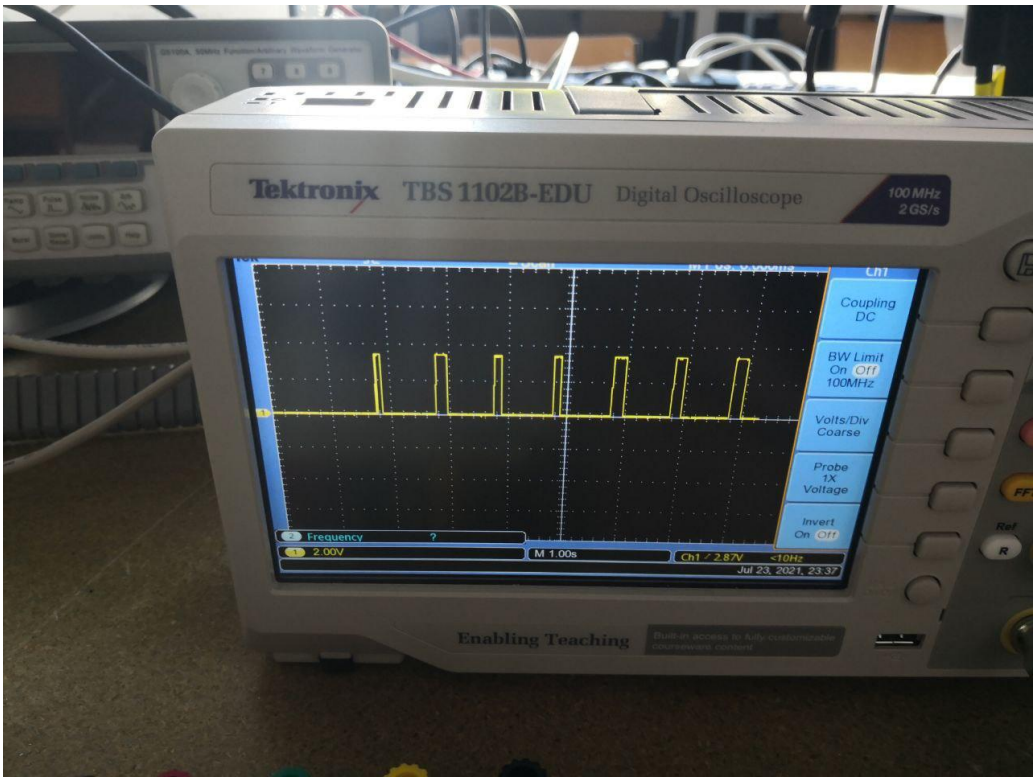

Figure 4: Picture of the 2 seconds low pattern at the end of a minute

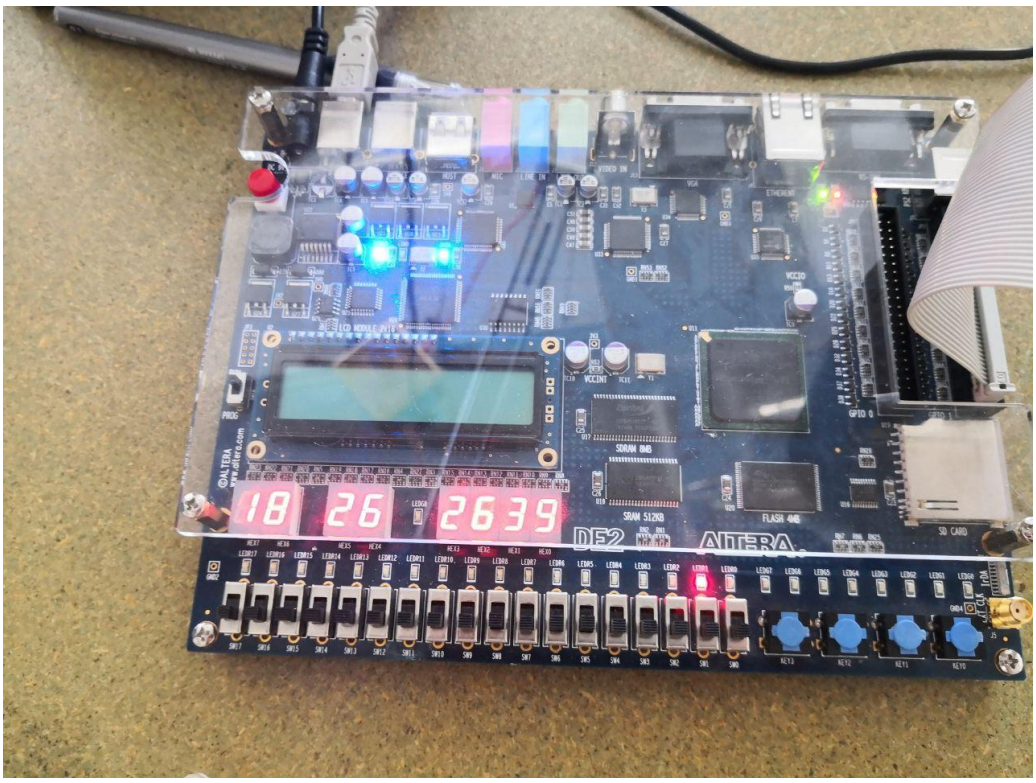

Figure 5: Picture of the machine displaying the correct time