GUJARAT TECHNOLOGICAL UNIVERSITY

PROG-ANALOG : THE PROGRAMMABLE ANALOG BOARD

A detailed report to be submitted
for
project-II(2181105),semester-VIII
in
Bachelor of Engineering(EC)

guided by,
Prof.Mayank G Mahant
Assistant professor
Department of Electronics and Communication Engineering
GCET,V.V.Nagar,Gujarat,India

submitted by,

Hiren Moradiya	**160110111031**
Kruparth Patel	**160110111033**
Ammar Vahora	**160110111052**

Department of Electronics and Communication Engineering
G.H.Patel College of Engineering and Technology
Bakrol road,V.V.Nagar-388120

G.H.Patel College of Engineering and Technology

CERTIFICATE

This is to certify that project-II entitled ***"Prog-Analog : The Programmable Analog Board"*** which is being submitted by ***Hiren Moradiya,Kruparth Patel,Ammar Vahora*** ,Team ID-81880 in semester VIII in **Bachelor of Engineering(Electronics and Communication)** to **Gujarat Technological University** is record of candidate's own work carried out by them under my supervision and guidance during the period of December-2019 to April-2020.

Prof.Mayank G Mahant
Faculty guide

Dr.Hitesh B Shah
Head,EC department

Dr.Himanshu B Soni
Principal,GCET

Contents

ACKNOWLEDGEMENT

It's a great pleasure and privilege to take this project work entitled ***"Prog-Analog : The Programmable Analog Board"***.The time has arrived at this stage that we would like to show our deep gratitude towards the people associated with this dissertation for their support,encouragement and guidance throughout this thesis.

We would like to express our sincere gratitude toward out guide ***Prof.Mayank Mahant***,Assistant professor,Dept. of EC engineering,GCET college,for their guidance,support,encouragement throughout the project.Their readiness for consultation all the time,educative comments and assistance have been invaluable.

we would like to thank all those teaching and non-teaching staff,classmates of EC department who have helped us in completion of this project.

Lastly,we would like to thank almighty GOD and our family for their continuous support.

Hiren Moradiya,

Kruparth Patel,

Ammar Vahora

Abstract

Prototyping of analog circuits is hair stretching work,and often get's complicated because one has to work with breadboard.To eliminate breadboarding of big digital systems,FPGAs were developed over the past years for prototyping purposes.We have come up with similar thing for analog world. It's like FPGA,but instead of digital it will create analog circuits like integrator, differentiator,adder based on coding.

We have one plan to make it possible. FPGAs use RTL coding like VHDL/verilog and has their own s/w which converts coding to circuit netlist and which gets implemented in FPGAs,now at this stage we don't have that much knowledge to develop our own synthesizer s/w,hence we'll use following plan. We will have OP-AMPs in circuit,and passive components which has capability to change it's value based on programming.For resisters we use something known as digital POTs and for capacitors NCD2100 which is digital programmable variable capacitor.

We'll have interconnection between all of them via FETs,which will act as programmable switches. Now for programming,one has to write commands,which will be decoded by ASCII codes and accordingly switch matrix is programmed to form desired circuit.There is digital circuit which accepts ASCII bits and programs solid state switches,and with this one can implement amps,integrator,differentiators,adders, instrument amplifiers and combination of all above.Application of this thing can be found in prototyping ,educational purposes and implementation of PID controllers.

List of Figures

List of Tables

1 Introduction

1.1 General Information

Electronic switching is the basic requirement to achieve programmability in circuit synthesization.Instead os fixed connection,we need variable connection between electronic components.Prototyping of analog circuits is hair stretching work,and often get's complicated because one has to work with breadboard.To eliminate breadboarding of big digital systems,FPGAs were developed over the past years for prototyping purposes.We have come up with similar thing for analog world. It's like FPGA,but instead of digital it will create analog circuits like integrator, differentiator,adder based on coding. We have one plan to make it possible. FPGAs use RTL coding like VHDL/verilog and has their own s/w which converts coding to circuit netlist and which gets implemented in FPGAs,now at this stage we don't have that much knowledge to develop our own synthesizer s/w,hence we'll use following plan.

We will have OP-AMPs in circuit,and passive components which has capability to change it's value based on programming.For resisters we use something known as digital POTs and for capacitors NCD2100 which is digital programmable variable capacitor. We'll have interconnection between all of them via FETs,which will act as programmable switches. Now for programming,one has to write commands,which will be decoded by ASCII codes and accordingly switch matrix is programmed to form desire circuit.There is digital circuit which accepts ASCII bits and programs solid state switches.And with this one can able to implement amps,integrators,differentiators,adders,instrument amplifiers and combination of all above.Application of this thing can be found in prototyping ,educational purposes and implementation of PID controllers.

1.2 Block Diagram

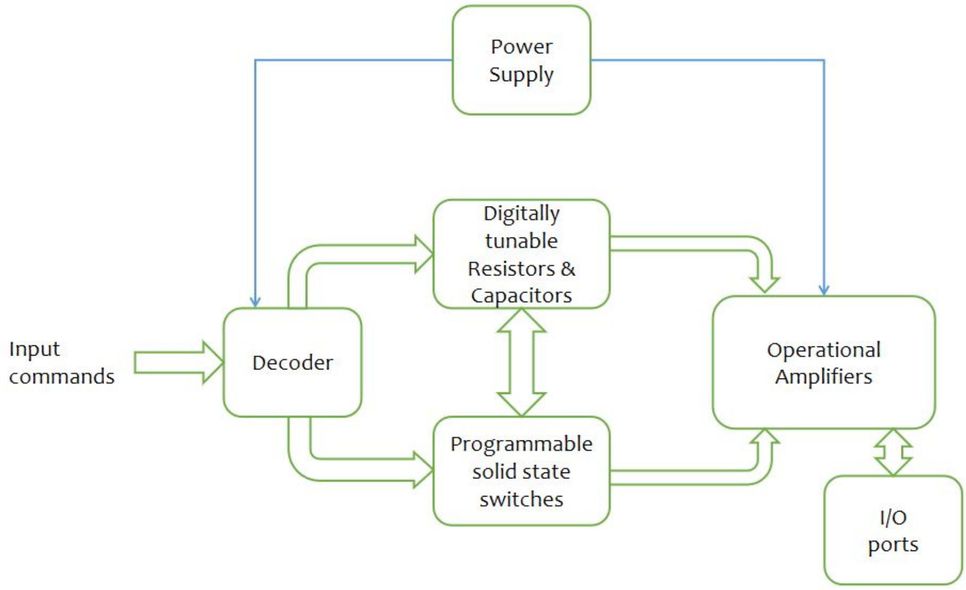


Figure 1: Block Diagram

The block diagram is pretty self explanatory.Operational amplifiers are the key components in almost all analog designs.It has bank of OP-AMPs and digitally tunable POTs and CAPs in input of the OP-AMP as well as in feedback.Digitally tunable POTs and CAPs has fixed inbuilt resisters and capacitor banks with swiching transistors and decoding/interfacing logic all built upon a silicon wafer inside DIP/SOP form-factor.

Programmable solid state switches is crossbar switch matrix which is the heart of Telecomm switching systems.It has cross-point FET switches with decoding/interfacing logic circuit inbuilt in DIP/QFP/PLCC form-factor.However such things are made for low power applications and often has low bandwidth problem and cross-talk problem.

1.3 Programmable circuits : How does it work?

Those who have used FPGAs might know it about it's working.First there goes a software/compiler which allows you to write command which implements the functionality you want.They also allows you to simulate your designs before you synthesize it.VHDL/verilog codes then converted into opcodes that goes into your FPGA board,where it has LUT(Look-up table) and cross-bar switches to have interconnect between them,with which your circuits gets synthesized.

Our Prog-Analog board will work exactly same way.Where we have an 8-bit processor which will do the job of compiler,it decodes the incoming commands.Based on inputted command,processor will make/brake switches in cross-matrix switch IC and programs the inputted/calculated value for passive parameters(Resistors and Capacitors) in programmable POTs and CAPs.

1.4 Objective of the project

Hardware and Firmware design of analog development board which can allow to synthesize circuits based on programming.

1.5 Present solutions

FPAA abbreviation of **Field Programmable Analog Arrey** exists which does the job of synthesizing analog circuits.There are CAB(Configurable analog blocks) and programmable interconnects,some includes OP-AMPs as well.Such things are based on "Switched capacitor technology",which is popular because capacitor is easy to fabricate on a silicon wafer then the resistor,but it's not "truly" analog.

2 Literature Review

2.1 Patents Referred

2.1.1 Programmable Analog Array

Inventors : Edmund Pierzchala,Milwaukie,Marek A. Perkowski
Date : 28th September,1999
Publication no. : US005959871A
Patent no. : 5959871

Abstract

There is disclosed a programmable analog or mixed analog/ digital circuit. More particularly, this invention provides a circuit architecture that is flexible for a programmable electronic hardware device or for an analog circuit whose input and output Signals are analog or multi-valued in nature, and primarily continuous in time. There is further disclosed a design for a current-mode integrator and Sample-and-hold circuit, based upon Miller effect.

Comments :

This patent has same application as we thought,but it does not include any OP-AMP based circuits.Plus it doesn't mention anything about the way of programming it.

2.1.2 Design approaches to field programmable analog integrated circuits

Inventors : Dean R. D'Mello , P.Glenn Gulak
Date : 15th July,1996
Journal : Analog ICs and signal processing 17,7-34

Anstract :

The drive towards shorter design cycles for analog integrated circuits has given impetus to several developments in the area of Field-Programmable Analog Arrays (FPAAs). Various approaches have been taken in implementing structural and parametric programmability of analog circuits. Recent extensions of this work have married FPAAs to their digital counterparts (FPGAs) along with data conversion interfaces, to form Field Programmable Mixed-Signal Arrays (FPMAs). This survey paper reviews work to date in the area of programmable analog and mixed-signal circuits. The body of work reviewed includes university and industrial research, commercial products and patents. A time-line of important achievements in the area is drawn, the status of various activities is summarized, and some directions for future research are suggested.

Comments :

Here the authors were focused on programmability in circuit parameters like gain,to implement it as AGC(Automatic gain controllers).Auther imagined a mixed signal circuit just as we thought of one.With different analog blocks to realize analog functionality and programmable interconnects between them.Here as of above no discussion about programming techniques.

2.1.3 Mixed mode analog/digital programmable interconnect architecture

Inventor : Khaled A. El-Ayat
Date : 13th February,1991
App. No : 654699

Abstract :

A user programmable IC contains user programmable analog portion,a user programmable digital portion and one interface portion which contains ADC and DAC,and one user configurable interconnect portion.

Comments :

This Mixed signal IC is amalgamation of FPGA and FPAA.It's slightly different from our pure analog configurable circuit board.Otherwise the way of realizing programmability in interconnect is same as we are planning.There is no discussion on programming method as well.

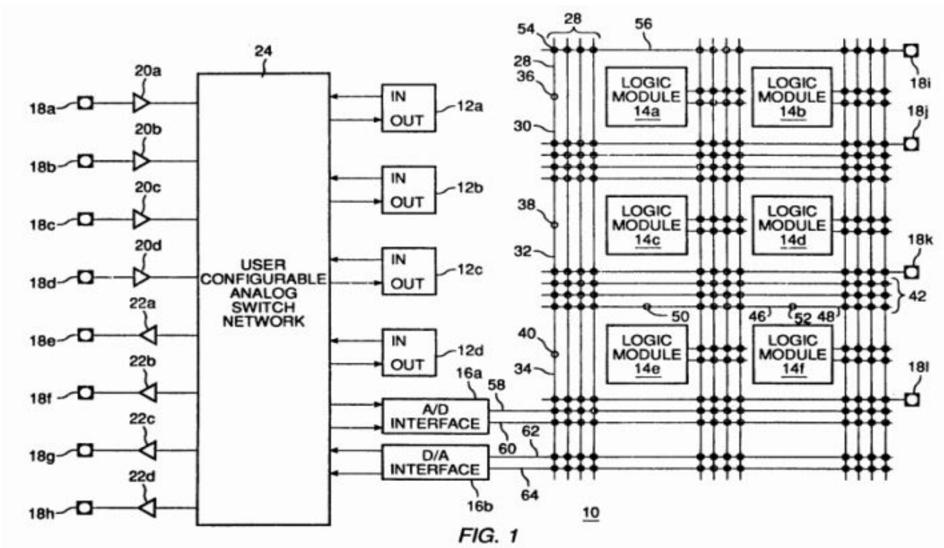


Figure 2: Architecture of mixed signal configurable IC

2.1.4 Field programmable analog array with memristors

Inventors : Jianhua Yang,Muhammad Shakeel Qureshi,Gilberto Medeiros Reibeiro,R. stanley Williams
Date : 29th April,2014

Abstract :

A field-programmable analog array (FPAA) includes a digital signal routing network, an analog signal routing network,Switch elements to interconnect the digital signal routing network with the analog signal routing network, and a configurable analog block (CAB) connected to the analog signal routing network and having a programmable resistor array. The Switch elements are implemented via digital memristors, the programmable resistor array is implemented via analog memristors, and/or antifuses within one or more of the digital signal routing network and the analog signal routing network are implemented via digital memristors.

Comments :

This is work is same as what we want to do.It includes CAB(Configurable analog blocks),which has resistor and capacitor banks which is used to achieve desired value of respective parameter.Switching network for programmable interconnection between CABs.This paper displays total hardware information.It proposes the use of 'Memristor' to eliminate low speed isolated gate transistors,which is used as switch.Most of the configurable passive elements available with few op-amps.This paper has much in-depth technical information compare to our level.

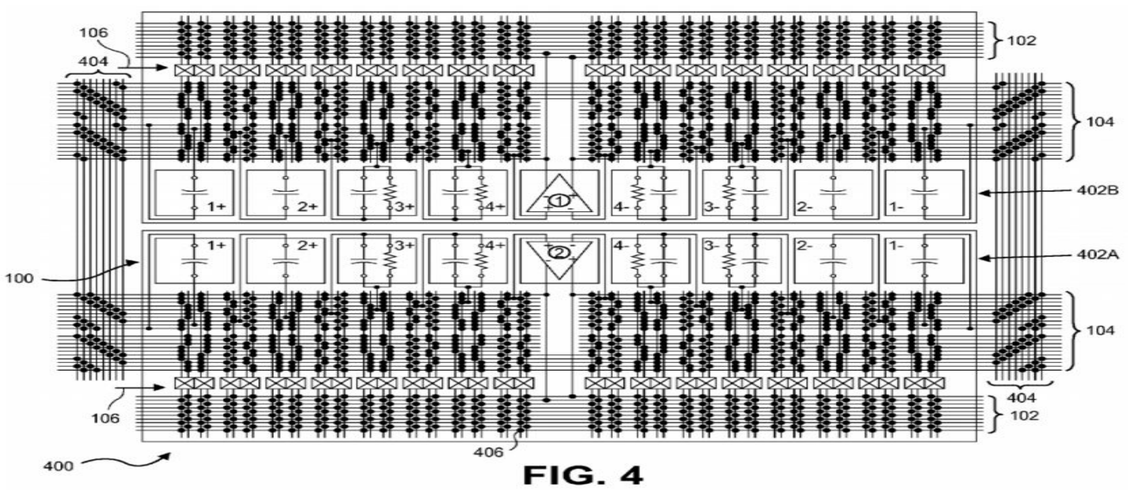


Figure 3: Architecture of FPAA with Memristors

2.1.5 Double differential comparator and programmable analog block architecture using same

Authors : James L. Gorecki,Bill G. Gazeley,Yaohua Yang
Date : 2nd March,2004
Patent no. : US6701340B1

Abstract :

A double differential comparator can be efficiently implemented utilizing a first comparator Stage having a folded cascode with floating gate input terminals and clamped Single-ended output, and a capacitively coupled input stage for transferring a weighted Sum of input Signals to the floating gates of the first comparator Stage. Additionally, the differential comparator can be integrated into fully differential programmable analog integrated circuits. Such fully differential programmable analog integrated circuits can also include a differential output digital-to-analog converter to be used with or without the double differential comparator.

Comments :

This paper is different then our product.Authors discussed mainly comparators circuits and programmability in the same.There were no use of OP-AMPs.

3 Detailed description of project

3.1 Hardware Part

3.1.1 Cross-Matrix switch IC

Programmable XMatrix switch is the heart of our project.It comes with programmable inter-connect solid state switches w/ programming,decoding,level shifting circuits.

We are using IC CD22M3494 from Renesas Electronics.It's a 16 x 2 (128 total switches)bidirectional cross-matrix switch IC.

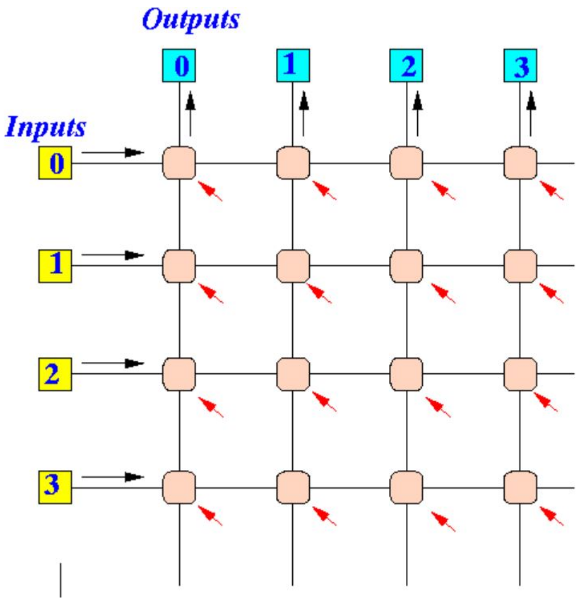


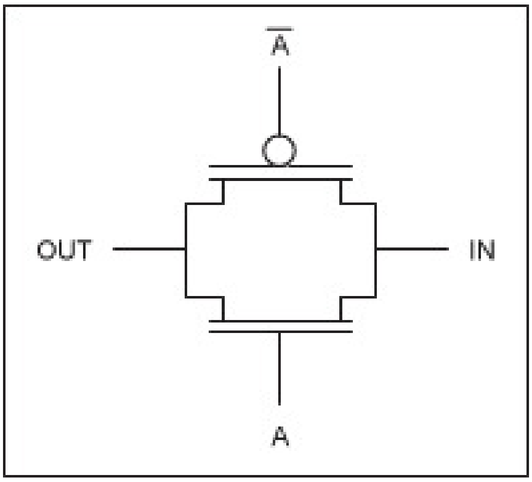
Figure 4: Cross-bar switch

Each of skin like coloured box is a **transmission gate**.It's a bidirectional FET switch controlled by logic '1' or '0'.

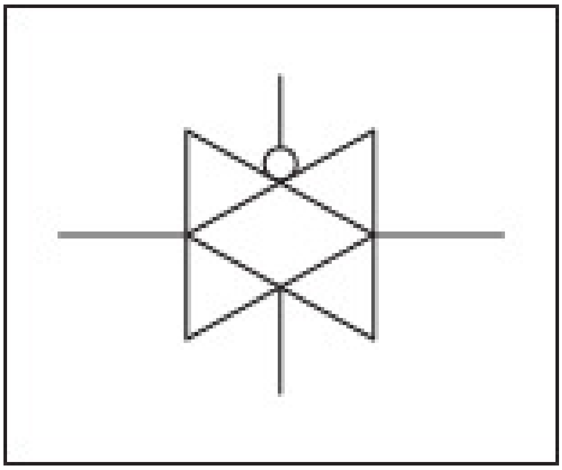
- When TG(Transmission gate) at 00 intersection is closed,Input0 is connected to output0.
- When all TGs along Input0 is closed,In0 is connected to all 4 outputs.
- When TGs at 00 and 10 is connected,then in0 and in1 is connected to each other as well.

3.1.2 Transmission Gate

A transmission gate is a electronic device,which either blocks or passes signal from input to output based on status of control signal.It's often called 'Analog switch'.



(a) Schematic



(b) Symbol

Figure 5: Transmission gate circuit and symbol

It consist of P-channel and N-channel MOSFETs in parallel,thus allowing bi-directional current flow.It permits signal to swing up-to the supply rails.Beside the 2 MOSFETs,there are additional logic circuit to make it a fully functional switch.

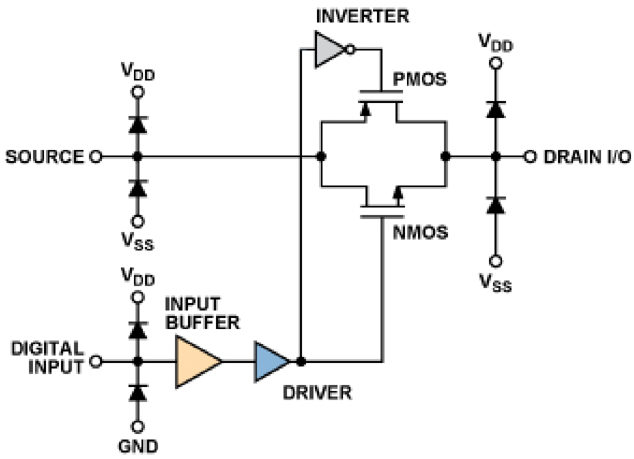


Figure 6: Analog switch circuitry

Diodes at the input and output terminals are for ESD protection.Now we know that the negative V_{GS} will break the channel in NMOS and positive V_{GS} will break channel in PMOS(considering depletion type MOSFETs as shown in figure 6 on page 10)

When positive voltage (V_{DD}) is applied at the digital input,it turns ON the NMOS and complementary negative rail from inverter will turn ON the PMOS.Now as Drain voltage approaches the gate voltage,channel begins to pinch from the drain side also known as saturation.But here is the catch,when one MOS is having it's channel pinching off,other MOS starting to having it's channel coming out of pinching and since both MOS are in parallel,it's like having 2 resistors in parallel,when one of is increasing resistance,other is decreasing hence parallel combination maintains equivalent resistance of TG fairly constant for the signal swinging upto the rails as shown in plot of resistance below...

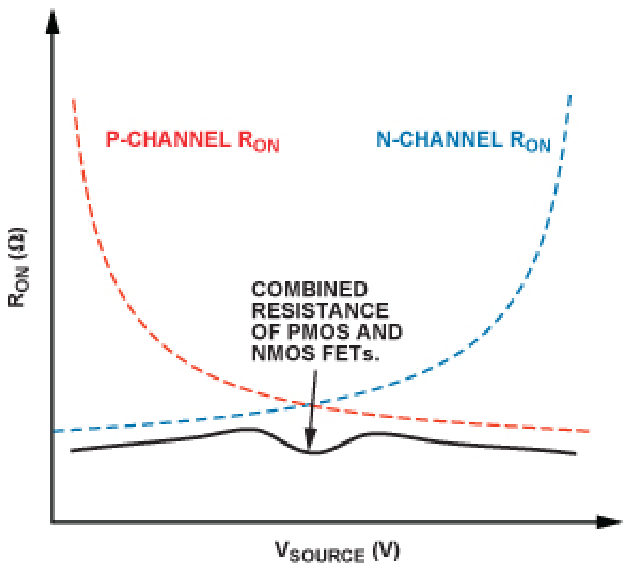


Figure 7: Analog switch R_{ON} plot

Above discussion justifies the use of TG instead of using single MOS.As in absence of body diode,a MOS can act as bidirectional switch but to have optimum performance with rail to rail swinging,we need TG.

3.1.3 More about CD22M3494

CD22M3494 is an array of 128 switches arranged in 16x8.Meaning it has 16 horizontal lines and 8 vertical lines with each intersection containing one TG.Below the block diagram of CD22M3494...

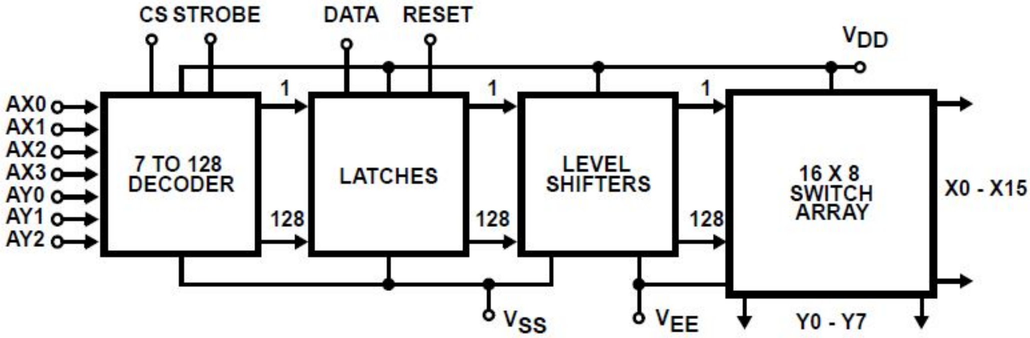


Figure 8: CD22M3494 block diagram

Now let's discuss each block one by one.At the front end we got 7 to 128 decoder which points to any one out of 128 TGs,as on 7-bit code on input.It has directly 7 bit data lines,some other commercial products do come with SPI,I2C blocks as a front end! Which occupies lesser pins of your microprocessor.The 7 bit code determines that ON or OFF command has to be given to which TG.

Latches block contains D-latches.This acts as a memory block which contains the record of ON and OFF of all 128 TGs.Data has to be written here only once.Note that it's a volatile memory and has a power on reset function,meaning in power on condition,all the TGs will be OFF by default.

RESET pin is active HIGH RESET.Upon triggered it resets outputs of the D latches to '0'.DATA pins is used to determine any TG(pointed by 7-bit code to the decoder) to ON or OFF.Writing '0' on Latches will turn OFF TG,while writing '1' on latches will turn ON TG.STROBE pin provides the clock for the latches,which are negative edge triggered.

Level shifter converts unipolar digital signal to bipolar control signal for all TGs.As input signal is swinging upto the rails.Using unipolar digital to the gates of TGs will leads you to the inappropriate results.Consider depletion type PMOS for example,if we apply logic '0' to it's gate to turn it ON,but input signal is swinging upto the rails,so when V_s is negative,it makes V_{GS} positive and reduces the conductivity of the channel.Hence if we want signal to be passed nicely with rail to rail swing then we need to convert logic levels V_{DD} and 'DGND' to V_{DD} and V_{EE}.Such cross,metrics switch ICs are mixed signal ICs,meaning it has digital and analog portions.So we need different 'DGND' and 'AGND'.Level shifter block does the job of isolating DGND from AGND.

And the last switch array block contains all TGs and 16X8 IOs.Level shifter output is given to Gates of the FETs.

- Electrical parameters of CD22M3494

Max DC supply voltage V_{DD} w.r.t V_{EE}	16 Volts
Max DC Transmission Gate current	25 mA
Typical ON resistance r_{ON}	36-40 Ω
Leakage current I_L	10 μA
-3 dB frequency response	50 MHz
Cross talk @ 1 MHz	-30 dBV(As per our own measurement)

Table 1: Electrical parameters of CD22M3494

For more information go to the datasheet of CD22M3494 *here* or the link: https://www.renesas.com/in/en/www/doc/datasheet/cd22m3494.pdf

3.1.4 ATmega64A Microcontroller

ATmega64A is an 8-bit microcontroller from AVR(Advanced Virtual RISC) family by ATMEL.It's the brain for our Prog-Analog board.The number 64 in it indicates that it has 64 Kbyte of flash(code) memory.This is the bridge between programmer and the board.It communicates with the computer via USB,with software called 'Tera Term'.It's a terminal software and it is the place where programming code will be written.Microcontroller will receive this codes and decode(comparing it with prestored and identify that which one is entered!) it,then it does 2 things,(1)make/brake switches in Xmatrix switch IC and (2)Programs the given/computed resistance values to the digital trim POT X9C103.

ATmega64 is doing the job of an interpreter.One by one it decodes and executes instructions written by the programmer.It also does the job of checking of any harmful connection for example,say you made direct connection between OP-AMP's output to the inverting input.Now if some reason if you connect inverting pin of OP-AMP to the ground then it'll short output of OP-AMP to the ground and that can damage the OP-AMP or may be it pass the current way higher then XMatrix switch IC's capabilities,thus by damaging it.All this will be done by firmware that will goes inside the chip.

Controller also points out all kinds of error that it can identify,like invalid instruction,connection error,etc.It has 2 LEDs on board on is green(for OK) and other is red(for ERROR).They will have certain blinking pattern based on which error can be displayed or it can be shown on the terminal software Tera Term.

ATmega64A is clocked from 16 MHz crystal oscillator.It's capable upto 20 MHz.Below are some features of the ATmega64A...

Operating voltage	2.7 - 5.5 Volts
Brown out detector	YES
Flash size	64 Kbyte
Watchdog timer	Available
Pin count	64
Packages	DIP,QFP,QFN
EEPROM size	2 Kbytes
USART	2
General purpose registers	32
PWM channels	8
SRAM size	2 Kbytes

Table 2: ATmega64A Features

3.1.5 OP07Cx

OP07C is another very important component.It's a precision operational amplifier from Texas Instruments.Below are the list of features it has...

- Low noise
- Low input offset voltage(60 μV)
- Wide supply range($\pm$18 Volts)
- ESD rating(HBM/CDM) upto 1000 Volts
- Differential voltage gain(at specified conditions) 400 V/mV
- GBP of 600 KHz
- slew rate is 0.3 V/μs
- CMRR of -120 dBV
- Input resistance r_i is about 33 MΩ

OP07Cx is precision OP-AMP.Meaning it has very low inherent noise,low parameters drift,low quiescent current.All of our circuit that can be synthesized on,will contain a OP-AMP.We are using 3 OP07C OP-AMPs in our design.We got one OP-AMP and digital POTs(X9C103),fixed capacitors,XMatrix switch build around it as a one block.We have such 3 blocks on our board.

Each block's output can be fed directly to any other block including the block itself.Thus allowing cascading of the blocks.Allows to implement n-order filters(in our case n is 3).For example each block can synthesize 1^{st} order butterworth filter,then all blocks can be cascaded by providing output from each block to the input of next block and we can synthesize 3^{rd} order butterworth filter.Now any block can get input from any other block e.g. feedback from 3^{rd} block to 1^{st} block.Thus allowing to synthesize more complex circuits like bi-quad filters like circuits.OP07C's input offset voltage is not that impressive but it does come with offset null pins.We have trim pot connected with null pins hence you can reduce the offset voltage by adjusting it.

3.1.6 Digital potentiometer - X9C103

Digital POT is another very important component in our project.It allows to synthesize the resistance of whatever value we want.Now trim pots has infinite resolution or extremely tiny step size is achievable,but the digital POT is as it name suggests is digital(discrete) and has some what bigger step size.Step size means the amount of resistance it can increase/decrease.Digital POTs are available in resistance range like 100Ω,1KΩ,10KΩ,100KΩ.Each has different step size,higher the value higher the step size.For the all resistance values shown before the step size is 1Ω,10Ω,100Ω, and 1KΩ respectively.

X9Cxxx are the digital POTs from Intersil as 8-pin IC.They are bit too costly but looking to their performance with lower parasitics,it totally worth it!All discussion above and from now are for particular X9Cxxx series digital POTs.They have array of fixed value resistance etched out on a silicon die along with wiper switches,control section and interface section,and small non-volatile memory.

- Features of the X9C103

Supply voltage V_{CC}	5 Volts
Max voltage on V_H and V_L w.r.t V_{SS}	±8 Volts
ΔV =—V_H - V_L—	10 Volts
Max wiper current(I_W)	10 mA
Power rating	10 mW
Wiper resistance	40 Ω
Wiper parasitic capacitance	25 pF
Resistance variation	±20 %
Temperature coefficient	±300 PPM/°C

Table 3: X9C103 Features

Working of the X9C103 is very simple.103 number indicates it is the 10KΩ POT.It has a step size of 100 Ω.Step size also referred as the resolution.Which is 1% of the POT's value.This is the amount by which resistance value is increased/decreased.

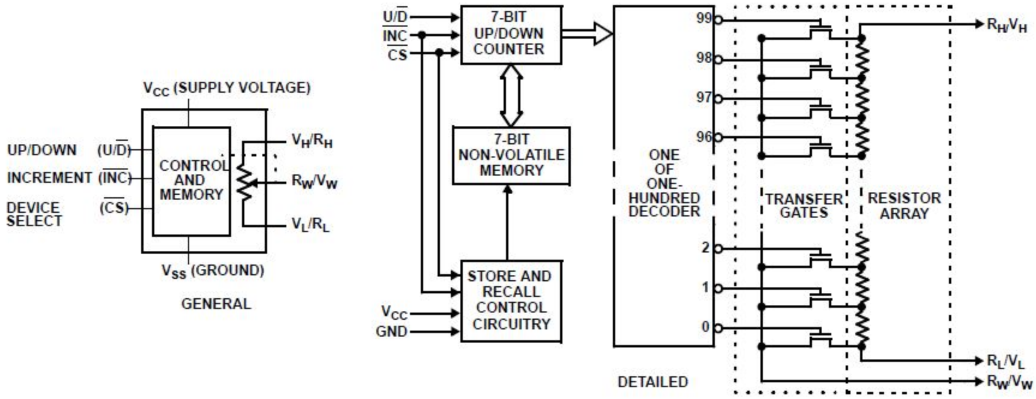


Figure 9: X9C103 Block diagram

There are 100 resistors of about the same values are built in.Each is of value equals to the resolution(i.e 100 Ω for the our case).Now as shown in the figure : 9 there are 100 pass transistors as well.All of which is controlled by binary to decimal decoder for 0 to 99.When for example 50^{th} transistor is turned on,all the resistance before that will come in series and adds up their resistance.You see that it has 3 terminals V_H,V_W and V_L because it's a POT.There are ICs available as a digital rheostats which comes with only 2 terminals.

Now the controlling action.It has 3 pins for the controlling of the DPOT.Datasheet say it as a 3 - wire interface.Those pins are U/$\overline{D}$,$\overline{INC}$,$\overline{CS}$.It has 7-bit UP/DOWN counter on chip,who's output is given to decoder which decodes 0 to 99 and resets to 0 in other cases.U/$\overline{D}$ pin decides whether to UP count or DOWN count.$\overline{CS}$ for chip select use full when we have chained the number of X9C103s like in our case.$\overline{INC}$ for the input pulse which acts as a clock input for the UP/DOWN counter.Getting to the any resistor is like getting higher gears in bike.You have to start from the lower gears.Same is the case with this,we have to start from the lower resistance and goes up to the max limit and roll off back to the lower.Lower limit is not the *dead short* but it's equal to wiper resistance mentioned in table 3.

It also consists a 7-bit EEPROM.Where any 7-bit code from the counter can be stored and it will be applied to decoder after *POWER ON RESET* as a default.By taking $\overline{CS}$ pin to HIGH while keeping the $\overline{INC}$ to HIGH will copy the content of the counter into the EEPROM.

3.1.7 Power supply design

For our board we require dual rail power supply as normal OP-AMP based circuits need.We designed ±5 Volt power supply,with old style linear regulator based design.We have used L7805 for +5 Volts and L7905v for -5 Volts.Each has current delivering capacity of 1.5 Amps which is way more then what we need!

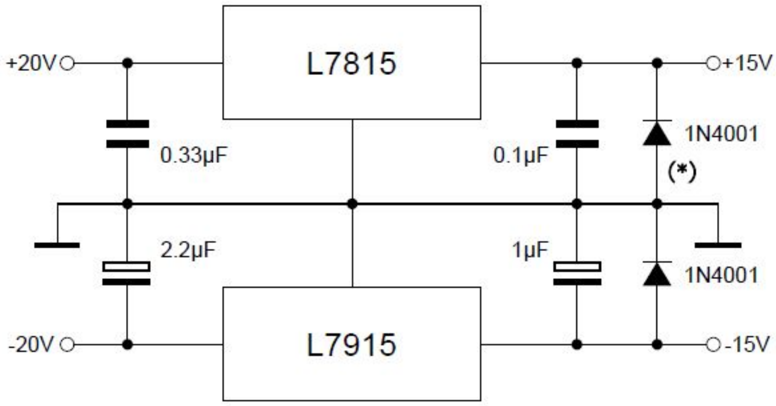


Figure 10: Power supply circuit

One down side of the L78xx and L79xx based design is that it's high noise.Noise level is as high as 200 μV_{RMS}.Noise level is not good if we want to have some audio processing using the prog-analog board.We have used it's SMD version,the package D^2PAK.The front end has step-down transformer then the FBR and then the circuit shown in the figure 10.

3.1.8 Quad SPST solid state switch - ADG202A

Initially we wanted to have NCD2100 IC,which is digital variCAP.It's design and working is pretty much same as X9C103.It has pre-built capacitors array and series pass transistors.But due to it's high cost,low capacitance value(few pico-Farads only),unavailability in Indian market,we droped it.There no other alternatives to that IC with higher capacitance value and lower cost.It seems that all those ICs are designed to be implemented in high frequency designs upto hundreds of MHz,but our requirement is different.We have moderate frequency OP-AMPs and we have designed our board by keeping the 100 kHz limit in mind.

So we decided that we will go with the fixed values passive capacitors.We chose all ceramic capacitors because of it's low cost,wide range of values,small size and it's non polarized.We have used SMD(CDC and MLCC) ceramic capacitors.So we have now DPOT and fixed value capacitors.But we still want some choices on the fixed value capacitor so we decided to put lot off fixed value capacitors with interconnect switches so that user can select between fixed value capacitors.For that some of capacitors are directly connected to the XMatrics switch but there are already lot of components connected with XMatrix,so we included another small switching IC.

IC is ADG202A.It's a 4 channel,SPST solid state switch from Analog devices.We have selected it because of it's low cost and availability to the local vendor.

Max supply voltage range	44 Volts
Signal range	±15 Volts
ON resistance(R_{ON})	60 Ω
Leakage current I_L	0.5 nA
Power dissipation	33 mW
Cross talk	-80 dB
Parasitic capacitances(C_S and C_D)	5 pF

Table 4: ADG202A features

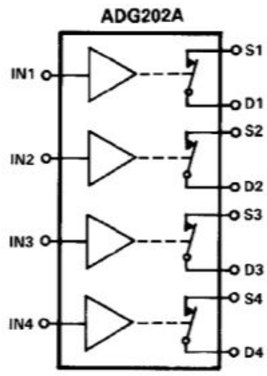
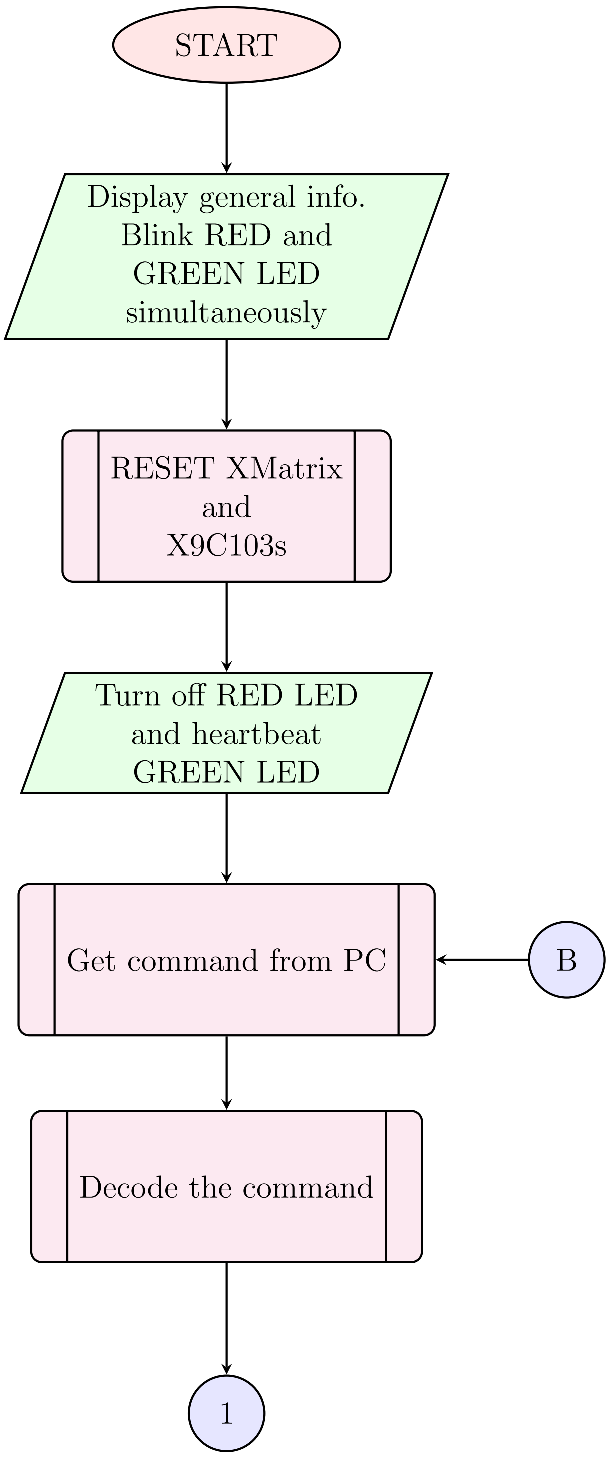
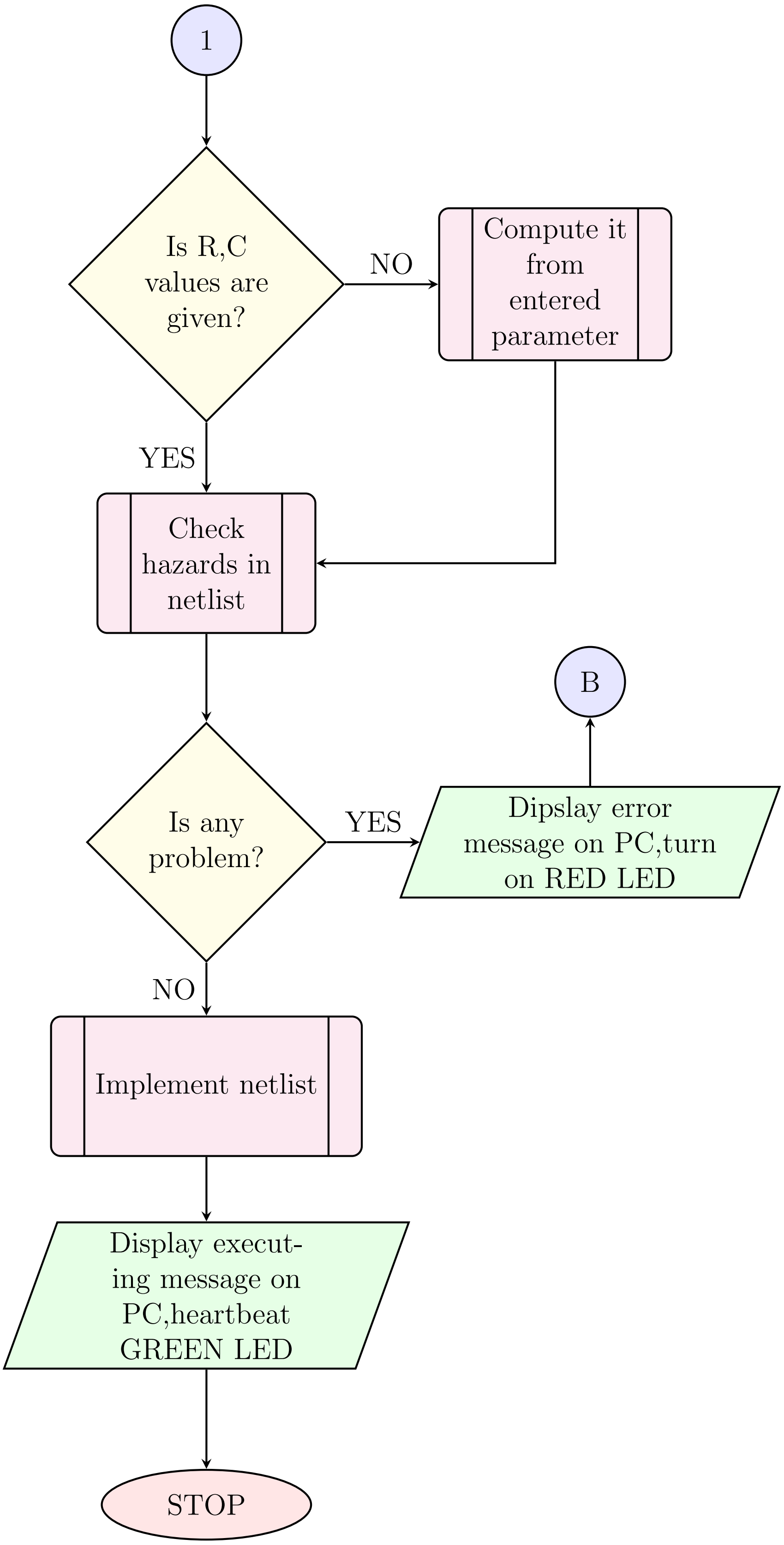


Figure 11: ADG202A

3.2 Software Part

3.2.1 Main program




1
Is R,C values are given?
NO
Compute it from entered parameter
YES
Check hazards in netlist
B
Is any problem?
YES
Dipslay error message on PC,turn on RED LED
NO
Implement netlist
Display executing message on PC,heartbeat GREEN LED
STOP

4 Outcome of the project

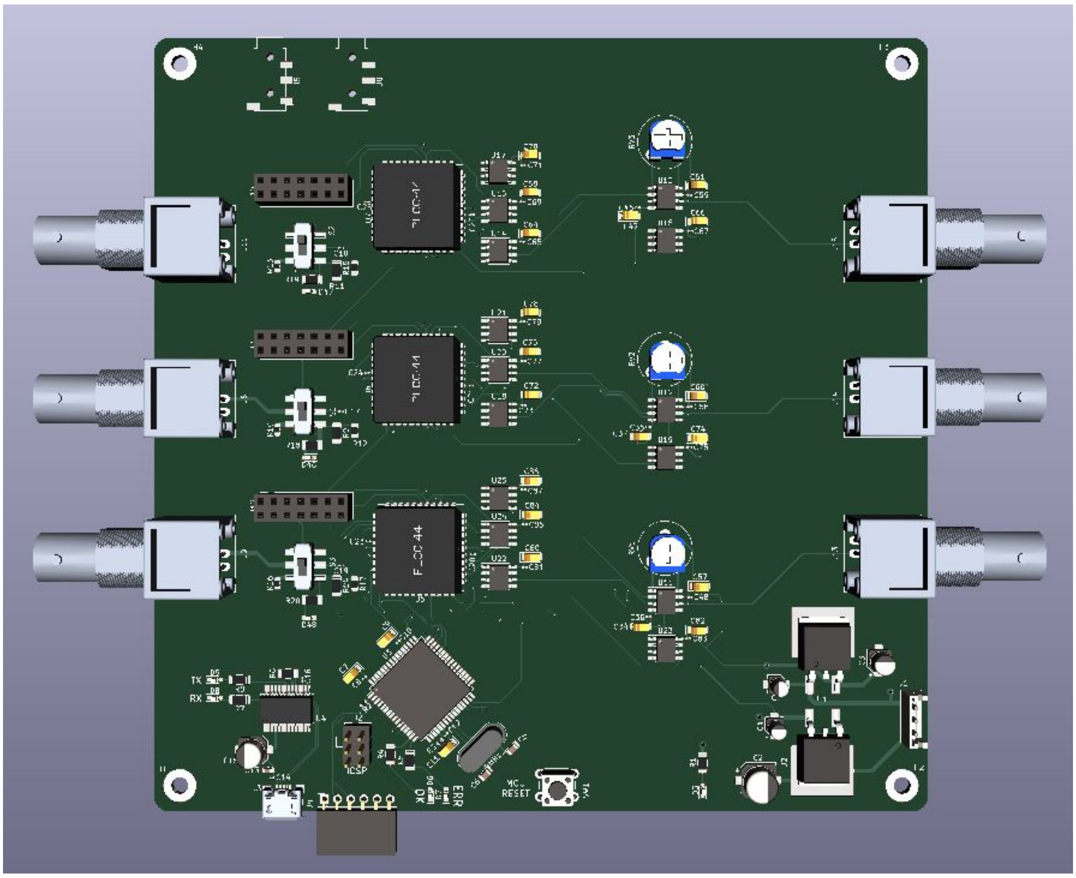


Figure 12: Virtual 3D model of Prog-Analog board

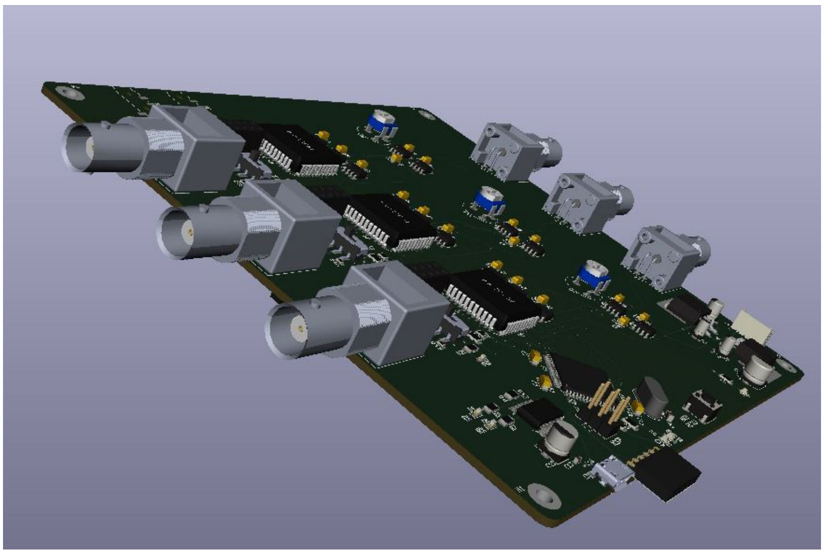
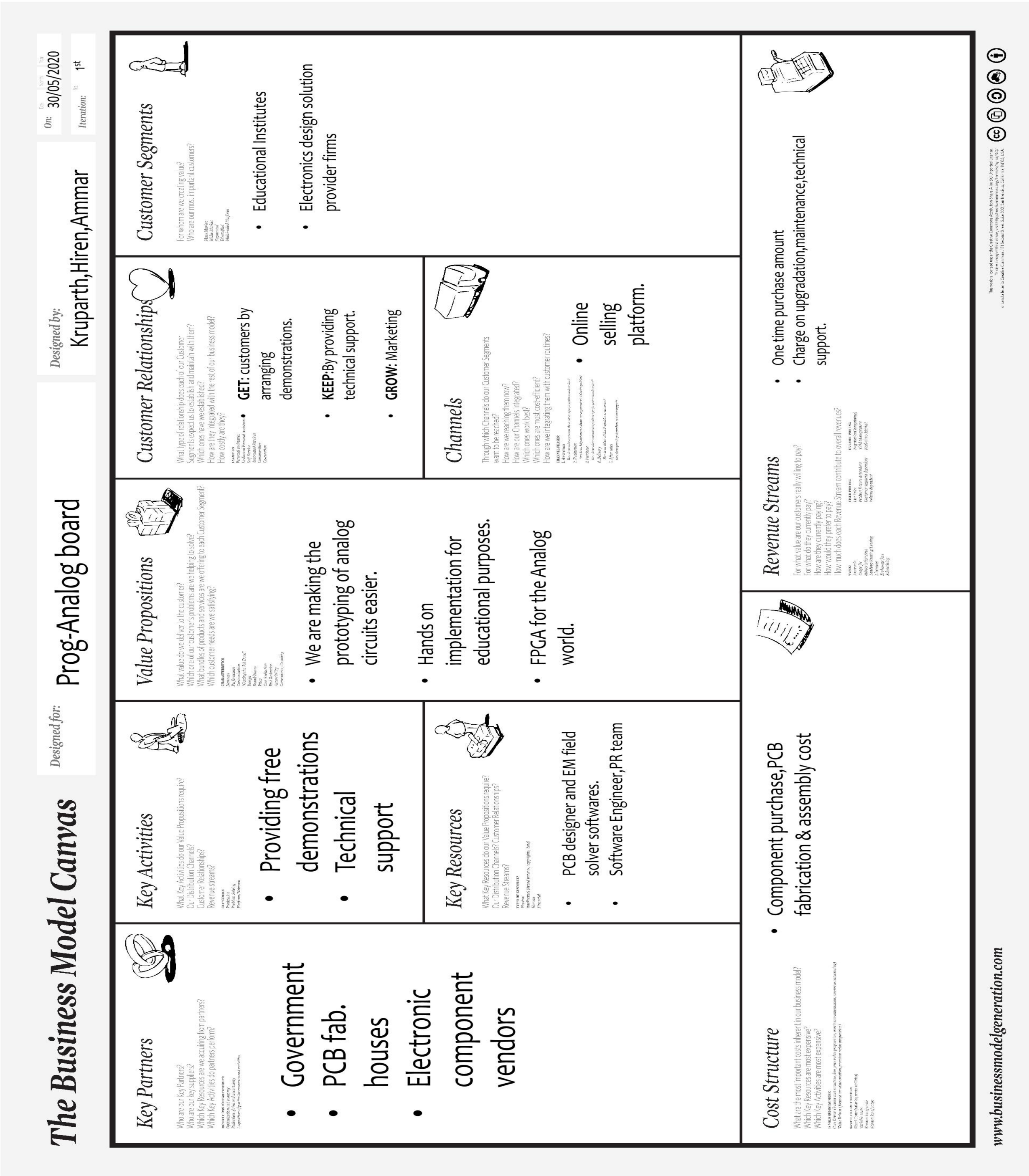


Figure 13: Side view

Comments on board design

Pictures on the page no.21 shows the virtual 3D look of our Prog-Analog board.It's a 2 layer PCB with components on both the side.Power supply on the bottom right,microcontroller with USB 2.0 support hardware on bottom left(see figure 12).In middle we have 3 CD22M3494 XMatrix switch ICs.We have 6 BNC connectors,3 for Input and 3 for Output.So it's much convenient to provide input directly from the function generator.Total 180+ components.OP-AMPs on the right portion of the board with offset trim POTs,directly connected to Output BNCs.Top left we got 2 Audio SMD female jacks for Audio input.Female header is also provided for each block for extra inputs and external components connection.Slider switch is given for setting the Input impedance to either HIGH-Z or 50 Ω.Small LED for indication of 50 Ω.At the bottom we have *ERROR* RED LED and GREEN *OK* LED.

5 Business Model Canvas



6 Conclusion

In the world of simulations.designers need their designs to be quickly implemented on the lab for testing purposes.In Electronic industry simulation and practical implementation,both are necessary.Special emphasis on practical implementation is given,because electronics can behave differently when are assembled.For the lack of field programmable boards for Analog world is not acceptable.Our project is partially fulfilling that requirement.With development of programming software,this thing can come out loud in future!

Appendix - 1 : Patent Drafting Exercise

College	:	G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR
Department	:	Electronics & Communication Engineering
Discipline	:	BE
Semester	:	Semester 8
Project Name	:	Prog-Analog : The programmable analog board
Team ID	:	81880

Form 1 – APPLICATION FOR GRANT OF PATENT

Applicants :

Sr. No	Name	Nationality	Address	Mobile No.	Email Id
1	Patel Kruparth	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	9512505290	patelkruparth3004@gmail.com
2	Moradiya Hiren Dineshbhai	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	9737398473	hirenmoradiya704@gmail.com
3	Vahora Ammarbhai Munafbhai	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	7383683968	ammarzamzam41@gmail.com

Inventors :

Sr. No	Name	Nationality	Address	Mobile No.	Email Id
1	Patel Kruparth	Indian	Electronics & Communication	9512505290	patelkruparth3004@gmail.com

			Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.		
2	Moradiya Hiren Dineshbhai	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	9737398473	hirenmoradiya704@gmail.com
3	Vahora Ammarbhai Munafbhai	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	7383683968	ammarzamzam41@gmail.com

I/We, the applicant(s) hereby declare(s) that:

Following are the attachments with the applications :

Form 2 - PROVISIONAL/COMPLETE SPECIFICATION

1 . Title of the project/invention :
Prog-Analog : The programmable analog board

2. Preamble to the description :
Provisional

3. Description
a) Field of Project / Invention / Application :
None

b) Prior Art / Background of the Project / Invention :
None

c) Summary of the Project / Invention :
None

d) Objects of Project / Invention :

None

e) Drawings :

f) Description of Project / Invention : (full detail of project) :

None

g) Examples :

None

h) Claims (Not required for Provisional Application) / Unique Features of Project

None

4. Claims

5. Date and signature

6. Abstract of the project / invention :

None

Form 3 – STATEMENT AND UNDERTAKING UNDER SECTION 8

Name of the applicant(s) :	I/We, Patel Kruparth ,Moradiya Hiren Dineshbhai ,Vahora Ammarbhai Munafbhai Hereby declare :
Name,Address and Nationality of the joint applicant :	(i) that I/We have not made any application for the same/substantially the same victim invention outside India. (ii) that the rights in the application(s) has/have been assigned to

Name of the Country	Date of Application	Application Number	Status of the Application	Date of Publication	Date of Grant
N/A	N/A	N/A	N/A	N/A	N/A

(iii)That I/We undertake that upto the date of grant of the patent by the Controller, I/We would keep him informed in writing the details regarding corresponding applications for patents filed outside India within three months from the date of filing of such application.

Dated this 29 day of May 2020

To be signed by the applicant or his authorised registered patent agent :	Signature................
Name of the Natural Person who has signed :	Patel Kruparth ,Moradiya Hiren Dineshbhai ,Vahora Ammarbhai Munafbhai

To,
The Controller of Patents,
The Patent Office,
At Mumbai

College : G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR
Department : Electronics & Communication Engineering
Discipline : BE
Semester : Semester 8
Project Name : Prog-Analog : The programmable analog board
Team ID : 81880

Form 1 – APPLICATION FOR GRANT OF PATENT

Applicants :

Sr. No	Name	Nationality	Address	Mobile No.	Email Id
1	Patel Kruparth	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	9512505290	patelkruparth3004@gmail.com
2	Moradiya Hiren Dineshbhai	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	9737398473	hirenmoradiya704@gmail.com
3	Vahora Ammarbhai Munafbhai	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	7383683968	ammarzamzam41@gmail.com

Inventors :

Sr. No	Name	Nationality	Address	Mobile No.	Email Id
1	Patel Kruparth	Indian	Electronics & Communication	9512505290	patelkruparth3004@gmail.com

			Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.		
2	Moradiya Hiren Dineshbhai	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	9737398473	hirenmoradiya704@gmail.com
3	Vahora Ammarbhai Munafbhai	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	7383683968	ammarzamzam41@gmail.com

I/We, the applicant(s) hereby declare(s) that:

Following are the attachments with the applications :

Form 2 - PROVISIONAL/COMPLETE SPECIFICATION

1 . Title of the project/invention :

Prog-Analog : The programmable analog board

2. Preamble to the description :

Provisional

3. Description

a) Field of Project / Invention / Application :

Embedded field, Analog electronics, signal processing

b) Prior Art / Background of the Project / Invention :

We found the need for programmable analog board while working on our small audio amplifier project, and way to implement that form current FPGA boards.
We can simulate analog circuits but cannot implement it directly on something which can give us the real-time

output. Something like this can be used in the validation of your circuit if your concerns are only about functionality.

c) Summary of the Project / Invention :

Programmable circuits are very popular in the field of digital electronics in the form of FPGAs. Something likes that lake in analog word. We tried to fulfill that thing, by designing something capable to synthesize not all but some of the frequently used analog circuits. Now there is n number of challenges in prototyping something like that. There are some ICs available that have the capability of digital tuning. We'll use that to achieve the desired value of resistors & capacitors. We use JFETs to achieve switching to synthesize circuits. There are no hardware description languages like in VHDL, VeriLOG exists for analog so we've to find a solution to it. And at the last even after prototyping such a thing.

d) Objects of Project / Invention :

The main objective behind this project is to create something like FPGA boards for the analog world. For the quick prototyping of analog circuits, to get rid of messy breadboarding.reducing the time and perform various analog operation easily.

e) Drawings :

f) Description of Project / Invention : (full detail of project) :

Electronic switching is the basic requirement to achieve programmability in-circuit synthesization. Instead of a fixed connection, we need a variable connection between different components. Prototyping of analog circuits is hair stretching work and often gets complicated because one has to work with a breadboard. To eliminate the breadboarding of big digital systems, FPGAs were developed over the past years for prototyping purposes. We have come up with similar things for the analog world. It's like FPGA, but instead of digital, it will create analog circuits like integrator, differentiator, adder based on coding. We have one plan to make it possible. FPGAs use RTL coding like VHDL/verilog and has their own s/w which converts coding to circuit netlist and which gets implemented in FPGAs, now at this stage we don't have that much knowledge to develop our own synthesizer s/w, hence we'll use the following plan.
We will have OP-AMPs in the circuit, and passive components that can change its value based on programming. For resisters, we use something known as digital POTs and for capacitors NCD2100 which is a digital programmable variable capacitor. We'll have interconnection between all of them via FETs, which will act as programmable switches. Now for programming, one has to write commands, which will be decoded by ASCII codes, and accordingly switch matrix is programmed to form the desired circuit. There is a digital circuit that accepts ASCII bits and programs solid state switches. And with this one can able to implement amps, integrators, differentiators, adders, instrument amplifiers, and combination of all above. Application of this thing can be found in prototyping, educational purposes & implementation of PID controllers.

g) Examples :

h) Claims (Not required for Provisional Application) / Unique Features of Project

Microcontroller, a digitally tunable resister and capacitors, op-Amps, digitally switching circuit, USB port, and other ICs.

4. Claims

5. Date and signature

6. Abstract of the project / invention :

Programmable circuits are very popular in the field of digital electronics in the form of FPGAs. Something likes that lake in analog word. We tried to fulfill that thing, by designing something capable to synthesize not all but some of the frequently used analog circuits. Now there is n number of challenges in prototyping something like that. There are some ICs available that have the capability of digital tuning. We'll use that to achieve the desired value of resistors & capacitors. We use JFETs to achieve switching to synthesize circuits. There are no hardware description languages like in VHDL, VeriLOG exists for analog so we've to find a solution to it. And at the last even after prototyping such a thing.

Form 3 – STATEMENT AND UNDERTAKING UNDER SECTION 8

Name of the applicant(s) :	I/We, Patel Kruparth ,Moradiya Hiren Dineshbhai ,Vahora Ammarbhai Munafbhai Hereby declare :
Name,Address and Nationality of the joint applicant :	(i) that I/We have not made any application for the same/substantially the same victim invention outside India.

(ii) that the rights in the application(s) has/have been assigned to

Name of the Country	Date of Application	Application Number	Status of the Application	Date of Publication	Date of Grant
N/A	N/A	N/A	N/A	N/A	N/A

(iii)That I/We undertake that upto the date of grant of the patent by the Controller, I/We would keep him informed in writing the details regarding corresponding applications for patents filed outside India within three months from the date of filing of such application.

Dated this 29 day of May 2020

To be signed by the applicant or his authorised registered patent agent :	Signature.................
Name of the Natural Person who has signed :	Patel Kruparth ,Moradiya Hiren Dineshbhai ,Vahora Ammarbhai Munafbhai

To,
The Controller of Patents,
The Patent Office,
At Mumbai

College : G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR
Department : Electronics & Communication Engineering
Discipline : BE
Semester : Semester 8
Project Name : Prog-Analog : The programmable analog board
Team ID : 81880

Form 1 – APPLICATION FOR GRANT OF PATENT

Applicants :

Sr. No	Name	Nationality	Address	Mobile No.	Email Id
1	Patel Kruparth	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	9512505290	patelkruparth3004@gmail.com
2	Moradiya Hiren Dineshbhai	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	9737398473	hirenmoradiya704@gmail.com
3	Vahora Ammarbhai Munafbhai	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	7383683968	ammarzamzam41@gmail.com

Inventors :

Sr. No	Name	Nationality	Address	Mobile No.	Email Id
1	Patel Kruparth	Indian	Electronics & Communication	9512505290	patelkruparth3004@gmail.com

			Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.		
2	Moradiya Hiren Dineshbhai	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	9737398473	hirenmoradiya704@gmail.com
3	Vahora Ammarbhai Munafbhai	Indian	Electronics & Communication Engineering , G. H. PATEL COLLEGE OF ENGINEERING & TECHNOLOGY, V V NAGAR , Gujarat Technologycal University.	7383683968	ammarzamzam41@gmail.com

I/We, the applicant(s) hereby declare(s) that:

Following are the attachments with the applications :

Form 2 - PROVISIONAL/COMPLETE SPECIFICATION

1 . Title of the project/invention :

Prog-Analog : The programmable analog board

2. Preamble to the description :

Provisional

3. Description

a) Field of Project / Invention / Application :

Embedded field, Analog electronics, signal processing

b) Prior Art / Background of the Project / Invention :

We found the need for programmable analog board while working on our small audio amplifier project, and way to implement that form current FPGA boards.
We can simulate analog circuits but cannot implement it directly on something which can give us the real-time

output. Something like this can be used in the validation of your circuit if your concerns are only about functionality.

c) Summary of the Project / Invention :

Programmable circuits are very popular in the field of digital electronics in the form of FPGAs. Something likes that lake in analog word. We tried to fulfill that thing, by designing something capable to synthesize not all but some of the frequently used analog circuits. Now there is n number of challenges in prototyping something like that. There are some ICs available that have the capability of digital tuning. We'll use that to achieve the desired value of resistors & capacitors. We use JFETs to achieve switching to synthesize circuits. There are no hardware description languages like in VHDL, VeriLOG exists for analog so we've to find a solution to it. And at the last even after prototyping such a thing.

d) Objects of Project / Invention :

The main objective behind this project is to create something like FPGA boards for the analog world. For the quick prototyping of analog circuits, to get rid of messy breadboarding.reducing the time and perform various analog operation easily.

e) Drawings :

f) Description of Project / Invention : (full detail of project) :

Electronic switching is the basic requirement to achieve programmability in-circuit synthesization. Instead of a fixed connection, we need a variable connection between different components. Prototyping of analog circuits is hair stretching work and often gets complicated because one has to work with a breadboard. To eliminate the breadboarding of big digital systems, FPGAs were developed over the past years for prototyping purposes. We have come up with similar things for the analog world. It's like FPGA, but instead of digital, it will create analog circuits like integrator, differentiator, adder based on coding. We have one plan to make it possible. FPGAs use RTL coding like VHDL/verilog and has their own s/w which converts coding to circuit netlist and which gets implemented in FPGAs, now at this stage we don't have that much knowledge to develop our own synthesizer s/w, hence we'll use the following plan.
We will have OP-AMPs in the circuit, and passive components that can change its value based on programming. For resisters, we use something known as digital POTs and for capacitors NCD2100 which is a digital programmable variable capacitor. We'll have interconnection between all of them via FETs, which will act as programmable switches. Now for programming, one has to write commands, which will be decoded by ASCII codes, and accordingly switch matrix is programmed to form the desired circuit. There is a digital circuit that accepts ASCII bits and programs solid state switches. And with this one can able to implement amps, integrators, differentiators, adders, instrument amplifiers, and combination of all above. Application of this thing can be found in prototyping, educational purposes & implementation of PID controllers.

g) Examples :

h) Claims (Not required for Provisional Application) / Unique Features of Project

Microcontroller, a digitally tunable resister and capacitors, op-Amps, digitally switching circuit, USB port, and other ICs.

4. Claims

5. Date and signature

6. Abstract of the project / invention :

Programmable circuits are very popular in the field of digital electronics in the form of FPGAs. Something likes that lake in analog word. We tried to fulfill that thing, by designing something capable to synthesize not all but some of the frequently used analog circuits. Now there is n number of challenges in prototyping something like that. There are some ICs available that have the capability of digital tuning. We'll use that to achieve the desired value of resistors & capacitors. We use JFETs to achieve switching to synthesize circuits. There are no hardware description languages like in VHDL, VeriLOG exists for analog so we've to find a solution to it. And at the last even after prototyping such a thing.

Form 3 – STATEMENT AND UNDERTAKING UNDER SECTION 8

Name of the applicant(s) :	I/We, Patel Kruparth ,Moradiya Hiren Dineshbhai ,Vahora Ammarbhai Munafbhai Hereby declare :
Name,Address and Nationality of the joint applicant :	(i) that I/We have not made any application for the same/substantially the same victim invention outside India.
	(ii) that the rights in the application(s) has/have been assigned to

Name of the Country	Date of Application	Application Number	Status of the Application	Date of Publication	Date of Grant
N/A	N/A	N/A	N/A	N/A	N/A

(iii)That I/We undertake that upto the date of grant of the patent by the Controller, I/We would keep him informed in writing the details regarding corresponding applications for patents filed outside India within three months from the date of filing of such application.

Dated this 29 day of May 2020

To be signed by the applicant or his authorised registered patent agent :	Signature.................
Name of the Natural Person who has signed :	Patel Kruparth ,Moradiya Hiren Dineshbhai ,Vahora Ammarbhai Munafbhai

To,
The Controller of Patents,
The Patent Office,
At Mumbai

Appendix - 2 : Plagiarism Report

Plagiarism Checker X Originality Report

This report is generated by the Unregistered PlagiarismCheckerX **Demo version!**

Plagiarism Quantity: 0% Duplicate

Date	Saturday, May 30, 2020
Words	0 Plagiarized Words / Total 161 Words
Sources	More than 1 Sources Identified.
Remarks	No Plagiarism Detected - Your Document is Healthy.

Appendix - 3 : References

References

[1] Analog Filter Design by M.E.Van Valkenburg,Holt - Saunders International Edition,ISBN - 4-8338-0091-3

[2] CD22M3494 datasheet
https://www.renesas.com/in/en/www/doc/datasheet/cd22m3494.pdf

[3] ATmega64A datasheet
http://ww1.microchip.com/downloads/en/DeviceDoc/atmel-8160-8-bit-avr-microcontroller-atmega64a-datasheet.pdf

[4] FT232R datasheet
https://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT232R.pdf

[5] X9C103 datasheet
https://www.renesas.com/in/en/www/doc/datasheet/x9c102-103-104-503.pdf

[6] ADG202A datasheet
https://www.analog.com/media/en/technical-documentation/data-sheets/ADG201A_202A.pdf

[7] OP07C datasheet
http://www.ti.com/lit/ds/symlink/op07c.pdf

[8] L7805 datasheet
https://www.st.com/resource/en/datasheet/l78.pdf

[9] Analog Devices web-reference
https://www.analog.com/en/analog-dialogue/articles/switch-and-multiplexer-design-for-hostile-environ.html

[10] Maxim Integrated web-reference
https://www.maximintegrated.com/en/design/technical-documents/tutorials/4/4243.html