(PCC-02) Microprocessors

Teaching Scheme	Evaluation Scheme
Lectures: 3 Hrs/ Week Labs: 2Hr. / Week Self Study: 1 Hour/week	**Theory:** MES:30 Marks, TA:10 Marks ESE:60 Marks **Laboratory**: CIE:100 Marks

Course Outcomes

Upon completion of this course students will be able to:

1. **Design** a microcomputer around 8086b CPU in minimum mode
2. **Explain** importance of power on reset circuit in the microcomputer
3. **Develop** assembly language programs for 8086 CPU
4. **Explain and write** programs for dedicated interrupts (Break Point, Overflow) of 8086
5. **Design and Test** interfacing of 8255, 8279, 8259, 8251,DMA and interfacing of 8237 to 8086
6. **Design** maximum mode CPU module for coprocessor configuration and multiprocessor system for local bus and system bus

Course Contents

Design of Microcomputer: Von Pneumann's Principle, 8086 Architecture, Advantages of pipelining and segmentation, Simultaneityand concurrency, Demultiplexing of address and data bus, ALE, Even and Odd Bank, BHE, Static memory organisation, Design of memory map, Design of Interfacing of static memory to 8086.Reset in, Power on Reset Circuit, Bus cycle, Instruction cycle, Organising program for Basic Input Output System or Boot Strap loader after reset, clock input, 8284 clock driver, Design of minimum mode CPU module. **[8 Hrs]**

Programming with 8086: Programming modelof 8086,Physical Address, Segment Address and Logical address/offset, Addressing modes, Instruction codes, default segment assignment, Instruction Groups, Flags, Important instructions of the group, flags, prefixes. Programming in Assembly Language of 8086. I/O interfacing. I/O mapped I/O versus Memory mapped I/O. In and OUT. Interfacing of 8 bit input port and outport in I/O mapped I/O mode. Disadvantage of memory mapped I/O in design of multitasking Microcomputer. **[8 Hrs]**

Interrupts: Interrupt structure of 8086, Dedicated Interrupts, flags associated with interrupts, hardware interrupts, non vectoredinterrupt, INTR and INTA, Software Interrupts **[4 Hrs]**

I/O Interafcing: Program driven data transfer versus Interrupt driven data transfer, Interfacing design and demonstrating modes of 8255, simple I/o, Strobed input and output, bidirectional strobed I/O, BSR, 8279, encoded and decoded scan, 2 key lockout and N key rollover, sensor matrix, strobed keyboard, 8259, EOI, Non specific and specific EOI, Priority structure, Initialisation and Operational Command words, cascaded mode, buffered and non buffered **[6 Hrs]**

Serial Communication, DMA mode: Serial I/O, Asynchronous and synchronous mode, design of serial communication using 8251 USART and RS232C drivers, Direct Memory Access and Interfacing of 8237 **[4 Hrs]**

Multiprocessing in 8086: Design of maximum mode CPU module, 8288 bus controller and 8289 bus arbiter, coprocessor configuration, Introduction to NDP8087, Resident Bus and System bus, loosely coupled and closely coupled configuration. Protected mode of 80286 for improved memory management and task switching for multiprogramming or multitasking, PVAM, Register set, segment descriptors, selector, virtual address space, single level and multiple level tasks, cache memory and its management **[8 Hrs]**

Self Study Unit:

- *Emu86 or suitable assembler, Study of assembler directives, Instruction templates, No. of Bus cycles and clock cycles for execution of instructions, All instructions of 8086, Prefixes, Programming practice in assembly language of 8086,*
- *Function calls of DOS and BIOS Interrupts for display and keyboard of IBM PC*
- *Interfacing and programming for 4x4 keymatrix and 4 seven segment multiplexed displays to 8255*

[8 Hrs]

Note:

- All the Course outcomes 1 to 3 will be judged by 75% of the questions and outcomes 4, 5 and 6 will be judged by 25 % of questions.
- To measure CO3 and CO4, some questions may be based on self-study topics

Text Book:

John P Uffenbeck, The 8086/8088 Family Design, Programming and Interfacing, PHI

Reference Books

Yu-Cheng Liu, Glenn A. Gibson, Microcomputer Systems: The 8086/8088 family Architecture, Programming and Design II Edition