COMPUTER COMPONENTS & DESIGN

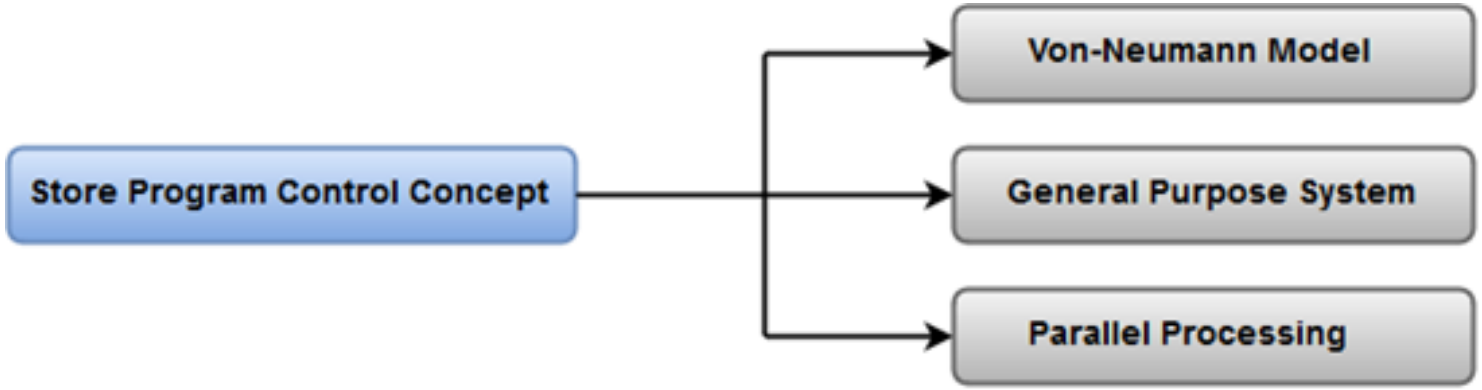
I2

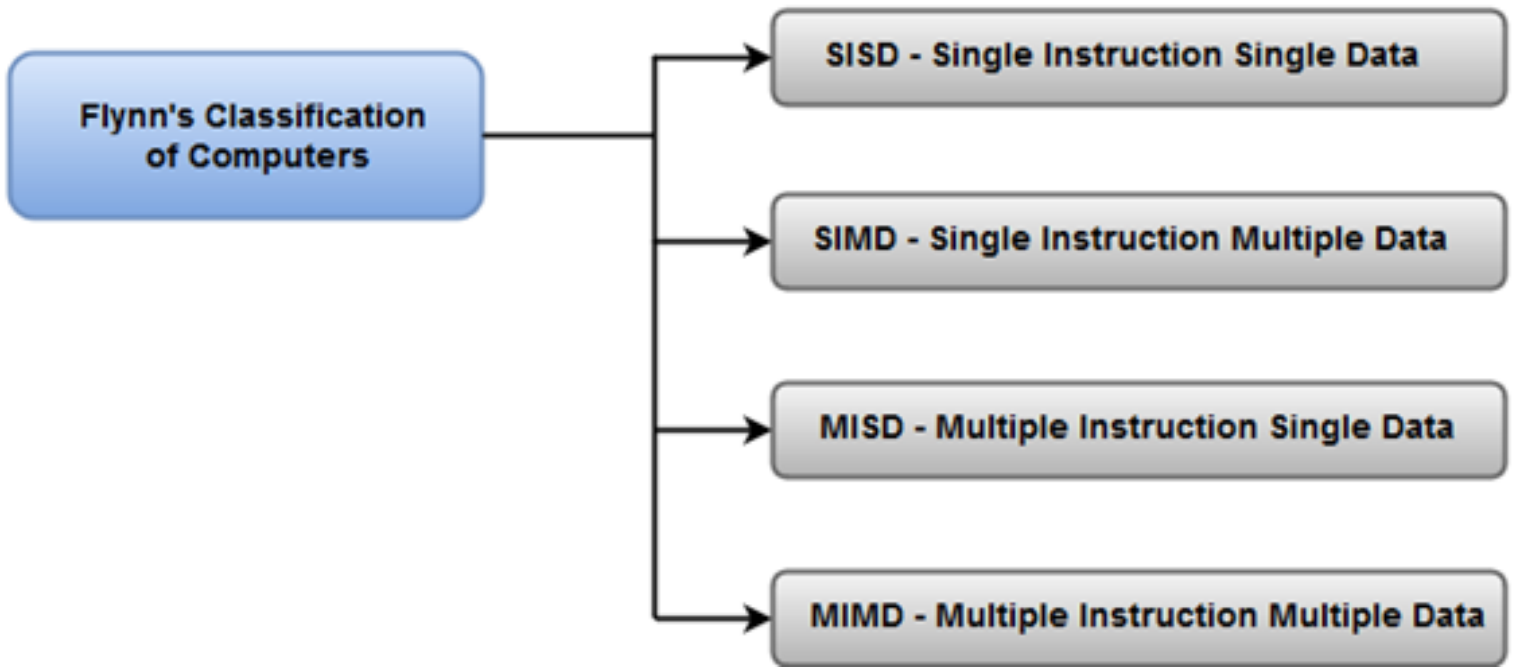
By Thavorac

GENERAL SYSTEM ARCHITECTURE

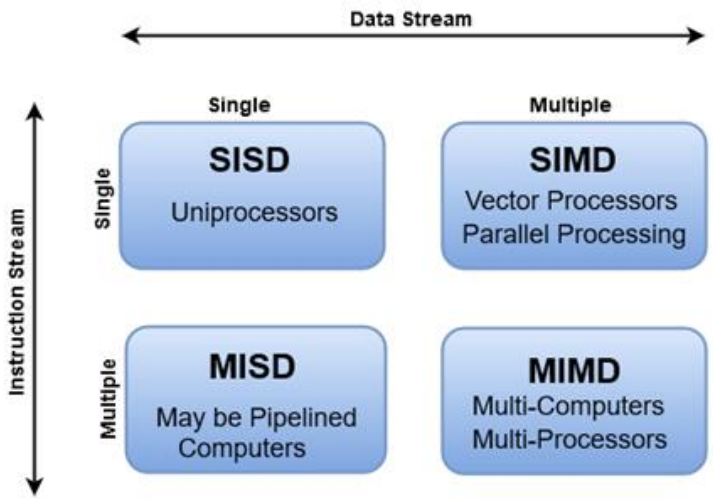
In Computer Architecture, the General System Architecture is divided into two major classification units:

1. Store Program Control Concept : the storage of instructions in computer memory to enable it to perform a variety of tasks in sequence or intermittently. **ENIAC** (in 1940s) was built based on this concept.
2. Flynn's Classification of Computers : classification for the organization of a computer system by the number of instructions and data items that are manipulated simulstaneously.

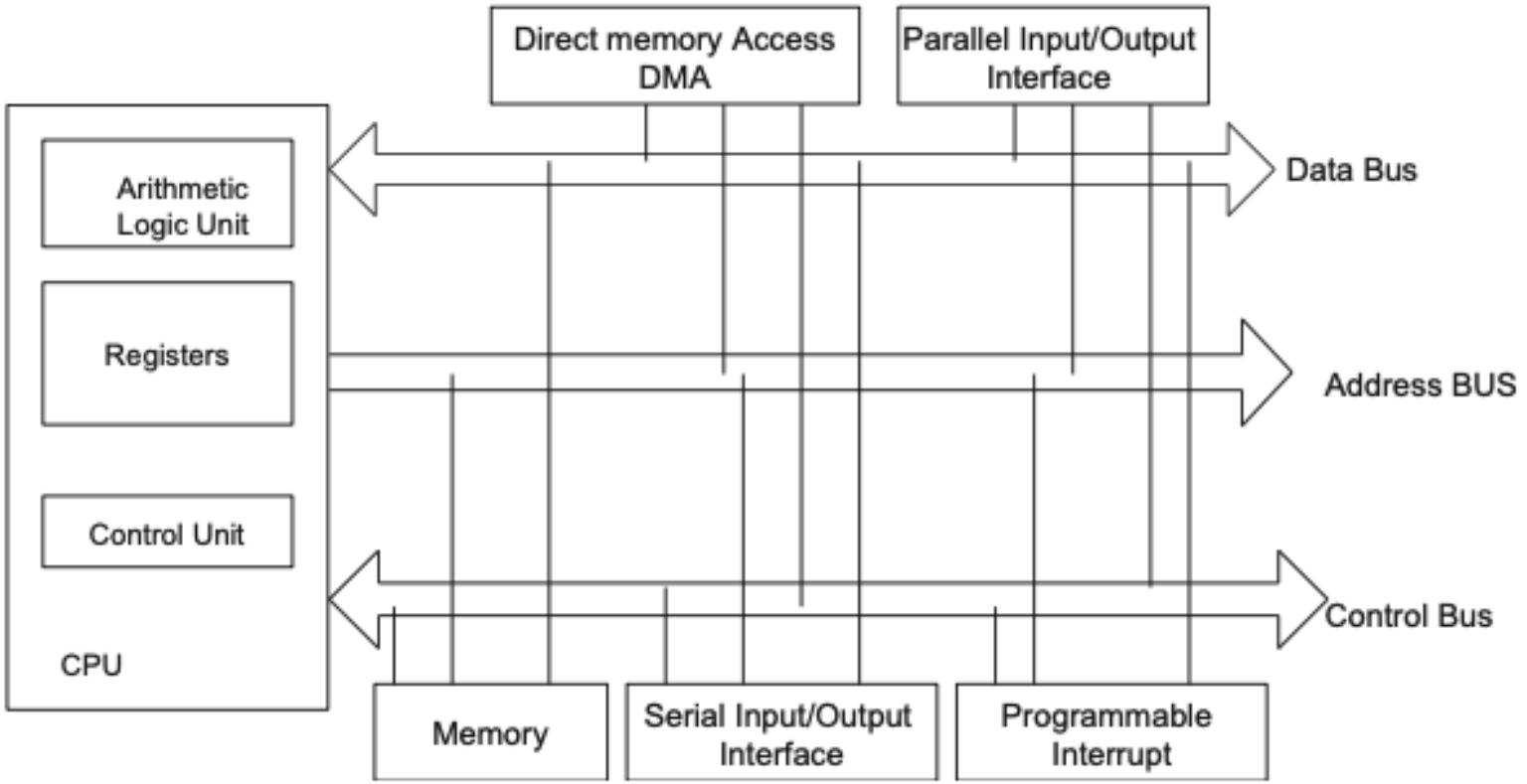


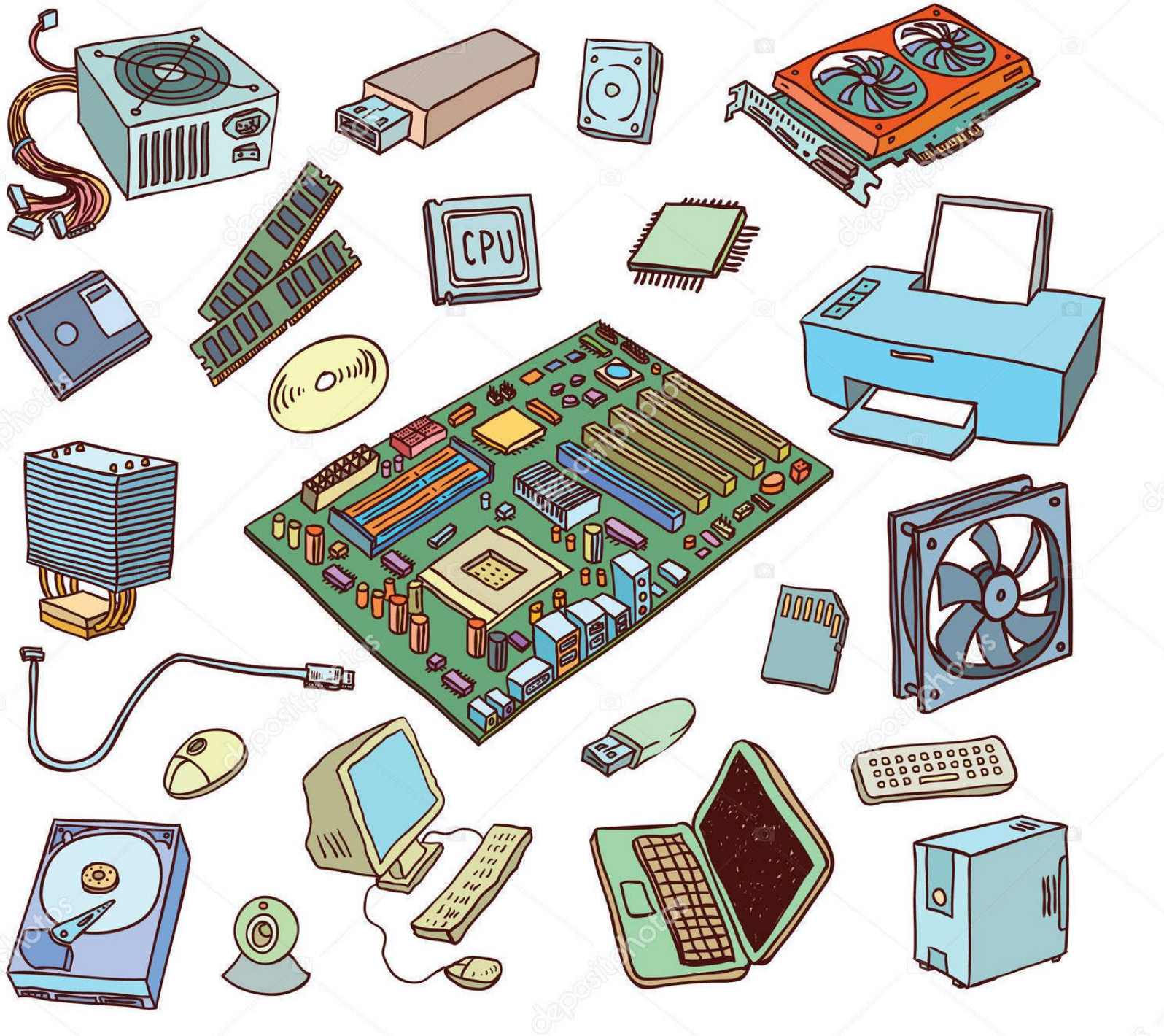


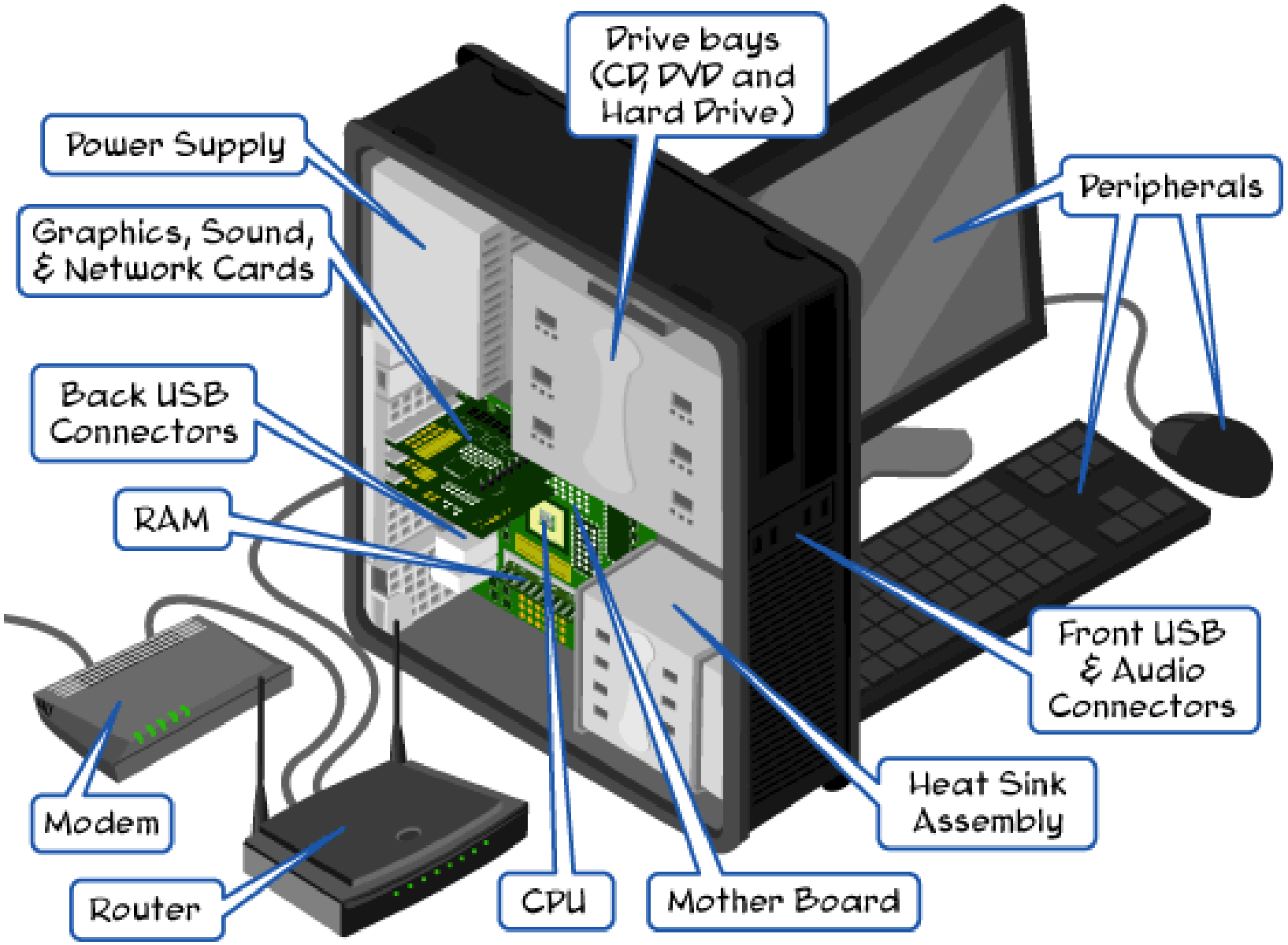
Flynn's Classification of Computers

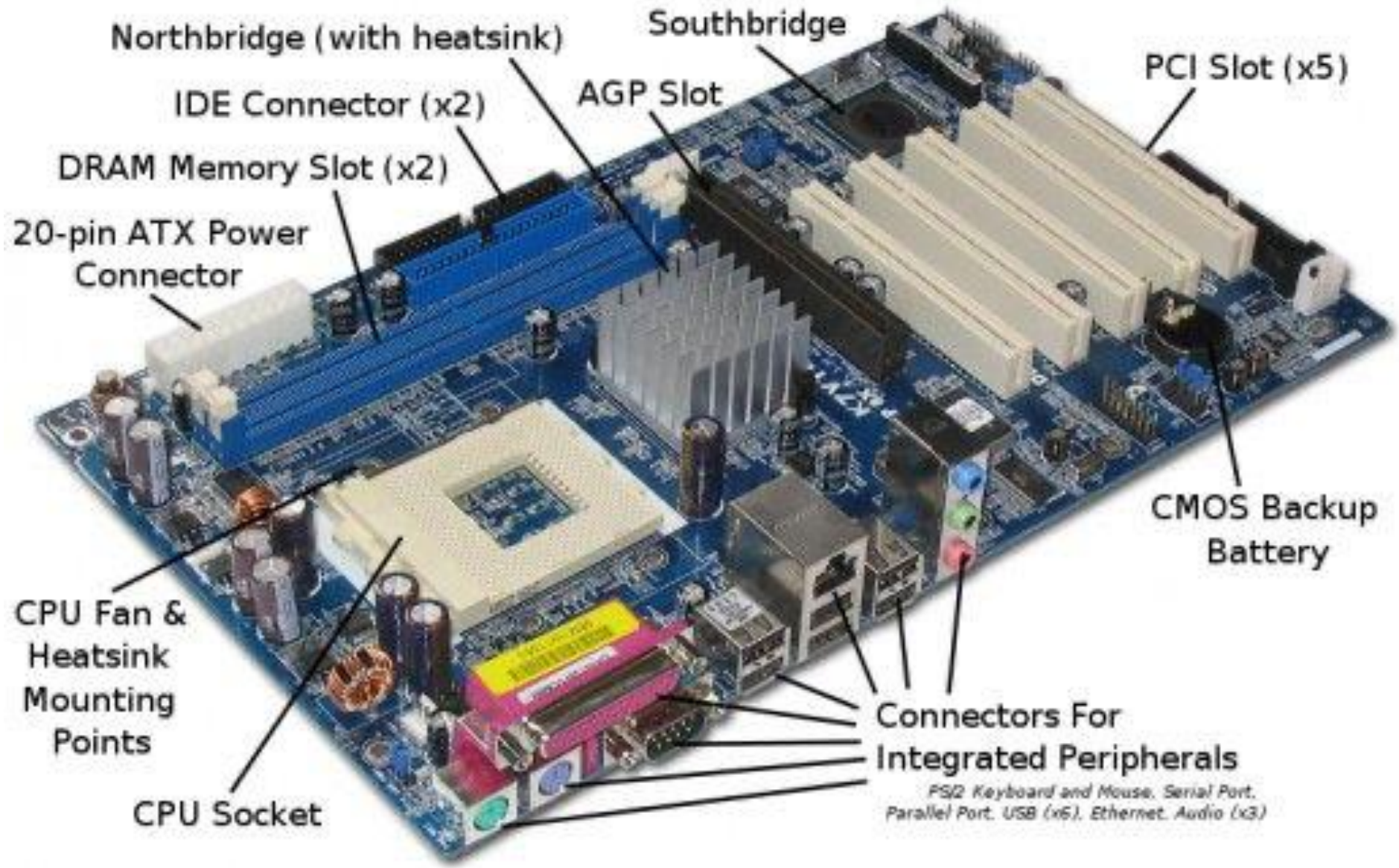


COMPONENTS OF A MICROCOMPUTER




CPU


Drive bays (CD, DVD and Hard Drive)
Power Supply
Graphics, Sound, & Network Cards
Back USB Connectors
RAM
Peripherals
Front USB & Audio Connectors
Heat Sink Assembly
Modem
Router
CPU
Mother Board


Northbridge (with heatsink)
Southbridge
IDE Connector (x2)
AGP Slot
PCI Slot (x5)
DRAM Memory Slot (x2)
20-pin ATX Power Connector
CMOS Backup Battery
CPU Fan & Heatsink Mounting Points
CPU Socket
Connectors For Integrated Peripherals
PS/2 Keyboard and Mouse, Serial Port, Parallel Port, USB (x6), Ethernet, Audio (x3)

LET'S PLAY AROUND WITH COMPUTER COMPONENTS

Go to this link: https://pcpartpicker.com/list/

Build a computer base on your preference with the budget limit of 500$. Choose the components with reason.

You have 15minutes.

Share your draft in the chat box

Example

Central Processing Unit (CPU)

The central processing unit is the “brain” of the computer:

- Accepting data from input devices
- Processing the data into information
- Transferring the information to memory and output devices

CPU is composed of:

1. Arithmetic logic unit (ALU): perform arithmetic opeations such as addition, substraction, division and multiplication and logic operations such as AND OR and NOT.
2. Control unit: control input/output devices, generate control signals to the other components, perform instruction execution.
3. Registers: fastest memory in a computer which holds information for instruction execution.
4. Cpu buses

CPU Buses

There are 3 types of buses:

- Address Bus: The address bus defines the number of addressable locations in a memory IC by using the 2^n formula, where n represents the number of address lines.

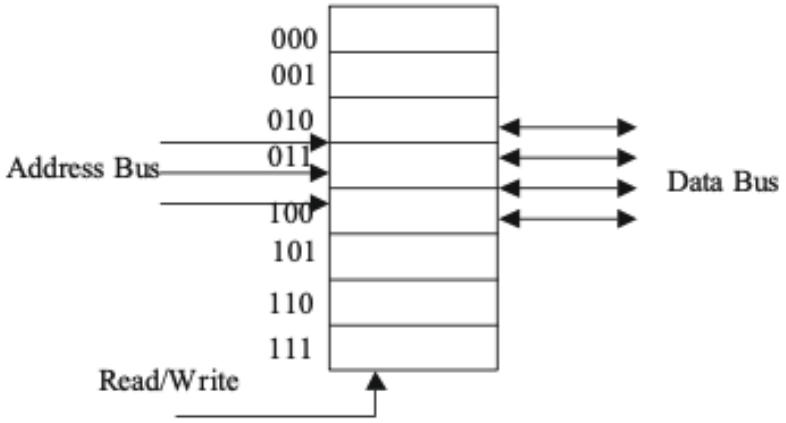


Fig1. A memory with three address lines and four data lines

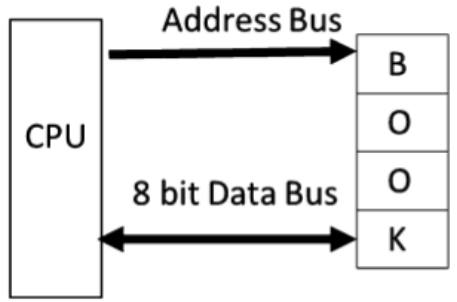
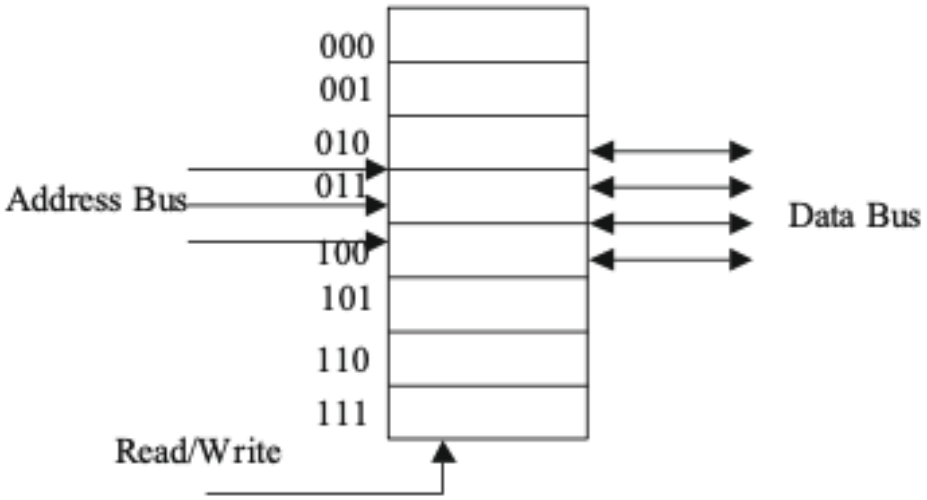


Fig 2. CPU with 8 bit Data Bus

If the address bus is made up of three lines, then there are 23 1⁄4 8 addressable memory locations. The size of the address bus directly determines the maximum numbers of memory locations that can be accessed by the CPU

- Data Bus: is used to carry data to and from the memory.



The size of memory is represented by 2^n x m where n is the number of address lines and m is the size of each location.

In the example on the left, the size of memory is

2^3 x 4 = 32 bits

The size of data bus plays important factor on CPU performance, current CPU's data bus is 32 bits or 64 bits, and a CPU with 32-bit data bus means it can read or write 32 bits of data in and from memory.

Fig 1.2 represent the 8 bits data bus and to transfer "BOOK", it requires CPU to access memory 4 times.

- Control Bus : The control bus carries control signals from the control unit to the computer components in order to control the operation of each component.

Some of the control signals are:

Read signal: The control bus carries control signals from the control unit to the computer components in order to control the operation of each component.

Write signal: The write line is used to write data into the memory.

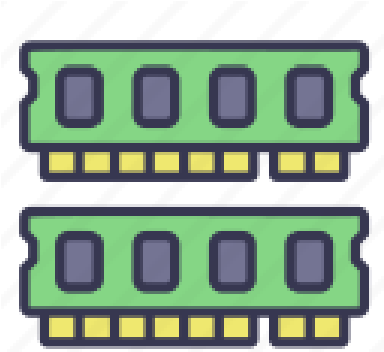
Interrupt: Indicates an interrupt request.

Bus request: The device is requesting to use the computer bus.

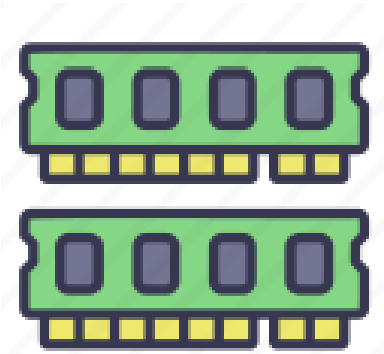
Bus Grant: Gives permission to the requesting device to use the computer bus.

Example of CPU accessing data in memory

Send Memory address via address bus → CU send signal read via control bus → Data is sent back to CPU via data bus



Send Memory address via address bus → Send data via data bus → CU send signal write via control bus



32 bit versus 64 bit CPU

32 bits or 64 bits CPU refer to:

- The size of data the processor can perform operation (instruction size, data transfer)
- The size of register
- The size of ALU

Most desktop and server computers are using AMD and Intel processors; they might use 32 bits or 64 bits. Intel and AMD processor use the same architecture; this means a program in computer with Intel processor can run on a computer with AMD processor.

Practice time: Find the differences of 32 bits and 64 bits CPU (also check if it is related to Operating System)

CPU Technology

CISC (Complex Instruction Set Computer) In 1978, Intel developed the 8086 microprocessor chip. The 8086 was designed to process a 16-bit data word; it had no instruction for floating point operations. At the present time, the Pentium processes 32-bit and 64-bit words, and it can process floating point instructions.

Example: Pentium Processor, VAX 11/780 (has more than 300 instructions with 16 different addressing modes)

The major characteristics of CISC processor are as follows:

1. A large number of instructions.
2. Many addressing modes.
3. Variable length of instructions.
4. Most instruction can manipulate operands in the memory.
5. Control unit is microprogrammed.

CPU Technology

RISC Until the mid-1990s, computer manufacturers were designing complex CPUs with large sets of instructions. At that time, a number of computer manufacturers decided to design CPUs capable of executing only a very limited set of instructions.

Example: PowerPC, MIPS processor, IBM RISC System/6000, ARM and SPARC

The major characteristics of RISC processor are as follows:

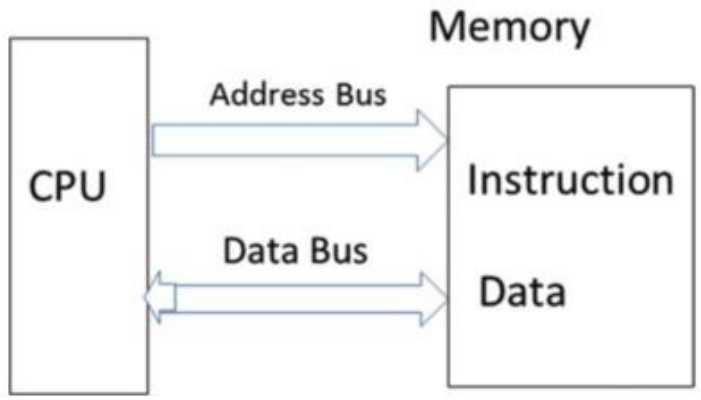
1. Require few instructions.
2. All instructions are the same length (they can be easily decoded).
3. Most instructions are executed in one machine clock cycle.
4. Control unit is hardwired.
5. Few address modes.
6. A large number of registers.

CISC	RISC
Variable instruction length	Fixed instruction length
Variable opcode length	Fixed opcode length
Memory operands	Load/store instructions
Example: Pentium	ARM, MIPS

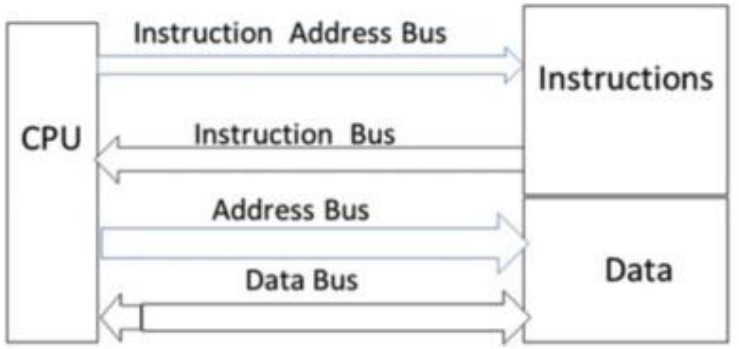
CPU Architecture

There are two types of CPU architecture:

- **Von Neumann Architecture** It is a program consists of code (instructions) and data. Von Neumann uses the data bus to transfer data and instructions from the memory to the CPU.



- **Harvard Architecture Harvard architecture** uses separate buses for instructions and data. The instruction address bus and instruction bus are used for reading instructions from memory. The address bus and data bus are used for writing and reading data to and from memory

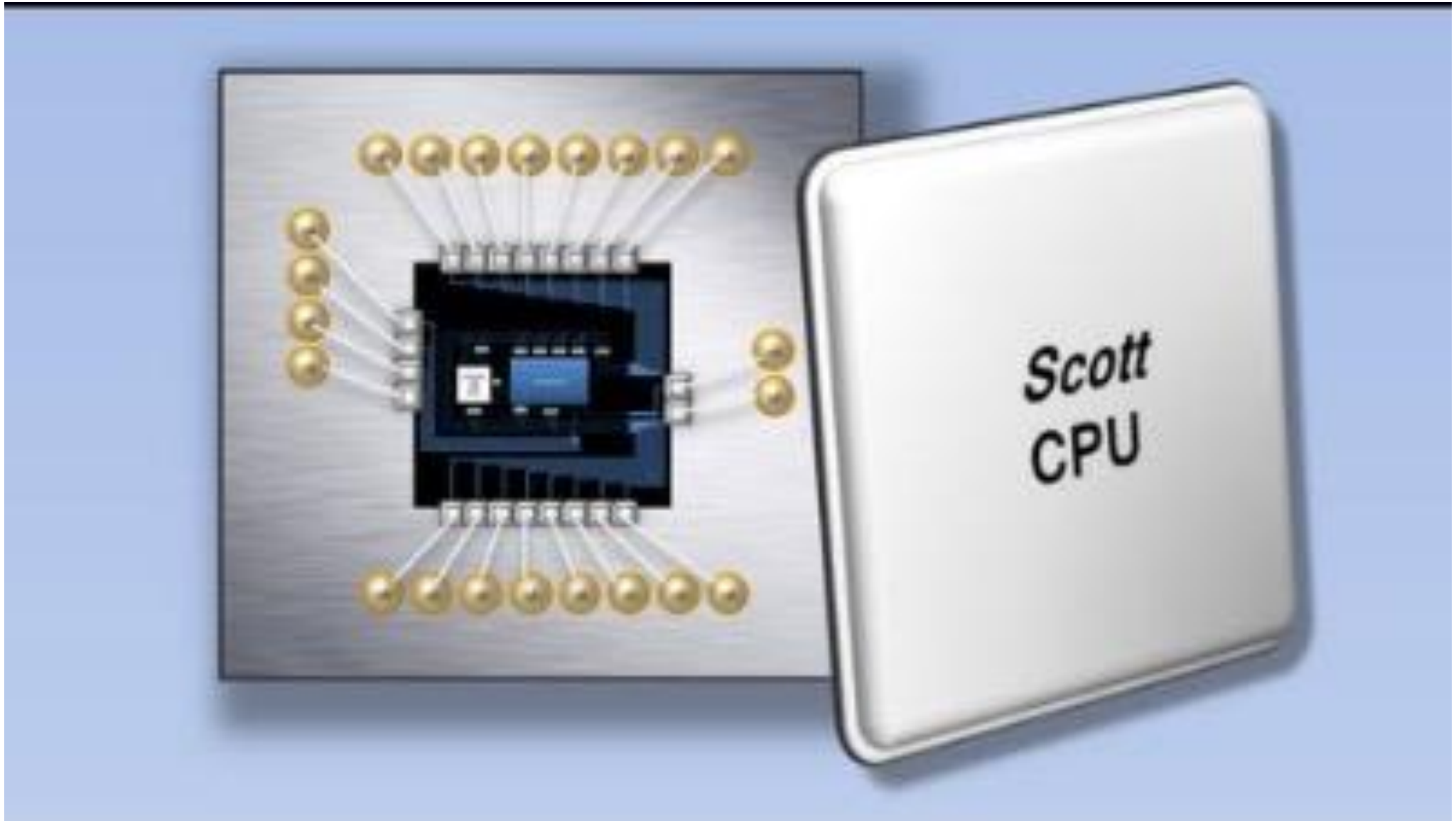


PRACTICE TIME

You are going to watch a video. Figure out/Answer to the following key term/questions:

1. CPU clock:
2. The default pattern of CPU request data from RAM
3. How cpu read data from RAM in SCOTT CPU
4. How cpu write data from RAM in SCOTT CPU
5. Instruction Set
6. **How CPU execute an instruction**
7. Flag

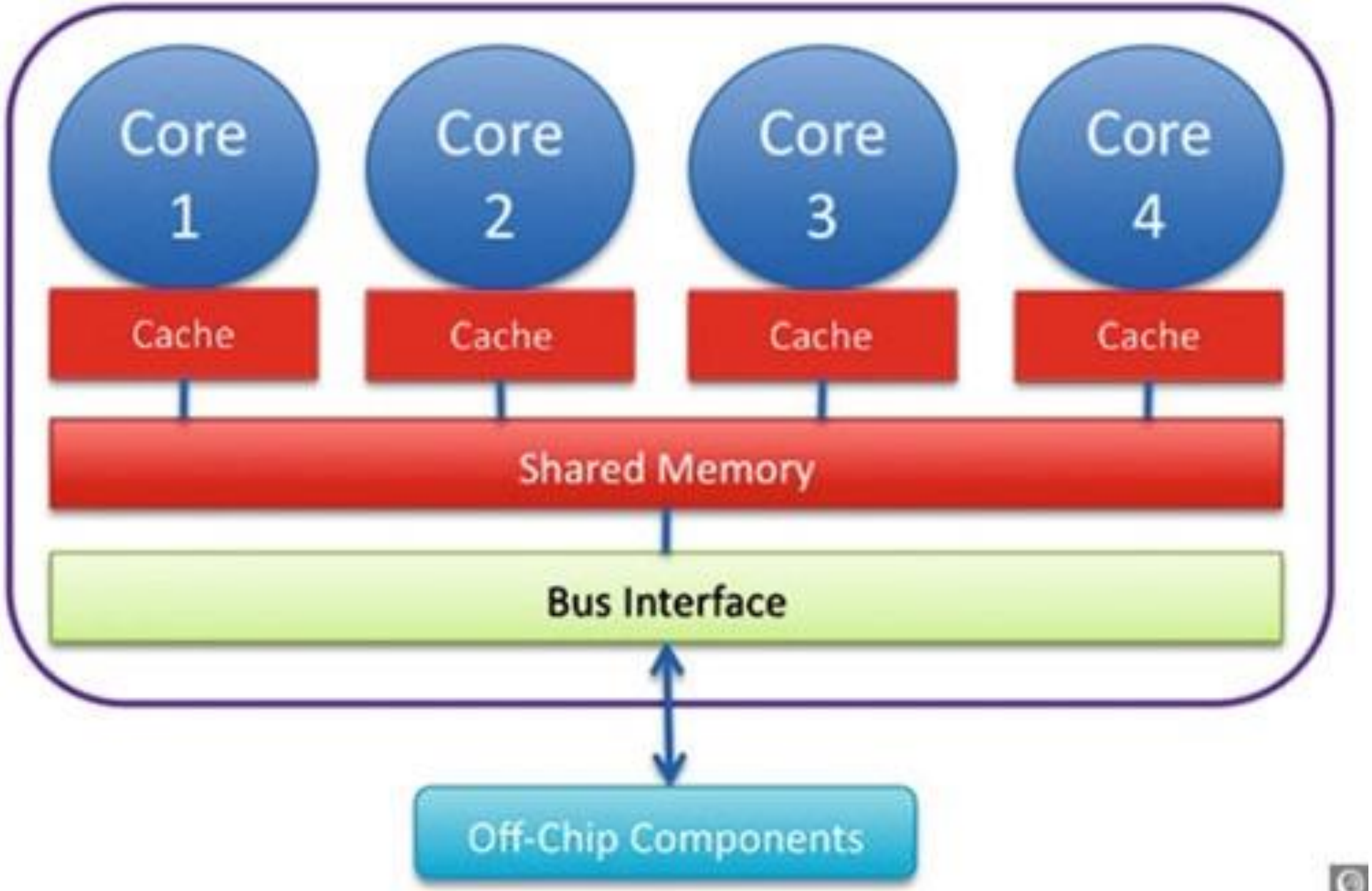
Example of SCOTT CPU



https://www.youtube.com/watch?v=cNN_tTXABUA

MULTICORE PROCESSORS

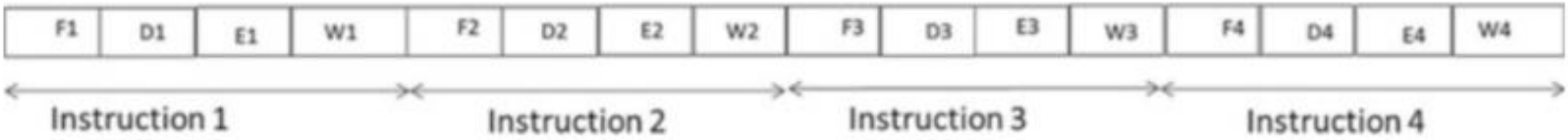
- integrated circuit (IC) with two or more independent CPU which is called core
- they are executing multiple instructions simultaneously in order to increase performance
- A quad-core processor is a chip with four independent units called cores that read and execute instructions such as add, move data, and branch
- Two cores (dual-core CPUs) such as AMD Phenom II X2 and Intel Core Duo
- Three cores (tri-core CPUs) such as AMD Phenom II X3
- Four cores (quad-core CPUs) such as AMD Phenom II X4, Intel's i5 and i7 Processors
- ……


Core 1
Core 2
Core 3
Core 4
Cache
Cache
Cache
Cache
Shared Memory
Bus Interface
Off-Chip Components

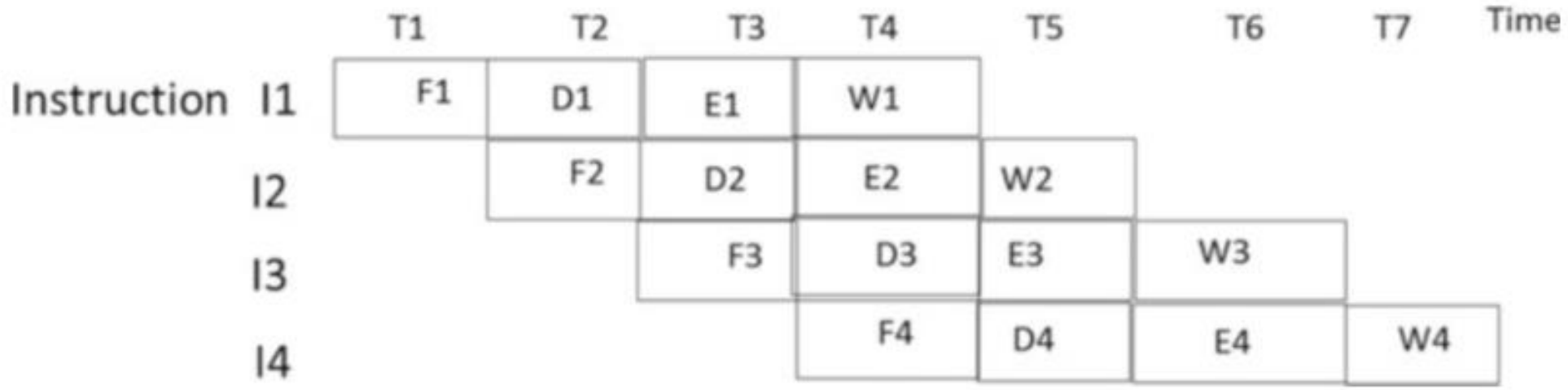
CPU INSTRUCTION EXECUTION

Steps to execute one instruction:

1. Fetch instruction (F): Moving Instruction from memory to CPU.
2. Decode instruction (D): Determine types of instruction such as ADD, AND, OR, and Store operands into registers if needed.
3. Execute instruction (E): Execute the instruction such as addition.
4. Write results (R): Store the result of execution into register or memory.



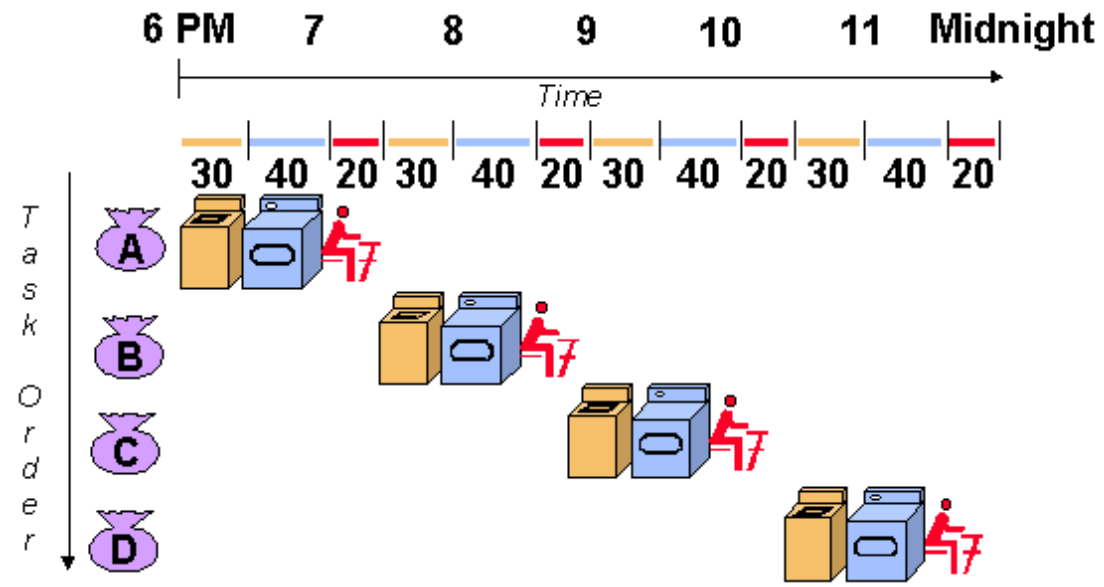
Execution of instruction without pipeline



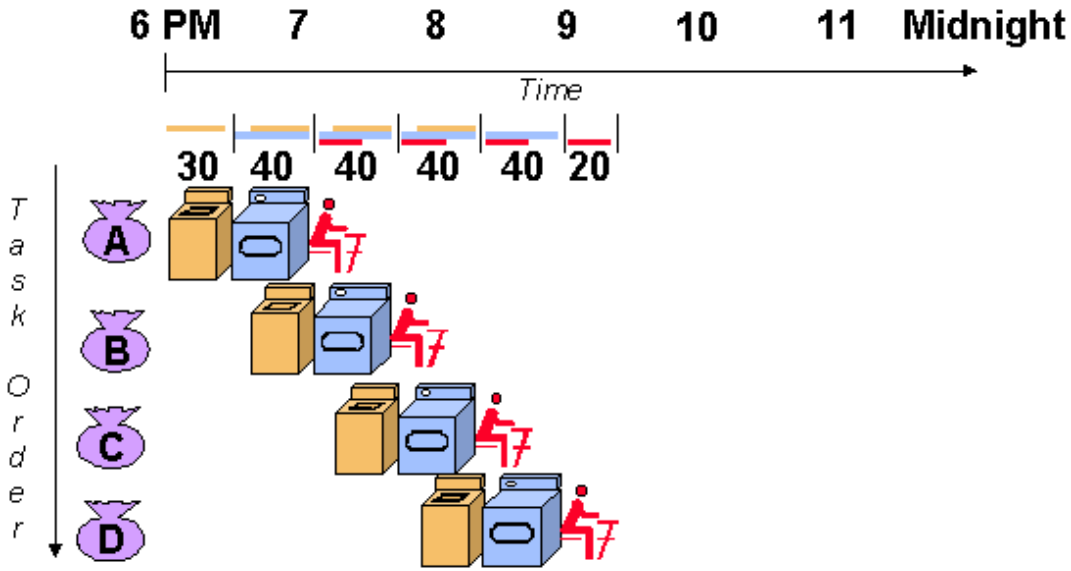
Execution of instruction using pipeline

PIPELINING

- Pipelining will increase the performance of CPU meaning executing more instructions in less time.
- a standard feature in RISC processors, is much like an assembly line. Because the processor works on different steps of the instruction at the same time, more instructions can be executed in a shorter period of time.



Operation without pipeline



Operation with pipeline

MICROCOMPUTER BUS

Some of the computer BUS are ISA, MCA, EISA, VESA PCI, FireWire, USB, and PCI Express.

ISA Bus

The industry standard architecture (ISA) bus was introduced by IBM for the IBM PC using an 8088 microprocessor. The ISA bus has an 8-bit data bus and 20 address lines at a clock speed of 8 MHz. The PC AT type uses the 80,286 processor which has a 16-bit data bus and 24-bit address lines and is compatible with the PC.

Microchannel Architecture Bus

The microchannel architecture (MCA) bus was introduced by IBM in 1987 for its PS/2 microcomputer. The MCA bus is a 32-bit bus that can transfer four bytes of data at a time and runs at a 10 MHz clock speed. It also supports 16-bit data transfer and has 32-bit address lines. Microchannel architecture was so expensive the non-IBM vendors developed a comparable but less expensive solution called the EISA bus.

EISA Bus

The extended ISA (EISA) bus is a 32-bit bus that also supports 8- and 16-bit data transfer bus architectures. EISA runs at 8-MHz clock speeds and has 32-bit address lines.

VESA Bus

The video electronics standard association (VESA) bus, which is also called a video local bus (VL-BUS), is a standard interface between the computer and its expansion. As applications became more graphically intensive, the VESA bus was introduced to maximize throughput of video graphics memory. The VESA bus provides fast data flow between stations and can transfer up to 132 Mbps.

PCI Bus

The peripheral component interconnect (PCI) bus was developed by Intel Corporation. PCI bus technology includes a 32-/64-bit bus that runs at a 33/66 MHz clock speed. PCI offers many advantages for connections to hubs, routers, and network interface cards (NIC). In particular, PCI provides more bandwidth: up to 1 gigabit per second as needed by these hardware components.

PCI card

The PCI bus was designed to improve the bandwidth and decrease latency in computer systems. Current versions of the PCI bus support data rates of 1056 Mbps and can be upgraded to 4224 Mbps. The PCI bus can support up to 16 slots or devices in the motherboard.

Bus type	ISA	EISA	MCA	VESA	PCI	PCI-64
Speed (MHz)	8	8.3	10	33	33	64
Data bus bandwidth (bits)	16	32	32	32	32	66
Max. data rate (MB/s)[a]	8	32	40	132	132	508
Plug and play capable	No	No	Yes	Yes	Yes	Yes

[a] *MB/s* megabytes/second

Comparing different bus architecture

Universal Serial Bus (USB)

- The universal serial bus (USB) is a computer serial bus which enables users to connect peripherals such as the mouse, keyboard, modem, CD-ROM, scanner, and printer, to the outside of a computer without any configuration.
- This means that a USB has the capability to detect when a device has been added or removed from a PC
- USB is a true plug-and-play bus. Up to 127 peripherals can be connected to a PC with a USB.

USB's Versions:

USB version 1.1 was released in 1998 which supports data rate of 12 Mbps (full speed) and 1.5 Mbps (low speed);

USB version 2 is a high speed (480 Mbps) that is compatible with USB 1.1 and was announced in 1999. The maximum cable length for USB is 5 meters.

In 2000, the first USB flash drives were released and sold on the commercial market by IBM and Trek Technology.

USB version 3 can transfer data up to 5 Gbps and was released on November 12, 2008

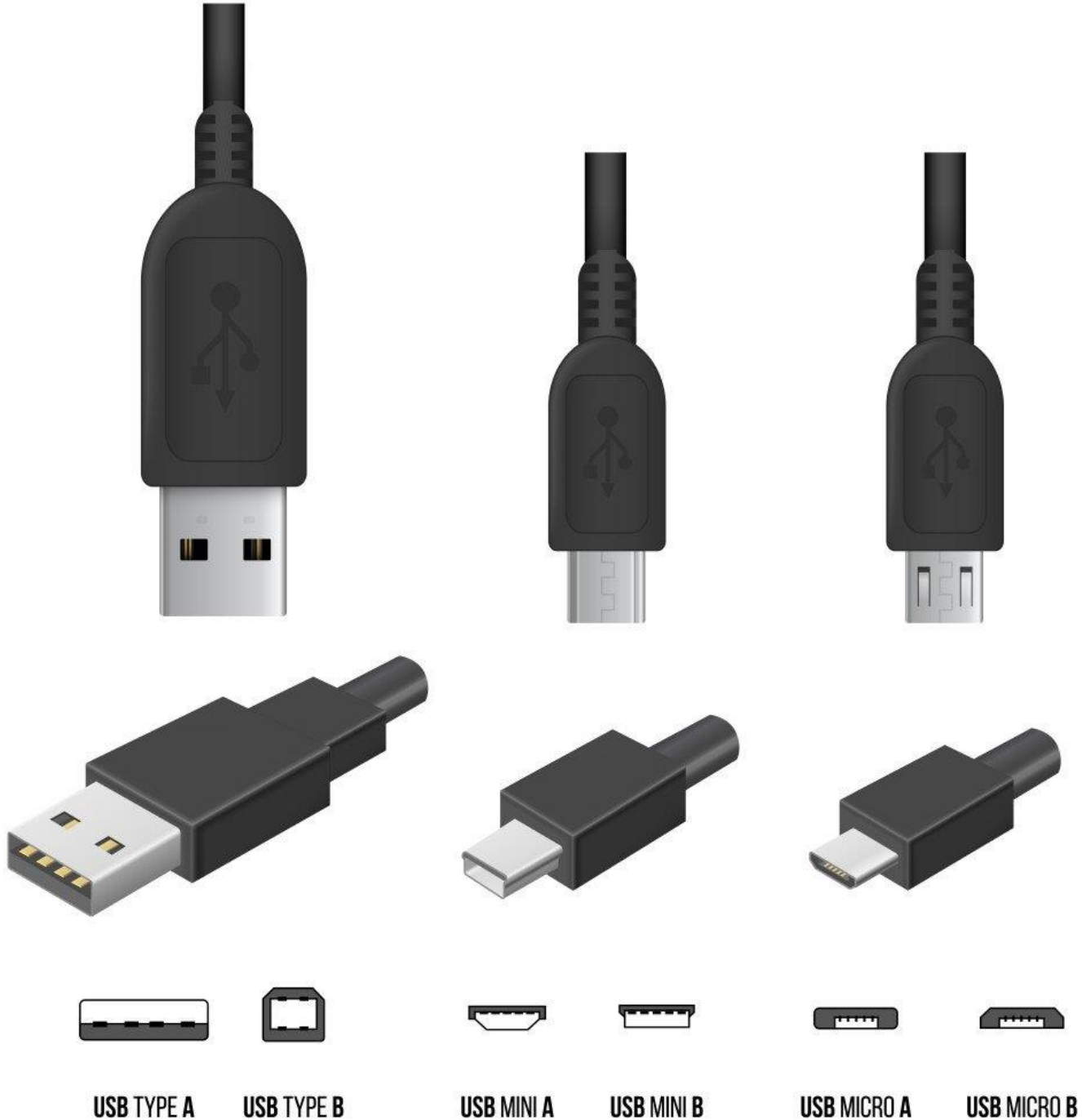
USB version 3.1 was released in July 2013, providing data transfer up to 10Gbps.

USB version 3.2 was released in September 2017. It introduced the USB-C connector, providing data transfer rates up to 20 Gbps

Here are the key takeaways:

- USB Type-C is not the same thing as USB 3.2
- A Type-C connector does not automatically indicate that a USB port will support USB 3.2 Gen 2 or USB 3.2 Gen 2x2 data transfer speed (10Gbps or 20Gbps)
- The term “USB 3.1” or “USB 3.2” *may* be used to describe ports that support either 5 Gbps data transfer (USB 3.2 Gen 1) or 10 Gbps data transfer (USB 3.2 Gen 2).

	Top speed	Max power output	Power direction	Cable configuration	Availability
USB 1.1	12Mbps	2.5V, 500mA	Host to peripheral	Type-A to Type-B	1998
USB 2.0	480Mbps	2.5V, 1.8A	Host to peripheral	Type-A to Type-B	2000
USB 3.0	5Gbps	5V, 1.8A	Host to peripheral	Type-A to Type-B	2008
USB 3.1	10Gbps	20V, 5A	Bi-directional	Type-C both ends, reversible plug orientation	2015


USB TYPE A
USB TYPE B
USB MINI A
USB MINI B
USB MICRO A
USB MICRO B

Type-A

usbtypec.info

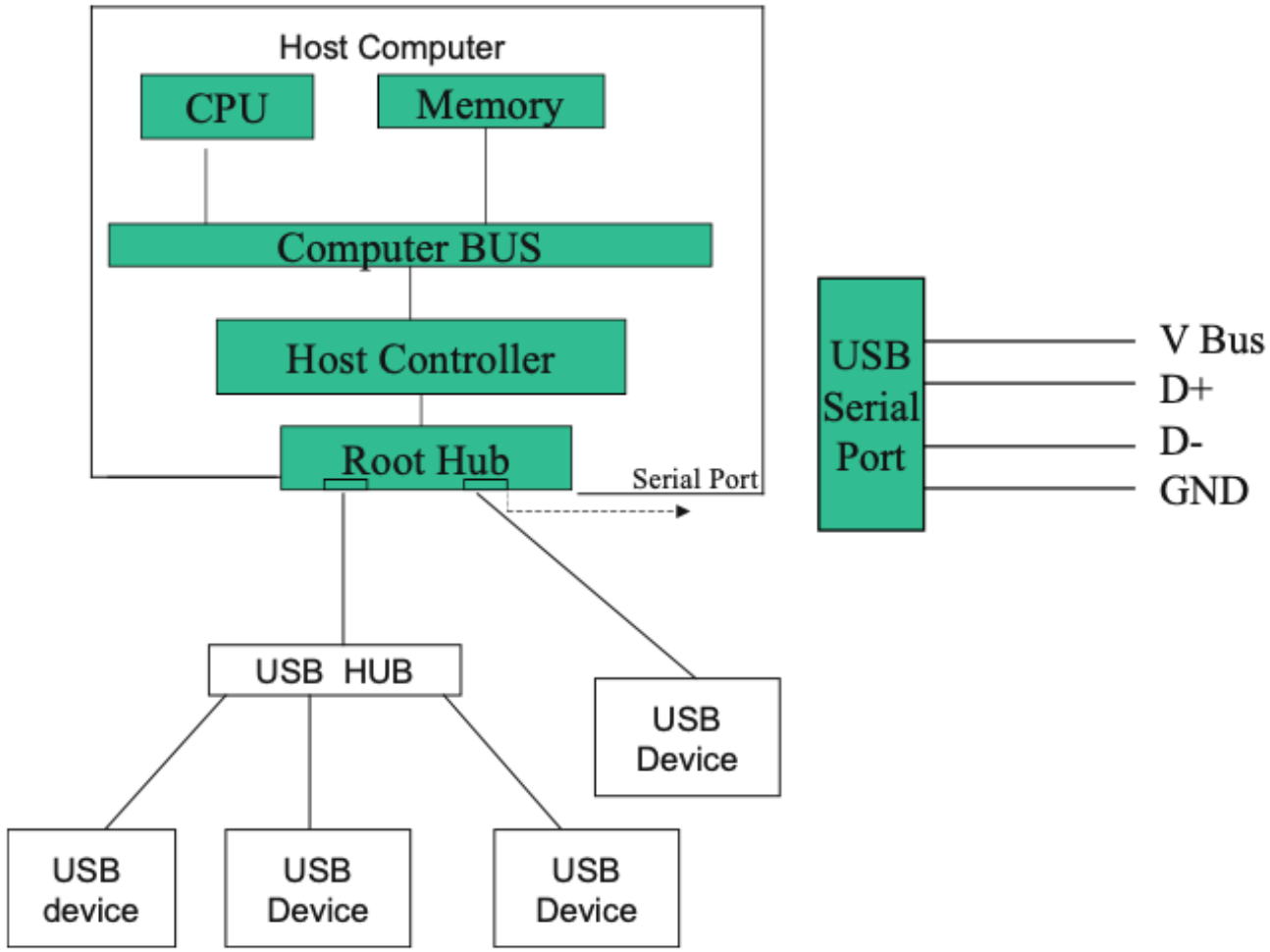
Type-B

Type-C

usbtypec.info

USB Architecture

A USB system consists of **USB host controller, USB root hub, USB hub, USB cable, USB device, client software,** and **host controller software.**



Host Controller initiates all data transfer, and root hub provides a connection between devices and host controller. The host controller uses polling to detect a new device and is connected to the bus or disconnected from. Also, USB host controller performs the following functions:

a. Host controller sets up the device for operation (device configuration).
b. Packet generation.
c. Serializer/deserializer
d. Process request from device and host.
e. Manage USB protocol.
f. Managing flow between host and USB devices.
g. Assign address to the devices.
h. Execute client software.
i. Collecting status bit from USB ports.

Root Hub The root hub performs power distribution to the devices, enables and disables the ports, and reports status of each port to the host controller. The root hub provides the connection between the host controller and USB ports.

Hub Hubs are used to expand the number of devices connected to the USB system. Hubs are able to detect when a device is attached or removed from port.

In downstream transmission, all devices that are connected to the hub will receive the packet, but only the device accepts the packet that the device address matches with address in the token.

In upstream transmission, the device sends the packet to the hub, and hub transmits the packet to its upstream port only.

PCI Express Bus

PCI express was introduced in mid-1990 with 33 MHz frequency, and during the time the speed of BUS was increased to 66 MHz. Due to new development in networking technology such as Gigabit Ethernet and I/O devices that demand more bandwidth, there is a need for a new bus technology with higher bandwidth. The PCI express was approved by Special Interest Group in 2002, and chipset starts shipping in 2004. The PCI express has the following features:

- PCI express is point-to-point connection between devices.
- PCI express is a serial bus.
- PCI express uses pocket and layer architecture.
- Compatible with PCI bus through software.
- End-to-end link data integrity (error detection).
- Isochronous data transfer.
- Selectable bandwidth.

HDMI (High Definition Multimedia Interface)

HDMI is an interface between two devices for transferring uncompressed video data and compressed or uncompressed digital audio data. Some of the applications of HDMI are computer monitor, digital TV, and video projector.