
STM32
CubeMX

1. Description

1.1. Project

Project Name	SR_Linefollower
Board Name	NUCLEO-F303K8
Generated with:	STM32CubeMX 6.0.0
Date	04/26/2021

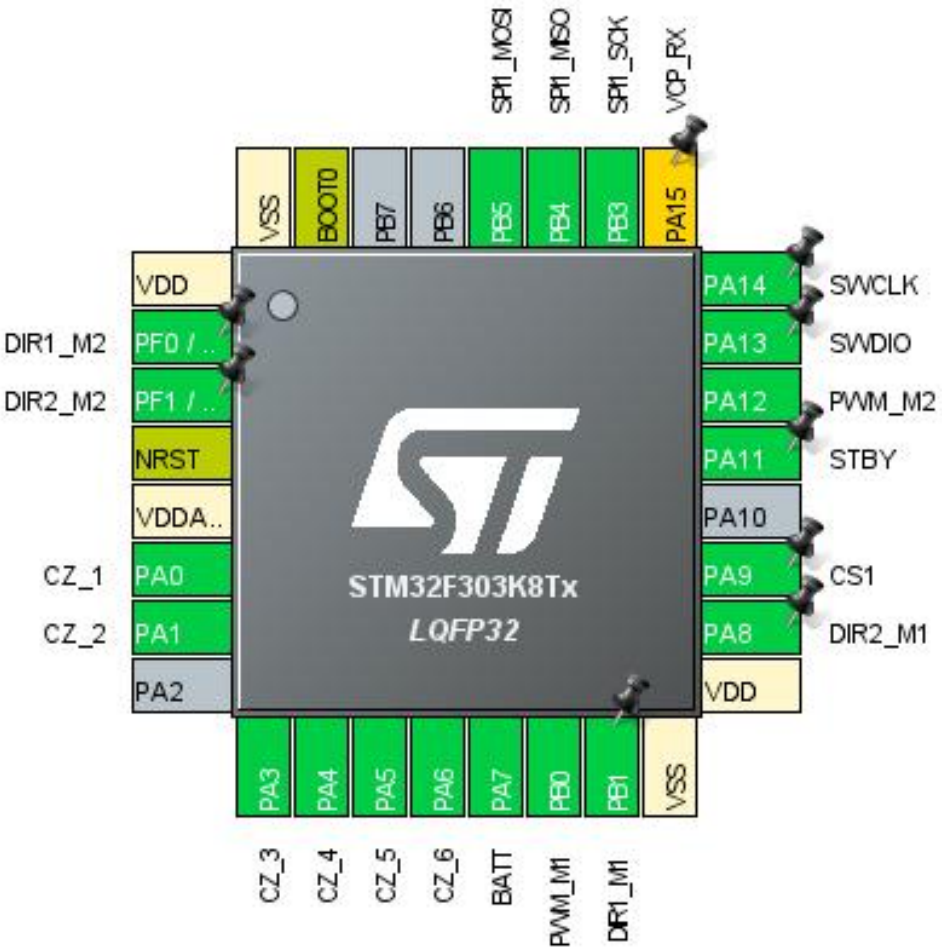
1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303K8Tx
MCU Package	LQFP32
MCU Pin number	32

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



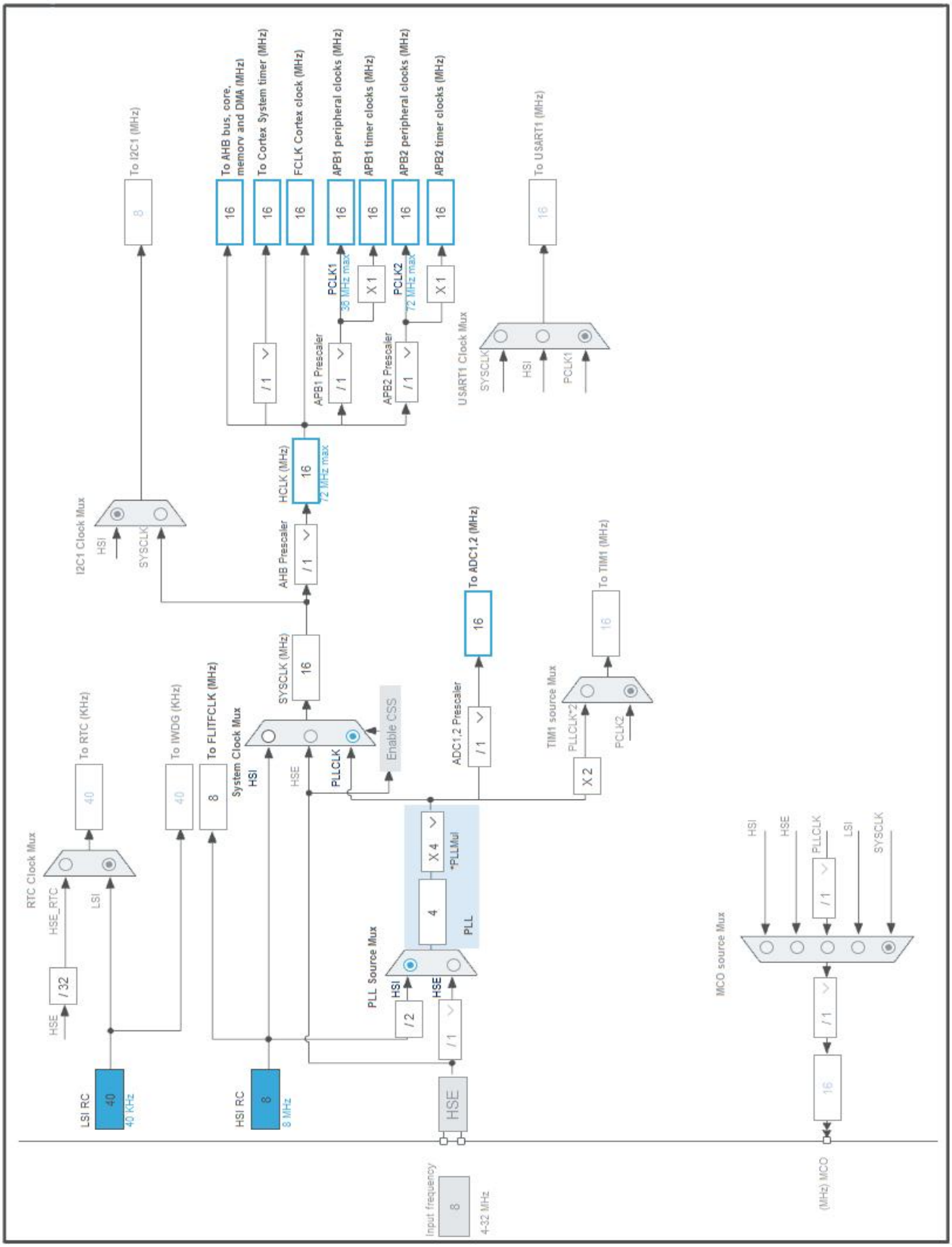
3. Pins Configuration

Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PF0 / OSC_IN *	I/O	GPIO_Output	DIR1_M2
3	PF1 / OSC_OUT *	I/O	GPIO_Output	DIR2_M2
4	NRST	Reset		
5	VDDA/VREF+	Power		
6	PA0	I/O	ADC1_IN1	CZ_1
7	PA1	I/O	ADC1_IN2	CZ_2
9	PA3	I/O	ADC1_IN4	CZ_3
10	PA4	I/O	ADC2_IN1	CZ_4
11	PA5	I/O	ADC2_IN2	CZ_5
12	PA6	I/O	ADC2_IN3	CZ_6
13	PA7	I/O	ADC2_IN4	BATT
14	PB0	I/O	TIM3_CH3	PWM_M1
15	PB1 *	I/O	GPIO_Output	DIR1_M1
16	VSS	Power		
17	VDD	Power		
18	PA8 *	I/O	GPIO_Output	DIR2_M1
19	PA9 *	I/O	GPIO_Output	CS1
21	PA11 *	I/O	GPIO_Output	STBY
22	PA12	I/O	TIM16_CH1	PWM_M2
23	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
24	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
25	PA15 **	I/O	USART2_RX	VCP_RX
26	PB3	I/O	SPI1_SCK	
27	PB4	I/O	SPI1_MISO	
28	PB5	I/O	SPI1_MOSI	
31	BOOT0	Boot		
32	VSS	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	SR_Linefollower
Project Folder	C:\Users\clayf\STM32CubeIDE\workspace_1.4.0\SR_Linefollower
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F3 V1.11.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	No
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC1_Init	ADC1
5	MX_SPI1_Init	SPI1
6	MX_ADC2_Init	ADC2
7	MX_TIM3_Init	TIM3
8	MX_TIM16_Init	TIM16

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303K8Tx
Datasheet	DS9866_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.6

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

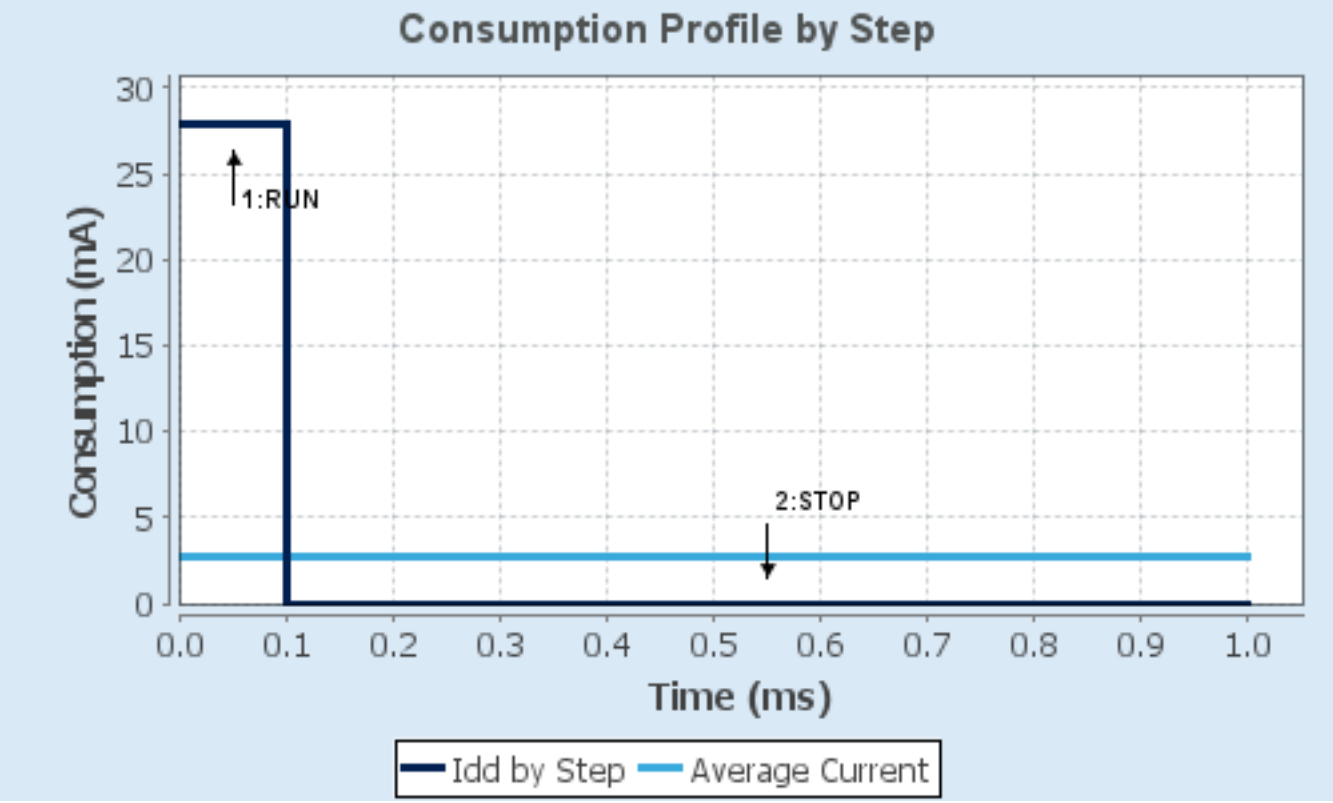
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	RAM	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSEBYP PLL	Regulator_LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	27.84 mA	9.55 µA
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	98.99	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.79 mA
Battery Life	1 month, 20 days, 5 hours	Average DMIPS	90.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
30
25
20
15
10
5
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. ADC1

IN1: IN1 Single-ended

IN2: IN2 Single-ended

mode: IN4

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	**ADC 8-bit resolution ***
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**3 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 2 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**3 ***
Channel	**Channel 4 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset

Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC2

IN1: IN1 Single-ended

IN2: IN2 Single-ended

IN3: IN3 Single-ended

mode: IN4

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	**ADC 8-bit resolution ***
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**4 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1

Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 2 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**3 ***
Channel	**Channel 3 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	**Channel 4 ***
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. GPIO

7.4. RCC

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.5. SPI1

Mode: Full-Duplex Master

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**8.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.6. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.7. TIM3

Channel3: PWM Generation CH3

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1599 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**99 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.8. TIM16

mode: Activated

Channel1: PWM Generation CH1

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1599 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**99 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

CH Idle State	Reset

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	CZ_1
	PA1	ADC1_IN2	Analog mode	No pull up pull down	n/a	CZ_2
	PA3	ADC1_IN4	Analog mode	No pull up pull down	n/a	CZ_3
ADC2	PA4	ADC2_IN1	Analog mode	No pull up pull down	n/a	CZ_4
	PA5	ADC2_IN2	Analog mode	No pull up pull down	n/a	CZ_5
	PA6	ADC2_IN3	Analog mode	No pull up pull down	n/a	CZ_6
	PA7	ADC2_IN4	Analog mode	No pull up pull down	n/a	BATT
SPI1	PB3	SPI1_SCK	Alternate Function Push Pull	No pull up pull down	**High ***	
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull up pull down	**High ***	
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull up pull down	**High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
TIM3	PB0	TIM3_CH3	Alternate Function Push Pull	No pull up pull down	Low	PWM_M1
TIM16	PA12	TIM16_CH1	Alternate Function Push Pull	No pull up pull down	Low	PWM_M2
Single Mapped Signals	PA15	USART2_RX	Alternate Function Push Pull	No pull up pull down	**High ***	VCP_RX
GPIO	PF0 / OSC_IN	GPIO_Output	Output Push Pull	No pull up pull down	Low	DIR1_M2
	PF1 / OSC_OUT	GPIO_Output	Output Push Pull	No pull up pull down	Low	DIR2_M2
	PB1	GPIO_Output	Output Push Pull	No pull up pull down	Low	DIR1_M1
	PA8	GPIO_Output	Output Push Pull	No pull up pull down	Low	DIR2_M1
	PA9	GPIO_Output	Output Push Pull	No pull up pull down	Low	CS1
	PA11	GPIO_Output	Output Push Pull	No pull up pull down	Low	STBY

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	Low
ADC2	DMA1_Channel2	Peripheral To Memory	Low

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Byte ***
Memory Data Width:	**Byte ***

ADC2: DMA1_Channel2 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Byte ***
Memory Data Width:	**Byte ***

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel2 global interrupt	true	0	0
ADC1 and ADC2 interrupts	true	0	0
TIM1 update and TIM16 interrupts	true	0	0
TIM3 global interrupt	true	0	0
SPI1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
Floating point unit interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	true	true	false
Hard fault interrupt	true	true	false
Memory management fault	true	true	false
Pre-fetch fault, memory access fault	true	true	false
Undefined instruction or illegal state	true	true	false
System service call via SWI instruction	true	true	false
Debug monitor	true	true	false
Pendable request for system service	true	true	false
System tick timer	true	true	true
DMA1 channel1 global interrupt	true	true	true
DMA1 channel2 global interrupt	true	true	true
ADC1 and ADC2 interrupts	true	true	true
TIM1 update and TIM16 interrupts	true	true	true
TIM3 global interrupt	true	true	true

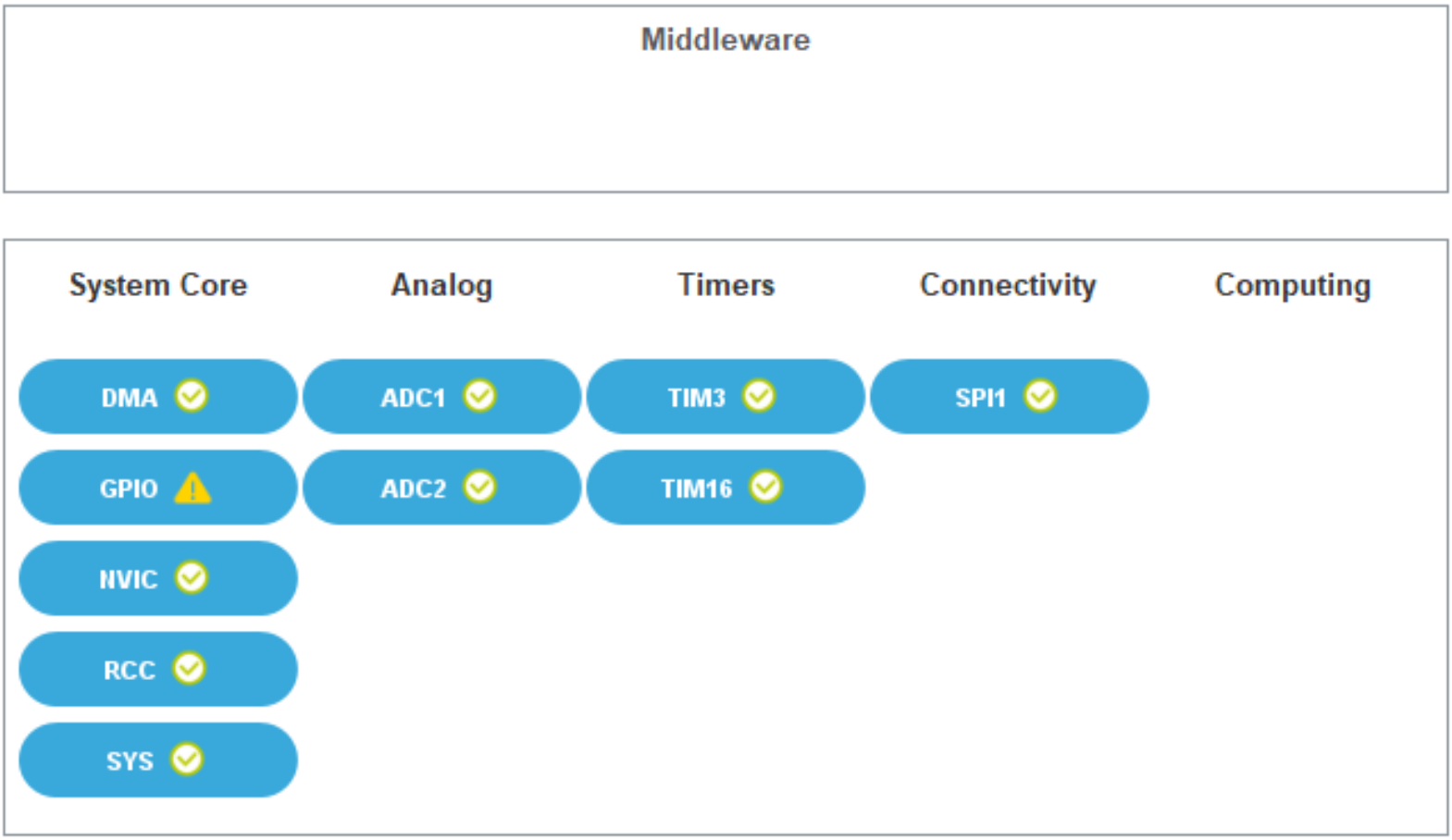
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
SPI1 global interrupt	true	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00092070.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00043574.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00109011.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00047998.pdf
Application note	http://www.st.com/resource/en/application_note/DM00053084.pdf
Application note	http://www.st.com/resource/en/application_note/DM00070391.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00074240.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00083249.pdf
Application note	http://www.st.com/resource/en/application_note/DM00085385.pdf
Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00121474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00157785.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note	http://www.st.com/resource/en/application_note/DM00210617.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00260340.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note	http://www.st.com/resource/en/application_note/DM00269146.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00355687.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00445657.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00607955.pdf
Application note	http://www.st.com/resource/en/application_note/DM00442720.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf