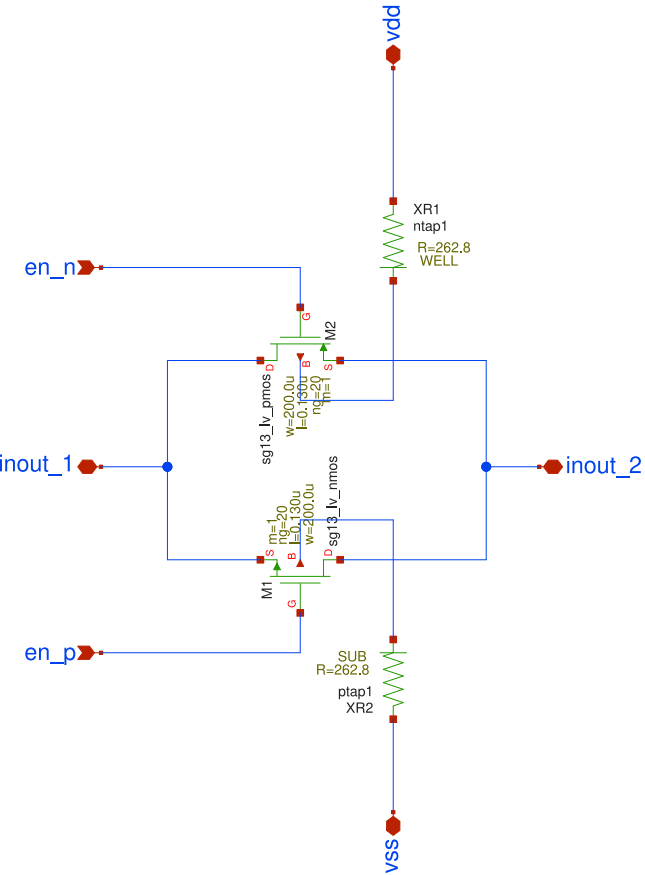
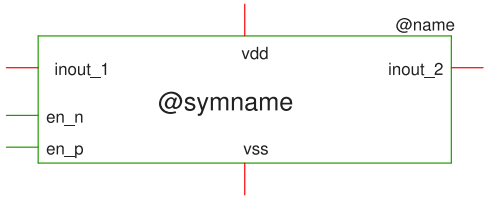
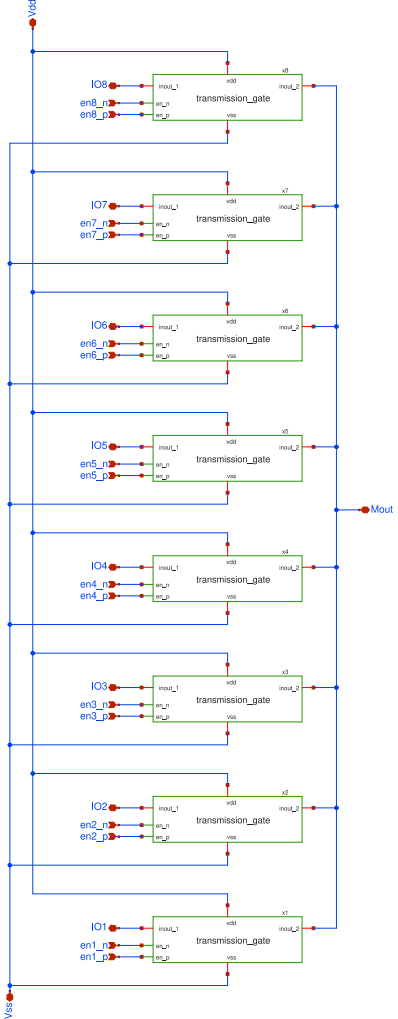
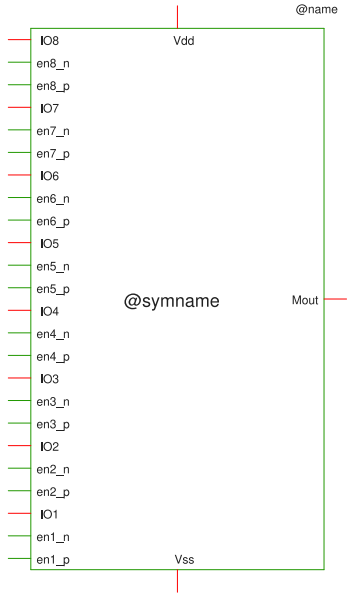

vdd
XR1
ntap1
R=262.8
WELL
en_n
M2
sg13_lv_pmos
w=200.0u
l=0.130u
ng=20
m=1
inout_1
inout_2
sg13_lv_nmos
m=1
ng=20
l=0.130u
w=200.0u
M1
en_p
SUB
R=262.8
ptap1
XR2
vss


@name
vdd
inout_1
inout_2
@symname
en_n
en_p
vss


Vdd
IO8
en8_n
en8_p
transmission_gate
IO7
en7_n
en7_p
IO6
en6_n
en6_p
IO5
en5_n
en5_p
IO4
en4_n
en4_p
IO3
en3_n
en3_p
IO2
en2_n
en2_p
IO1
en1_n
en1_p
Mout
Vss


@name
IO8
Vdd
en8_n
en8_p
IO7
en7_n
en7_p
IO6
en6_n
en6_p
IO5
en5_n
en5_p
IO4
@symname
Mout
en4_n
en4_p
IO3
en3_n
en3_p
IO2
en2_n
en2_p
IO1
en1_n
en1_p
Vss