# Intel College Excellence Program
# Project Synopsis

## “4Bit Adder/Subtractor”

<table>
<tr><th colspan="4">Team member’s detail</th></tr>
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<tr><th colspan="4">Faculty(college) mentor detail</th></tr>
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<tr><th colspan="4">College/University Name</th></tr>
<tr><td colspan="4"><b>Lovely Professional University</b></td></tr>
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## BACKGROUND

### 4 BIT ADDER

Binary addition involves combining two binary numbers bit by bit, similar to the familiar decimal addition we perform in everyday arithmetic. The project's objective is to create a functional 4-bit binary adder circuit using basic digital logic gates such as XOR (exclusive OR), AND, and OR. These gates, essential building blocks in digital circuitry, are employed to perform the logical operations necessary for binary addition.

The XOR gate is utilized to compute the sum of individual bits, while the AND gate identifies the carries generated during addition. The OR gate then combines these carries to produce the final carry-out. By cascading these gates appropriately, a 4-bit binary adder circuit is constructed, capable of adding two 4-bit binary numbers and providing a 4-bit binary output along with a carry-out.

### 4 BIT SUBTRACTOR

Binary subtraction involves subtracting one binary number from another, similar to its decimal counterpart. The project aims to create an efficient and functional 4-bit binary subtractor circuit that can accurately compute the result of subtracting one 4-bit binary number from another. Unlike addition, subtraction often involves borrowing, which poses a unique challenge in digital circuit design. The IC 7483 is a 4-bit binary full adder that plays a pivotal role in this project. It is employed to add the two's complement of the second operand to the first operand, effectively achieving binary subtraction. The two's complement is obtained by inverting each bit (using NOT gates) and adding 1 to the least significant bit.

The NOT gates are used to invert the bits of the second operand, and the resulting inverted values are fed into the inputs of the IC 7483. The carry input of the IC 7483 is set to 1, simulating the addition of the two's complement. The sum output of the IC 7483 provides the result of the subtraction, while the carry-out represents any borrow that may occur.

## PROBLEM FACED

While I was Doing this project firstly I had gone through the Truth table of adder and as I have knowledge on adder and subtractor I have drawn the circuit diagrams of them. Then I have implemented the same in proteus software by using the XOR gate, OR gate, AND gate, Logic State and Logic Probe. But as I was into the subtractor I was confused a bit and I was not getting the correct output. Then IC 7483 got into my mind as it can be used in adder or subtractor. Then I have used IC 7483 in my project for 4 Bit subtractor.

## PROPOSED SOLUTION

- IC 7483 can be used For Adder/Subtractor.

## SOFWARE REQUIREMENTS

*1.Proteus 8 software.*

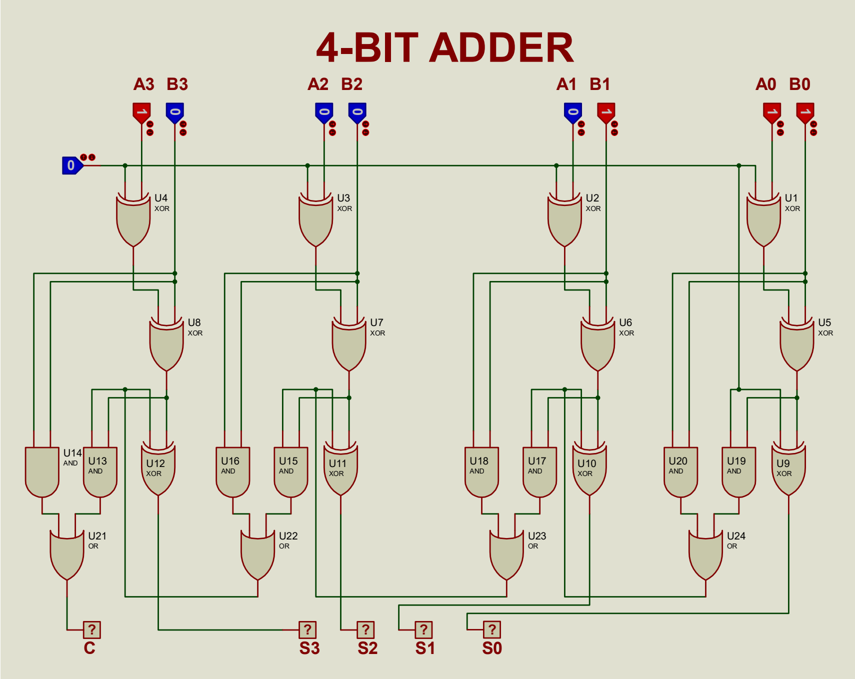
2.Libraries of proteus.

3. Laptop

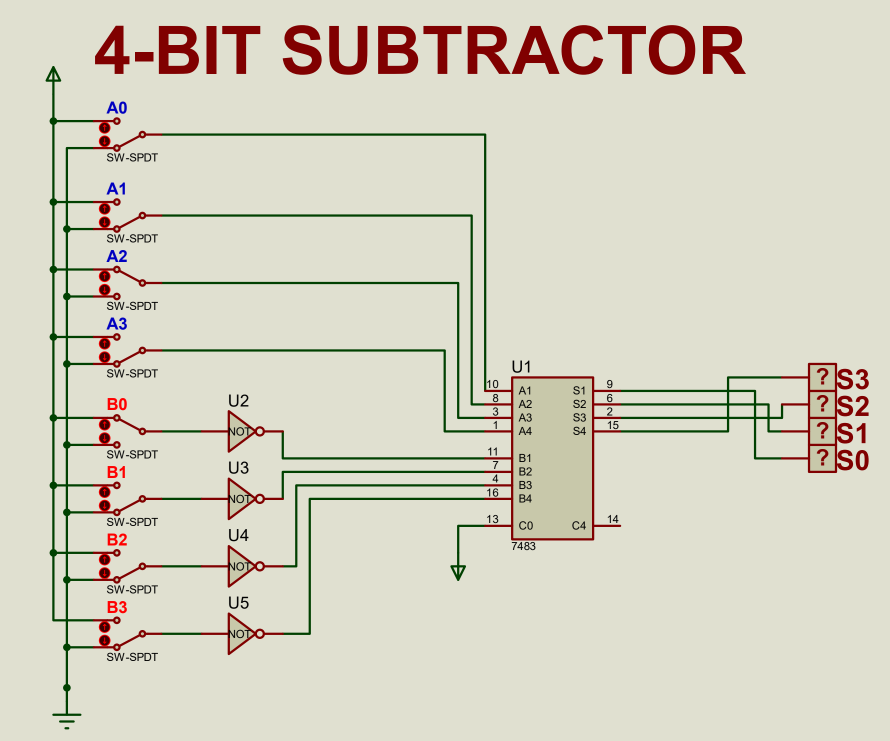
### Components Used In proteus

- XOR gate
- OR gate
- AND gate
- IC 7483
- NOT gate
- Logic State
- Logic Probe
- Power
- Switches

## CIRCUIT DIAGRAM & DESCRIPTION



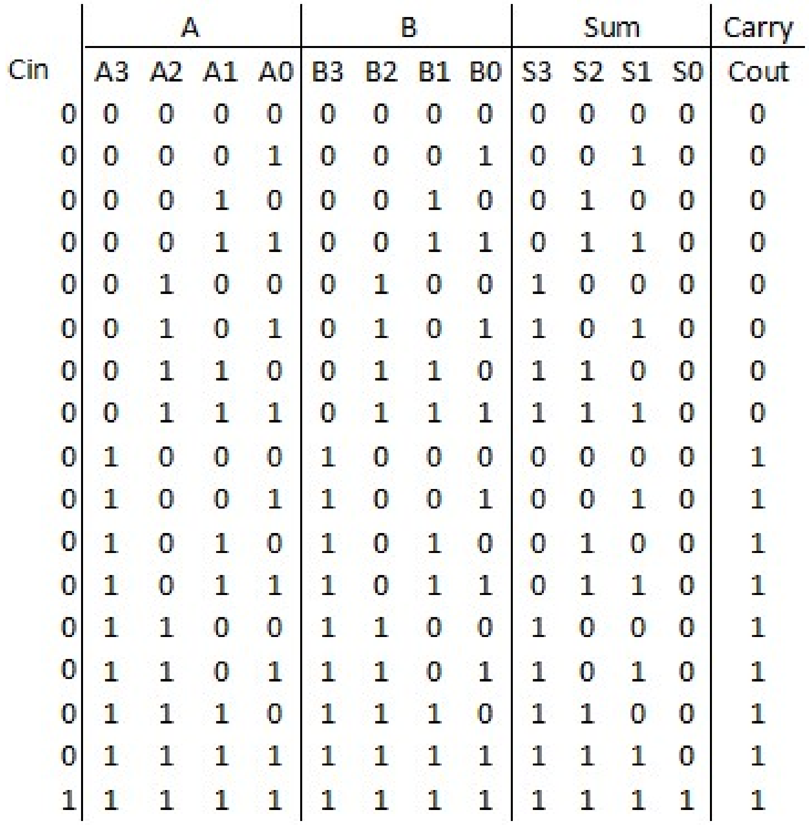
A 4-bit binary adder is a digital circuit designed to perform the addition of two 4-bit binary numbers. In the realm of digital electronics, binary addition is a fundamental operation, and a 4-bit adder is a basic building block for more complex arithmetic circuits. The circuit typically consists of XOR gates, AND gates, and OR gates, arranged in a specific configuration to achieve the desired functionality.



A 4-bit binary subtractor is a digital circuit designed to perform the subtraction of one 4-bit binary number from another. Unlike addition, binary subtraction involves the possibility of borrowing, and the design of a binary subtractor circuit needs to account for this. The circuit typically incorporates components such as NOT gates and a 4-bit binary full adder IC, such as the IC 7483, to achieve accurate subtraction.

## TRUTH TABLES

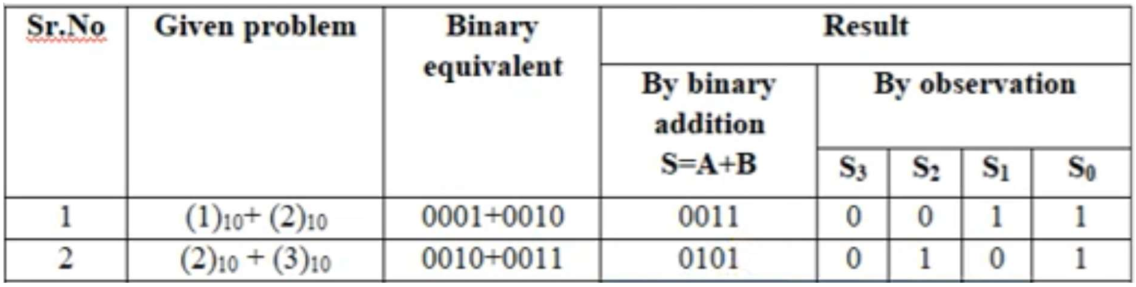
### 4 BIT ADDER:



| | A | | | | B | | | | Sum | | | | Carry |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Cin | A3 | A2 | A1 | A0 | B3 | B2 | B1 | B0 | S3 | S2 | S1 | S0 | Cout |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

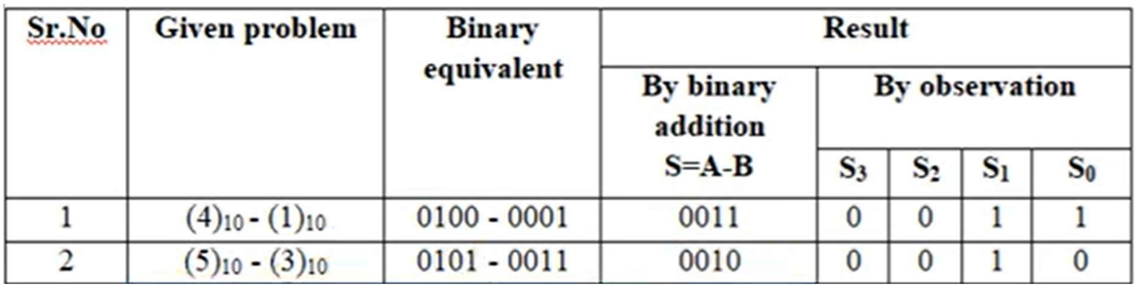
## OBSERVATION TABLE

### 4 BIT ADDER:



| Sr.No | Given problem | Binary equivalent | Result | | | | |
|---|---|---|---|---|---|---|---|
| | | | By binary addition S=A+B | By observation | | | |
| | | | | $S_3$ | $S_2$ | $S_1$ | $S_0$ |
| 1 | $(1)_{10}+ (2)_{10}$ | 0001+0010 | 0011 | 0 | 0 | 1 | 1 |
| 2 | $(2)_{10} + (3)_{10}$ | 0010+0011 | 0101 | 0 | 1 | 0 | 1 |

### 4 BIT SUBTRACTOR:



| Sr.No | Given problem | Binary equivalent | Result | | | | |
|---|---|---|---|---|---|---|---|
| | | | By binary addition S=A-B | By observation | | | |
| | | | | $S_3$ | $S_2$ | $S_1$ | $S_0$ |
| 1 | $(4)_{10} - (1)_{10}$ | 0100 - 0001 | 0011 | 0 | 0 | 1 | 1 |
| 2 | $(5)_{10} - (3)_{10}$ | 0101 - 0011 | 0010 | 0 | 0 | 1 | 0 |

## OPERATIONAL PROCESS

### 4 Bit Adder

- Each bit of the binary numbers is fed into corresponding inputs of XOR gates.
- XOR gates compute the sum of the individual bits, and the resulting sum bits are generated.
- Additionally, AND gates are used to identify the carry generated when adding each pair of bits.
- The carry bits are then fed into the next higher-order XOR gate and combined with the sum bits.
- This cascading process continues until the least significant bit to the most significant bit is processed.
- The final output consists of the 4-bit binary sum, and any carry-out indicates an overflow in the addition process

### 4 Bit Subtractor

- The second operand is transformed into its two's complement by inverting each bit using NOT gates and adding 1 to the least significant bit.
- The two's complement is then added to the first operand using a 4-bit binary full adder (IC 7483).
- The carry input of the IC 7483 is set to 1 to simulate the addition of the two's complement.
- The sum output of the IC 7483 provides the result of the subtraction, and any carry-out represents a borrow that occurred during the subtraction process.

## FUTURE SCOPE

### Bit Width Scalability:

- Extend the design to accommodate larger bit widths. This scalability is vital for applications requiring higher precision in arithmetic operations, such as in advanced computing systems and signal processing.

## CONCLUSION

In the journey of exploring and implementing 4-bit binary adders and subtractors, we've delved into the fundamental concepts of digital circuit design and arithmetic operations. The significance of these circuits lies not only in their practical applications but also in their role as building blocks for more complex digital systems.

The 4-bit binary adder, with its XOR, AND, and OR gates, embodies the essence of binary addition, showcasing the elegance of digital logic. Understanding and mastering the design principles of a binary adder is a crucial step for anyone venturing into the expansive realm of digital electronics.

On the other hand, the 4-bit binary subtractor, with the utilization of NOT gates and the IC 7483, introduces the concept of two's complement representation. This project demonstrates the versatility of digital circuits, where an adder can be repurposed to efficiently perform subtraction, highlighting the interconnectedness of various digital components.

In conclusion, the exploration of 4-bit binary adders and subtractors not only provides a hands-on experience in digital circuit design but also serves as a foundation for understanding the inner workings of more advanced computational systems. As we navigate the ever-evolving landscape of technology, these projects lay the groundwork for future innovations, pushing the boundaries of what is possible in the realm of digital electronics. The journey doesn't end here; it's a stepping stone towards a future filled with exciting possibilities and advancements in the world of digital circuitry.

## REFERENCES

https://github.com/Kshatri-Sahil/DLD_Project.git