Indian Institute of Technology, Delhi

Department of Computer Engineering and Engineering

COL215: Digital Logic and System Design

Prof. Anshul Kumar

Digital Clock

Designed by:

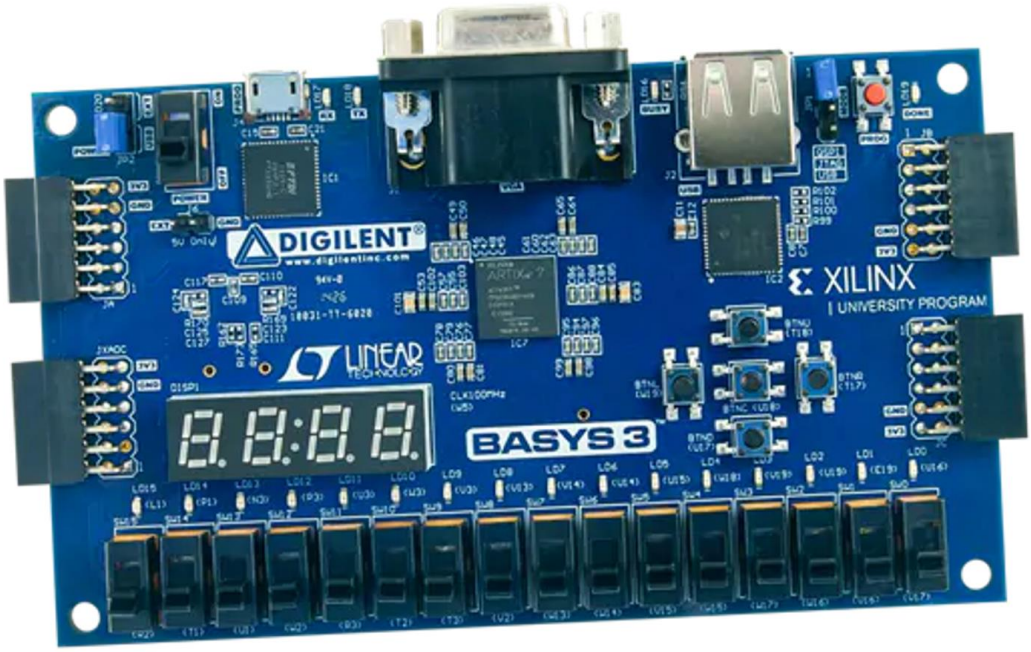
Kshitiz Bansal, 2019CS50438

Date: *18/12/20*

Introduction

This is a design of a digital clock which displays time in hours, minutes and seconds. It has been implemented on a BASYS3 FPGA board. The main features are :

- 24 hour format
- 2 display modes which show HH.MM and MM.SS (with decimal point blinking at each second)
- Digit wise setting clock time
- Reset clock with just one click



Design Overview:

All of the major design decisions were taken keeping in mind the convenience of the user. Some of them are:

- Chose to provide the feature of being able to set each digit independently. It is much more convenient.
- Chose against a seconds setting option. I believe that there is no practical use of being able to change the seconds in a clock. If in some situation it is really needed, then it can be done in a maximum time of 60 seconds by changing the minutes value.
- Incorporated both increment and decrement because I believe it is much more convenient to do 5 presses of a button instead of 10 to reach the desired value. For 4 digits, it is a maximum of 20 presses. Had I only implemented increment, it would have been 40 presses.

We were told to keep user convenience in mind, so I chose to use the 5^{th} button too to implement decrement. According to me, having dedicated buttons for increment and decrement on the clock is more convenient than having to sit and press a button for say 40 times.

- Incorporated two display modes. One of them displays time in the format HH.MM. The other mode displays time in the format MM.SS. The central decimal point blinks at each second in both the modes.

Design Description:

Two entity-architecture pairs have been defined:

- to_display
- dig_clock

Their specifications have been discussed after the state diagram.

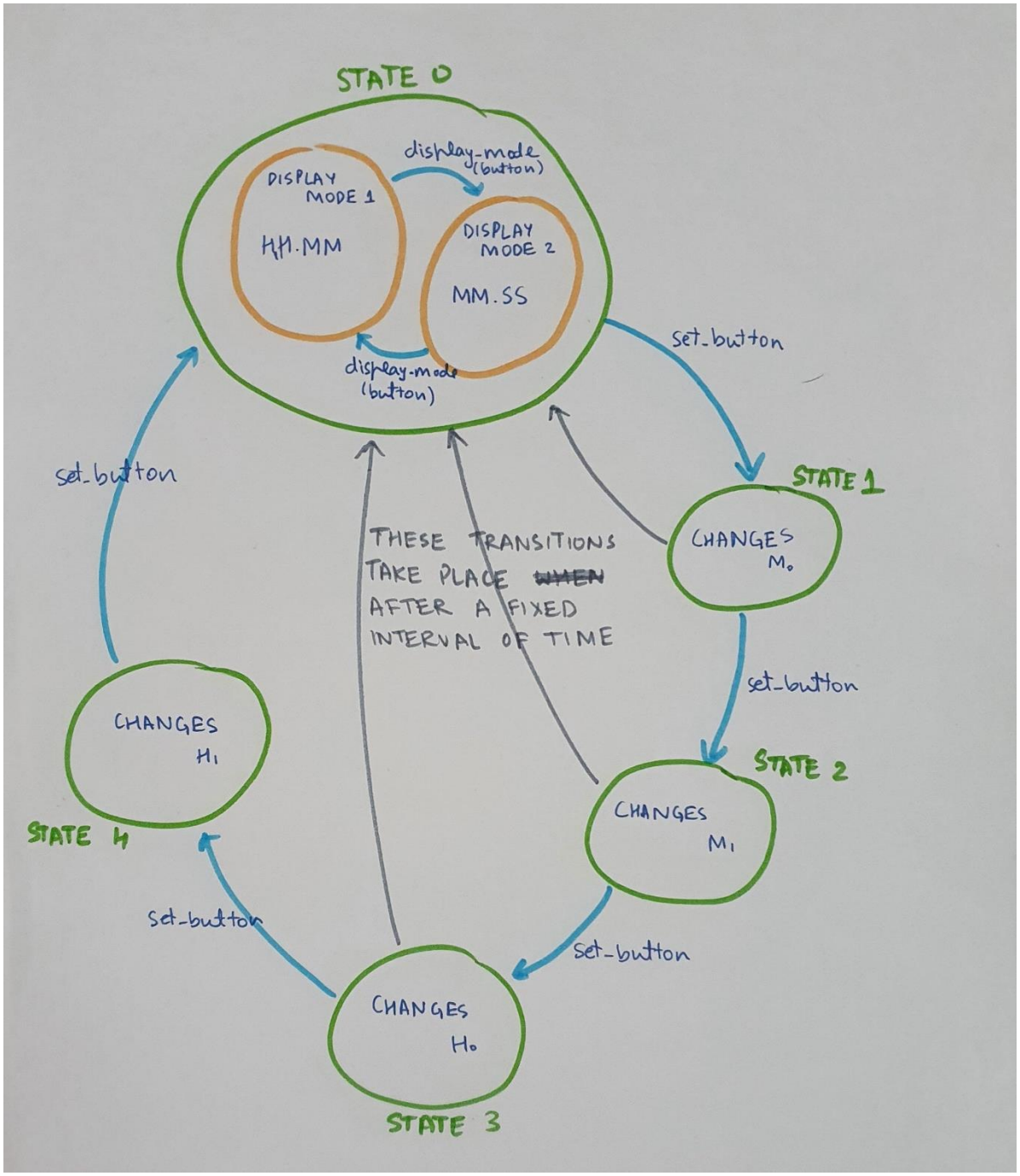
Inputs:

- Display_mode (Button 1)
- Set_button (Button 2)
- Increment (Button 3)
- Decrement (Button 4)
- Reset (Button 5)
- Master clock

Outputs:

- Seven-segment display cathode and anode values

State Diagram:-



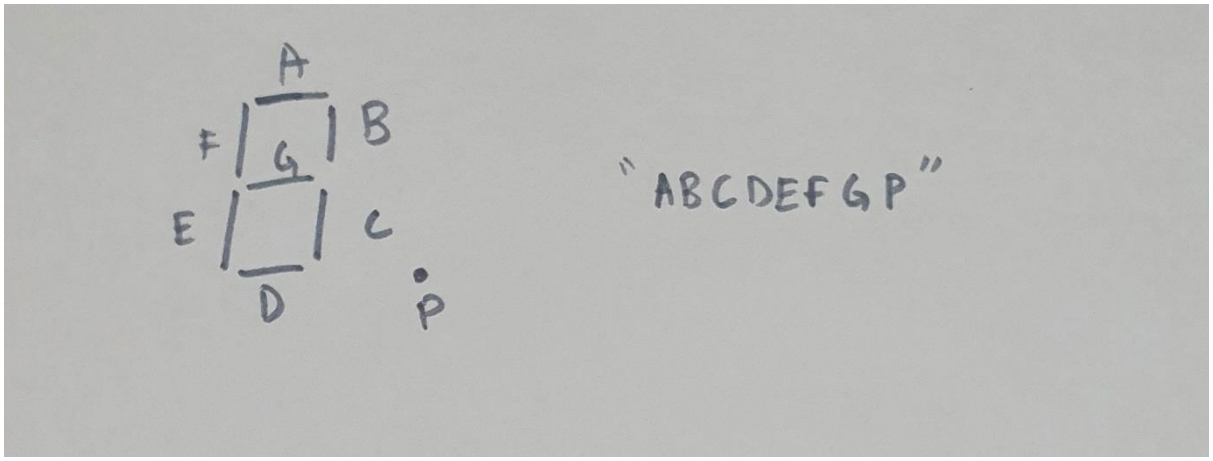
NOTE: The colours of transitions are referred to in the description

VHDL Code Description:

Note: Please read the comments in the code too.

1. to_display

This architecture-entity pair has been defined to convert the numbers to be displayed to the corresponding cathode values. It outputs a std_logic_vector of length 8 whose values correspond to seven segment as :



NOTE: 0 = LED ACITIVE, 1 = LED NOT ACTIVE

2. dig_clock

Signals used:

- myclk1, myclk2, myclk3 : They are derived periodic signals created from the master clock. They are of frequency 1Hz, 2Hz and 250Hz respectively.
- count1, count2, count3: They are the counting signals used to create the needed clocks.
- st1, st2, st3, st4, st5, st6: They are the signals which store the state value for the last six seconds or the six clock cycles of myclk1. They are used to change back to the base state (display state) when left idle after setting the time. If they all are same at one point, it means that the set_button has not been pressed in the past six seconds. So it should go back to the base state.
- h1, h0, m1, m0, s1, s0: They are the time values. (Tens and units digits)
- h1_disp, h0_disp, m1_disp, m0_disp, s1_disp, s0_disp: They are the cathode values for the time signals.
- state: It is the state signal. Used to move between states.
- disp: It is used to toggle between the two display modes.
- prev_display_mode, prev_set_button, prev_increment, prev_decrement, prev_reset: These signals are used to ensure that one press leads to only one operation (have to be left and then pressed again to repeat operation). They are needed to check the rising edges of signals coming from the push buttons.

- x: It is used to display the numbers. It takes values in range [0, 3] where each value corresponds to one of the display digits. Helps to display the four digits one by one which are perceived as constant by us.
- blink: It is the toggling signal used to drive the central decimal point in a blinking fashion representing the seconds.

Processes:

- Line 70 [process(clk)]
  It creates the desired clocks myclk1, myclk2 and myclk3.
- Line 93 [process(myclk1)]
  It implements the grey coloured (move to base state when idle) transitions.
- Line 106 [process(myclk1, display_mode, set_button, increment, decrement, reset)]
  It first of all implements the reset feature and updates the time value periodically. After that, it moves on to implement the blue coloured transitions (driven by the push buttons). Checks set_button, increment and decrement and does the required work. Also checks the display_mode button and toggles the display.
- Line 235 [process(myclk2)]
  It just toggles the value of signal blink to be able to facilitate flashing of the decimal point.
- Line 244 [process(myclk3)]
  This is the displaying process. It displays out the numbers. One special step done here is the tweaking of cathodes value of the 2^{nd} digit (in display board) to make the associated decimal point blink. Cathodes(0) is replaced with blink.