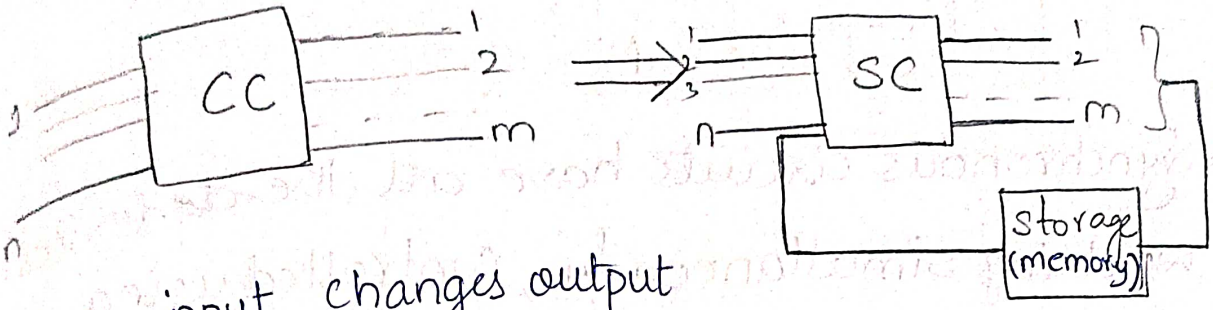
06/08/2022

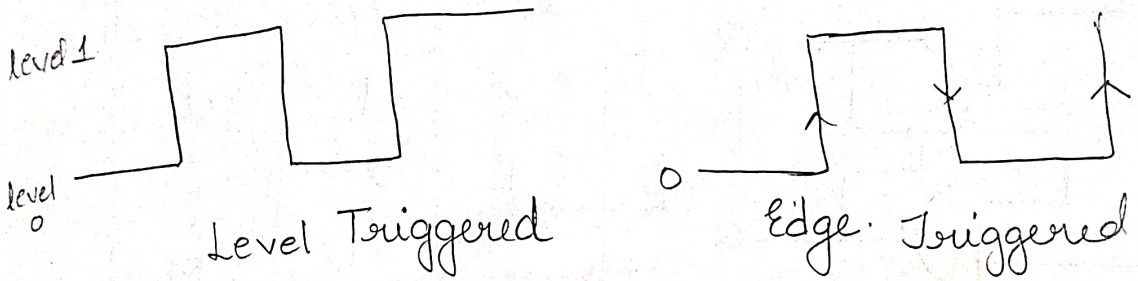
UNIT-4

SEQUENTIAL CIRCUITS



When input changes output also changes i.e. asynchronous behaviour.

→ 1MHz = 1×10^6 cycles/sec

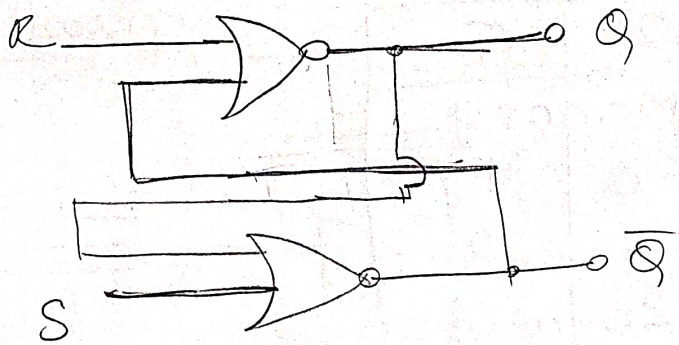


* Output depends on input as well as positive clock pulse. – LEVEL TRIGGERED

* Output depends on ~~repeat~~ input; depends on edge trigger → EDGE TRIGGERED.

clocked – flipflop
unclocked – latch

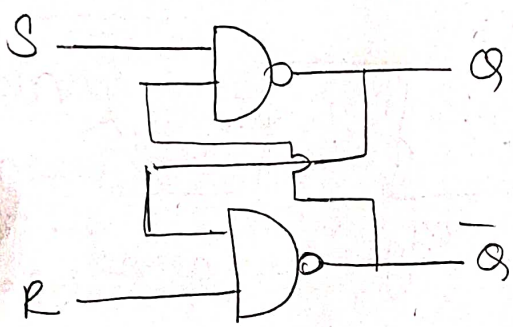
* SR LATCH: (NOR)



Reset	Set	Q	$\overline{Q}$
0	0	Memory	
0	1	1	0
1	0	0	1
1	1	Invalid	

* Synchronous circuits have all the ~~de~~ devices working simultaneously., controlled using clock.

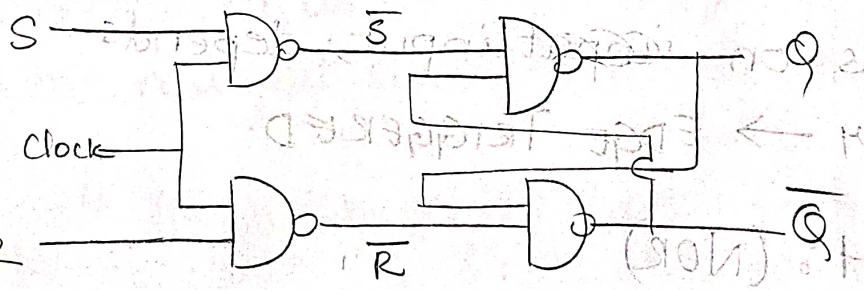
* SR LATCH: Asynchronous → holds the data for sometime but not controlled



R	S	Q	$\overline{Q}$
0	0	Invalid	
0	1	0	1
1	0	1	0
1	1	Memory	

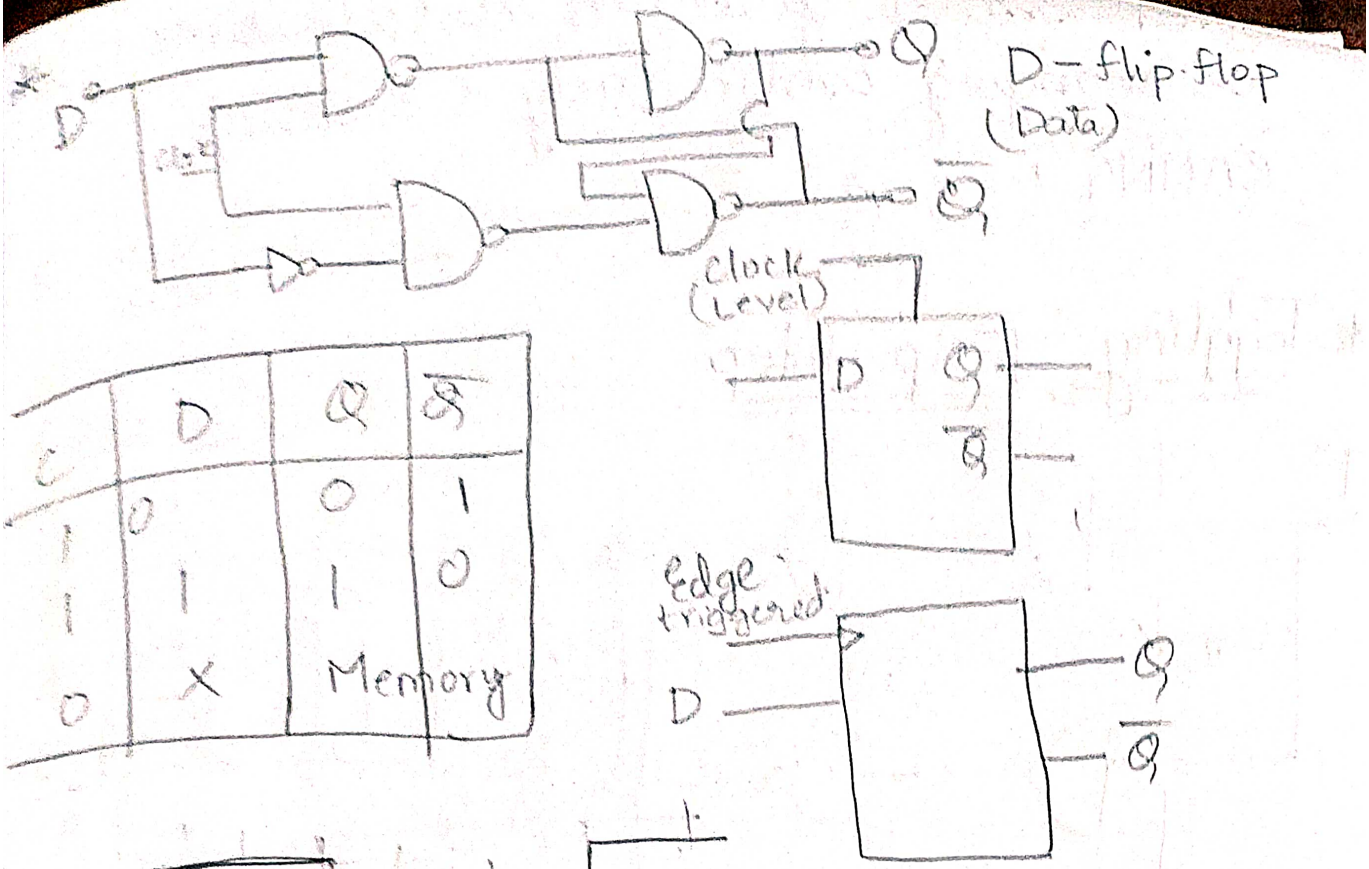
No control.

* Clocked SR Latch: Synchronous (flip-flop) SR

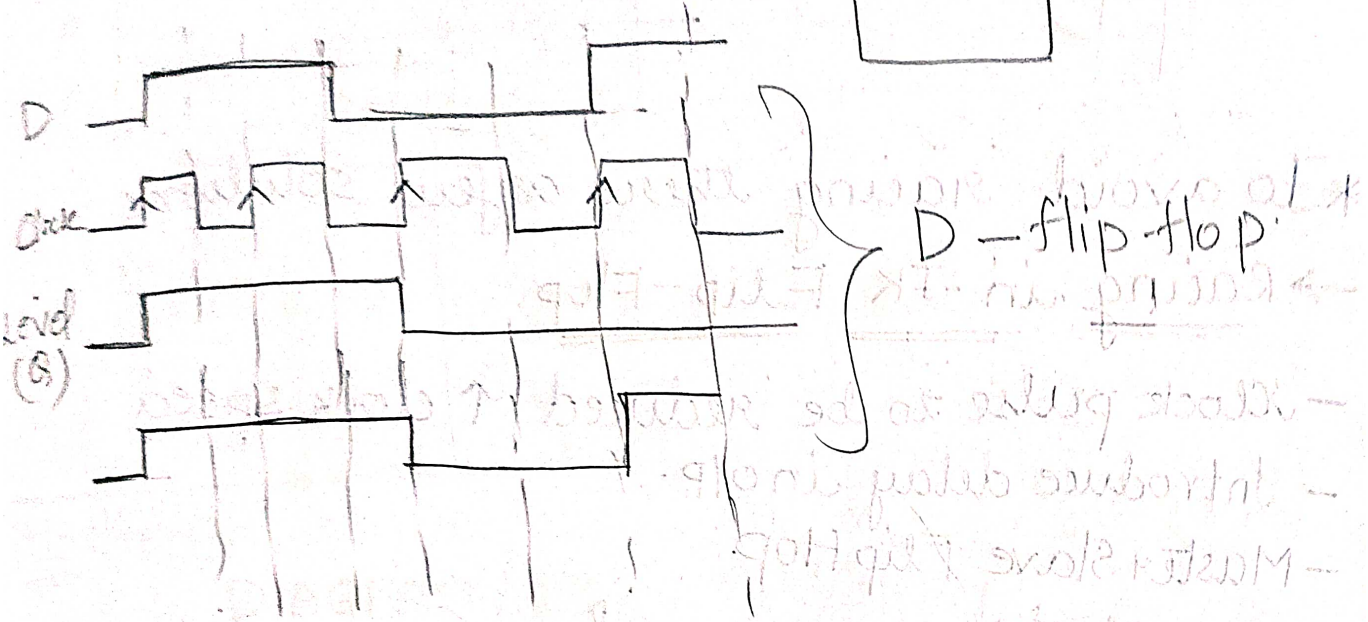


→ 1 single bit requires this complete circuit

Clock	S	R	Q	$\overline{Q}$
1	0	0	Memory	
1	0	1	0	1
1	1	0	1	0
1	1	1	Invalid	
0	x	x	Memory	

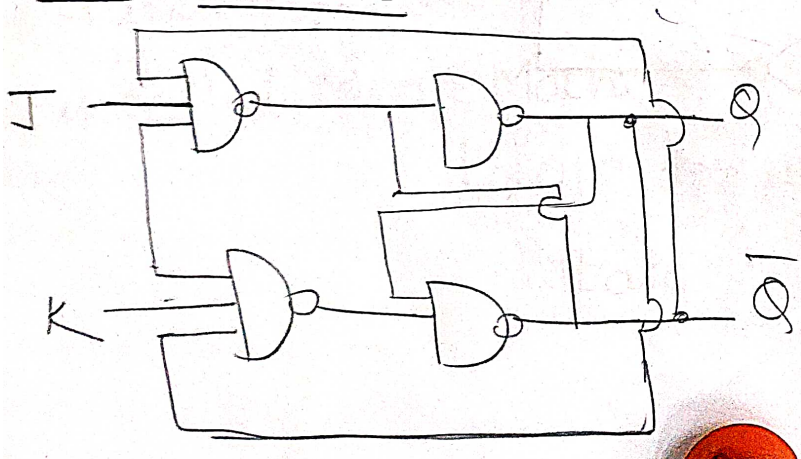


C	D	Q	$\overline{Q}$
1	0	0	1
1	1	1	0
0	x	Memory	



* The problem with SR latch is Invalid (1-1 condition)

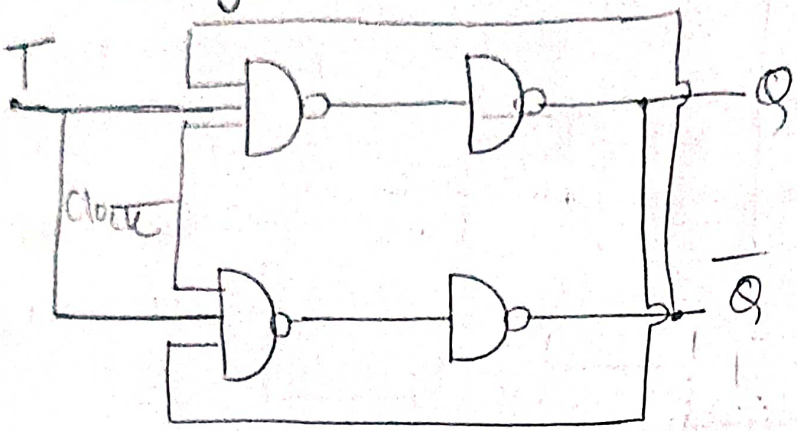
*JK Flip flop



clock	J	K	Q $\overline{Q}$
0	x	x	Memory
1	0	0	Memory
1	0	1	0 1
1	1	0	1 0
1	1	1	Racing

- If the values given in certain time are changing continuously i.e. called RACING (Toggling)

* Toggling Flip-Flop:

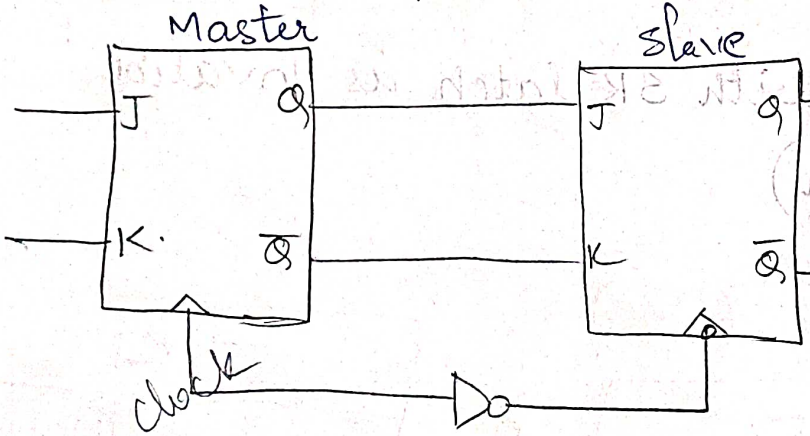


Clock	T	Q
0	X	Mem
1	0	Mem
1	1	Toggl

* To avoid racing there are few solutions.

→ Racing in JK Flip-Flop:

- Clock pulse to be reduced ↑ clock speed
- Introduce delay in O/P.
- Master Slave Flip flop



clock	S	R	Qn+1
0	X	X	Qn
1	0	1	0
1	1	0	1
1	1	1	Invalid

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* I/P + Present state ⟶ Next state Qn+1 : Characteristic behaviour

* Present state + Next state ⟶ I/P's : Excitation Table

* Characteristics Table: Clock = 1

S	R	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Qn
1	1	1	Qn

* Excitation Table:

Clock = 1

Qn	Qn+1	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

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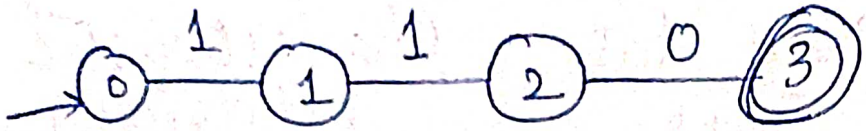
* STATE DIAGRAM / STATE MACHINE:

→ Initial State / start : → ○ on state

→ Terminate / Final : ◎ off state

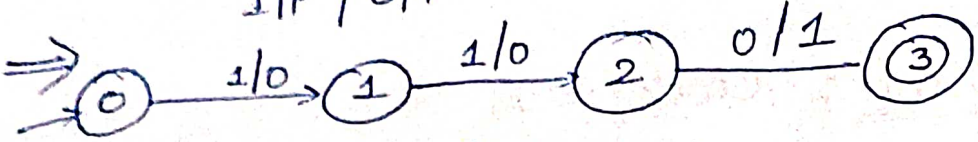
* A machine designed for a particular string is called Moore Machine.

↳ O/P dependent on present State.



* Success – O/P : 1 else 0

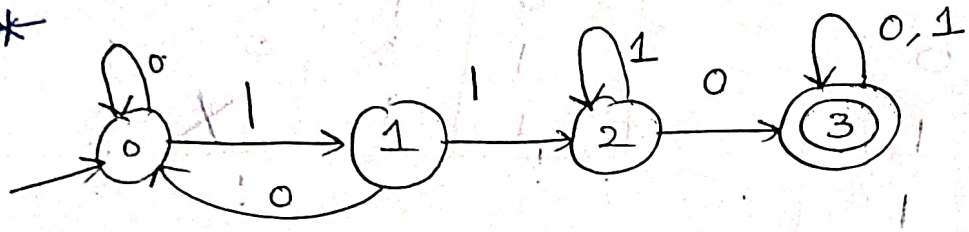
I/P / O/P



Mealy Machine

↳ O/P is dependent on I/P & present state

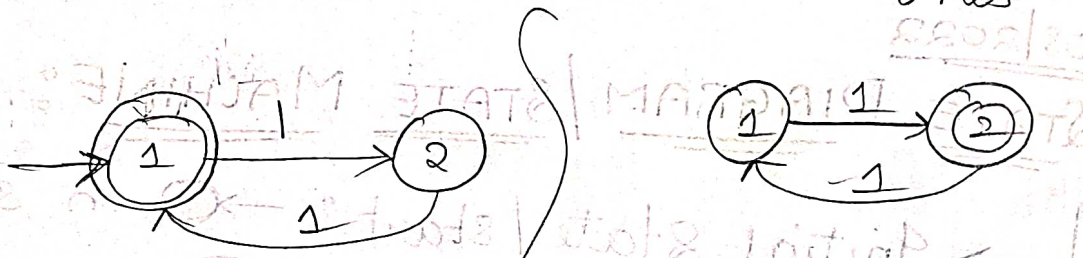
*



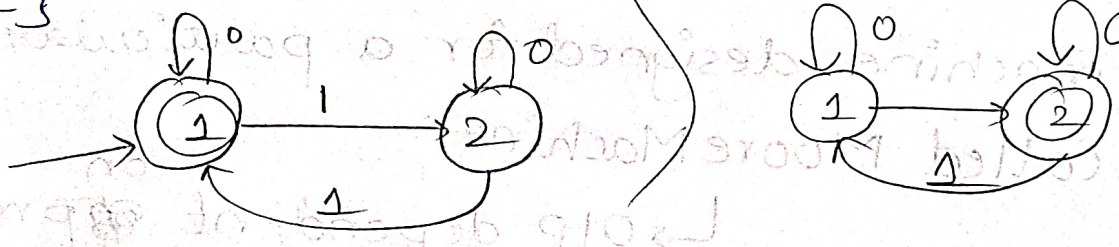
* Draw a state diagram to accept even no. of ones

Odd no. of ones

$\Sigma = \{1\}$



$\Sigma = \{0, 1\}$



Sequence detector

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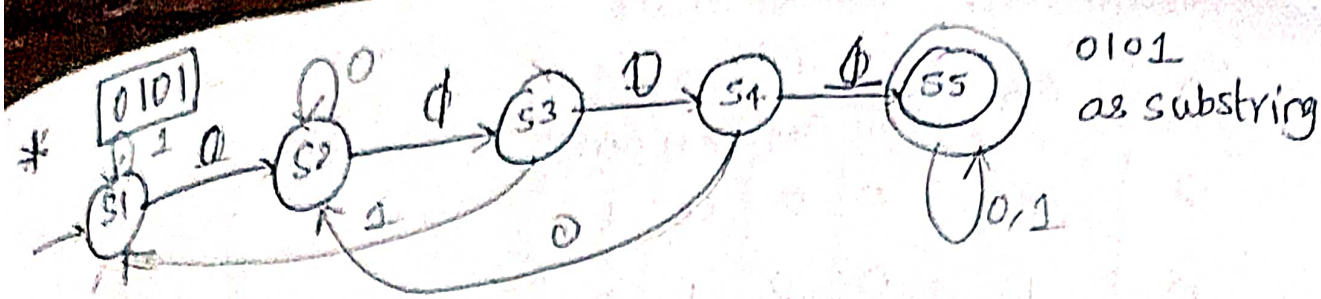
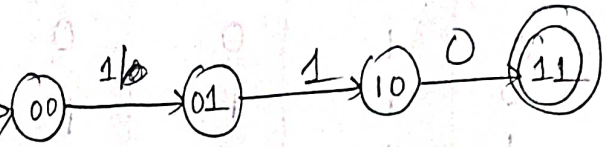


* State diagram to sequential circuit

1) For a given problem draw state
2) Label the states in binary function/form
3) State Table preparation.
4) Excitation table of the flip-flop.
5) Boolean function significance
6) Circuit.



* State Table of 110.

Design a sequence detector that detects 110 using T-flipflop.

Present state		Next state		
		$x=0$ (input)	$x=1$	
Q_A	Q_B	Q_{A+1}	Q_{B+1}	
0	0	0	0	1
0	1	0	1	0
1	0	1	1	0
1	1	1	1	1

Clock	T	Q_{n+1}
0	x	Q_n
ϕ	0	Q_n
1	1	$\overline{Q_n}$

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

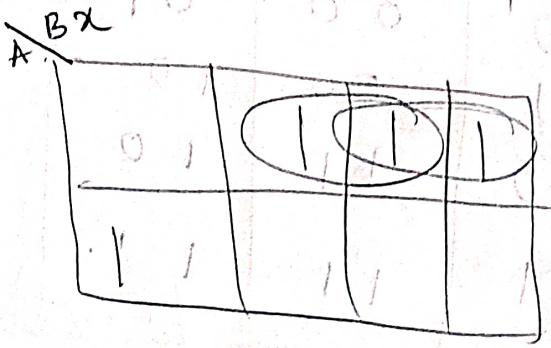
No. of flip-flops depends upon no. of bits in P.S.

Present State		Next State			
		$x=0$		$x=1$	
Q_A	Q_B	Q_{A+1}	Q_{B+1}	Q_{A+1}	Q_{B+1}
0	0	0	0	0	1
0	1	0	0	1	0
1	0	1	1	1	0
1	1	1	1	1	1

Q_A	Q_B	x (I/P)	Q_{A+1}	Q_{B+1}	T_A	T_B
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	0	0	1
0	1	1	1	0	1	1
1	0	0	1	0	1	0
1	0	1	1	1	0	1
1	1	0	1	0	0	0
1	1	1	1	1	0	0

$T_A = \bar{Q}_A Q_B x$

$T_B = \Sigma(1,2,3,4)$

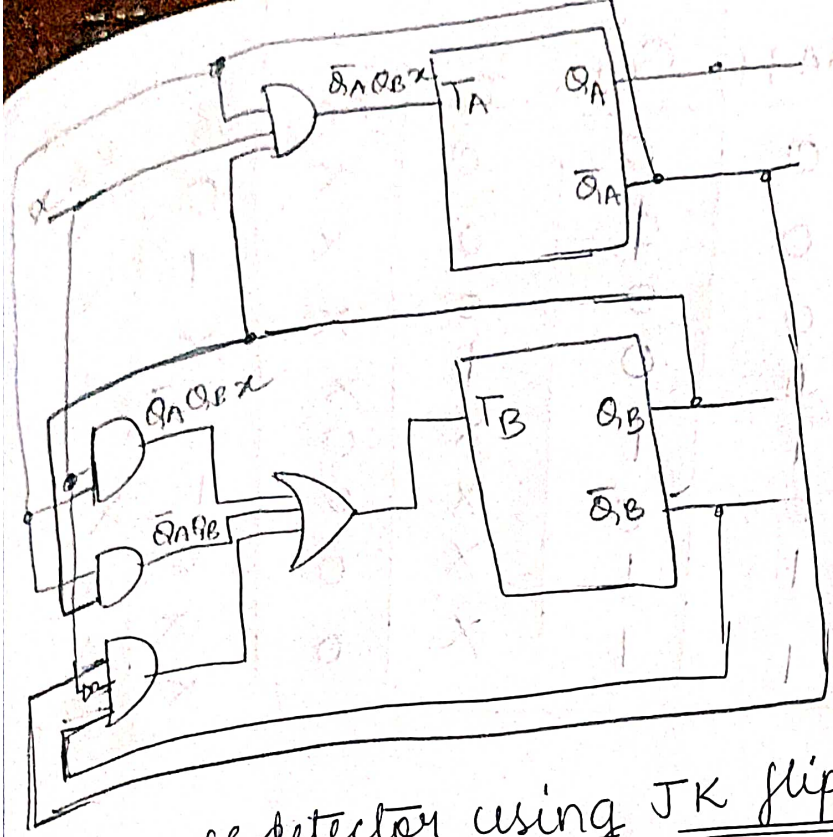


$T_A = \bar{Q}_A Q_B x$

$T_B = \bar{Q}_A x + \bar{Q}_A Q_B + Q_A \bar{Q}_B \bar{x}$

* Circuit

T – flipflop



*Sequence detector using JK flip flop:

characteristic table:

C	J	K	Q_{n+1}
0	X	X	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}_n$

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Excitation Table:

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q_A	Q_B	x	Q_{A+1}	Q_{B+1}	J_A	K_A	J_B	K_B
0	0	0	0	0	0	×	0	×
0	0	1	0	ϕ	0	×	1	×
0	1	0	0	0	0	×	×	1
0	1	1	1	0	1	×	×	1
1	0	0	1	1	×	0	1	×
1	0	1	1	0	×	0	0	×
1	1	0	1	1	×	0	×	0
1	1	1	1	1	×	0	×	0

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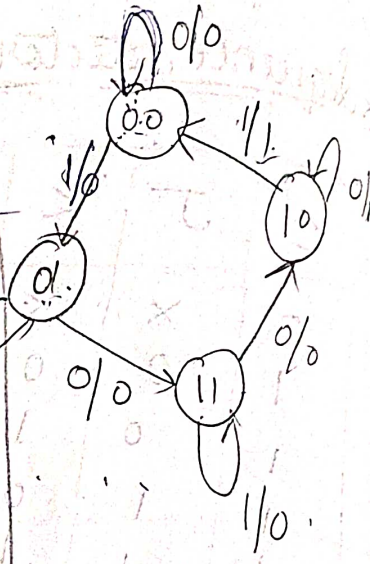
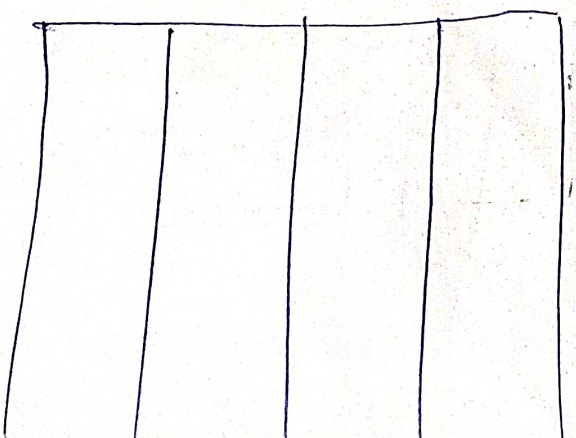
Q_A	Q_B	x input	Q_{A+1}	Q_{B+1}	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	ϕ	0	1	1	0
0	1	1	0	1	0
ϕ	0	0	1	0	1
1	0	1	0	0	1
1	1	0	1	0	0
1	1	1	1	1	0



SR - F.F:



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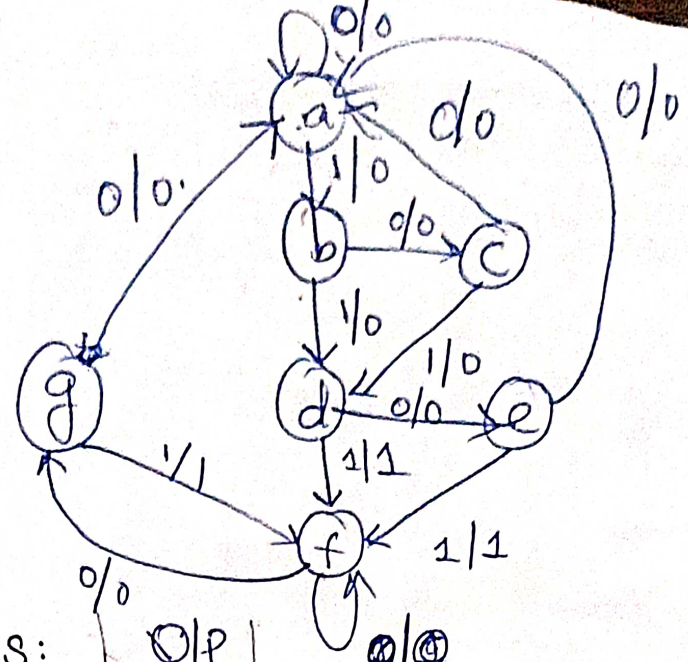
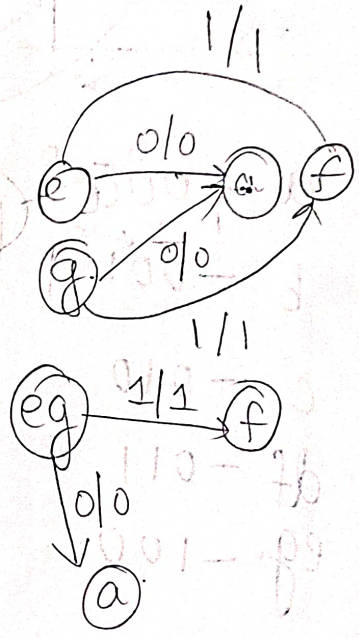
a - 000
b - 001
c - 010
d - 011
e - 100
f - 101
g - 110

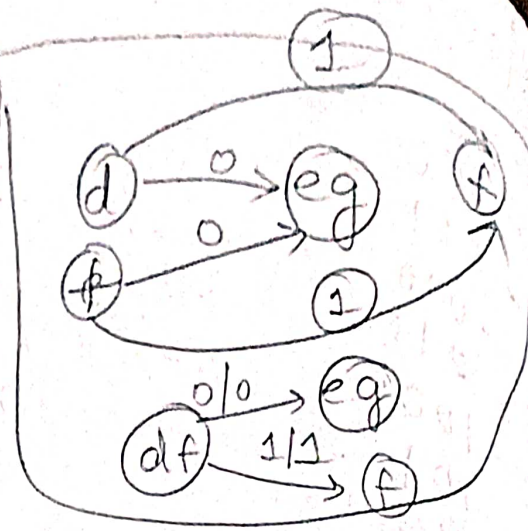


P.S	I/P	N S:	O/P
a	0	a *	0
a	1	b	0
b	0	c	0
b	1	d	0
c	0	a *	0
d	1	d	0
d	0	e	0
d	1	f	1
e	0	a	0
e	1	f ✓	1
f	0	g	0
f	1	f	1
g	0	a	0
g	1	f ✓	1



Both o/Ps and I/Ps shd match while merging

a	0	a	0
a	1	b	0
b	0	c	0
b	1	df	0
c	0	a	0
c	1	df	0
df	0	eg	0
df	1	df	1
eg	0	a	0/
eg	1	df	ϕ



a – 000
b – 001
c – 010
df – 011
eg – 100

P.S	I/P	N.S	O/P
000	0	000	0
000	1	001	0
001	0	0ϕ0	0
001	1	011	0
010	0	000	0
010	1	011	0
011	0	100	0
011	1	011	1
100	0	000	0
100	1	011	1

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LST

Truth table: D-flip-flop

Clock	D	Q_{n+1}
0	x	Q_n
1	0	0
1	1	1

Excitation Table

Q	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

$D = Q_{n+1}$

Characteristic Table

Clock = 1

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

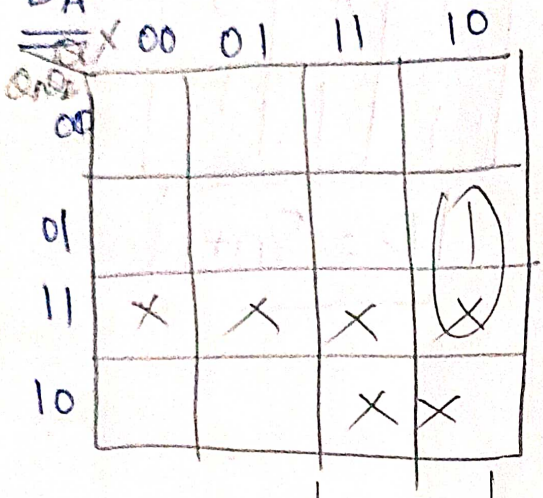
Q_A	Q_B	Q_C	Q_{A+}	Q_{B+}	Q_{C+}	D_A	D_B	D_C
0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	0	1	0	1	1	0	1	1
0	1	0	0	0	0	0	0	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
0	1	1	1	0	1	1	0	1
1	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	1	1

$D_A = \Sigma m(6) + d(10 \text{ to } 15)$

$D_B = \Sigma m(2,3,5,7,9) + d(10 \text{ to } 15)$

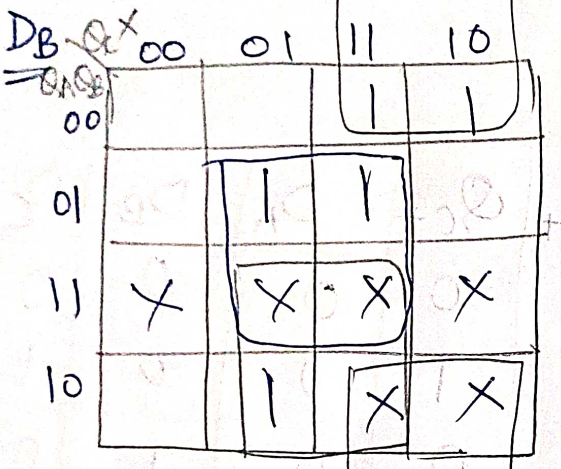
$D_C = \Sigma m(1,3,5,7,9) + d(10 \text{ to } 15)$

D_A



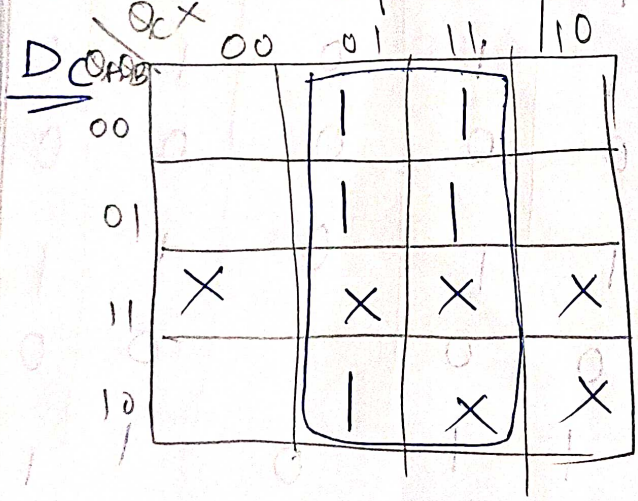
$D_A = Q_B Q_C \overline{X}$

D_B



$D_B = Q_B X + \overline{Q_B} Q_C + Q_A X$

D_C



$D_C = X$

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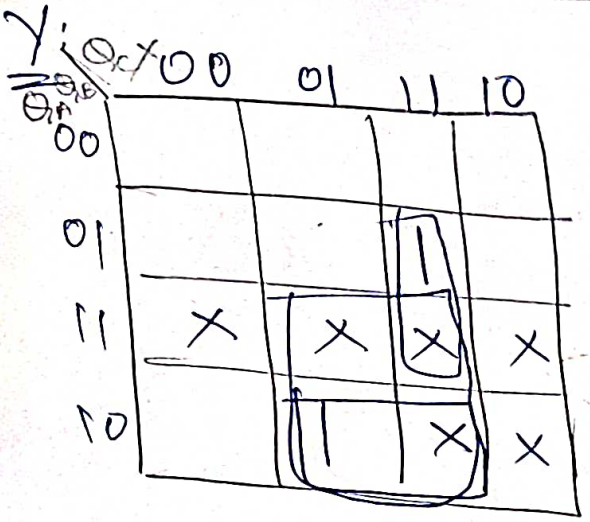
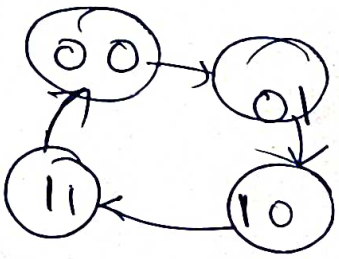


$$Y = Q_A X + Q_B Q_C X$$

*

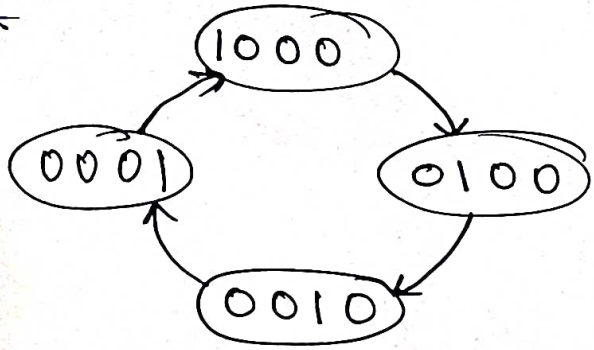


Q_A	Q_B	Q_{A+1}	Q_{B+}	D_A	D_B
0	0	0	1	0	1
0	1	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	0

Counter - 0-3 (or) mod 4
(or) Modulo 4 counter.

$$D_A = Q_A \oplus Q_B$$
$$D_B = \overline{Q_B}$$

*



Ring Counter.

0
1
2
3 ↕ up counter.

3
2
1
0 ↑ down counter.

* DIFFERENT TYPES OF COUNTER:

- Up counter
- Down counter
- Modulo 4 counter
- Ring counter.
- Johnson Counter.

* Ripple Counter:

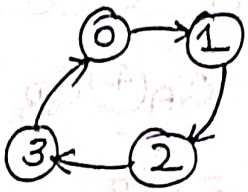
up: 0 to 5 (low to high)
down: 5 to 0 (high to low)

mod 7: 2/7.

0 0 0
0 0 1
0 1 0
0 1 1
1 0 0
1 0 1
1 1 0
1 1 1

ring: 1000, 0100, 0011, 0001

* mod 4



Present State		Next State	
A	B	A^+	B^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

D-flip-flop:

Excitation Table

Qn	Qn+	D
0	0	0
0	1	1
ϕ	0	0
1	1	ϕ

A	B	A^+	B^+	D_A	D_B
0	0	0	1	0	ϕ
0	1	1	0	1	0
1	0	1	1	1	1
1	1	0	0	ϕ	0

$D_A = A \oplus B$

$D_B = \overline{B}$

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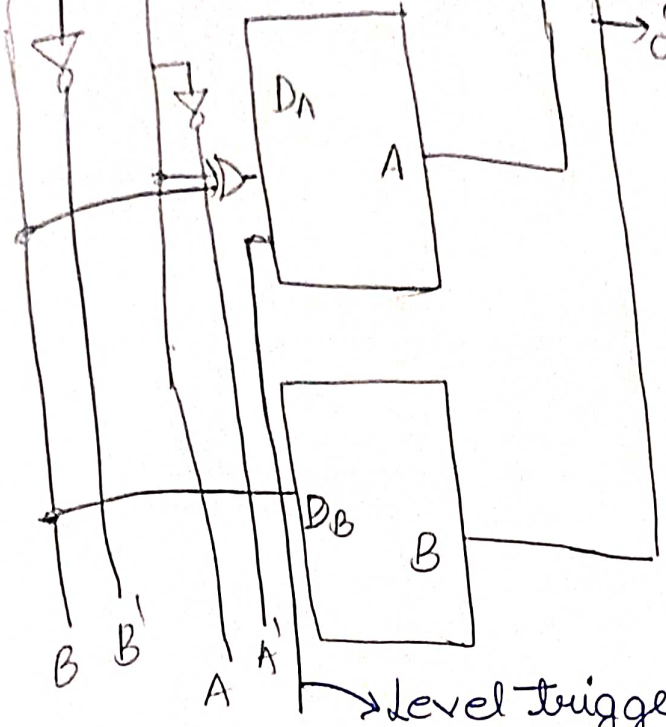


→ SYNCHRONOUS:

There is a extra clock which is defining the whole circuit.

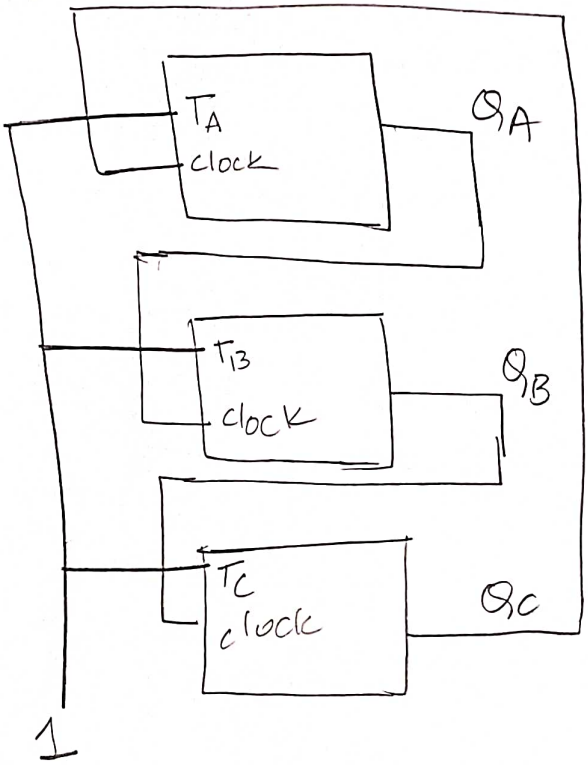
→ Level trigger.

* ~~Relay Counter~~:

* Ripple counter: 3-bit counter

↳ Delay in processing the input.

* Use of behaviour of ripple to get output.



* D, SR, JK, T : 0 = Memory

* T : 1 → Toggle.