

17/01/2022

LINE REGULATION: Protecting R_L from AC fluctuations.

$V_{in} \rightarrow \text{vary} \Rightarrow R_L \rightarrow \text{const}; I_L \rightarrow \text{const}$

• $V_{in} \uparrow \text{ses}$

$I_T \uparrow \text{ses}$

$I_z \uparrow \text{ses}$

$V_z \rightarrow \text{const}$ (by virtue of its property)

• $V_{in} \downarrow \text{ses}$
 $I_T \downarrow \text{ses}$
 $I_z \downarrow \text{ses}$
 $V_z \rightarrow \text{const}$

LOAD REGULATION: $V_{in} \rightarrow \text{const} I_T \rightarrow \text{const}$

$R_L \rightarrow \text{vary} I_L \rightarrow \text{vary}$.

• $R_L \uparrow \text{ses}$

$I_L \downarrow \text{ses}$

$I_z \uparrow \text{ses}$

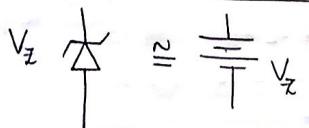
$V_z \rightarrow \text{const}$

I_z should not ~~exceed~~ $\uparrow \text{se}$

above $I_z(\text{max})$

• $R_L \downarrow \text{ses}$
 $I_L \uparrow \text{ses}$
 $I_z \downarrow \text{ses}$ (I_z should not reduce beyond $I_z(\text{min})$)
 $V_z \rightarrow \text{const}$

* Equivalent circuit:



$$V_{in} = I_T R_s + V_z$$

$$R_s = \frac{V_{in} - V_z}{I_T}$$

$$R_s = \frac{V_{in} - V_z}{I_z + I_L}$$

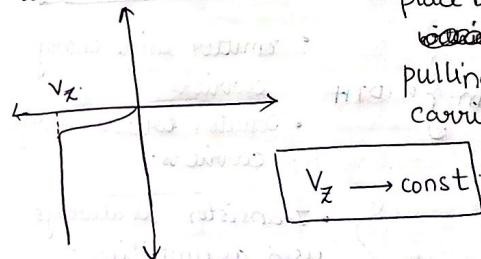
$$I_z = \frac{V_{in} - V_z}{R_s} - I_L$$

* Breakdown Mechanisms in Zener diode:

→ Zener breakdown

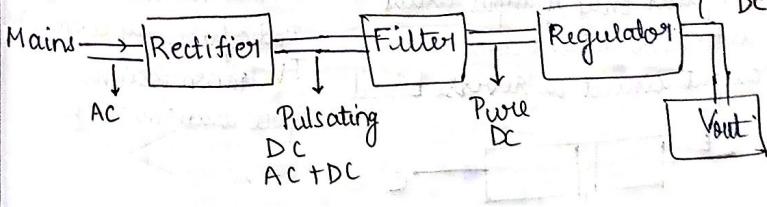
$< 6V$

Sufficient to pull the charge carriers from VB ~~area~~; depletion layer through, due to $\uparrow \text{ses}$ in velocity; collisions take place b/w atoms ~~area~~ apart from pulling away charge carriers.



* Continuous; successive multiplication of formation of charge carriers due to external electric field & heavy doping is called AVALANCHE

Regulated DC Voltage Power Supply:



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TRANSISTORS:

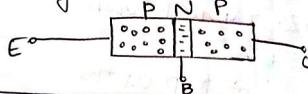
→ Transfer Resistor

→ Transferred

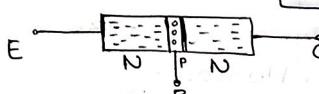
→ Signal is transferred from low resistance to high resistance region.

BJT: Bipolar Junction Transistor: → 2 functions

Two types: (i) NPN (ii) PNP.



NPN:



BJT is 3 layered device with 2 junctions

Collector → large
Emitter → medium } WIDTH.
Base → & thin

- Emitter emits charge carriers
- Collector collects charge carriers.

* Doping levels:

Emitter is heavily doped.

Base very lightly doped.

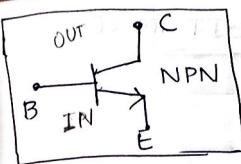
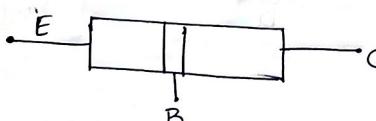
Collector moderately doped.

- Transistor is always used as amplifier

- Used as oscillators, switch, communication
- Radio frequency communication
- TV transmission, Space transmission

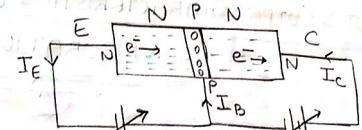
NPN BJT WORKING :

* Transistor operates as an amplifier only if input circuit is forward biased and output circuit is reverse biased



$$I_B = 5\% \text{ of } I_E$$

$$I_C = 95\% \text{ of } I_E$$



$$I_E > I_C > I_B$$

conventional current direction is opposite to e⁻ flow direction.

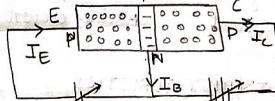
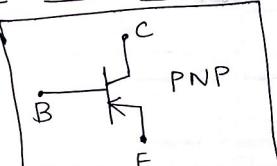
$$I_E = I_B + I_C$$

$$I_C = 95\% \text{ of } I_E + I_{CBO}$$

Reverse leakage current: Collector to base current when emitter is open (off state).

I_{CBO}

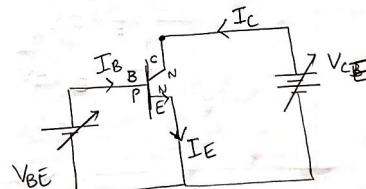
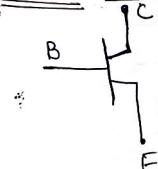
PNP BJT WORKING



There are 3 types of configurations:

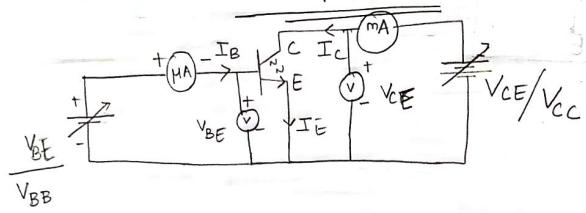
- Common Base
- Common Emitter
- Common Collector

COMMON EMITTER:



Collector of CE configuration is connected to the +ve terminal of battery to make output circuit gave

INPUT & OUTPUT CHARACTERISTICS OF BJT IN CE CONFIGURATION:



Note: To plot input characteristics of BJT can be plotted by varying INPUT VOLTAGE & noting down the input current by keeping output voltage constant.

This holds good for all the configurations.

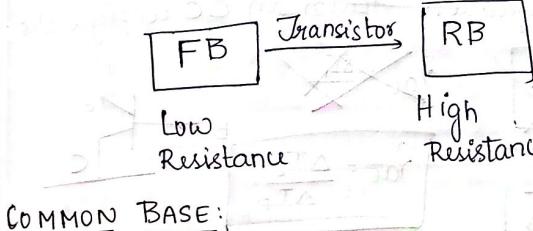
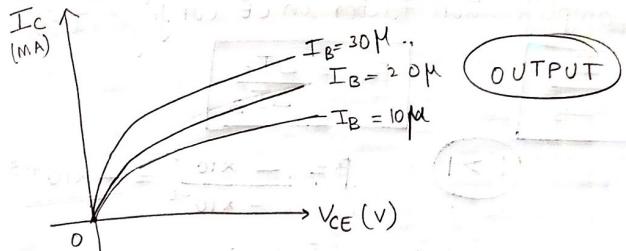
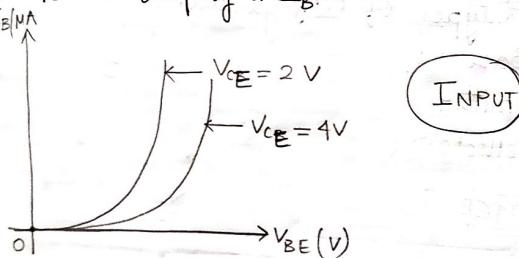
To plot output characteristics of BJT can be plotted by varying OUTPUT VOLTAGE; keeping input current constant & noting down output current.

INPUT CHARACTERISTICS

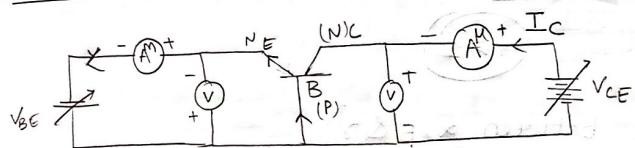
V_{BE} V/S I_B keeping V_{CB} const

OUTPUT CHARACTERISTICS:

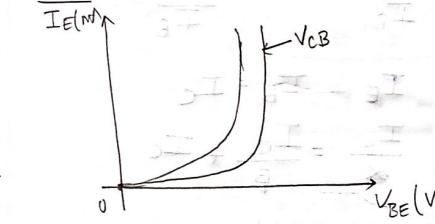
V_{CE} V/S I_C keeping I_B const.



COMMON BASE:



INPUT CHARACTERISTICS:



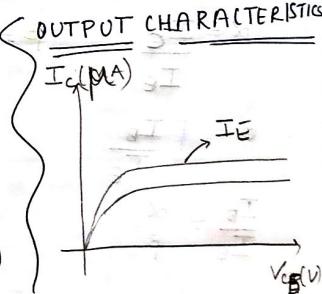
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TRANSISTOR PARAMETERS:

→ Current amplification factor in CB configuration:

$$\alpha_{dc} = \frac{\text{Output current}}{\text{Input current}} = \frac{I_C}{I_E} = \frac{\Delta I_C / I_0}{\Delta I_E / I_0} = \alpha_{ac}$$

$$[\alpha < 1] \quad \alpha = 0.95$$



Current amplification factor in CE configuration.

$$\beta_{dc} = \frac{I_c}{I_B}$$

$$\beta_{ac} = \frac{\Delta I_c}{\Delta I_B}$$

$\beta > 1$

$$\beta = \frac{- \times 10^{-3}}{- \times 10^{-6}} = - \times 10^3$$

0.95
0.05

→ Current amplification factor in CC configuration.

$$\gamma_{dc} = \frac{I_E}{I_B}$$

$$\gamma_{ac} = \frac{\Delta I_E}{\Delta I_B}$$

$\gamma > 1$

Relation between α , β & γ .

$$\alpha = \frac{I_E}{I_E + I_C} \quad \beta = \frac{I_C}{I_B} \quad \gamma = \frac{I_E}{I_B}$$

$$\alpha = \beta \frac{I_B}{I_E}$$

$$\frac{I_B}{I_E} = \frac{\alpha}{\beta}$$

$$I_E = I_B + I_C$$

$$\frac{I_C}{\alpha} = \frac{I_C}{\beta} + I_C$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\alpha = \frac{\beta}{\beta + 1}$$

$$\frac{1-\alpha}{\alpha} = \frac{1}{\beta}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

~~Defn:~~

$$\gamma = \beta + 1$$

$$\gamma = \frac{1}{1-\alpha}$$

$$I_C = 95\% I_E + I_{CBO}$$

$$I_C = \alpha I_E + I_{CBO}$$

→ CAPACITANCE IN DIODE:

There are 2 types of capacitance in diode. They are:

• Diffusion Capacitance (C_D)

• Transition Capacitance (C_T)

→ Diffusion Capacitance exists when diode is in FB.

→ Transition Capacitance exists when diode is in RB.

$$C = \frac{\epsilon_0 A}{d}$$

where ϵ_0 = permittivity

A = area

d = distance b/w 2 plates.

$$C_D > C_T$$

$$\therefore d_D < d_T$$

$$d_{fb} < d_{rb}$$

→ DIODE CURRENT EQUATION:

$$I = I_0 e^{\frac{(V - V_T)}{n k T}}$$

$n = 1 \rightarrow$ for Ge
 $n = 2 \rightarrow$ for Si

I_0 → Reverse Saturation Current

I → Forward current of the diode.

V → applied Voltage

V_T → Volt Equivalent of Temperature

$$V_T = \frac{T(K)}{11,600}$$

Reverse saturation current is in (μA) for Ge and and nA for Si.

$$I_o \rightarrow (\mu A) \rightarrow Ge$$

$$I_o \rightarrow (nA) \rightarrow Si$$

$$I_{o2} = I_{o1} \left[2^{\frac{\Delta T}{10}} \right]$$

$$\Delta T = (T_2 - T_1)^\circ C$$

The above expression says that the reverse saturation current doubles in every $10^\circ C$ rise in temperature.

B J T OPERATION

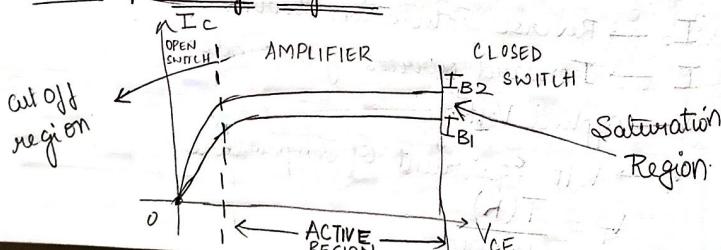
I/P	O/P	Operation
FB	RB	Amplifier
FB	FB	Closed-Switch
RB	RB	Open-Switch
RB	FB	Does not Operate

$$\text{Voltage gain} = \frac{\text{Output Voltage}}{\text{Input Voltage}}$$

$$\text{Power gain} = \frac{\text{Output Power}}{\text{Input Power}}$$

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* BJT operating region:



* If the voltage and current go beyond transistor rating; transistor is said to be in saturation region.

* In active region; output current is almost constant.
⇒ Transistor acts as amplifier in active region.

⇒ Cutoff region: Open switch

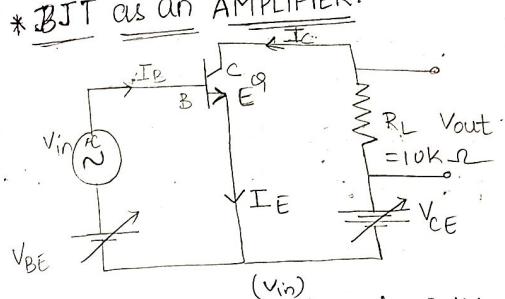
⇒ Active region: Amplifier

⇒ Saturation: Closed switch

→ Early effect / Base width modulation
→ BJT as an amplifier
→ CE Amplifier

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* BJT as an AMPLIFIER:



Vin → AC signal source

→ Signal to be amplified

→ VBE: DC power supply for biasing

→ RL: Load resistance across which amplified output signal is appearing

* Let input voltage increases by 0.1V

Let's assume that Ic increases by 0.5mA

Ib is negligible

$$I_c \approx I_e \Rightarrow I_c = 0.5 \text{ mA}$$

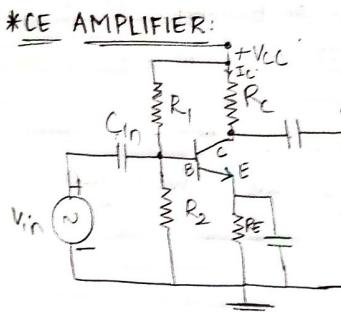
$$V_{out} = I_c \times R_L$$

$$R_L = 10k\Omega$$

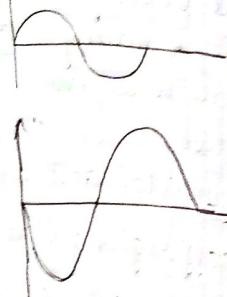
$$= 5V$$

$$\text{Gain} = \frac{V_{out}}{V_{in}} = \frac{5}{0.1} = 50$$

⇒ Transistor is amplifying the input signal by 50 times.



I/P



→ V_{in} is the input signal source. The signal to be amplified by the transistor is applied here.

→ V_{out} across the load.

→ Resistors R_1 and R_2 are used to forward bias the input circuit using common power supply V_{cc} . The method is called Voltage divider biasing.

→ Voltage divider biasing technique using R_1, R_2 is to forward bias the input circuit using the common power supply V_{cc} .

→ Collector resistor R_c is ~~selected~~ using collector resistor biasing technique to make output circuit ~~reverse~~ biased (V_{ce}) → using common power supply (V_{cc}).

INPUT CIRCUIT: FB: Voltage Divider Biasing (R_1, R_2)

OUTPUT CIRCUIT: RB: Collector Resistor biasing (R_c)

→ R_E is emitter resistor which is used to stabilize operating point at centre.

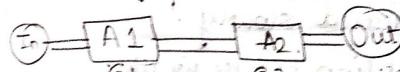
→ Without stabilizing the operating point:

output waveform is distorted.

* C_{in} (input capacitor) is used to couple the input signal V_{in} to base.

* C_{out} is used to couple output signal of transistor to the load in case of single stage amplifier.

In case of multi-stage amplifier C_{out} is used to couple the output of one stage to the input of next stage.



* CE is used to reduce harmonics and noise. Bypassed by C_E :

* Instead of using 2 power supplies at input (V_{BE}) and output (V_{CE}) we use single V_{cc} .

$$\text{From circuit: } V_{cc} = V_{out} + I_c R_c$$

V_{cc} & R_c → fixed

$$V_{out} = V_{cc} - I_c R_c \quad \text{--- (1)}$$

* $V_{in} \uparrow \text{ses}; I_c \uparrow \text{ses}; V_{out} \downarrow \text{ses}$

* $V_{in} \downarrow \text{ses}; I_c \downarrow \text{ses}; V_{out} \uparrow \text{ses}$.

→ As seen above:

Output is not in-phase with input.

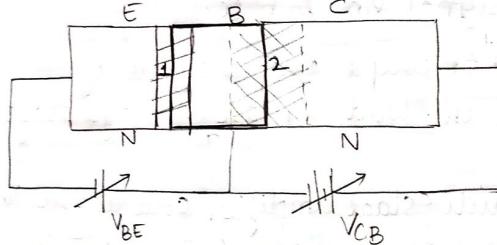
They are out of phase with each other.

* There is 180° phase-shift between output & input.

Hence in common emitter amplifier phase reversal occurs.

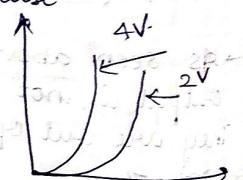
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EARLY EFFECT: [BAND WIDTH MODULATION]:

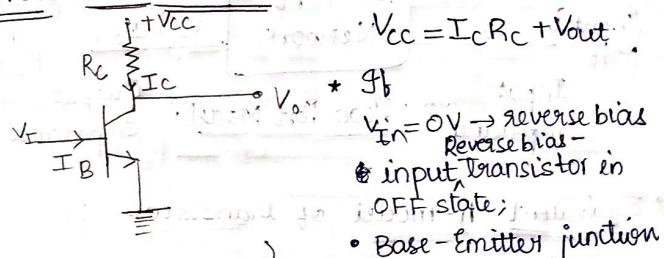


- V_{BE} is fixed at some depletion layer which is fixed.
- But V_{CB} is increased; with which depletion region - 2 is also increased slowly;
- which leads to the depletion of base width.
- due to which recombination of electrons and holes get reduced at the base and base current I_B is reduced.
- $I_E \approx I_C \Rightarrow$ Base width modulation.

→ Suppose at $V_{BE} = \infty$ and $V_{CB} = 2V$; diode is ON.
at $V_{CB} = 4V$; depletion region increases;
* Diode gets ON earlier than previous case.
The amount of input Voltage required to make the input circuit ON is less because.



* TRANSISTOR AS A SWITCH:



- $V_{in} = 0V \rightarrow$ reverse bias
- input transistor is OFF state;
- Base-Emitter junction

→ Transistor in OFF condition (diode is in OFF state) act as OPEN SWITCH.

→ No voltage drop.

$$V_{in} = 0; I_C = 0 \Rightarrow V_{cc} = V_{out}$$

$$V_{cc} = V_{out} = 1 \rightarrow \text{Inverter}$$

→ If $V_i = 1V$; transistor becomes ON; it starts conducting and it conducts I_C .

$$\Rightarrow V_{cc} - V_o = I_C R_C$$

⇒ Transistor is in ON state; act as closed switch and acts as a ~~resistor~~ wire; $\Rightarrow V_o = 0$

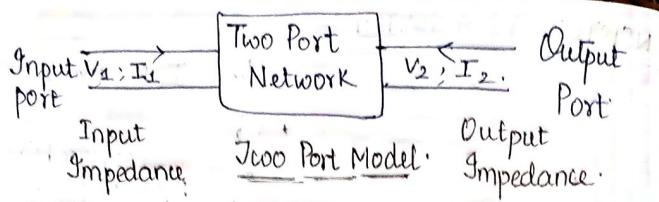
→ Voltage between 2 points is zero when there is no resistance \Rightarrow b/w points.

$$\Rightarrow V_o = I_C R_C$$

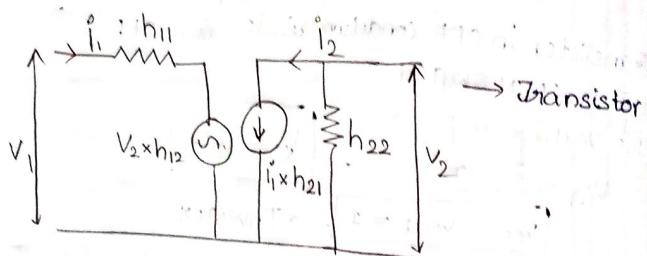
$$V_i = 1; V_o = 0 \rightarrow \text{Inverter}$$

* HYBRID PARAMETERS: [h-Parameters]

These parameters are mainly used in analysis of the BJT to use it as amplifier, ~~switch~~ switch etc. Given by h-parameters; z & y - parameters.



→ Equivalent h-model of transistor: (General)



h_{11} → Input Impedance (\underline{z})

h_{22} → Output Admittance ($\underline{\frac{1}{y}}$)

$$\text{Impedance} = \frac{1}{\text{admittance}}$$

• Transistor circuits consists of resistors and capacitors.

$$\cancel{\text{Applying KVL at I/P:}} \quad V_1 = i_1 h_{11} + V_2 h_{12} \quad \rightarrow ①$$

Applying KCL at O/P:

$$i_2 = i_1 h_{21} + V_2 h_{22} \quad \rightarrow ②$$

Let $i_1 = 0$; in ① & ②

I/Pckt is open. $V_1 = V_2 h_{12}$

$$h_{12} = \frac{V_1}{V_2}$$

$h_{12} \rightarrow$ reverse voltage transfer ratio

$$i_2 = V_2 h_{22}$$

$$h_{22} = \frac{i_2}{V_2}$$

$h_{22} \rightarrow$ output admittance

Let $V_2 = 0$ in ① & ② in output port. Ckt is closed. short circuited

$$V_1 = i_1 h_{11} \Rightarrow h_{11} = \frac{V_1}{i_1}$$

$h_{11} \rightarrow$ input impedance

$$i_2 = i_1 h_{21}$$

Output short circuited

$$h_{21} = \frac{i_2}{i_1}$$

Open circuit:

$$i = 0$$

$$V = \infty$$

Closed circuit:

$$i = \infty$$

$$V = 0$$

forward

$h_{21} \rightarrow$ reverse current transfer ratio

03/02/2022

→ When 2 points are shorted $i = \infty$; $V = 0$.

∴ There is a wire in b/w 2 points.

→ There are 4 parameters associated with this model.

input impedance

output admittance/conductance.

current gain

$$h_{11} - \Omega$$

$$h_{22} - \text{mhos.}$$

$$h_{12}, h_{21} \rightarrow \text{dimension less}$$

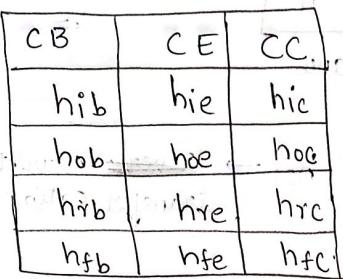
∴ Their units are completely different from each other; this set of parameters is called as hybrid parameters.

Forward current gain $= h_{21} = V_1/V_2$

Reverse voltage transfer $= h_{12} = i_2/i_1$

* IEEE Notations for h-model of BJT:

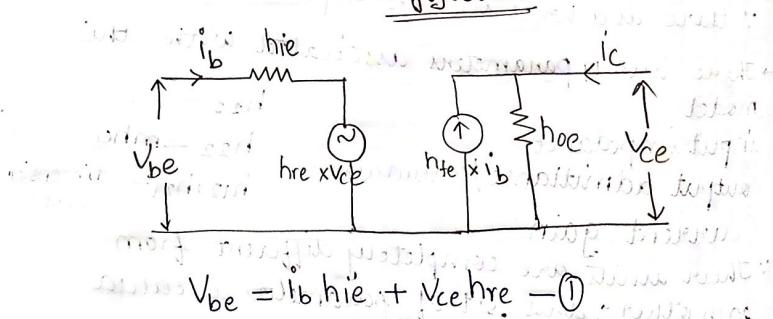
- $11 \rightarrow i$ (input) $h_{11} \rightarrow h_i$
 $22 \rightarrow o$ (output) $h_{22} \rightarrow h_o$
 $12 \rightarrow r$ (reverse) $h_{12} \rightarrow h_r$
 $21 \rightarrow f$ (forward) $h_{21} \rightarrow h_f$

* 

CB	CE	CC
h_{ib}	h_{ie}	h_{ic}
h_{ob}	h_{oe}	h_{oc}
h_{rb}	h_{re}	h_{rc}
h_{fb}	h_{fe}	h_{fc}

Representation of hybrid parameters in different configurations of BJT:

* h-model Equivalent circuit of BJT (CE) configuration:



$$V_{be} = i_b h_{ie} + V_{ce} h_{re} \quad \text{---(1)}$$

$$i_c = i_b h_{fe} + V_{ce} h_{oe} \quad \text{---(2)}$$

$$\text{in (1)} \quad V_{ce} = 0$$

$$h_{ie} = \frac{V_{be}}{i_b}$$

Output short circuited

$$\text{in (1)} \quad i_b = 0$$

$$h_{re} = \frac{V_{be}}{V_{ce}}$$

Input open circuit

$$\text{in (2)} \quad V_{ce} = 0$$

$$h_{fe} = \frac{i_c}{i_b}$$

Output short circuited

$$\text{in (2)} \quad i_b = 0$$

$$h_{oe} = \frac{i_c}{V_{ce}}$$

Input open circuit

* Hybrid model remains same for PNP and NPN.

FIELD EFFECT TRANSISTOR

04/02/22

→ Field Effect transistor is also used as amplifier and logic switches; impedance matching circuits.

* TYPES OF FET:

- 1) MOSFET (metal - oxide - semiconductor FET)
- 2) Depletion Mode (MOSFET)
- 3) JFET (Junction Field Effect Transistor)

MOSFET:

- Depletion mode MOSFET
- Enhancement type MOSFET

JFET:

- P-channel
- N-channel.

• BJT is a current controlled device.

• FET is a voltage controlled device.

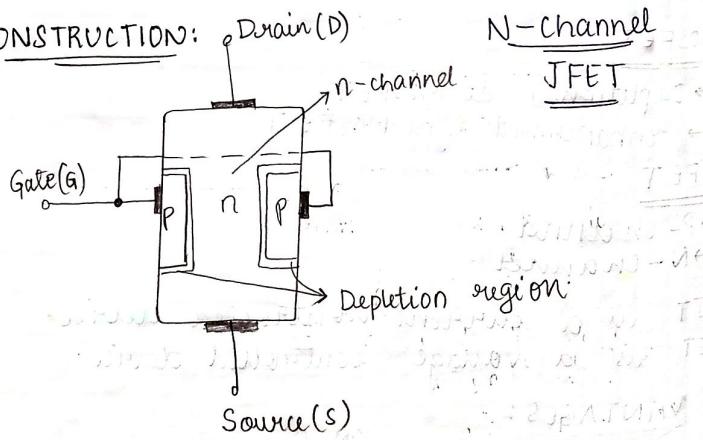
ADVANTAGES:

- 1) FET has input impedance compared to BJT (MOSFET). Input circuit

ADVANTAGES:

- 1) FET has high ^{input} impedance ($M\Omega$) compared to BJT. FET has ^{input circuit in forward} biased condition and BJT has input circuit forward biased condition.
- 2) FET has better temperature stability compared to BJT.
- 3) FET is smaller than BJT.
- 4) Because it is small; it is easy to fabricate in chip.
- 5) BJT is bipolar device; both holes & e⁻s involve in current conduction whereas FET is unipolar i.e. only one type of charge carriers used.
- 6) FET ~~has less noise~~ has less noise i.e. disturbance.

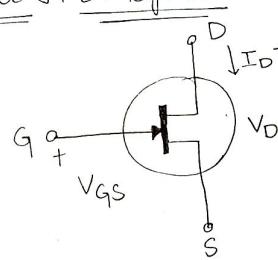
CONSTRUCTION:



→ Figure shows ~~an~~ N-channel JFET.

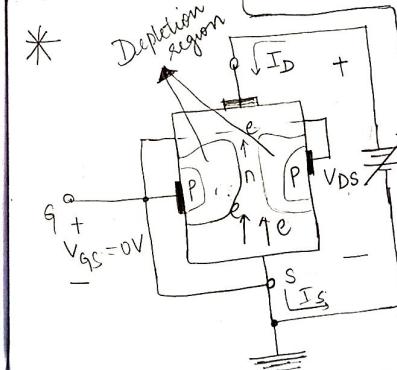
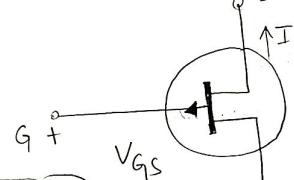
- It consists of n-type silicon channel; p-type material is fused as shown in figure.
- Both p-type materials are interconnected (internally).
- Gate is connected to p-type; Source and drain are connected to N-type.

* N-channel JFET symbol:



* Gate is the knob to control

* P-channel JFET symbol:



channel becomes narrower as V_{DS} is increased.

- N is moderately doped.
- P is heavily doped.

$\rightarrow g_b V_{GS} = +ve$; P type is FB; depletion region decreases. (both)

$\rightarrow g_b V_{GS} = -ve$; P type is RB; depletion region increases.

* Voltage at which depletion regions of both p-types touch each other is called Pinch off voltage.

At this voltage: FET is pinched off.

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* +ve terminal of V_{DD} injects holes into drain and then to n-channel. As P is heavily doped more no. of holes are available in P the holes coming from V_{DD} and holes in P repel each other. Thus depletion region towards drain side.

* Whereas e⁻s being pushed into device through source terminal from V_{DD} tend to recombine with holes in P. Thus depletion layer is less at source side. Hence depletion region is not circular instead it is wedge shaped.

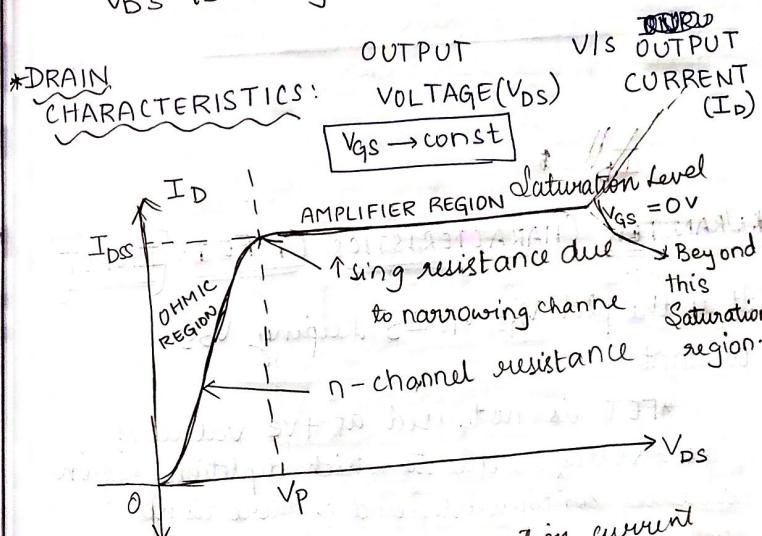
* When the voltage reaches pinch off voltage; even then if we ↑ Se voltage; current abruptly increases; depletion region further ↑s. \Rightarrow device reached saturation stage.

$\rightarrow V_{GS} = 0$ & V_{DS} is ↑ed from 0 to more +ve

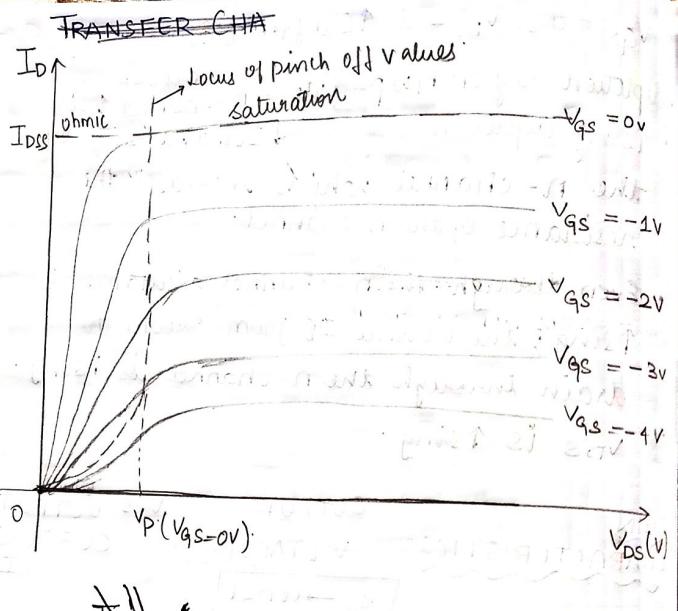
depletion region b/w p-gate & n-channel increases.

• ↑ing depletion region; ↓es the size of the n-channel which increases the resistance of the n-channel.

• Even though the n-channel resistance is ↑ing; the current I_D from source to drain through the n-channel is ↑ing. V_{DS} is ↑ing.



I_{DSs} = Drain to source saturation current
 At ohmic region: JFET acts as resistor.
 At amplifier region: JFET operates as a const (Pinchoff region). current device (or) amplifier



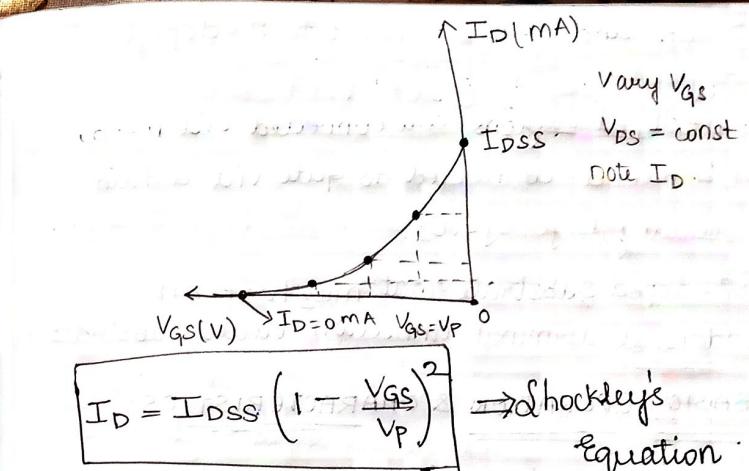
* TRANSFER CHARACTERISTICS OF FET: INPUT

It is the plot V_{GS} v/s I_D keeping V_{DS} constant.

*FET is not used at +ve values of gate voltages; due to which depletion region increases continuously and \therefore there is no control over current.

* $V_{GS} = -V_e$; we use this case.

\therefore The transfer characteristic graph is in IInd quadrant.



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* Input circuit is always reverse biased.

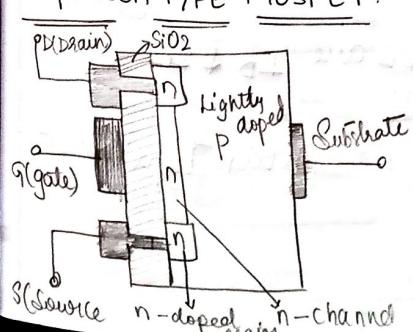
Gate is connected in P-TYPE.

* Depletion layers are far; channel width is more ~~reduces~~, drain current ~~increases~~.

* When V_{GS} reduces; depletion layer ~~increases~~; width decreases; current decreases.

* MOSFET:

Depletion Type MOSFET:



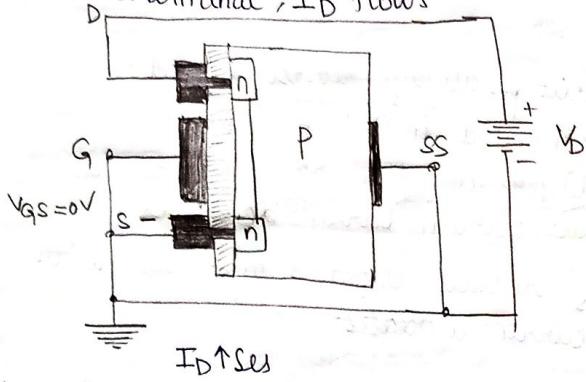
In any amplifier circuit it is desired to have input impedance very high.

→ MOSFET is also called insulated Gate FET.

- Drain and source connect to n-doped regions.
- n-doped regions are connected via n-channel.
- n-channel connected to gate via a thin insulating layer of SiO_2 .
- P-doped substrate that may have an additional terminal connection called substrate.

* BASIC OPERATION & CHARACTERISTICS:

$V_{GS} = 0$; V_{DS} is applied across drain to source terminal; I_D flows.

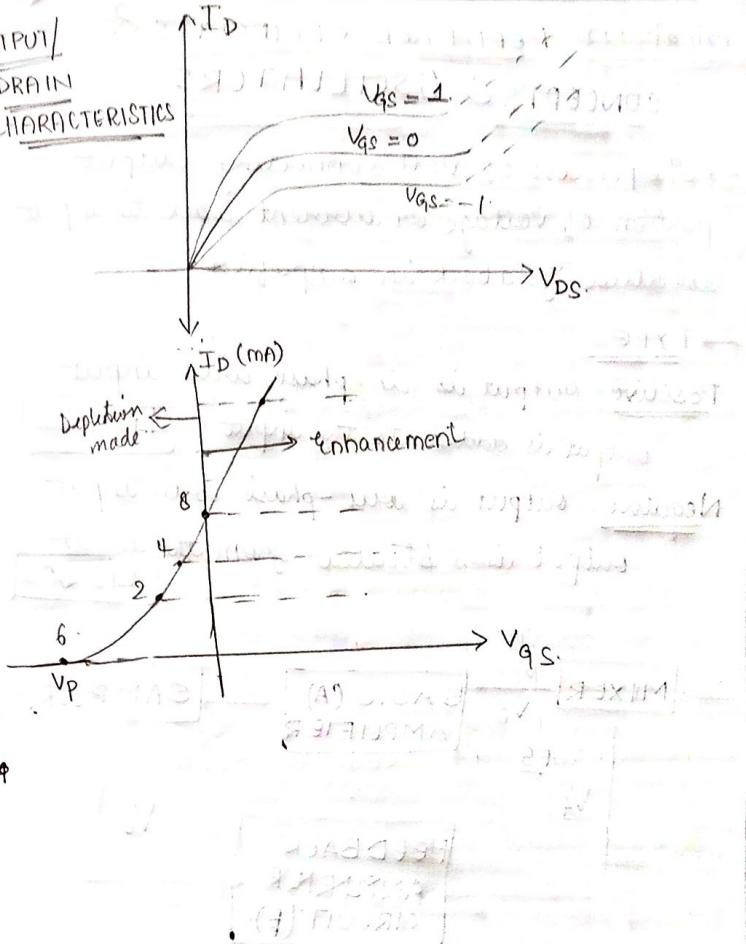


$V_{GS} = +\text{ve}$; MOSFET operates as enhancement type MOSFET.

$V_{GS} = -\text{ve}$; charge carriers are depleted off.

: Depletion Type MOSFET

OUTPUT / DRAIN CHARACTERISTICS



Depletion mode → Enhancement mode



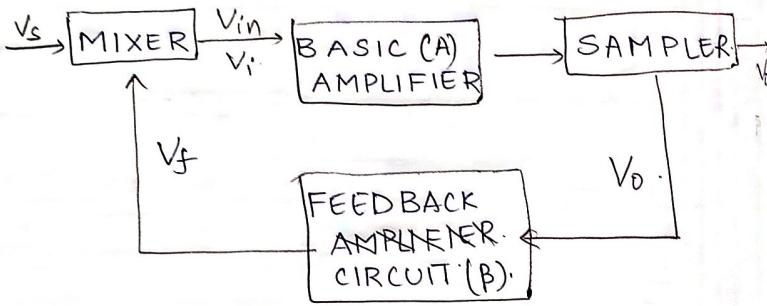
12/02/2022 FEEDBACK CIRCUITS & CONCEPTS & OSCILLATORS

→ The process of ~~not~~ connecting output portion of voltage or current back to input is called feedback in amplifier.

→ TYPES:

Positive: Output is in-phase with input.
output is added to the input. [IN ↑ses]

Negative: output is out-phase with input.
output is subtracted from the input [IN ↓ses]



A → Gain of amplifier without feedback.

A_f → Gain of amplifier with feedback.

$$A = \frac{V_o}{V_i}$$

$$A_f = \frac{V_o}{V_s}$$

Feedback factor $\beta = \frac{V_f}{V_o}$

$$V_i = V_s \pm V_f$$

$$V_f = +ve/-ve$$

$$A_f = \frac{V_o}{V_s} = \frac{V_o}{V_i \pm V_f} \quad \text{--- (1)}$$

Divide Nr & Dr by V_o

$$A_f = \frac{\frac{V_o}{V_o}}{\frac{V_i}{V_o} \pm \frac{V_f}{V_o}} = \frac{1}{\frac{1}{A} \pm \beta}$$

Relation b/w A & A_f :

$$A_f = \frac{A}{1 \pm AB} \quad \text{--- (2)}$$

From eq: 2 it can be seen that gain of an amplifier with feedback is related to that of without feedback depending on whether feedback is +ve (or) -ve.

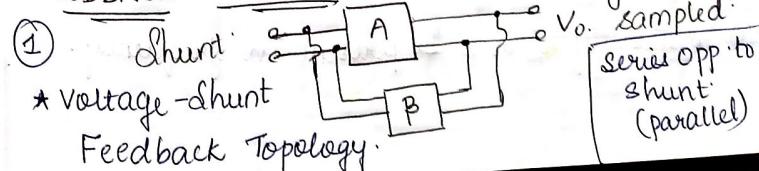
$$\bullet A_f(+ve) = \frac{A}{1-AB} \quad \bullet A_f(-ve) = \frac{A}{1+AB}$$

* Gain ↑ses with +ve feedback.

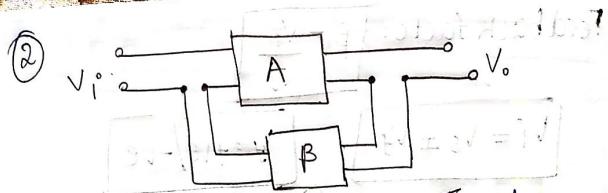
* Gain ↓ses with -ve feedback.

→ Even though gain reduces with -ve feedback practically -ve feedback is used; because it provides many advantages at the cost of gain.

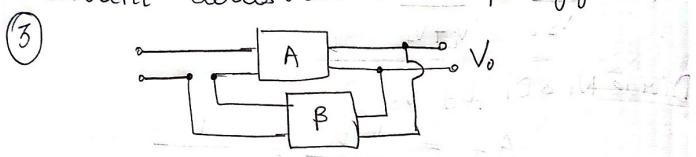
* FEEDBACK TOPOLOGIES:



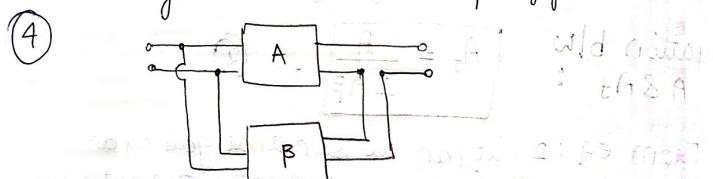
Voltage is sampled.
Series opp to shunt (parallel)



Current - Series feedback Topology.



Voltage Series feedback Topology.



Current Shunt feedback Topology.

*ADVANTAGES OF NEGATIVE FEEDBACK:

1) Gain Stabilisation:

- Gain should be stable so that a clear signal is obtained at reception.
- The frequency components given to an amplifier should be amplified to a constant value.
- No instability should be present in frequency.

* Why does gain vary?

Reasons:

- Aging of circuit components / devices.
- Replacement of components.
- Variation in instability is also due to temperature.

Gain of amplifier with negative feedback.

$$\text{Actual } Af = \frac{A}{1+AB} \quad \text{---(1)}$$

Diff wrt A

$$\frac{dAf}{dA} = \frac{1+AB - AB}{(1+AB)^2} = \frac{1}{(1+AB)^2}$$

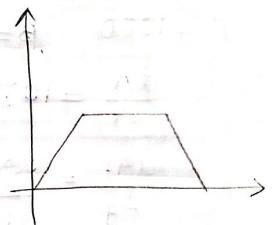
$$\text{ratio of } \frac{dAf}{dA} = \frac{1}{1+AB} \cdot \frac{Af}{A}$$

$$\frac{dAf}{Af} = \frac{1}{A(1+AB)} \cdot dA$$

$$\boxed{\frac{dAf}{Af} = \frac{dA/A}{1+AB}} \quad \text{---(2)}$$

* From eq: 2; It can be observed that change in gain of an amplifier is more than change in gain of with -ve feedback by $(1+AB)$ times.

Q: An amplifier has an open-loop gain (means output is not connected back without feedback) of 1000 and feedback ratio is 0.04. If open loop gain changes by 10%, find the % change in gain of an amplifier with feedback.



Q1: $A = 1000$ $B = 0.04$

$$\frac{dA}{A} = 10\%$$

$$\frac{dA_f}{A_f} = \frac{dA/A}{1+AB}$$

$$= \frac{10}{1+40} = \frac{10}{41} = 0.243\%$$

Change in gain is reduced by 41 times.

* Gain is stabilized by 41 times.

Q2: An amplifier has voltage gain with feedback of 100. If gain without feedback changes by 20%, & gain with feedback should not vary by more than 2%. Determine the value of open loop gain.

$$A_f = 100$$

$$A = ?$$

$$\frac{dA_f}{A_f} = \frac{dA/A}{1+AB}$$

$$\frac{dA_f}{A_f} = \frac{20}{100} = \frac{1}{5}$$

$$\frac{dA_f}{A_f} = \frac{2}{100}$$

$$\frac{2}{100} = \frac{1}{5} \Rightarrow A = ?$$

$$1 + AB = 10$$

$$\beta = ?$$

$$\beta = \frac{9}{1000}$$

$$\beta = 0.009$$

$$A_f = A$$

$$1 + AB$$

$$A = 100 \times 10$$

$$A = 1000$$

Open Loop

→ No feed back

2) Increase in Bandwidth:

Frequency Response of an amplifier with & without -ve feedback

→ Bandwidth is range of frequencies over which gain remains is called bandwidth and it is always measured at -3dB level.

gain in without feedback

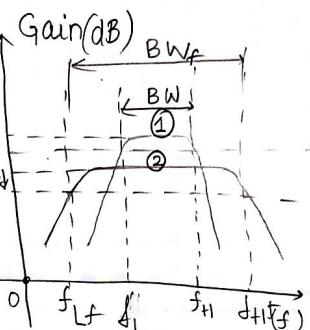
$$dB = \log \frac{V_o}{V_i}$$

$$dB = \log A$$

$$f_{lf} = \frac{f_L}{1+AB}$$

$$f_{hf} = f_H(1+AB)$$

$$BW_f = \frac{BW}{1+AB}$$



f_H = higher cutoff frequency

f_L = lower cutoff frequency

f_{lf} = lower cutoff frequency with feed back

f_{hf} = Higher cutoff frequency with feed back

$$B \cdot W =$$

⇒ The product of gain & BW of an amplifier with f_B = that of without f_B .