it-5:- Designing of combinational

logic devices

PLD (Programmable logic devices)

↳ ROM (Read Only Memory)

↳ PLA (Programmable logic Array)

↳ PAL (Programmable Array logic)

Memory :- RAM - volatile

ROM - Read

1 Byte = 8 bits

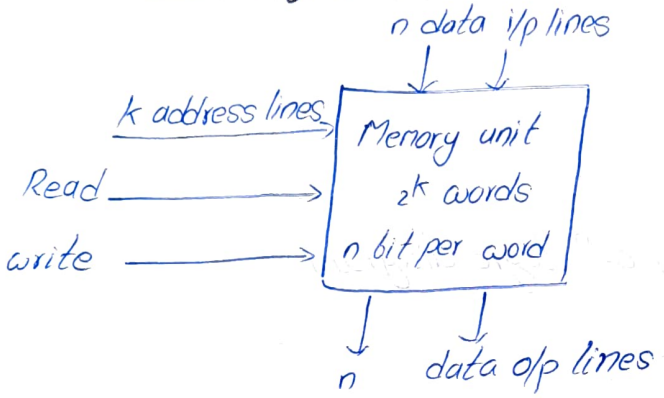
1 KB = 1024 bits = 2^{10}

1 MB = 2^{20}

1 GB = 2^{30}

1 word = 2 Bytes

Block diagram of memory unit

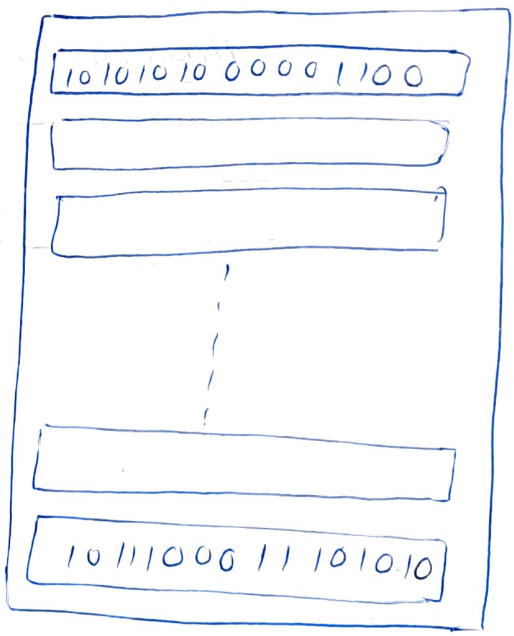


1024 x 16 memory —— address lines - 10

memory address

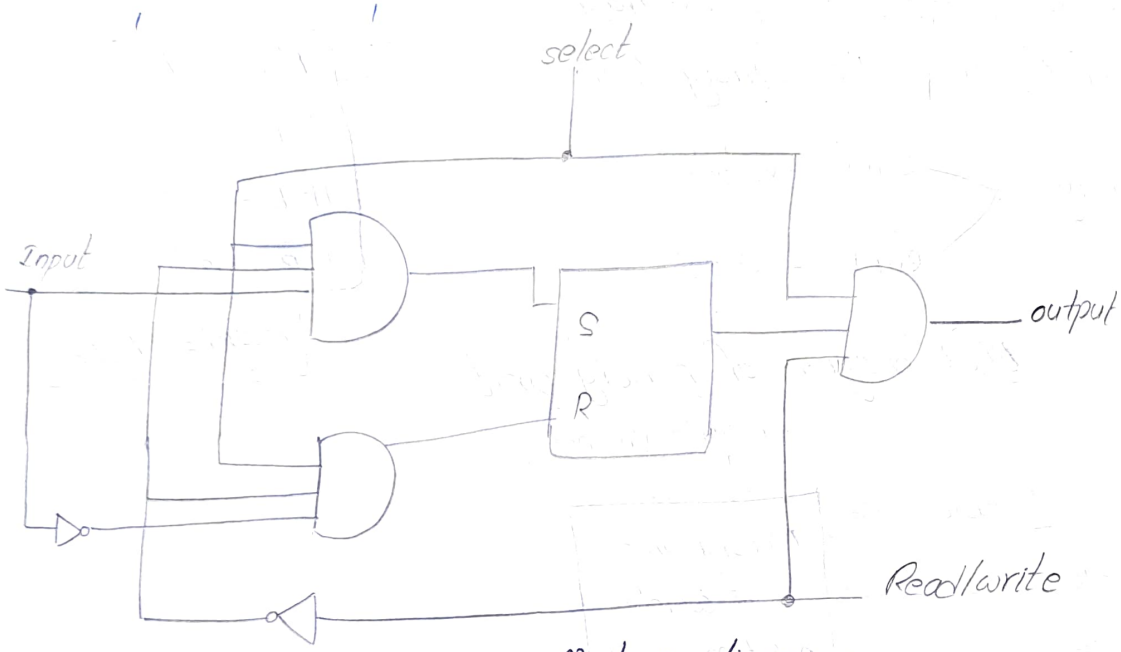
binary	decimal
0000000000	0
0000000001	1
0000000010	2
⋮	⋮
1111111110	1022
1111111111	1023

Memory content

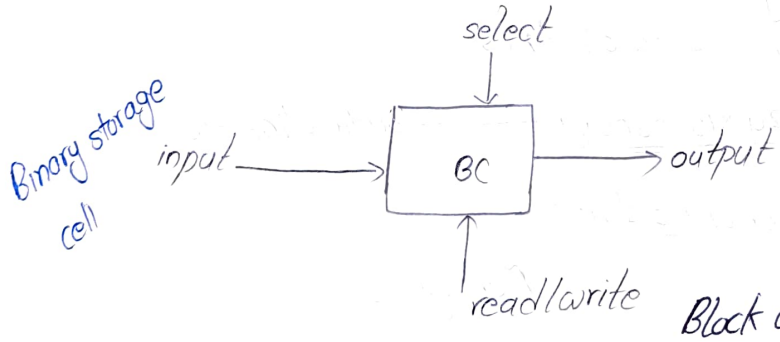


control i/p's to memory chip

memory enable	read/write	memory operation
0	x	None
1	0	write
1	1	read

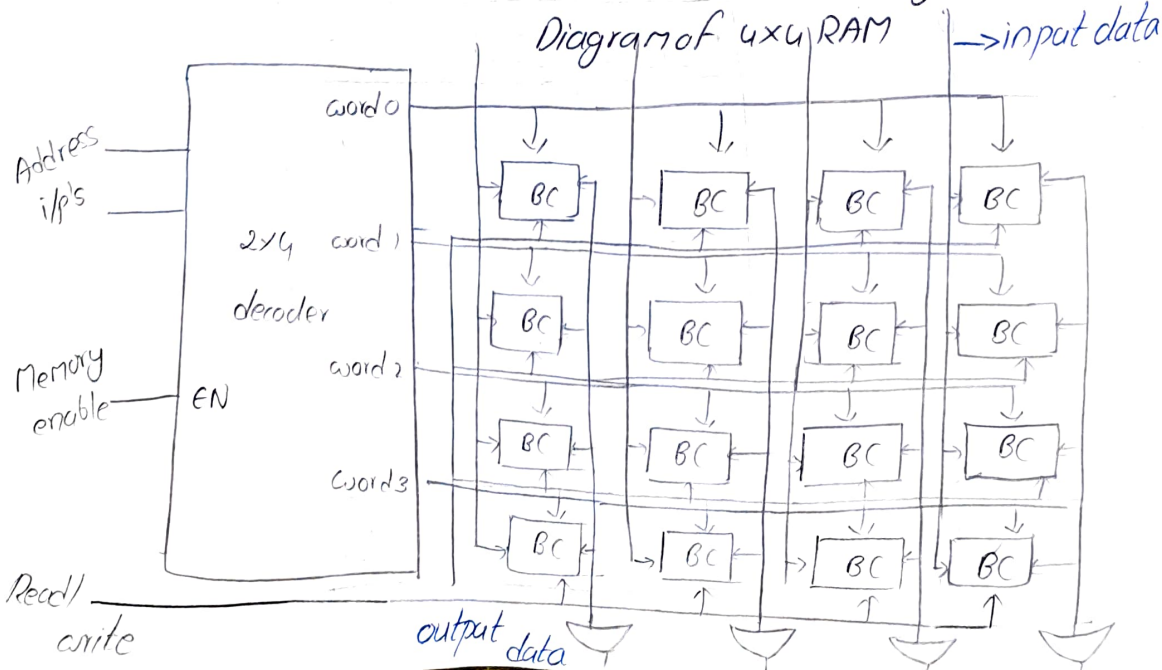


Memory cell logic diagram

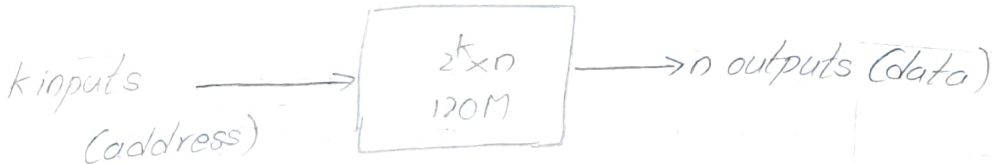


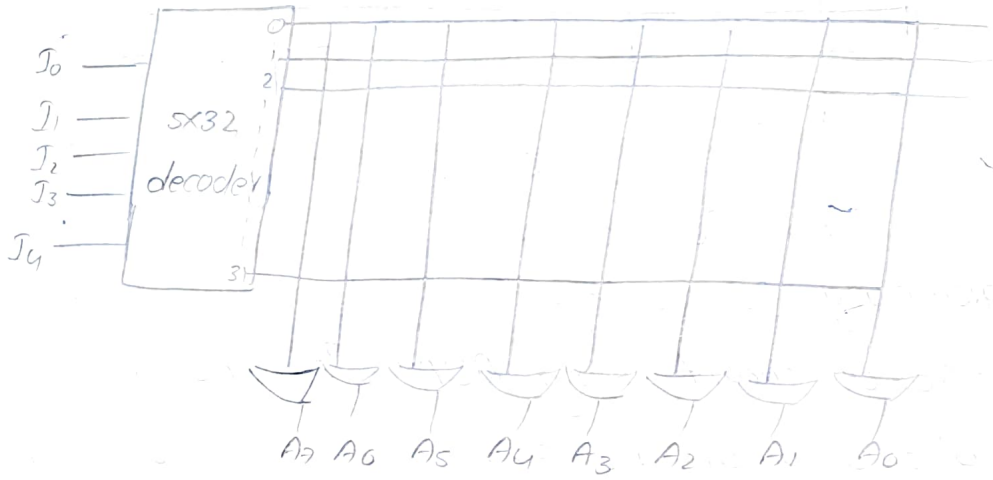
Block diagram

Diagram of 4x4 RAM



ROM block diagram

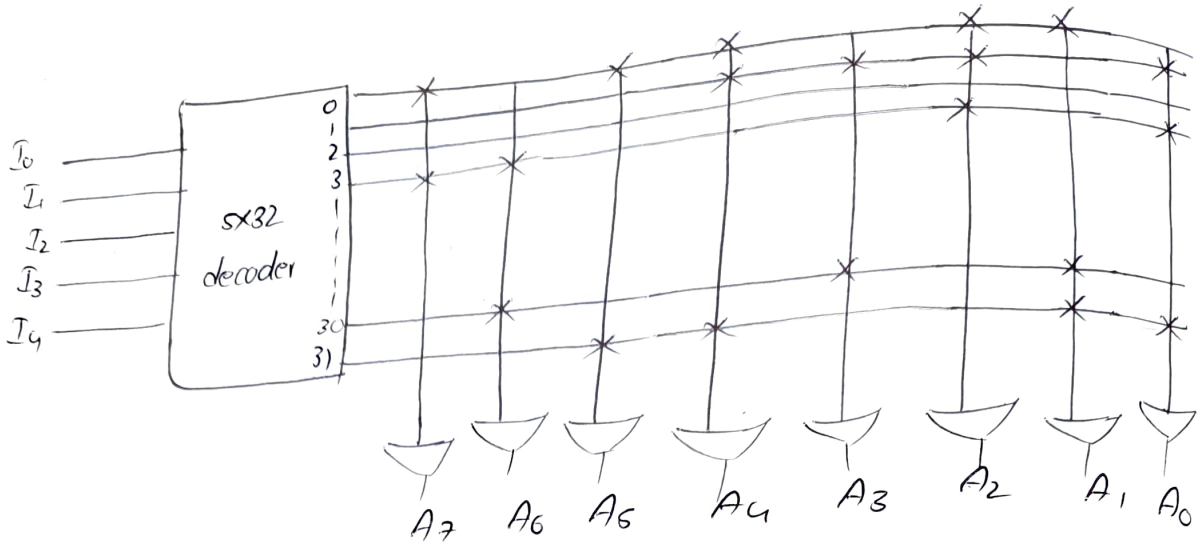




Internal logic diag of 32x8 ROM

ROM Truthtable

Inputs					Output							
I_4	I_3	I_2	I_1	I_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	1	0	1	1	1	0	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1



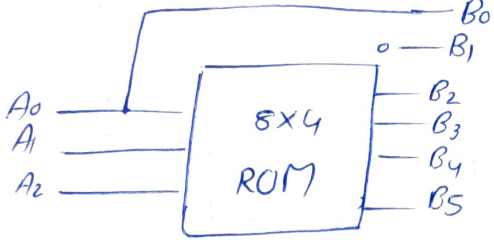
programming ROM using T-T

Q) Design a combinational circuit using ROM. The circuit accepts 3 bit number and o/p's a binary no equal to square of i/p n

Sol:-

Truth table for given problem

Inputs			outputs						Decimal
A_2	A_1	A_0	B_5	B_4	B_3	B_2	B_1	B_0	
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49



Block diagram

ROM Truth table

Inputs			outputs			
A_2	A_1	A_0	B_5	B_4	B_3	B_2
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	1	0
1	1	0	1	0	0	1
1	1	1	1	1	0	0

Types of ROM (2M): ***

ROM

PROM - Programmable ROM

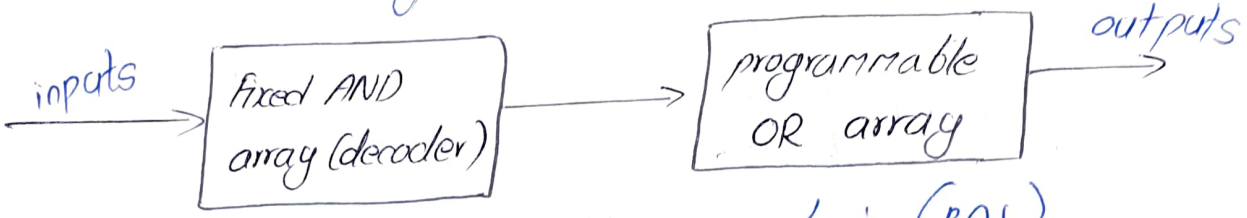
EPROM - Erasable programmble ROM

EEPROM - Electrical " " ROM

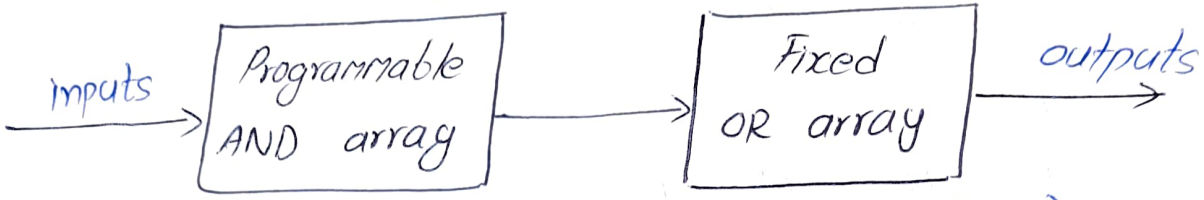
Flash memory

Flash memory devices are similar to EEPROM but have additional built in circuitory to selectively program, and erase the device in circuit without need of a special program.

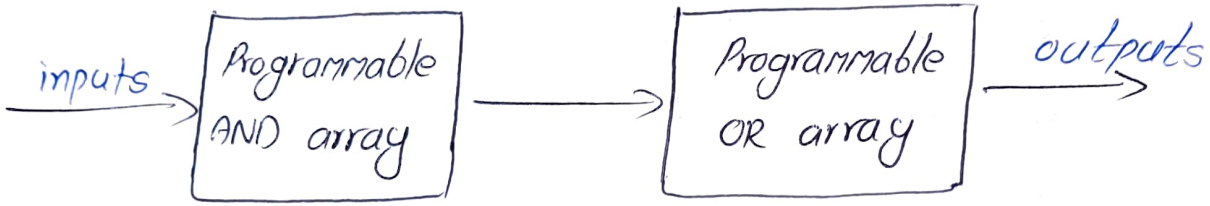
a) Programmable Read-Only-Memory (PROM)



b) Programmable array logic (PAL)



c) Programmable logic array (PLA)



Q) Design a PLA which implements the boolean functions

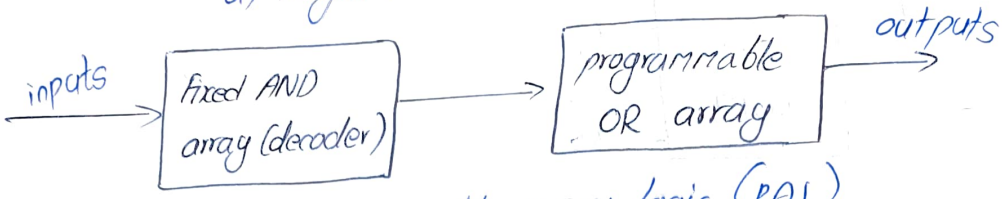
$$F_1 = AB' + AC + A'BC'$$

$$F_2 = (AC + BC)'$$

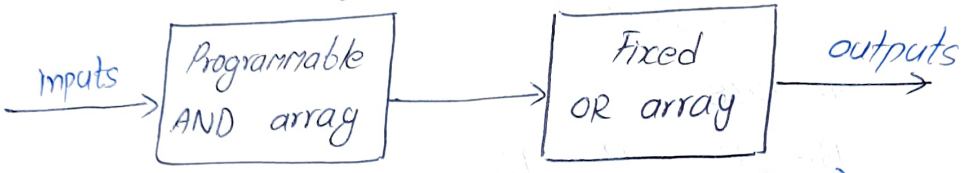
$A \oplus 0 = A$

$A \oplus 1 = A'$

a) Programmable Read-Only-Memory (PROM)



b) Programmable array logic (PAL)



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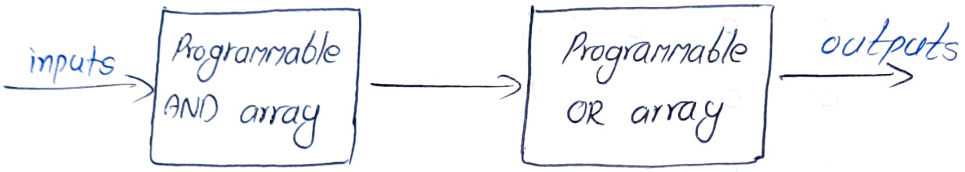

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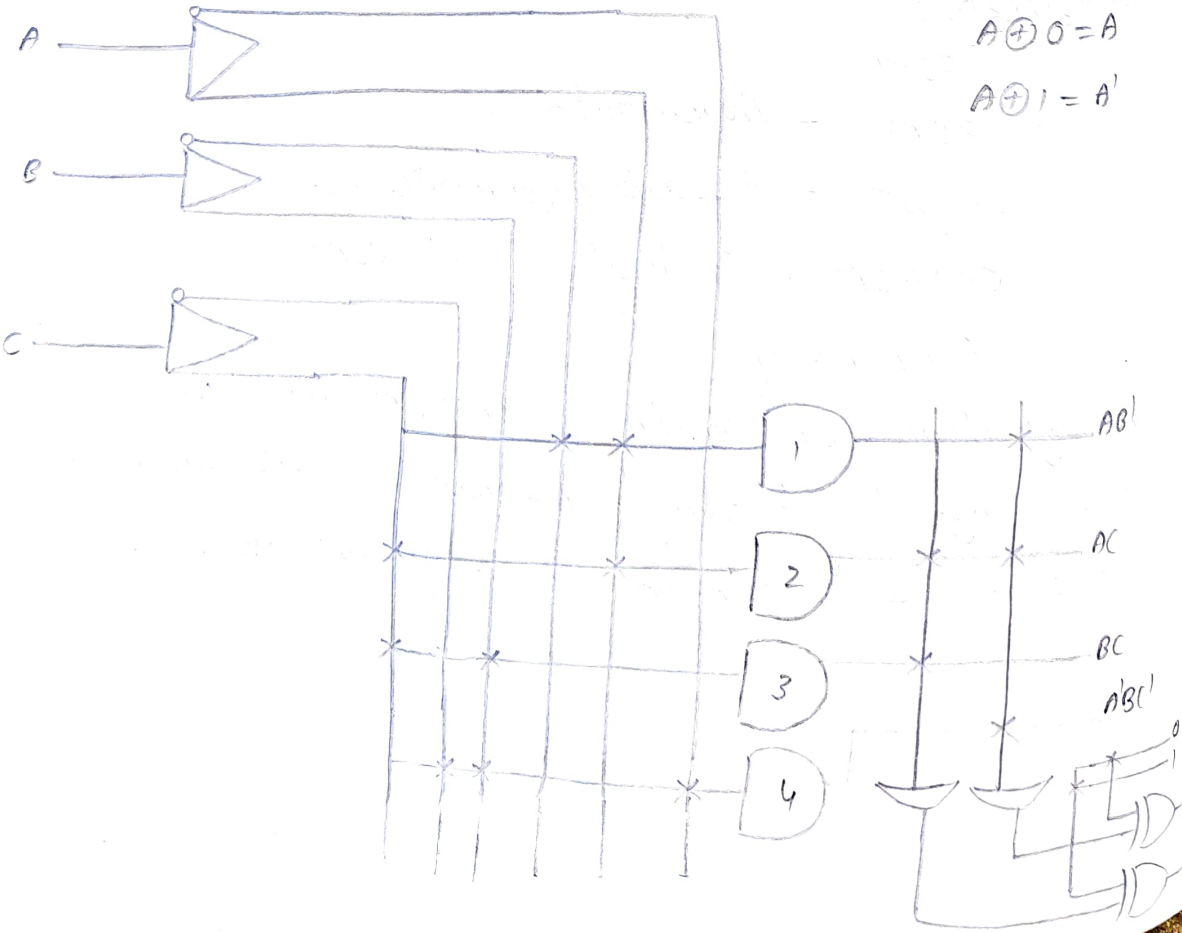
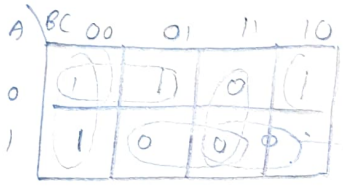


Product term		Inputs A	B	C	Outputs (T) F_1	(C) F_2
AB'	1	1	0	–	1	–
AC	2	1	–	1	1	1
BC	3	–	1	1	–	1
$A'BC'$	4	0	1	0	1	–

Q) Implement the following two boolean functions with PLA

$$F_1(A,B,C) = \Sigma(0,1,2,4)$$

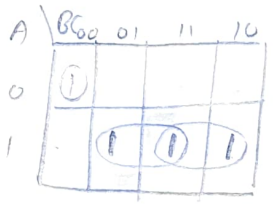
$$F_2(A,B,C) = \Sigma(0,5,6,7)$$



$F_1 = \bar{B}\bar{C} + \bar{A}\bar{B} + \bar{A}\bar{C}$

$F_1' = AB + AC + BC$

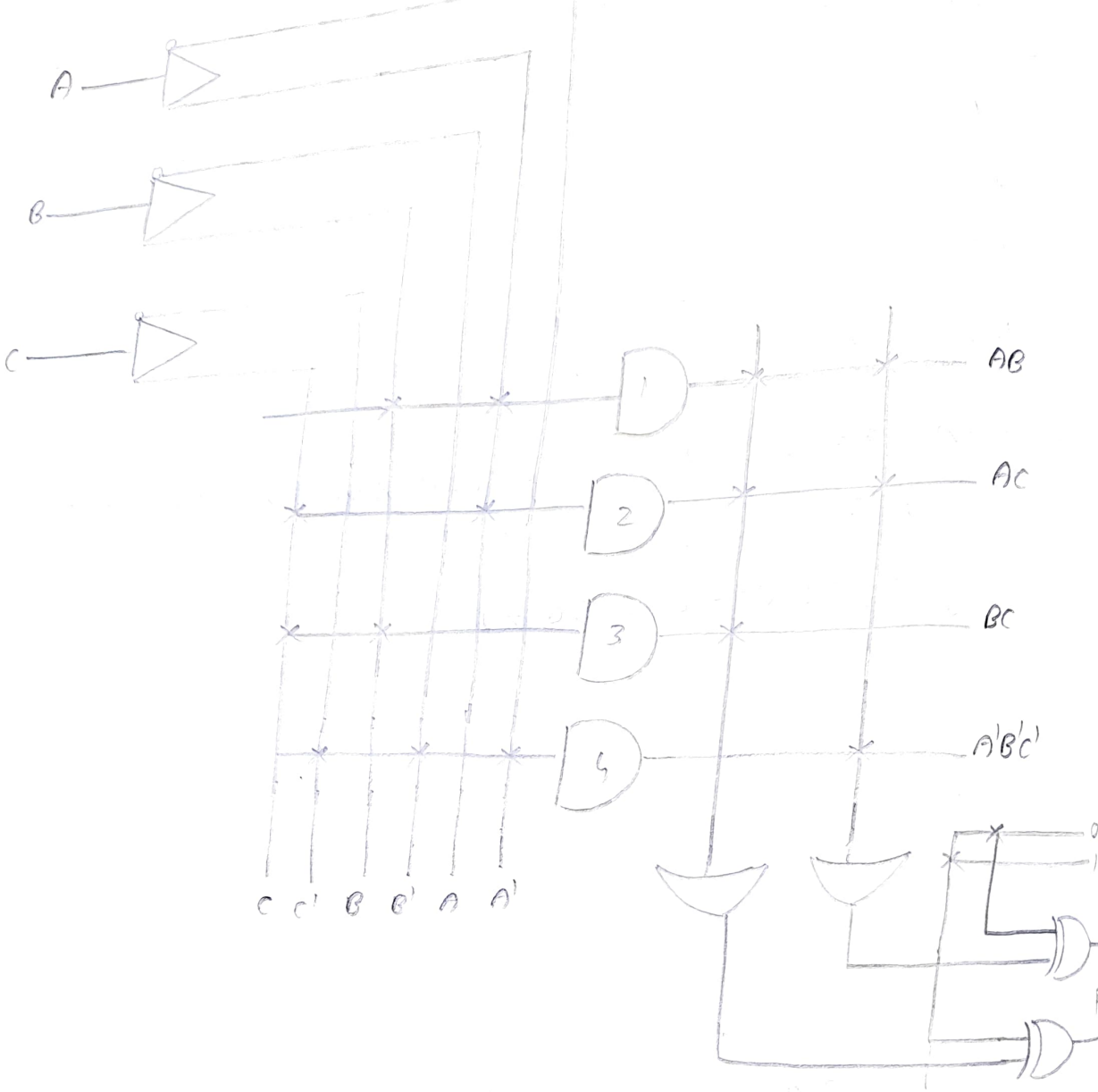
$F_1 = (AB + AC + BC)'$



$F_2 = AC + AB + \bar{A}\bar{B}\bar{C}$

PLA programming table

Product term		Inputs A	B	C	Outputs (C) F_1	(T) F_2
AB		1	1	–	1	1
AC		1	–	1	1	1
BC		–	1	1	1	–
$A'B'C'$		0	0	0	–	1



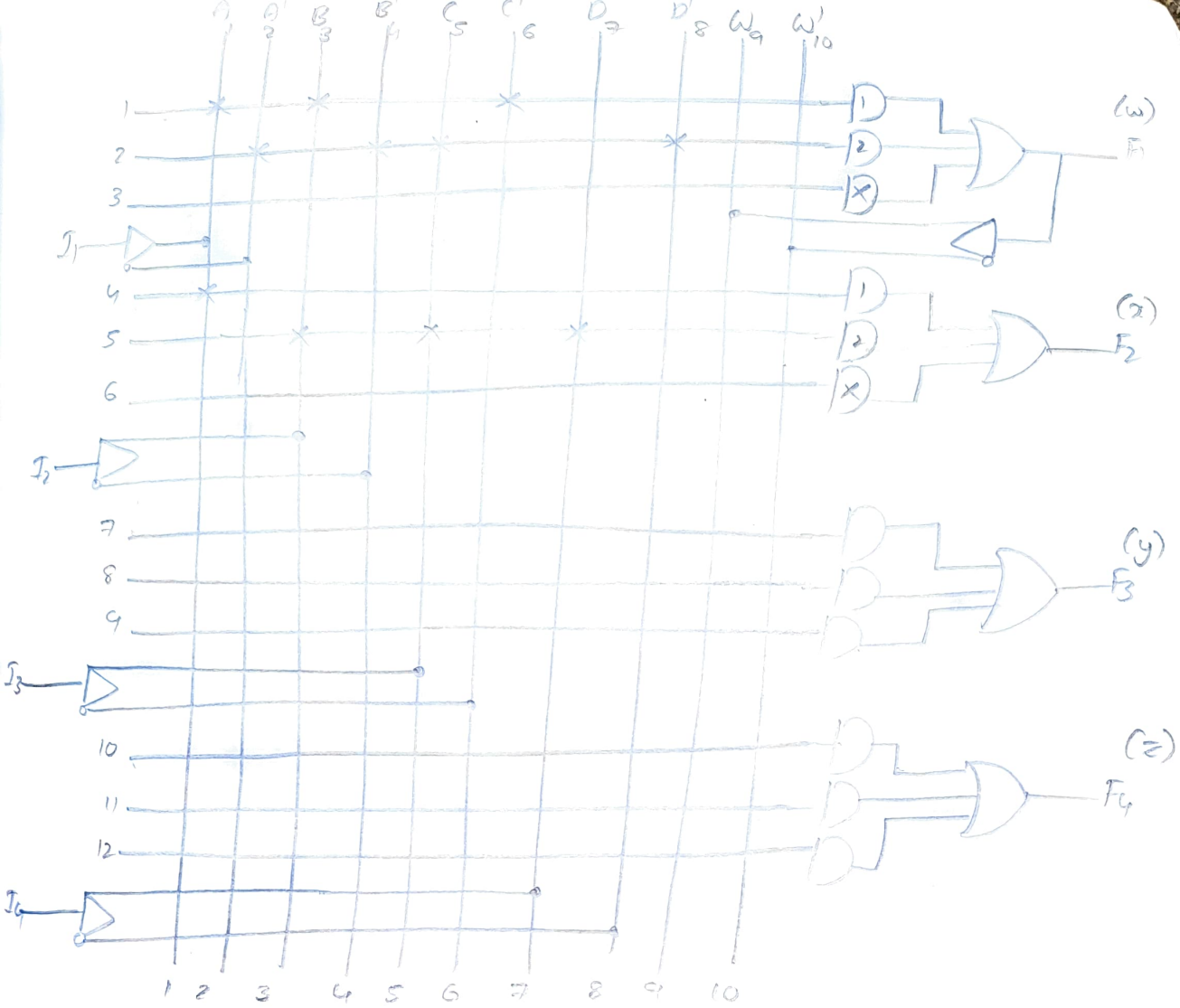
Q) Consider the following boolean functions given in sum of min terms form and design c-c using PAL.

$$w(A,B,C,D) = \Sigma(2,12,13)$$

$$x(A,B,C,D) = \Sigma(7,8,9,10,11,12,13,14,15)$$

$$y(A,B,C,D) = \Sigma(0,2,3,4,5,6,7,8,10,11,15)$$

$$z(A,B,C,D) =$$


A1
A2
B3
B4
C5
C6
D7
D8
W9
W'10
1
2
3
I1
4
5
6
I2
7
8
9
I3
10
11
12
I4
1 2 3 4 5 6 7 8 9 10
(w)
F1
(x)
F2
(y)
F3
(z)
F4