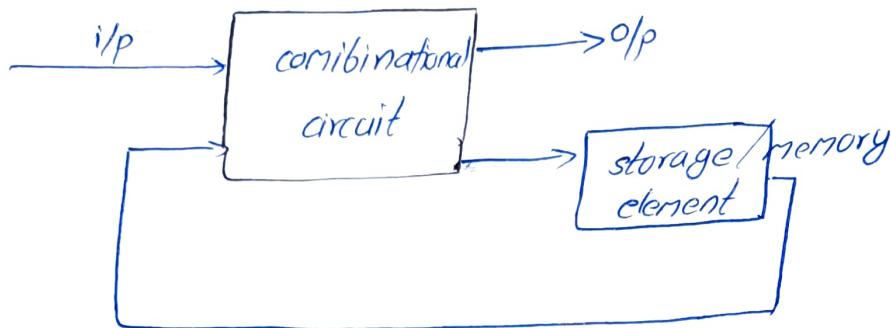


4. Synchronous Sequential logic

Sequential circuits

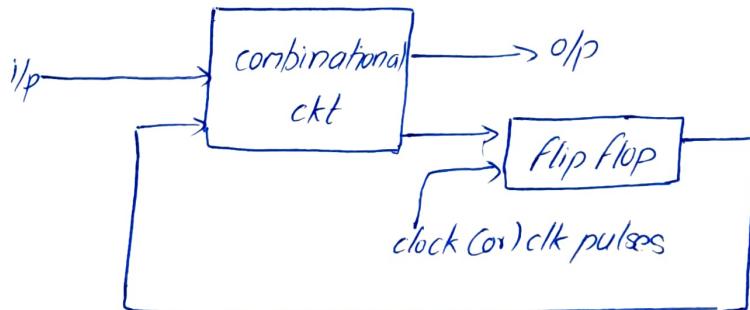


Note:- Block diagram of sequential circuit

The sequential circuit receives binary information from external i/p's that together with the present stage of the storage elements determine the binary value of the o/p.

*A sequential circuit is specified by a time sequence of i/p's, o/p's and internal states.

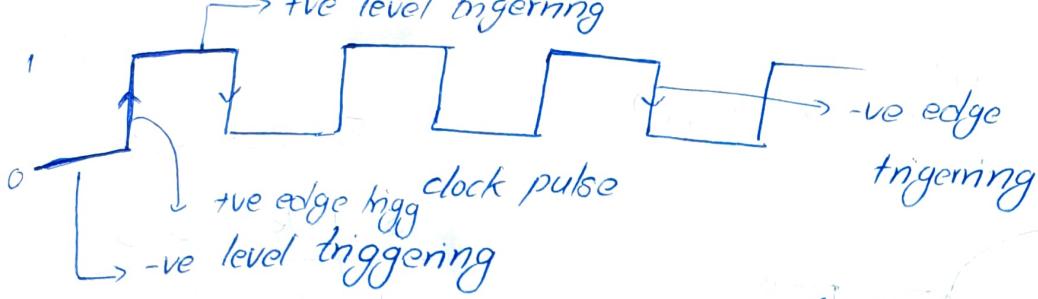
sequential cktls <--> Asynchronous S.C
 <--> Synchronous S.C



Block diag of synchronous sequential ckt

memory element

- └── Latch (Used in asynchronous)
- └── Flip Flop (going to change its content at particular time based on clock pulse)



A sequential ckt may be having a feedback among the logic gates which may become unstable at times. A synchronous seq ckt is a system whose behaviour can be defined from the knowledge of its signals at discrete instances of time (A synchronous seq ckt employs signals that affect the storage element at only discrete instances of time). Synchronisation is achieved by a timing - device called a clock generator, which provides a clock signal having the form of periodic train of clock pulses. Synchronous seq ckts that use clock pulses to control storage element are called clocked seq ckts. The storage elements used in clocked seq ckts are called flipflops. A flipflop is a binary storage device capable of storing 1 bit of information. The new value is stored (flipflop is updated) when the pulse of clock signal occurs.

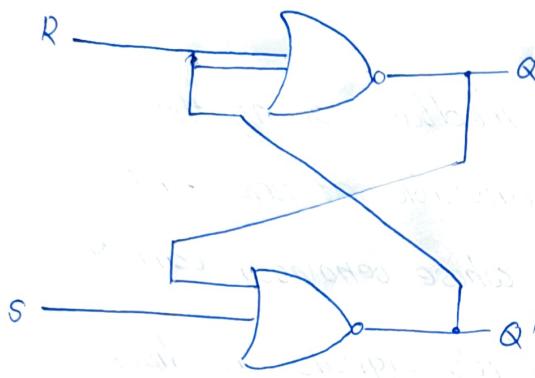
Storage elements: Storage elements that operate with signal levels (rather than signal transition) are referred to as latches, those controlled by a clock transition are flipflops. Latches are said to be level sensitive devices. Flipflops are edge sensitive devices

Latches :-

SR latch :-

(1)

S-set R → reset (0)



Function table

S	R	Q	Q'	
1	0	1	0	
0	1	0	1	
0	0	1	0	
0	0	0	1	→ 0
1	1	forbidden		

In S R no change → 0
 after S=1, R=0
 (Q=1, Q'=0)

after S=0, R=1 → 2
 (Q=0, Q'=1)

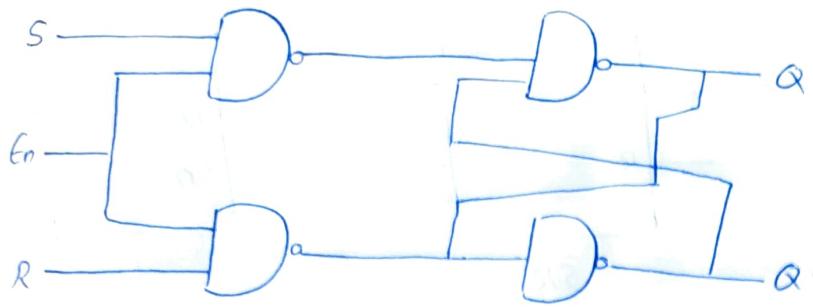
Function table

S	R	Q	Q'	
1	0	0	1	
0	1	1	0	
0	0	forbidden		
1	1	0	1	→ 0
1	1	1	0	→ 2

In S R (after S=1, R=0) → 0
 0 0 (Q=0, Q'=1)

(after S=0, R=1 → 2)
 (Q=1, Q'=1)

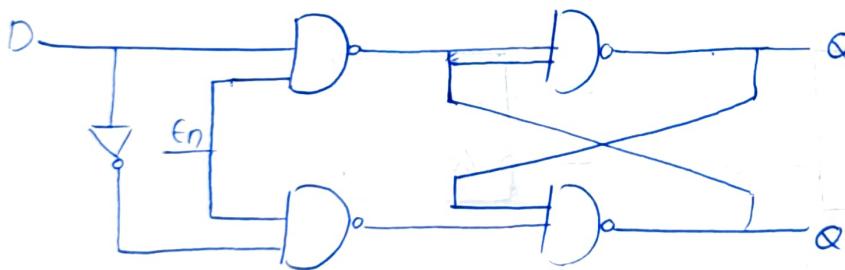
Logic circuit or latch with control i/p



En	S	R	Next state of Q
0	x	x	No change
1	0	0	No change
1	0	1	(Q=0, Q'=1, reset) state
1	1	0	(Q=1, Q'=0, set) state
1	1	1	Indetermined, indeterminate

Function table

D-latch (transparent latch)

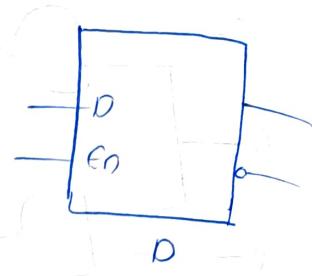
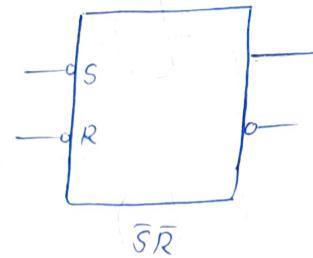
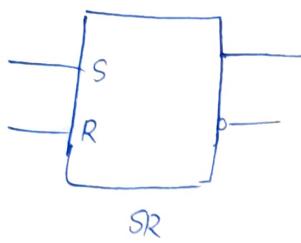


logic circuit d-latch with control i/p

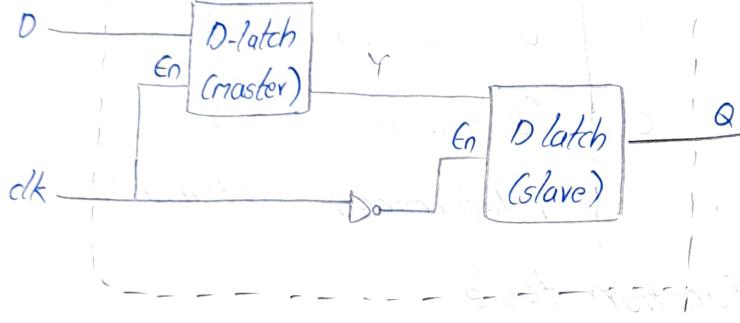
En	D	Next state of Q
0	x	no change
1	1	Q=1, set state
1	0	Q=0, reset state

Function table

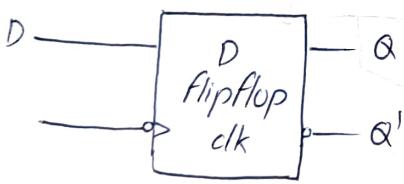
Graphical symbol for latches:-



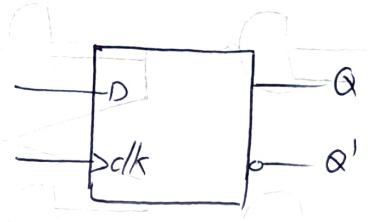
Flip-Flops :- edge triggered



(Master-slave) D-Flipflop



D-flipflop
(-ve edge)



D-flipflop
(+ve edge)

> dynamic indicator

Characteristic Table:

- * A characteristic table defines the logical properties of a flipflop by describing its operation in tabular form.
- * A characteristic table can be expressed with the characteristic equation as well

$Q(t)$ refers to the present state
 $Q(t+1)$ is the next state one clock period later thus
 $Q(t)$ denotes the state of the flipflop immediately before
the clock edge and $Q(t+1)$ denotes the state that result from
the clock transition.

Characteristics table D-Flip flop

D	$Q(t+1)$
0	0
1	1

$$Q(t+1) = D \rightarrow \text{Characteristic Equation}$$

JK-Flipflop

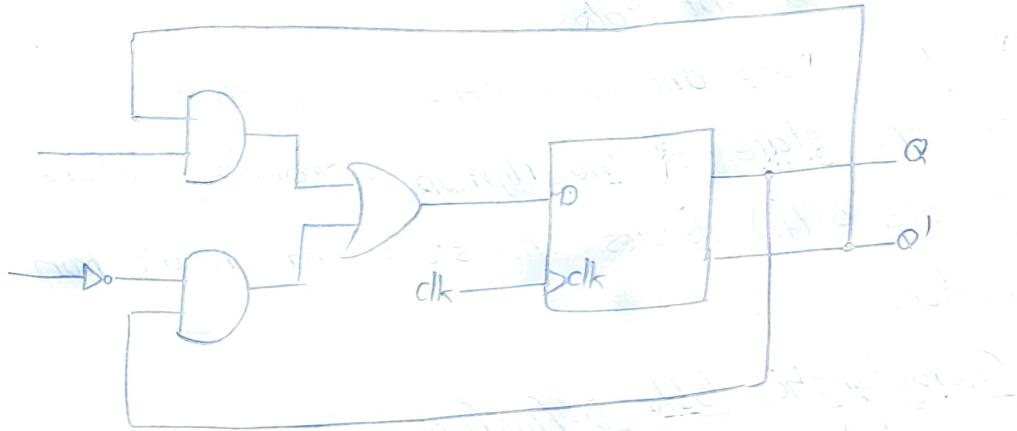
Characteristic table for JK Flipflop

J	K	$Q(t+1)$
0	0	$Q(t)$ (No change)
0	1	0 Reset state
1	0	1 set state
1	1	$Q'(t)$ (complement of previous state)

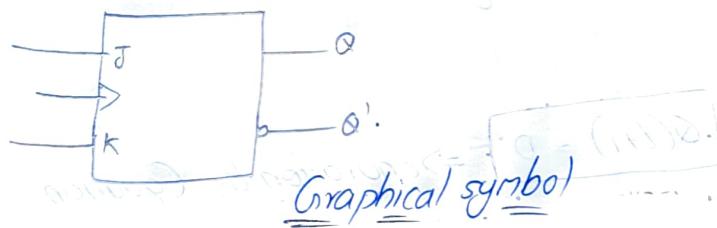
Q	JK			
	00	01	11	10
0	0	0	(1)	(1)
1	(1)	0	0	(1)

$$Q(t+1) = J(t)Q'(t) + K'(t)Q(t)$$

$$[Q(t+1) = JQ' + K'Q] \rightarrow \text{characteristic Eqn}$$



Circuit for JK Flipflop

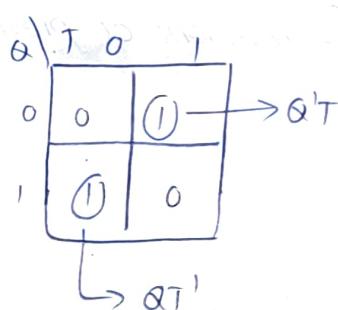


T(Toggle)-flipflop

Characteristic table for T flipflop

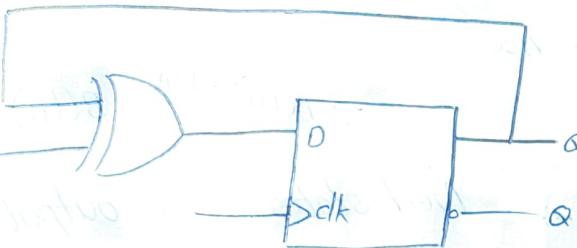
T	$Q(t+1)$
0	$Q(t)$
1	$Q'(t)$

No change
complement

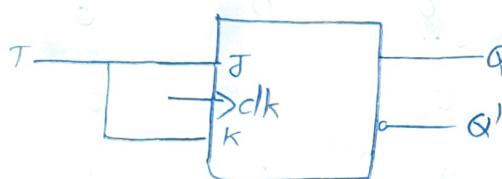


$$Q(t+1) = Q'T + Q'T' \Rightarrow \text{characteristic eq?}$$

$$= Q \oplus T$$



ckt for T-flipflop using D-flipflop

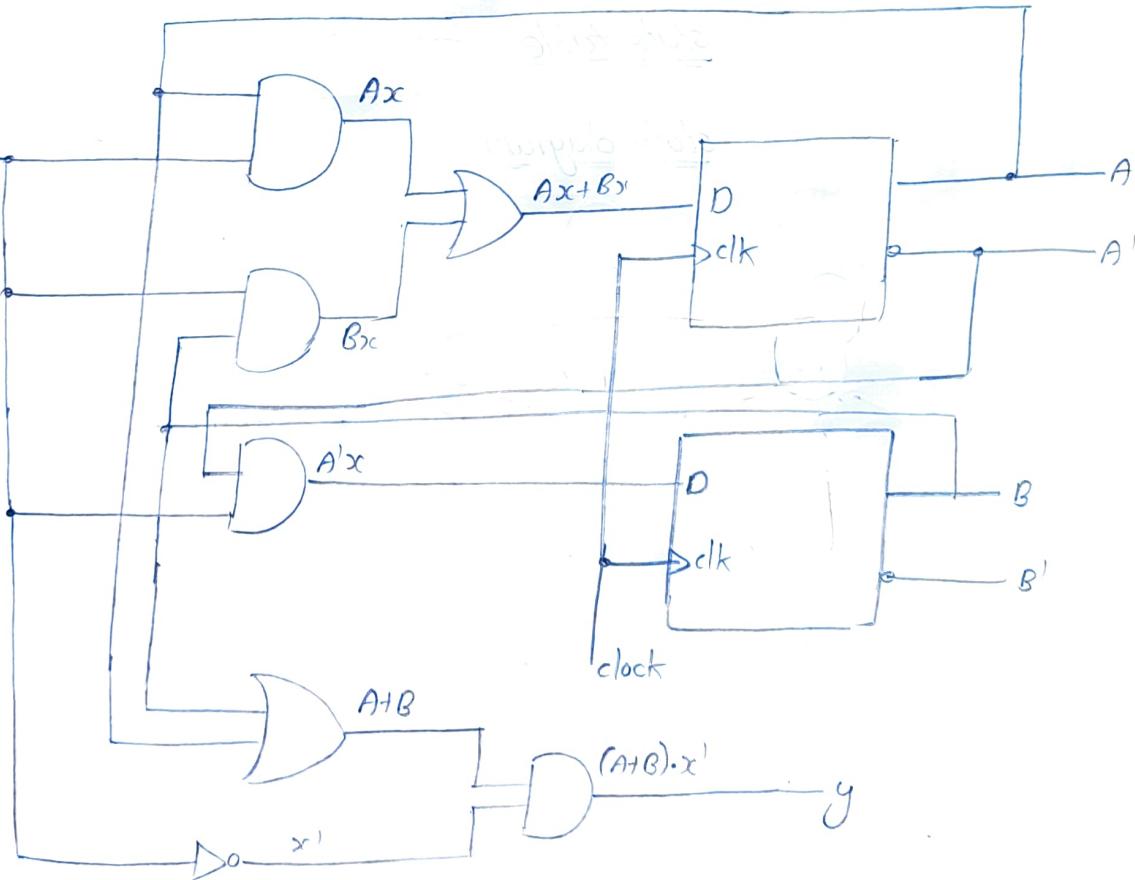


ckt of T flipflop using JK flipflop



Graphic symbol

Analysis of clocked sequential circuits



$$y = (A+B)x$$

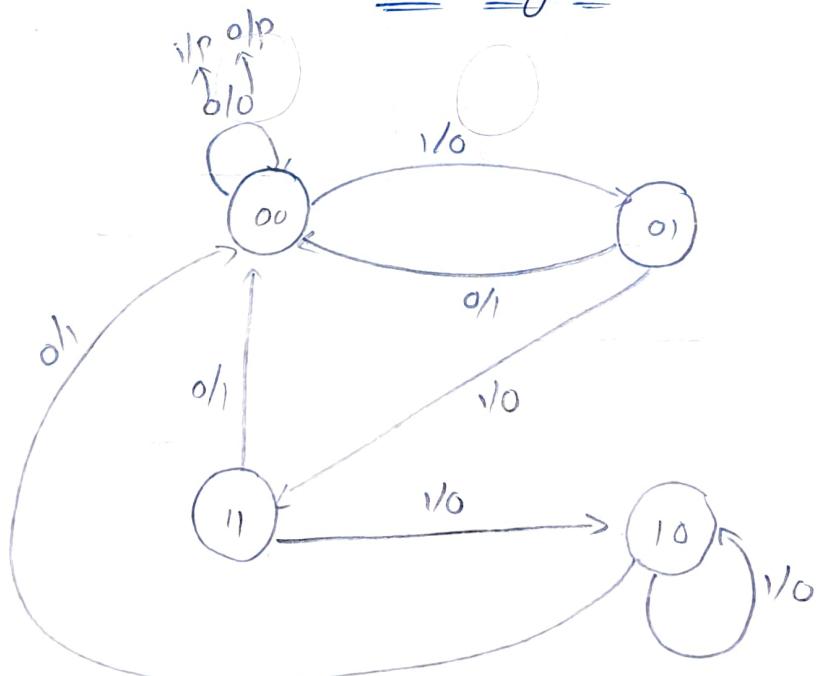
$$\therefore A(t+1) = D_A$$

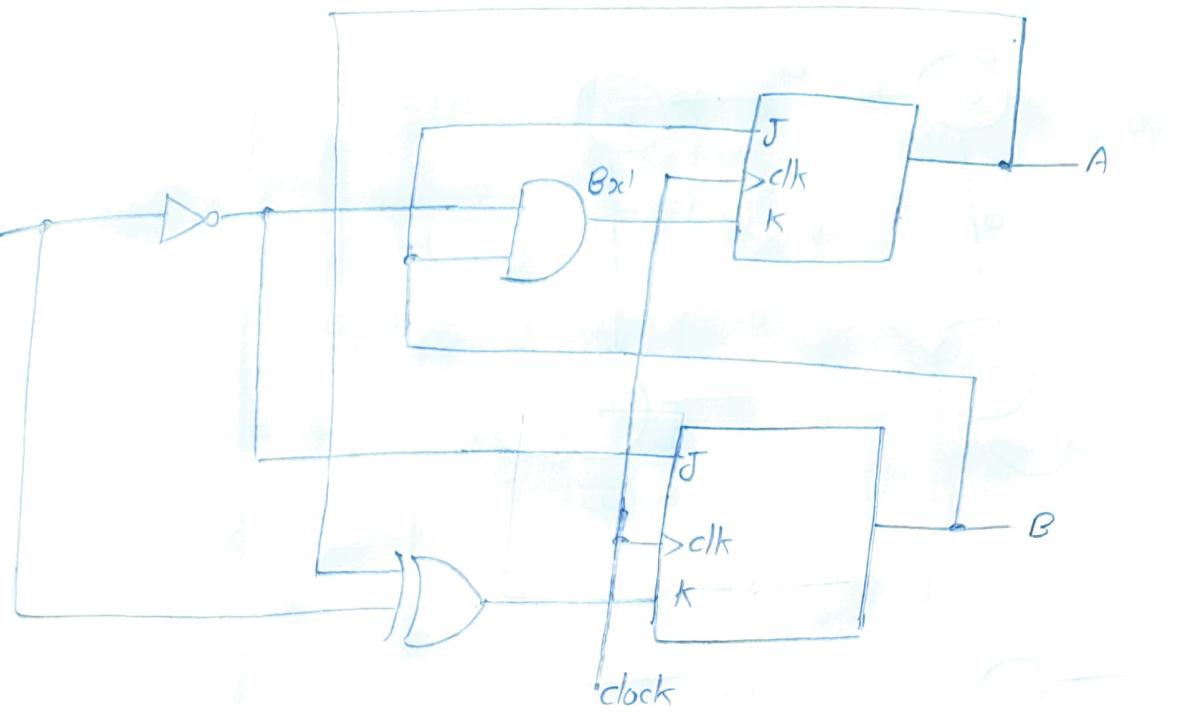
$$B(t+1) = D_B$$

present states		input	Next states		output
A	B	x	A(t+1)	B(t+1)	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

state table

state diagram



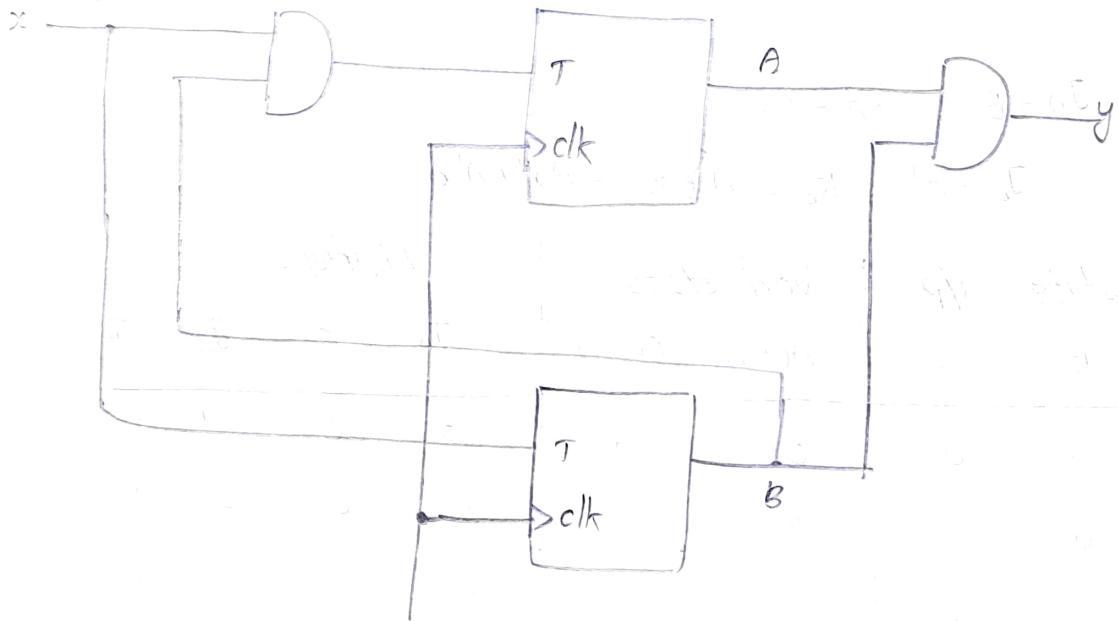
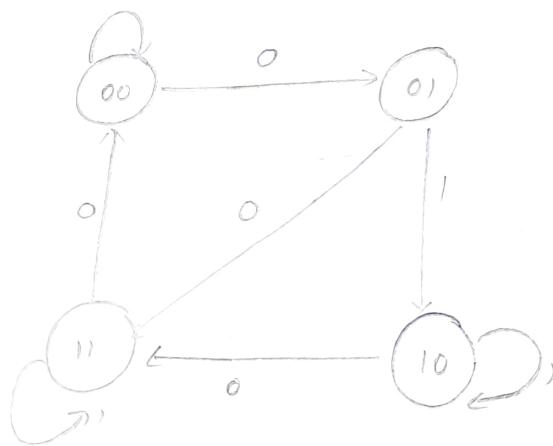


$$J_A = B \quad K_A = Bx'$$

$$J_B = x' \quad K_B = A \oplus x = Ax' + A'x$$

present state A B x			Next state A(t+1) B(t+1)		FlipFlops J _A K _A J _B K _B			
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	1	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

state table



Another form of representation

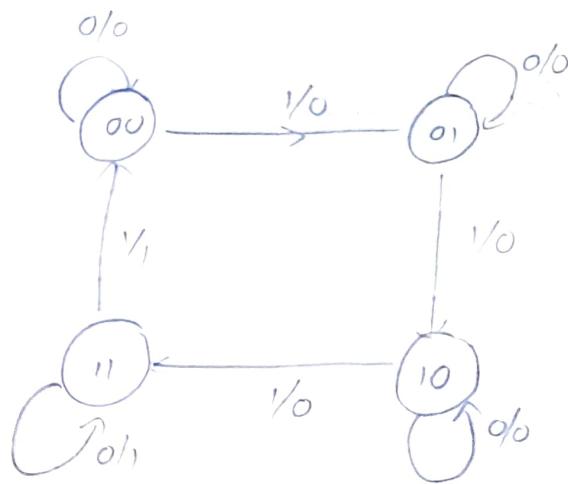
$$T_A = Bx$$

$$T_B = x$$

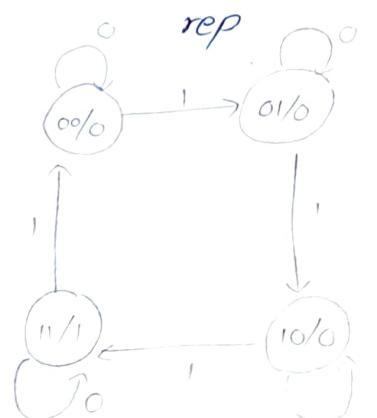
$$y = AB$$

A	B	$A(t+1)$ $x=0 \quad x=1$	$B(t+1)$ $x=0 \quad x=1$	y $x=0 \quad x=1$
0	0	0 0	0 1	0 0
0	1	0 1	1 0	0 0
1	0	1 1	0 1	0 0
1	1	1 0	1 0	1 1

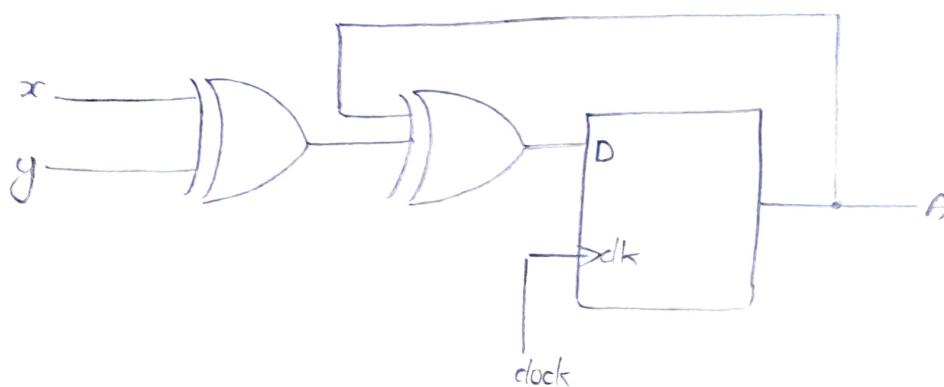
Present state A B	Input x	Next state A(t+1) B(t+1)		Output y	Flip flop inputs	
		A	B		T _A	T _B
0 0	0	0	0	0	0	0
0 0	1	0	1	0	0	1
0 1	0	0	1	0	0	0
0 1	1	1	0	0	1	1
1 0	0	1	0	0	0	0
1 0	1	1	1	0	0	1
1 1	0	1	1	1	0	0
1 1	1	0	0	1	1	1



Another form of rep



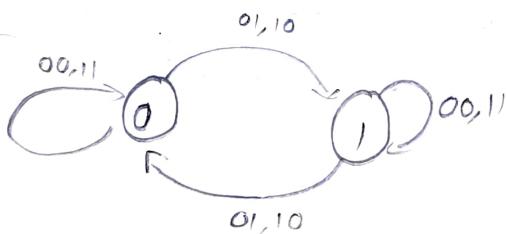
Q) Analyse the below circuit



$$D_A = x \oplus y \oplus A$$

Present state A	i/p s		Next state $A(t+1)$	D_A
	x	y		
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

state diagram



Two models of S-C:-

$$(Ex:- y = (A+B)x^1)$$

→ Mealy model / Machine (present state & i/p dependent)

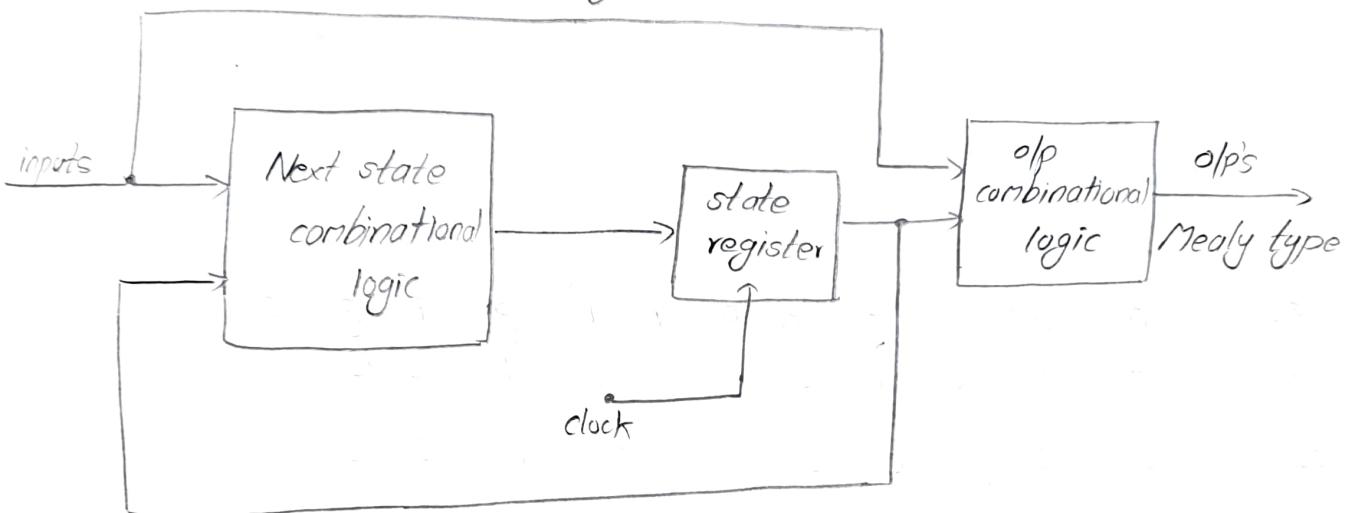
→ Moore model (depends on present state only) (Ex:- $y = AB$)

* All the transition diagram in general can be called as
Finite State Machine (FSM)

Mealy and Moorey models of FSM:-

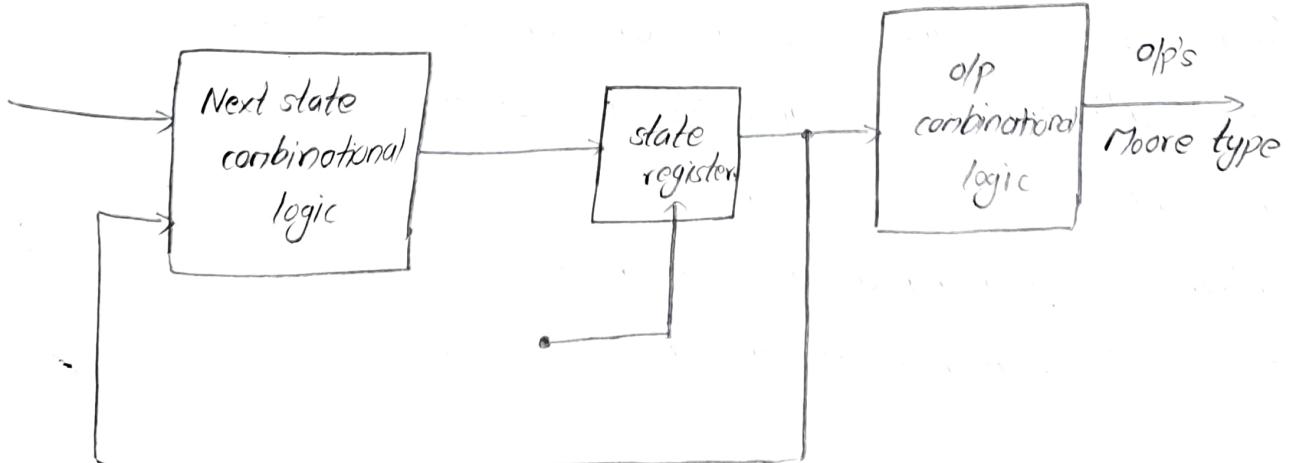
In Mealy model the output is a function of both present state and i/p

Mealy Machine



In Moore model the o/p is the function of only the present state

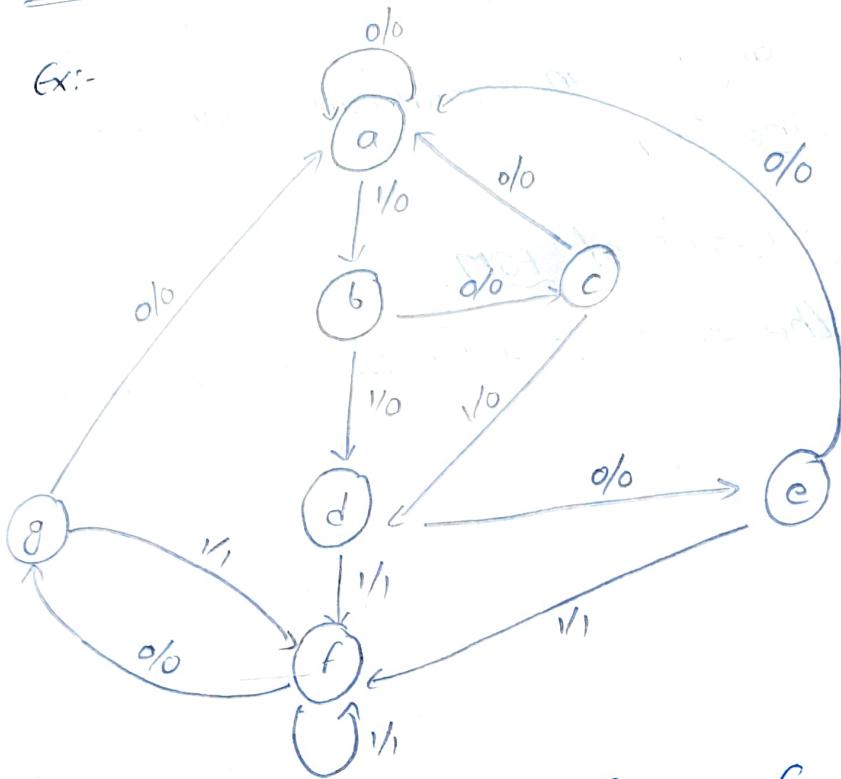
Moore Machine



State Reduction

State Reduction:-

Ex:-



state	a	ba	b	c	d	e	f	f	g	g	a
input	0	1	0	1	0	1	0	1	0	0	
output	0	0	0	0	0	1	1	0	1	0	0

- * Two states are said to be equivalent if for each member of the set of i/p's they give exactly the same o/p and send the circuit either to the same state or to the equivalent state.
- * When two states are equivalent one of them can be removed without altering the i/p and o/p relationship.
- * If identical i/p sequences are applied to the two circuits and identical o/p's occur for all i/p sequences, then the two circuits are said to be equivalent and one may be replaced by the other.

Present state

Next state

$x=0$ $x=1$

Output

$x=0$ $x=1$

a

a b

0 0

b

c d

0 0

c

a d

0 0

d

e f

0 1

e

a f

0 1

f

g f

0 1

g

a f

0 1

c and g are equivalent

remove state g

Present state

Next state

$x=0$ $x=1$

Output

$x=0$ $x=1$

a

a b

0 0

b

c d

0 0

c

a d

0 0

d

e f

0 1

e

a f

0 1

f

e f

0 1

state d and f are equivalent

remove F

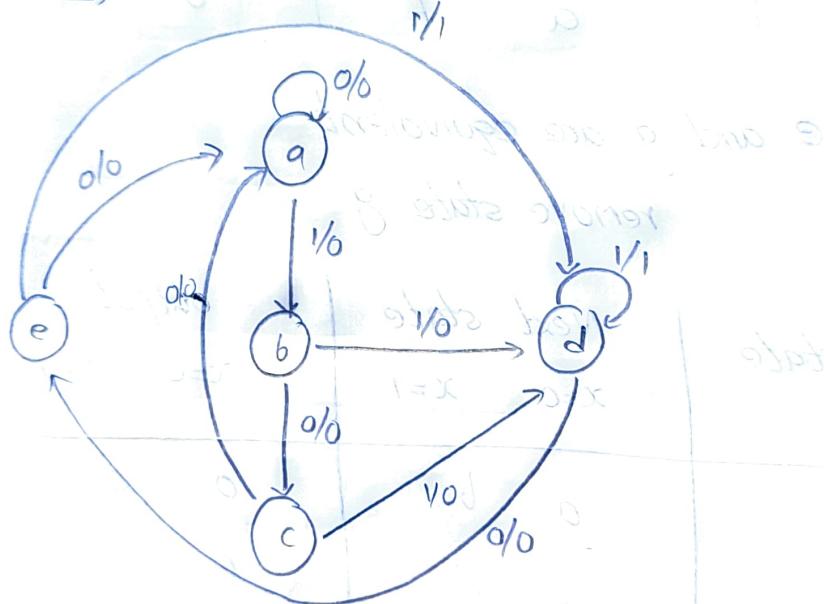
Present state

Next state
 $x=0$ $x=1$

Output
 $x=0$ $x=1$

	a	b	c	d	e	a	b	c	d	e
a	0	0	0	0	0	0	0	0	0	0
b	0	0	0	0	0	0	0	0	0	0
c	0	0	0	0	0	0	0	0	0	0
d	0	0	0	0	0	0	0	0	1	0
e	0	0	0	0	0	0	0	0	1	0

Reduced state diagram



state

	a	b	c	d	e	a	b	c	d	e
input	0	1	0	1	0	1	1	0	1	0
output	0	0	0	0	0	1	1	0	1	0

Three possible

State Assignment using binary code

Three possible binary state assignments

state	Assignment-1 Binary	Assignment-2 Gray code	Assignment-3 one-hot
a	0 0 0	0 0 0	0 0 0 0 1
b	0 0 1	0 0 1	0 0 0 1 0
c	0 1 0	0 1 1	0 0 1 0 0
d	0 1 1	0 1 0	0 1 0 0 0
e	1 0 0	1 1 0	1 0 0 0 0



P.S	N.S		O/p		
	$x=0$	$x=1$	$x=0$	$x=1$	
0 0 0	0 0 0	0 0 1	0	0	
0 0 1	0 1 0	0 1 1	0	0	
0 1 0	0 0 0	0 1 1	0	0	
0 1 1	1 0 0	0 1 1	0	1	
1 0 0	0 0 0	0 1 1	0	1	

Design procedure:- for seq ckt's:-

Design procedure specify hardware that will implement the desired behaviour

Steps:-

- ① From the word description and specifications of the desired operation derive a state diagram for the ckt
- ② Reduce the no of states if necessary
- ③ Assign binary values to the states.
- ④ Obtain the binary coded state table
- ⑤ Choose the type of flipflops to be used
- ⑥ Derive the simplified flipflop ip equations and op equations
- ⑦ Draw the logic diagrams.

Flip-flop Excitation

$Q(t)$	$Q(t+1)$					
		J	K	S_{in}	S_{out}	Q_{out}
0	0	0	0	0	0	0
0	1	1	0	0	0	1
1	0	1	1	0	1	0
1	1	0	0	1	1	1

Excitation of T-Flipflop

$Q(t)$	$Q(t+1)$	J	K			
				S_{in}	S_{out}	Q_{out}
0	0	0	x	0	0	0
0	1	1	x	0	0	1
1	0	x	1	0	1	0
1	1	x	0	1	1	1

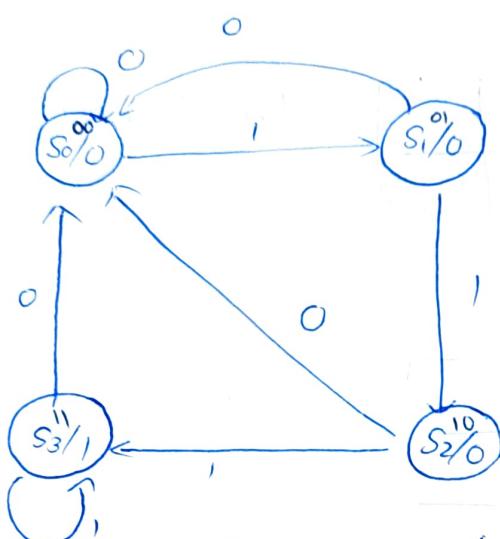
Excitation of JK Flipflop

$Q(t)$	$Q(t+1)$	D
0	0	0
0	1	1
1	0	0
1	1	1

Excitation table of
D-flipflop

Q) Design a circuit that detects the sequence of three or more consecutive one's in a string of bits coming through the I/O line

Sol:-



State diagram of sequence detector (consecutive three ones or more)

Present state A B	Input x	Next state A(t+1) B(t+1)		Output y	Output D _A D _B	
		A(t+1)	B(t+1)		D _A	D _B
0 0	0	0	0	0	0	0
0 0	1	0	1	0	0	1
0 1	0	0	0	0	0	0
0 1	1	1	0	0	1	0
1 0	0	0	0	0	0	0
1 0	1	1	1	0	1	1
1 1	0	0	0	1	0	0
1 1	1	1	1	1	1	1

Present state $A(t)$ $B(t)$	Next state $A(t+1)$		Output & Next st $B(t+1)$		$O/p(y)$ $x=0$ $x=1$
	$x=0$	$x=1$	$x=0$	$x=1$	
0 0	0 0	0 0	0 1	0 1	0 0
0 1	0 1	0 1	0 0	0 0	0 0
1 0	0 0	0 1	0 1	0 0	0 0
1 1	0 1	0 1	0 1	1 1	1 1

A	Bx			
	00	01	11	10
0	0	0	1	0
1	1	1	1	0

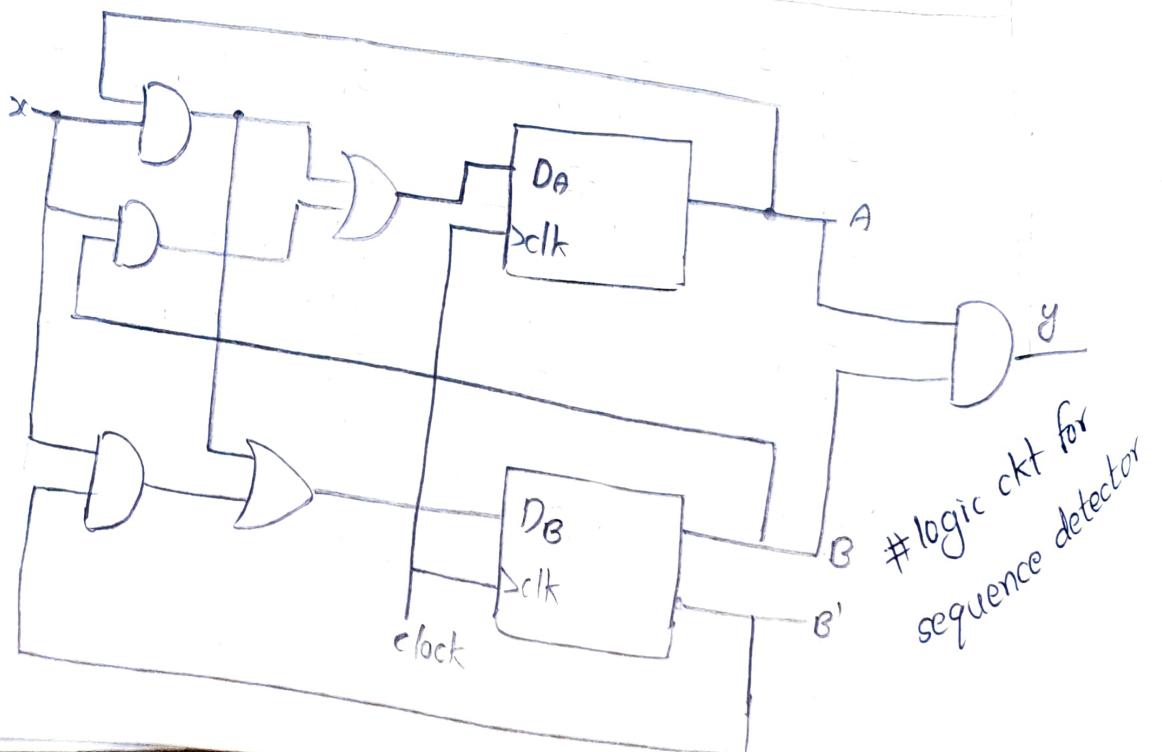
$$D_A = Bx + Ax$$

A	Bx			
	00	01	11	10
0	0	1	0	0
1	1	1	1	0

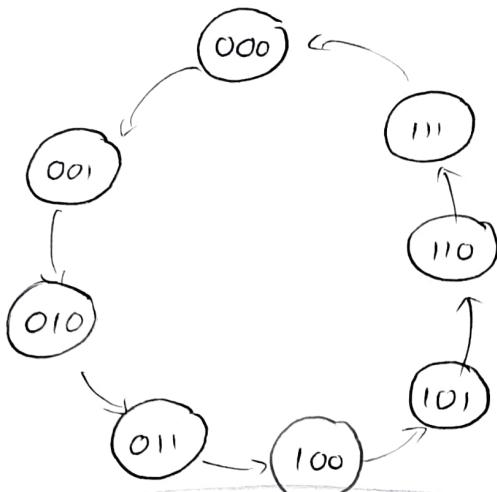
$$D_B = B'x + Ax$$

A	Bx			
	00	01	11	10
0	0	0	1	0
1	1	1	1	1

$$g = AB$$



Q) Design a three bit binary counter using T-Flipflop.



Present state (t)			Next state (t+1)			Flipflop inputs		
A_2	A_1	A_0	A_2	A_1	A_0	T_{A_2}	T_{A_1}	T_{A_0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	1	0	1	1	0	0	1
1	1	1	1	0	0	1	1	1

A_2	A_1 , A_0
0	00, 01, 11, 10
1	11, 10

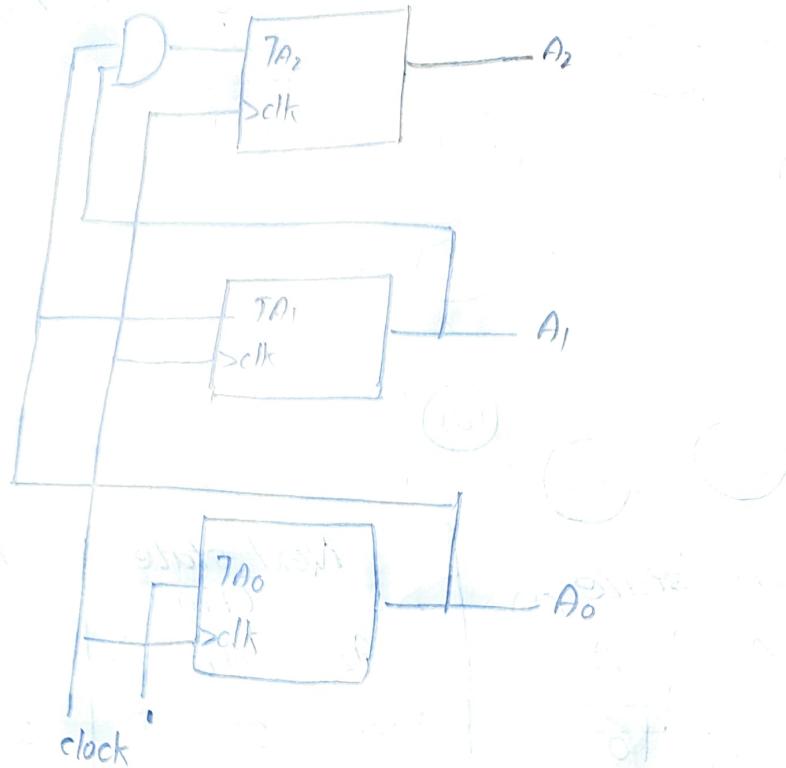
$$T_{A_1} = A_0$$

A_2	A_1 , A_0
0	00, 01, 11, 10
1	00

$$T_{A_2} = A_1 A_0$$

A_2	A_1 , A_0
1	1, 1, 1, 1
1	1, 1, 1, 1

$$T_{A_0} = 1$$



Logic circuit for 3-bit binary counter

Q) Synthesis using JK Flipflop

Present state	Input	Next state	JK inputs
A	B	x	J _A K _A J _B K _B
0	0	0	0 X 0 X
0	0	1	0 X 1 X
0	1	0	1 X X 1
0	1	1	0 X X 0
1	0	0	X 0 0 X
1	0	1	X 0 1 X
1	1	0	X 0 X 0
1	1	1	X 1 X 1

	Bx00	01	11	10
A				
0	x	x	x	x
1				

$$J_A = Bx^1$$

	Bx00	01	11	10
A				
0	x	x	x	x
1				

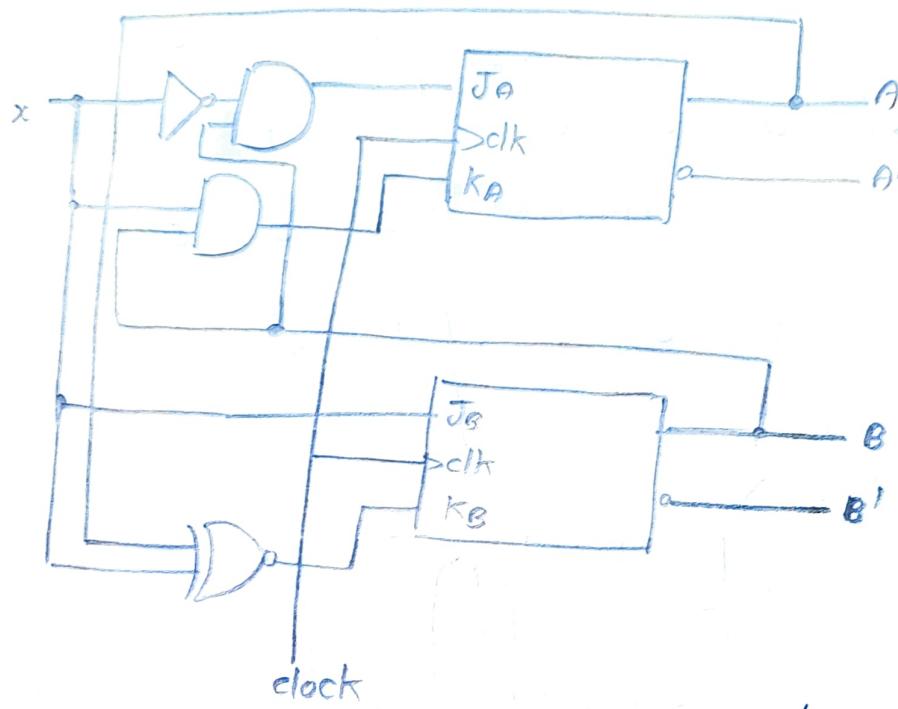
$$K_A = Bx$$

	Bx00	01	11	10
A				
0	x	x	x	x
1				

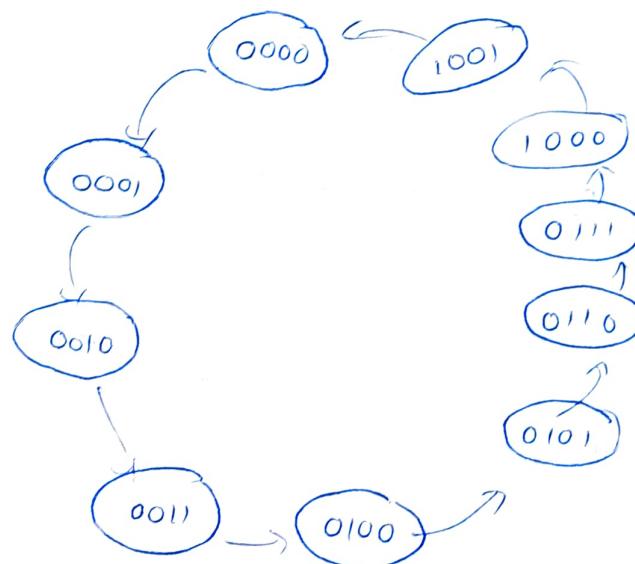
$$J_B = x$$

	Bx00	01	11	10
A				
0	x	x	x	x
1	x	x	x	x

$$K_B = A'x^1 + Ax = (A \oplus x)^1$$

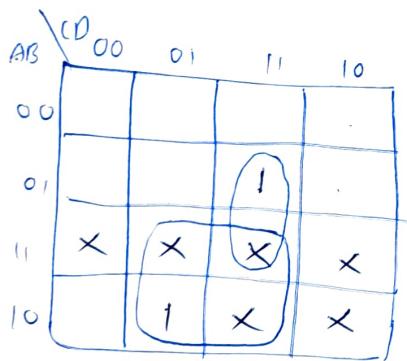


Design BCD counter

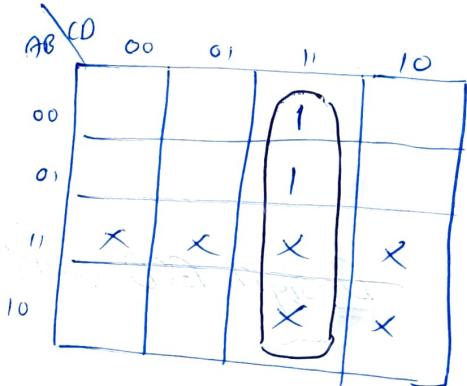


Q) Design BCD counter

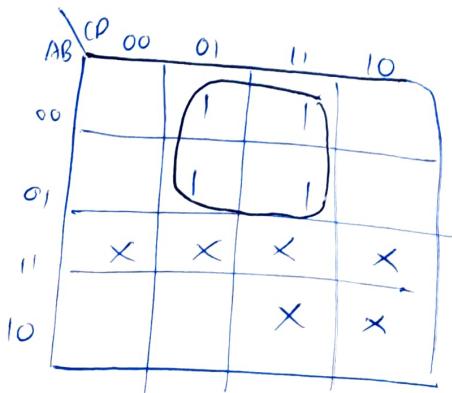
P State	A B C D				A(t+1)	B(t+1)	C(t+1)	D(t+1)	Next state			T_A	T_B	T_C	T_D	Flip flop
	A	B	C	D					0	0	0					
0000	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
0001	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1
0010	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	1
0011	0	0	1	1	0	1	0	0	0	0	0	0	1	1	1	1
0100	0	1	0	0	0	1	0	1	0	1	0	0	0	0	0	1
0101	0	1	0	1	0	1	1	0	0	1	1	0	0	0	0	1
0110	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	1
0111	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1
1000	1	0	0	0	1	0	0	1	0	0	1	0	0	0	0	1
1001	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1



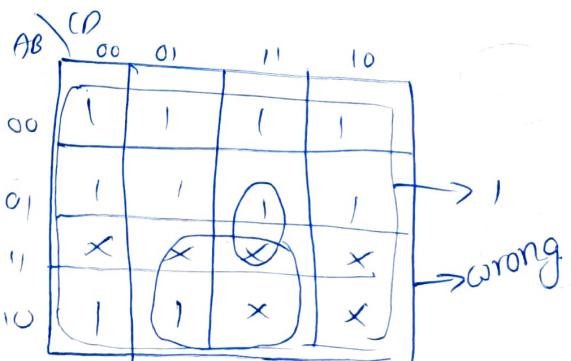
$$T_A = AD + BCD$$



$$T_B = CD$$



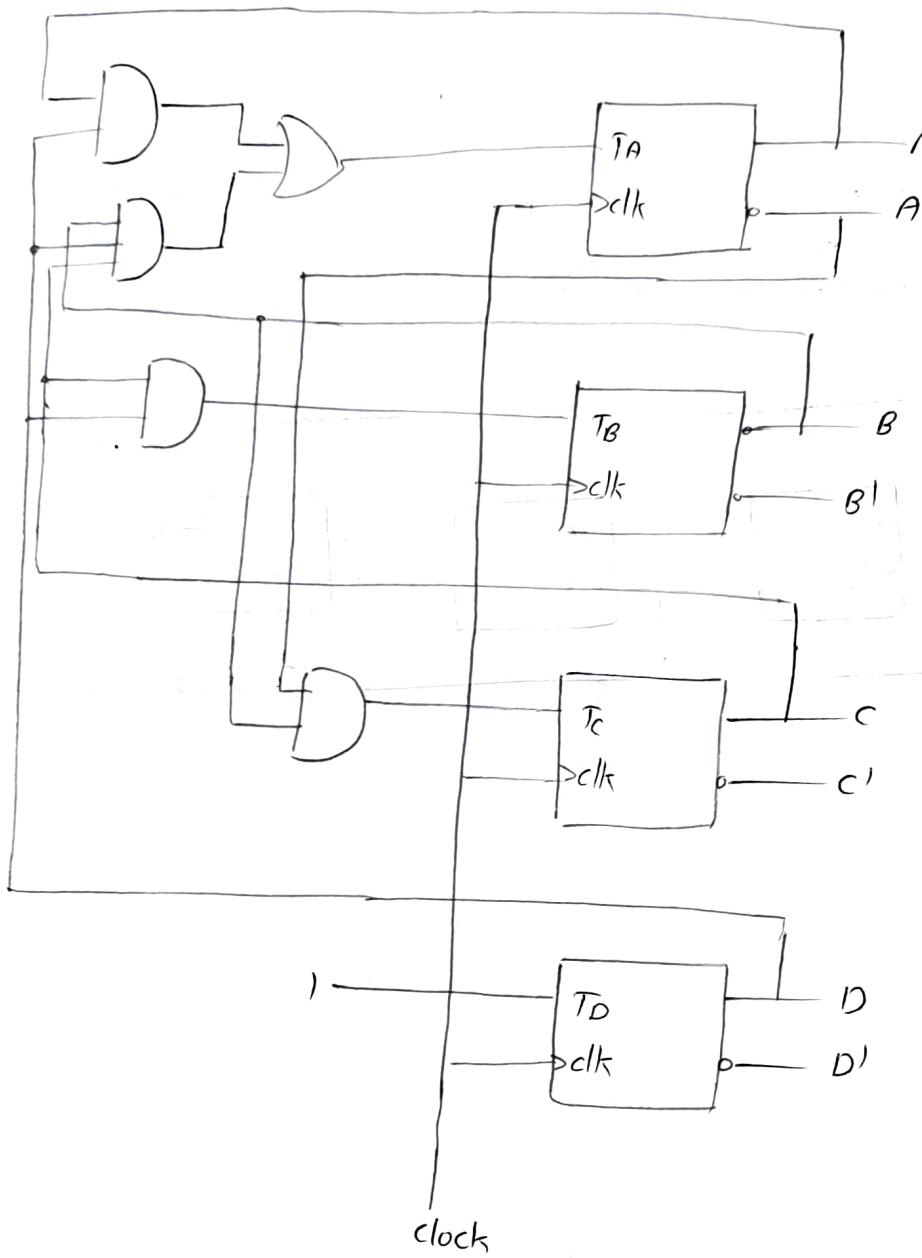
$$T_C = DA'$$



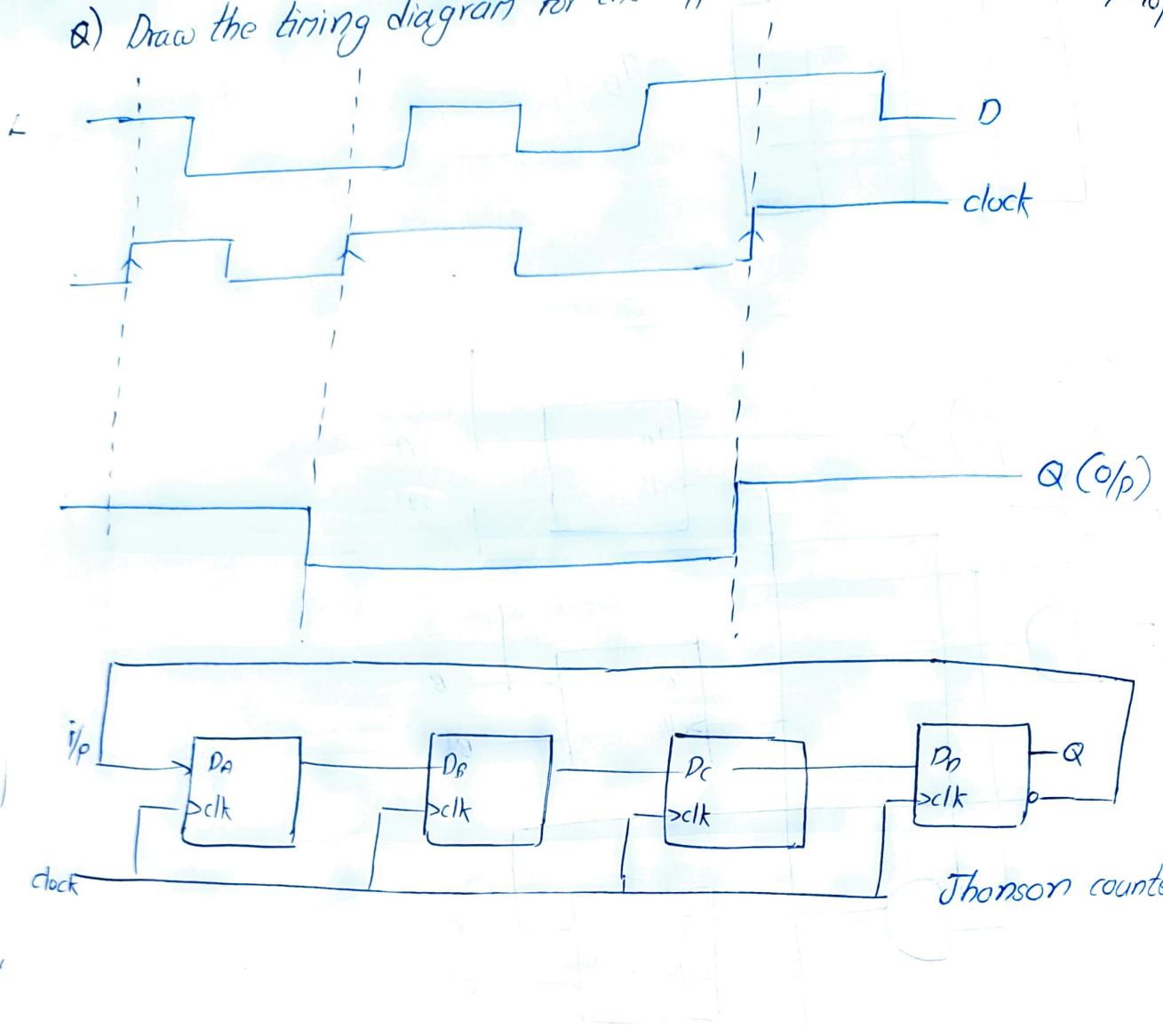
$$T_D = 1$$

	00	01	10	11
00	1	1	1	1
01	1	1	1	1
10	1	1	1	1
11	1	1	1	1

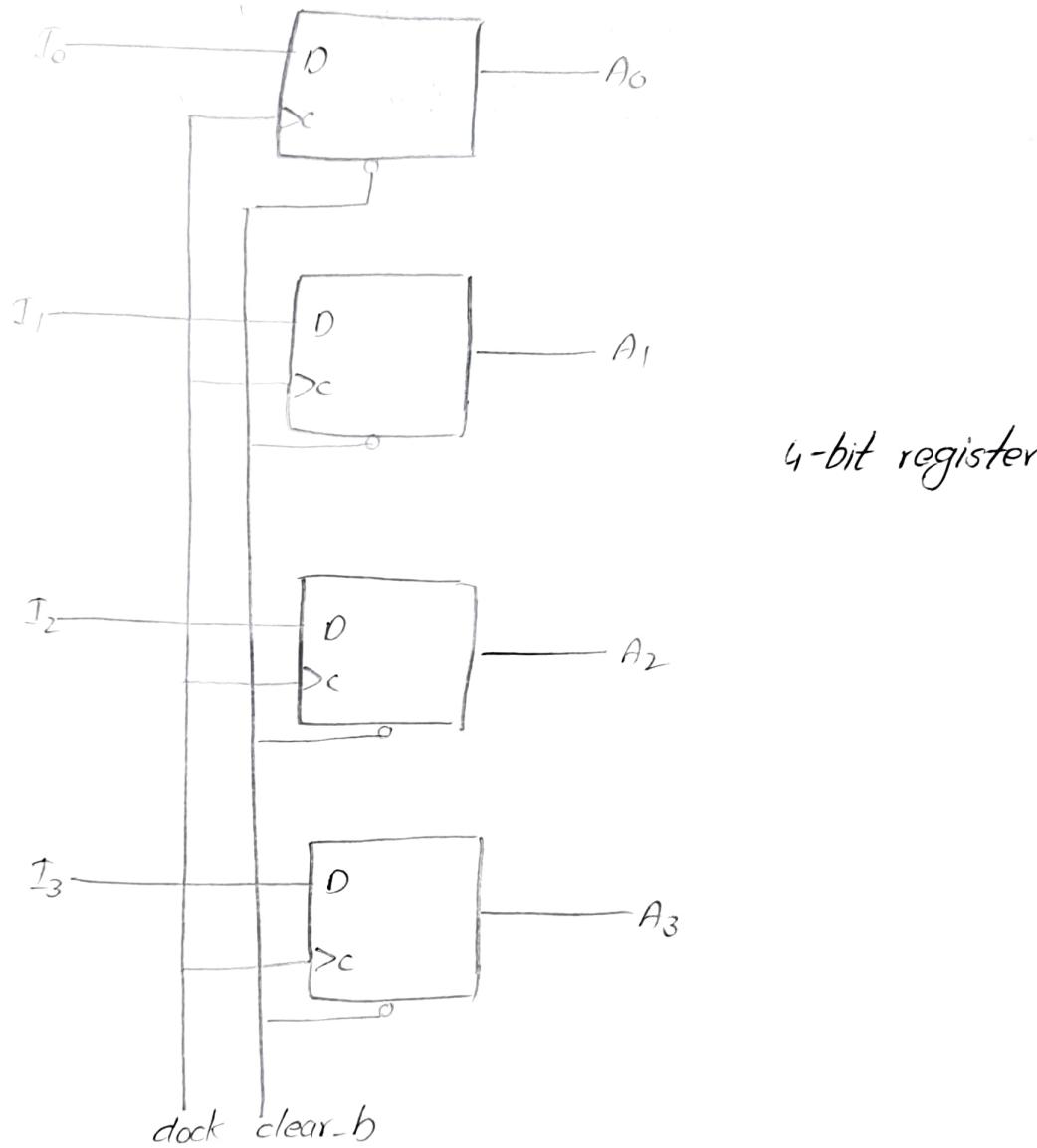
$$T_D = 1$$



Q) Draw the timing diagram for the o/p Q for 11P's or D-HipFlop

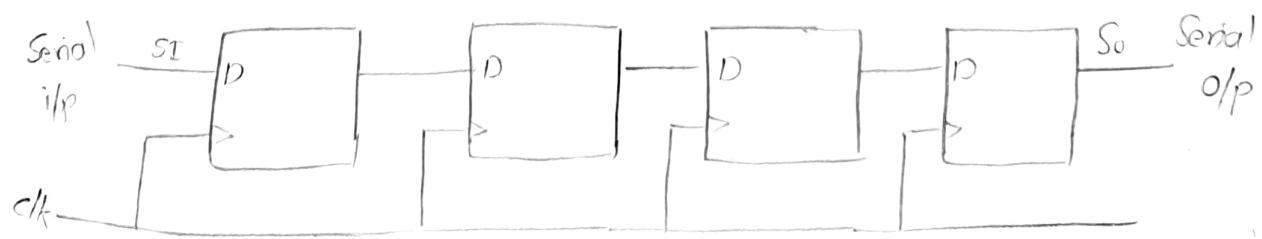


Register: A register is a group of flipflops each of which and is capable of storing 1 bit of information. An n-bit register consists of the group of n-flipflops capable of storing n bits of binary information.



Shift register: - A register capable of shifting the binary information held in each cell to its neighbouring cell in specified direction is called shift register

4-bit shift register

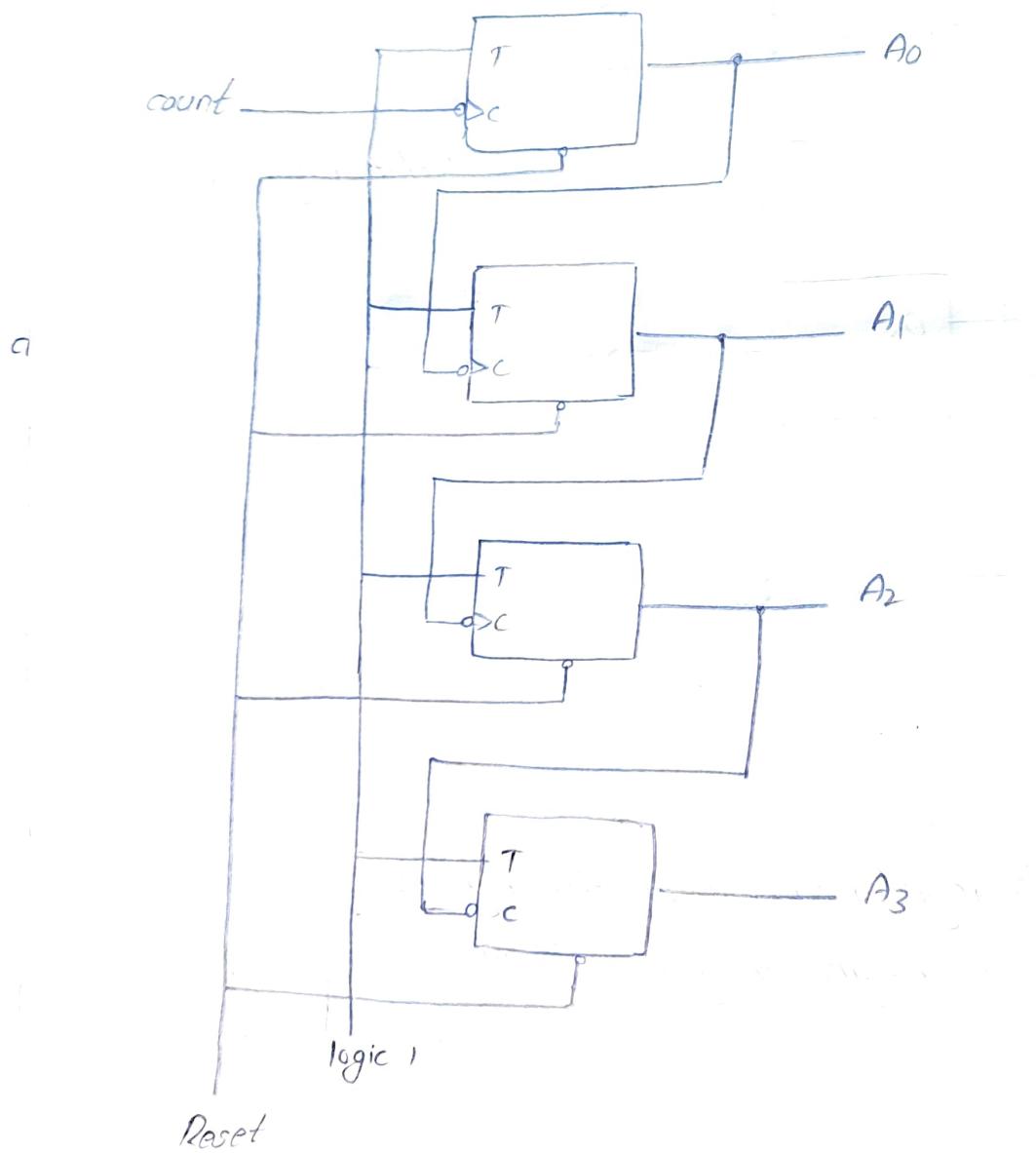


Counter: A counter is essentially a register that goes through a pre-determined sequence of a binary state. The gates in the counter are connected in such a way as to produce the prescribed sequence of states.

There are two categories of counters:-

- 1-Ripple counters
- 2- Synchronous counter

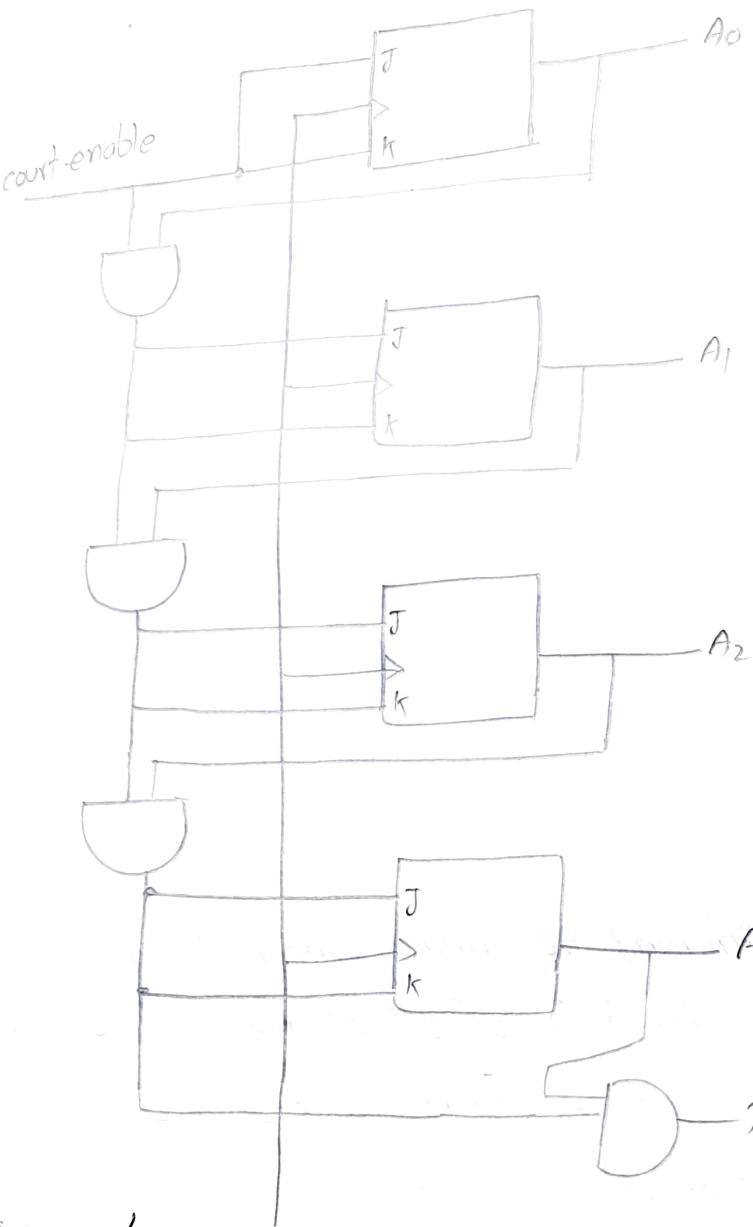
In a ripple counter, a flip flop output transition serves as the source for triggering other flip flops.



A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	1	1	1
1	1	1	1
1	1	1	1
0	0	0	0

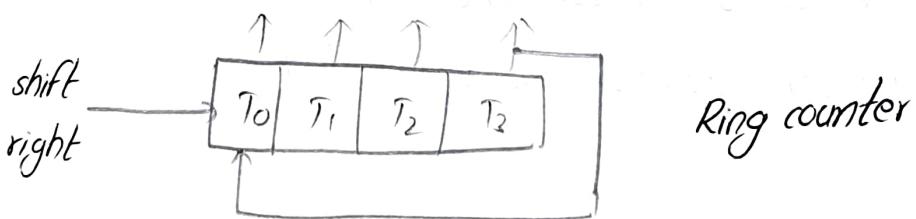
Synchronous counters are different from ripple counter. In that clock pulses are applied to the i/p's of all flipflops. A common clock triggers all flipflops simultaneously rather than one at a time in succession as in a ripple counter.

Binary counter :- In a synchronous binary counter the flipflop in the least significant position is complemented with every pulse. A flipflop in other position is complemented when all the bits in the lower significant position are equal to 1.

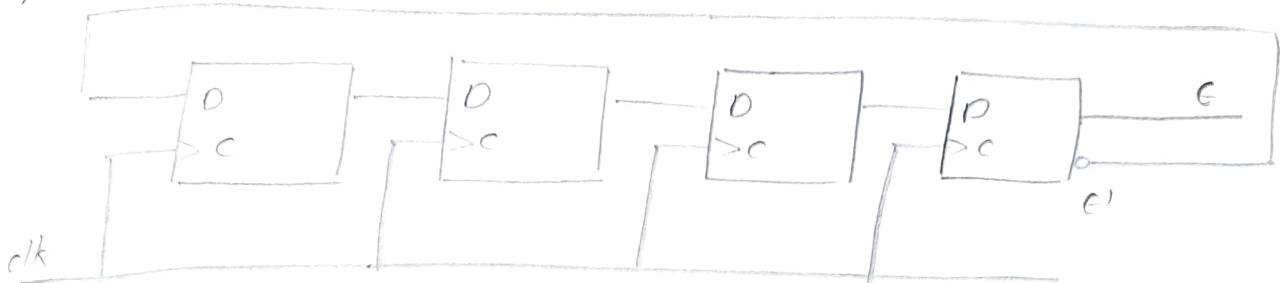


Four bit
synchronous
binary counter,

Ring counter: -
Ring counter is a circular shift register with only one flip flop being set at any particular time.



The no of states can be doubled if the shift register is connected switch tail ring counter. A switch tail ring counter is a circular shift register with complemented o/p of the flipflop connected to the i/p of the first flipflop.



Four stage switch tail ring counter