

# KUAN-YU CHANG

## VERIFICATION IP DESIGN ENGINEER

Avery Design Systems, Inc.  
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## PROFESSIONAL EXPERIENCES

**Verification IP (VIP) Design Engineer**  
*Upper Layer Group of PCI Express (PCIe) VIP Team*  
Avery Design Systems, Inc., Taiwan  
Jul. 2021 - present



- Research and Development Substitute Services until April 8th, 2023
- Focus on the Next Generation Protocols
  - Enhance VIP to support FLIT mode for upper layers of the PCIe 6.0 architecture
  - Develop Streaming Fabric Interface (SFI) Bus Functional Model
- Customer support of product usage
- Compliance test case design

## EDUCATION

National Tsing Hua University, Hsinchu, Taiwan

*Advisor: Prof. Chun-Yi Lee*

- M.S. in Computer Science – Jun. 2021
  - Thesis Title: *Mapping Nearest Neighbor Compliant Quantum Circuits onto a 2-D Hexagonal Architecture* [NDLTD]
- B.S. in Interdisciplinary Program of Science – Jun. 2017
  - Double expertise in *Computer Science* and *Chemistry*



## TECHNICAL SKILLS

Programming Languages	C/C++ , SystemVerilog, Verilog, Bash, Perl, Python
Software & Tools	Docker, LaTeX, MS Office
Operating Systems	Ubuntu, CentOS, macOS, MS Windows

## PUBLICATIONS

- [1] K.-Y. **Chang** and C.-Y. Lee, "Mapping Nearest Neighbor Compliant Quantum Circuits onto a 2-D Hexagonal Architecture," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, no. 10, pp. 3373–3386, Oct. 2022, ISSN: 1937-4151. DOI: 10.1109/TCAD.2021.3127868.
- [2] Y.-H. Chang, K.-Y. **Chang**, H. Kuo, and C.-Y. Lee, "Reusability and Transferability of Macro Actions for Reinforcement Learning," *ACM Trans. Evol. Learn. Optim.*, vol. 2, no. 1, Apr. 2022, ISSN: 2688-299X. DOI: 10.1145/3514260.
- [3] Y.-M. Chen, K.-Y. **Chang**, C. Liu, T.-C. Hsiao, Z.-W. Hong, and C.-Y. Lee, "Toward Synergism in Macro Action Ensembles," *ICML Workshop on Automated Machine Learning*, 2020. [pdf] [poster]