

KUAN-YU CHANG

DESIGN VERIFICATION ENGINEER

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PROFESSIONAL EXPERIENCES

Design Verification Engineer

Logic Design Department II, Research and Development Center
ASMedia Technology Inc., Taiwan
Jul. 2023 - present



- Universal Serial Bus 4 (USB4®) Version 2
 - Develop the Verification IP (VIP) using Universal Verification Methodology (UVM)
 - * PCI Express Tunneling

Verification IP (VIP) Engineer (RDSS)¹

Upper Layer Group of PCIe VIP Team
Avery Design Systems, Inc., Taiwan²
Jul. 2021 - Apr. 2023



- PCI Express® (PCIe) Revision 6.0.1
 - Enhance the Bus Functional Model (BFM) to support Flit mode.
 - * Flit_Marker mechanism
 - * Flit Ack, Nak, and Discard Rules
 - * Flit Replay Rules (especially the Selective Replay)
 - Enhance / Develop compliance test cases for Flit mode.
 - * 14-Bit Tag mechanism
 - * Orthogonal Header Content (OHC) of Transaction Layer Packets
 - * Shared Flow Control with extended virtual channels
- Streaming Fabric Interface (SFI) [Read more]
 - Design the architecture of the BFM.
 - Lead the schedule of the product development.
 - Develop the functionality to align with the latest specification.
- Resolved **350+** issues while supporting customers on the bug tracking system (Bugzilla)
 - **67.33%** Customer Issues / **27.56%** Product Enhancements
- Contributed **13k+** lines of SystemVerilog code on the Concurrent Versions System (CVS, Linux)
 - **16.07%** PCIe BFM / **25.96%** SFI BFM / **57.97%** Test cases

EDUCATION

National Tsing Hua University, Hsinchu, Taiwan

Advisor: Prof. Chun-Yi Lee

- M.S. in Computer Science – Jun. 2021
 - **Master's Thesis:** Mapping Nearest Neighbor Compliant Quantum Circuits onto a 2-D Hexagonal Architecture [NDLTD]
- B.S. in Interdisciplinary Program of Science – Jun. 2017
 - Double expertise in Computer Science and Chemistry



¹RDSS stands for Research and Development Substitute Services.

²Siemens Digital Industries Software acquired Avery Design Systems, Inc. in March 2023. [Read more]

PUBLICATIONS

(* denotes the communication author)

- [1] **K.-Y. Chang*** and C.-Y. Lee, “Mapping Nearest Neighbor Compliant Quantum Circuits onto a 2-D Hexagonal Architecture,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, no. 10, pp. 3373–3386, Oct. 2022, ISSN: 1937-4151. DOI: 10.1109/TCAD.2021.3127868.
- [2] Y.-H. Chang, **K.-Y. Chang**, H. Kuo, and C.-Y. Lee*, “Reusability and Transferability of Macro Actions for Reinforcement Learning,” *ACM Transactions on Evolutionary Learning and Optimization (TELO)*, vol. 2, no. 1, Apr. 2022, ISSN: 2688-299X. DOI: 10.1145/3514260.
- [3] Y.-M. Chen, **K.-Y. Chang**, C. Liu, T.-C. Hsiao, Z.-W. Hong, and C.-Y. Lee*, “Composing Synergistic Macro Actions for Reinforcement Learning Agents,” *IEEE Transactions on Neural Networks and Learning Systems (TNNLS)*, pp. 1–8, 2022. DOI: 10.1109/TNNLS.2022.3213606, Early Access.