KUAN-YU CHANG

DESIGN VERIFICATION ENGINEER

ASMedia Technology Inc.
6F, No. 115, Minquan Rd., Xindian Dist.,
New Taipei City 231, Taiwan, R.O.C.

Phone: +886-2-2219-6088#5244
Email: kuanyu_chang@asmedia.com.tw

PROFESSIONAL EXPERIENCES

Design Verification Engineer
Logic Design Division II, IC Design Center
ASMedia Technology Inc., New Taipei City, Taiwan
Jul. 2023 - present

- Universal Serial Bus 4 (USB4®), Version 1.0 [Read more]
  - Perform the design verification utilizing Synopsys® VC Verification IPs [Read more]
  - Develop compliance test cases based on USB4CV Compliance Test Specification (CTS). [Read more]
    - USB4™ Host Interface Compliance Test Specification
      - Host-to-Host (H2H) Tunneling transfer in Raw mode and Frame mode
      - End-to-End Flow Control
      - Multiple H2H Tunneling Paths (up to 20 paths operate concurrently)
    - USB4™ Logical Layer Compliance Test Specification for Router Assemblies
      - Lane Initialization including Phases and Lane Adapter States
      - Entry and Exit of Low Power States including CL2, CL1, and CL0s
      - Operation with Re-timers placed on a Link (up to six Re-timers)
    - USB4™ Protocol Compliance Test Specification
      - The Header Error Control (HEC) and the Error Correction Code (ECC) in a Transport Layer Packet
      - Several Flow Control (FC) schemes including Dedicated FC and Shared FC
      - Path Configuration including setup and teardown
  - Enhance Bus Functional Models (BFMs) that are co-worked with the RTL designs
    - The BFM for controlling the Sideband Channel
    - The BFM for accessing the Host Interface Adapter Layer's programming interface
  - Improve coverage rate via developing several test vectors that are not included in the USB4CV CTS
  - Develop test cases for profiling H2H performance as well as analyze potential bottlenecks

Verification IP (VIP) Engineer (RDSS)[1]
Upper Layer Group of PCIe VIP Team
Avery Design Systems, Inc., Taipei City, Taiwan[2]
Jul. 2021 - Apr. 2023

- PCI Express® (PCIe®) 6.0 [Read more]
  - Enhance the Bus Functional Model (BFM) to support Flit mode.
    - Flit_Marker mechanism
    - Flit Ack, Nak, and Discard Rules
    - Flit Replay Rules (especially the Selective Replay)
  - Enhance / Develop compliance test cases for Flit mode.
    - 14-Bit Tag mechanism
    - Orthogonal Header Content (OHC) of Transaction Layer Packets
    - Shared Flow Control with extended virtual channels
- Streaming Fabric Interface (SFI), Revision 1.0 [Read more]
  - Design the architecture of the BFM.
  - Lead the schedule of the product development.

[1] RDSS stands for Research and Development Substitute Services.
[2] Siemens Digital Industries Software acquired Avery Design Systems, Inc. in March 2023. [Read more]

  - Develop the functionality to align with the latest specification.
- Resolved **350+** issues while supporting customers on the bug tracking system (Bugzilla)
  - **67.33%** Customer Issues / **27.56%** Product Enhancements
- Contributed **13k+** lines of SystemVerilog code on the Concurrent Versions System (CVS, Linux)
  - **16.07%** PCIe BFM / **25.96%** SFI BFM / **57.97%** Test cases

Research Assistant
ELSA Laboratory
National Tsing Hua University, Hsinchu City, Taiwan
Feb. 2016 - Jun. 2021

- Research Interests
  - Design Automation for Quantum Computing [1]
  - Artificial Intelligence and Machine Learning [2], [3]
  - Evolutionary Learning and Optimization [2]
- Linux System Administration
  - Customization of Development Environments
  - Maintenance of Computational Servers
  - Construction of IT Infrastructure

EDUCATION

National Tsing Hua University, Hsinchu City, Taiwan

Advisor: Prof. Chun-Yi Lee

- M.S. in Computer Science – *Jun. 2021*
  - **Master's Thesis**: *Mapping Nearest Neighbor Compliant Quantum Circuits onto a 2-D Hexagonal Architecture* [Read more]
- B.S. in Interdisciplinary Program of Science – *Jun. 2017*
  - Double expertise in *Computer Science* and *Chemistry*

PUBLICATIONS

(* denotes the communication author)

[1] **K.-Y. Chang*** and C.-Y. Lee, "Mapping Nearest Neighbor Compliant Quantum Circuits onto a 2-D Hexagonal Architecture," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**)*, vol. 41, no. 10, pp. 3373–3386, Oct. 2022. DOI: 10.1109/TCAD.2021.3127868.

[2] Y.-H. Chang, **K.-Y. Chang**, H. Kuo, and C.-Y. Lee*, "Reusability and Transferability of Macro Actions for Reinforcement Learning," *ACM Transactions on Evolutionary Learning and Optimization (**TELO**)*, vol. 2, no. 1, Apr. 2022. DOI: 10.1145/3514260.

[3] Y.-M. Chen, **K.-Y. Chang**, C. Liu, T.-C. Hsiao, Z.-W. Hong, and C.-Y. Lee*, "Composing Synergistic Macro Actions for Reinforcement Learning Agents," *IEEE Transactions on Neural Networks and Learning Systems (**TNNLS**)*, vol. 35, no. 5, pp. 7251–7258, May 2024. DOI: 10.1109/TNNLS.2022.3213606.