

# KUAN-YU CHANG

## DESIGN VERIFICATION ENGINEER

ASMedia Technology Inc.  
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## PROFESSIONAL EXPERIENCES

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### Design Verification Engineer

Logic Design Department II, Research and Development Center  
ASMedia Technology Inc., Taiwan  
Jul. 2023 - present



- Universal Serial Bus 4 (USB4<sup>®</sup>), Version 1.0 [Read more]
  - Perform the design verification utilizing Synopsys<sup>®</sup> VC Verification IPs [Read more]
  - Develop compliance test cases based on USB4CV Compliance Test Specifications. [Read more]
    - \* USB4<sup>™</sup> Host Interface Compliance Test Specification Revision 1.9
      - Host-to-Host Tunneling transfer in Raw mode and Frame mode
      - End-to-End Flow Control
      - Multiple Host-to-Host Paths (up to 20 paths operate concurrently)
    - \* USB4<sup>™</sup> Logical Layer Compliance Test Specification for Router Assemblies Revision 1.10
      - Lane Initialization including Phases and Lane Adapter States
      - Entry and Exit of Low Power States including CL2, CL1, CL0s
    - \* Reproduce design issues reported by Customer feedback
  - Enhance Bus Functional Models (BFMs) that are co-worked with the RTL design
    - \* The BFM for controlling the Sideband Channel
    - \* The BFM for accessing the Host Interface Adapter Layer's programming interface

### Verification IP (VIP) Engineer (RDSS)<sup>1</sup>

Upper Layer Group of PCIe VIP Team  
Avery Design Systems, Inc., Taiwan<sup>2</sup>  
Jul. 2021 - Apr. 2023



- PCI Express<sup>®</sup> (PCIe<sup>®</sup>) 6.0 [Read more]
  - Enhance the Bus Functional Model (BFM) to support Flit mode.
    - \* Flit Marker mechanism
    - \* Flit Ack, Nak, and Discard Rules
    - \* Flit Replay Rules (especially the Selective Replay)
  - Enhance / Develop compliance test cases for Flit mode.
    - \* 14-Bit Tag mechanism
    - \* Orthogonal Header Content (OHC) of Transaction Layer Packets
    - \* Shared Flow Control with extended virtual channels
- Streaming Fabric Interface (SFI), Revision 1.0 [Read more]
  - Design the architecture of the BFM.
  - Lead the schedule of the product development.
  - Develop the functionality to align with the latest specification.
- Resolved **350+** issues while supporting customers on the bug tracking system (Bugzilla)
  - **67.33%** Customer Issues / **27.56%** Product Enhancements
- Contributed **13k+** lines of SystemVerilog code on the Concurrent Versions System (CVS, Linux)
  - **16.07%** PCIe BFM / **25.96%** SFI BFM / **57.97%** Test cases

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<sup>1</sup>RDSS stands for Research and Development Substitute Services.

<sup>2</sup>Siemens Digital Industries Software acquired Avery Design Systems, Inc. in March 2023. [Read more]

## EDUCATION

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National Tsing Hua University, Hsinchu, Taiwan

Advisor: Prof. Chun-Yi Lee



- M.S. in Computer Science – Jun. 2021
  - **Master's Thesis:** *Mapping Nearest Neighbor Compliant Quantum Circuits onto a 2-D Hexagonal Architecture* [NDLTD]
- B.S. in Interdisciplinary Program of Science – Jun. 2017
  - Double expertise in *Computer Science* and *Chemistry*

## PUBLICATIONS

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(\* denotes the communication author)

- [1] **K.-Y. Chang\*** and C.-Y. Lee, "Mapping Nearest Neighbor Compliant Quantum Circuits onto a 2-D Hexagonal Architecture," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, no. 10, pp. 3373–3386, Oct. 2022, ISSN: 1937-4151. DOI: 10.1109/TCAD.2021.3127868.
- [2] Y.-H. Chang, **K.-Y. Chang**, H. Kuo, and C.-Y. Lee\*, "Reusability and Transferability of Macro Actions for Reinforcement Learning," *ACM Transactions on Evolutionary Learning and Optimization (TELO)*, vol. 2, no. 1, Apr. 2022, ISSN: 2688-299X. DOI: 10.1145/3514260.
- [3] Y.-M. Chen, **K.-Y. Chang**, C. Liu, T.-C. Hsiao, Z.-W. Hong, and C.-Y. Lee\*, "Composing Synergistic Macro Actions for Reinforcement Learning Agents," *IEEE Transactions on Neural Networks and Learning Systems (TNNLS)*, vol. 35, no. 5, pp. 7251–7258, May 2024. DOI: 10.1109/TNNLS.2022.3213606.