Low-Noise, Low-Power Biomedical Signal Amplifier Circuit

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***Abstract*—With the advent of huge market prospects in bio-signal recording applications, the analog circuit designs for biomedical signals have to meet the requirements of low-power, low-noise and low-frequency operations. For the specific signal sensing and amplification target, the desired CMOS amplifiers should be able to amplify the low amplitude signals generated at hundreds of micron-hertz-to-hertz range level. In this paper, a bio-amplifier analog circuit is implemented and simulated built with the standard 45nm CMOS technology, in which all the transistors operating at the weak inversion or saturation regions. Basically, we completed the ac and noise theoretical analysis, considered the design trade-off between the noise and power performance, then decided the dimension parameters. Based on this circuit implementation, we did simulation on both the schematic and extracted layout models, and demonstrated the results including the response curves and other measured performance parameters. In experiments, the 2.2 V supplied amplifier realizes 43.2 dB gain with differential input signals ranging from 10 μHz to 1.38 kHz, an input-referred noise of 4.56 μV_{rms} level and 88 μW power consumption.**

***Index Terms*—Analog integrated circuits, Bio-signal amplifier, Low-power, low-noise and low-frequency circuit, Subthreshold region transistors.**

I. Introduction

With the rapid development in Microelectromechanical systems (MEMS) technology in recent decades, the bio-signal acquisition system, which can continuously monitor the patient's physical condition and provide real-time feedback during surgery, can be applied to various clinic areas such as Alzheimer's Disease (AD), Parkinson's Disease (PD) and Amyotrophic Lateral Sclerosis (ALS). This type of technology will make the diseases diagnosis and treatment easier and greatly promote the development of medicine. In these applications, the biomedical signals can be categorized into many different types according to where they are detected, the different amplitude and bandwidth they have. Some typical biomedical signals and their parameters are shown in Table I. The biomedical signals need to be amplified first before going through other process like analog-to-digital converter (ADC), analog multiplexer (MUX), then transmitted wireless to external equipment for further analysis to compose a complete bio-signal recording system [1].

The extremely low amplitude and frequencies as well as the special application areas brings us many challenges need to be solved. In order to detect these biomedical signals in muscles, heart or extremely micro nerves, the whole system must be quite small, which means the power that can be delivered to it will be greatly restricted. Furthermore, because the biomedical sensing system needs to have direct contact with human tissues for a long time period (approximately five years for replacing the system needs a surgery, which is costly as well as risky) during they are implanted inside, the power dissipated by it should be low enough to protect surrounding tissues from the harm of high temperature. This application field promotes the development of ultra low power consumption bio-signal acquisition systems. Besides, there is a large DC current offset in the contact surfaces, which has the typical value of 1$\sim$2V. We need to take all these limitations into consideration and carefully design a circuit to amplify the biomedical signals while achieving high gain level, low power consumption, low noise level, small chip area, proper working frequency range and high reliability.

TABLE I
Typical Biomedical Signals

Biomedical Signals	Organ	Amplitude(mV)	Bandwidth(Hz)
Electroencephalographic (EEG)	Brain	0.001 to 0.3	0.5 to 100
Electrocorticographic (ECoG)	Brain	Below 0.1	0.5 to 100
Local Field Potential (LFP) [2]	Brain	Below 5	Below 1
Electrocardiogram (ECG)	Heart	0.5 to 4	0.01 to 250
Electromyography (EMG)	Muscle	0.1 to 5	Up to 500

Jesús Ruiz-Amaya [3] shows us the structure diagram of the bio-signal recording system in Fig.1. First, the bio-signals will be detected in many electrodes, amplified and conditioned. Then extract salient information inside to lower the data rate. Finally the bio-signal will be send through antennas. The power consumption of each amplifier in multiple electrode channel will be monitored and constrained.

This project aims at building low-noise, low-power amplifier for the biomedical signals, and achieves desired function and performance including gain, noise level and power consumption. We decided the dimensions of all the transistors and properly supplied the bias current and voltage to make sure all transistors operating in subthreshold or saturation regions. These huge size input-stage transistors leveraged in this circuit can further lower the flicker noise level as well as obtain higher

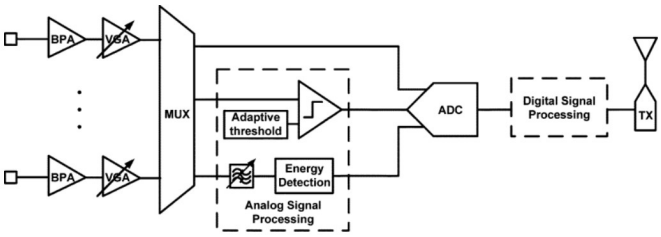

Fig. 1. A generic block diagram for a biopotential-recording system from [3].

gain, which also requires the usage of parallel PMOSs to optimize the compact layout drawing. In the end, the amplifier circuit realizes 43.2dB gain with bandwidth of 1.38 kHz range targeting amplification of the low-frequency bio-signals.

This paper writing is structured as follows: in Section II, we briefly introduced target applications and related works, then we discussed about the subthreshold conduction and small signal analysis as design modeling in Section III, and demonstrated the simulation spectrum and measured parameters for our implementation in Section IV, presented the layout extraction and implementation conclusions in Section V, VI.

II. Related Works

A. Low Noise Amplifier (LNA)

Many efforts have been made trying to achieve the low-noise amplification goal and optimize previous work to get better gain performance. In general, there are three different typical topologies of the low noise amplifier, which referring to the Capacitive Feedback Network (CFN), Miller Integrator Feedback Network (MIFN) and Capacitive Amplifier Feedback Network (CAFN), as demonstrated in [4]. Reid R. Harrison [1] adopted the Capacitive Feedback Network (CFN). The MOS-bipolar devices acting as pseudo resistors and large gate area PMOS transistors acting as input devices can minimize the negative impact of the flicker noise ($\frac{1}{f}$ noise). The 1000-channel amplifier experiment result achieves 2.2Vrms input-referred noise over 7.2kHz bandwidth with power dissipated only 80W and can be arrayed in $13\times13mm^2$ silicon die using 1.5m process technology. Benoit Gosselin [5] added an active inverting Miller integrator in the feedback path of a low noise amplifier to remove the DC current offset. The integration time is long enough to suppress low frequency signals, which is realized by high resistance near the origin of the MOS-bipolar device. Wei Zhao [6] put in a differentiator, which can remove DC current offset, and close-loop amplifier, which enables stable gain in the bandwidth. This new proposed low noise amplifier only needs small capacitors, thus the area can be greatly reduced. Woradorn Wattanapanitch [7] proposed using a bandpass filter after the gain stage. It becomes configurable to adjust for different types of bio-signals. It is realized by changing the bias current, thus the output bandwidth can be changed accordingly.

B. Operational Transconductance Amplifier (OTA)

Woradorn Wattanapanitch [7] modified the standard folded-cascode topology by biasing the OTA, which results in a great reduction in current going through $M_1 \sim M_{12}$, thus the noise generated by them is largely decreased and can be ignored. This modification lowers the current and the input-referred noise inside of OTA. The noise efficiency factor (NEF) becomes much closer to the theoretical limit. The experiment shows that it can achieve 40.9dB gain in 392 mHz$\sim$295Hz with total current only 743 nA. However, the use of the source-degeneration resistor makes the area still $0.16mm^2$ even using 0.5m process technology and increases the supply voltage from 2.5V to 2.8V. Fan Zhang [3] combined the salient features of the closed-loop fully-differential telescopic amplifier (BPA1) and the open-loop single-ended complementary-input amplifier (BPA2) to propose a closed-loop complementary-input amplifier (BPA3). With the use of the power-efficient complementary-input topology in BPA2 and BPA3, they have better performance in power noise reduction.

By analyzing the properties of MOSFET devices, Bulk-Driven (BD) is another commonly used way to operate transistors in the subthreshold region for low power supply with a higher open loop gain, as the typical 0.6V-supply design Fig.2 with 70dB gain demonstrated in [8]. Michael Trakimas and Sammeer Sonkusale [9] also followed this direction to give a two-stage pseudo-differential 65dB gain OTA with improved bulk-mode common-mode feedback (CMFB) circuit, whose self cascode load structure and partial positive feedback give larger signal swing. Another low power amplifier design operating at 1V from [10] used the technique of current driven bulk (CDB) to reduce the threshold voltages of input transistors, which has the performance of 71dB gain and 100dB CMRR. The CDB technique forces a constant current through the transistor bulk terminal, which is analyzed in the project of [11] in 2001. With this method, the researchers tried to bias the bulk as high as possible and alter the voltage of V_{BS}, leading to the possible solution to the conventional dead zone problem. In addition, the 0.6V-supply design in [12] also utilized the mentioned bulk-driven method, and achieved the performance of a voltage gain higher than 60dB as well as 150db CMRR, which is a suitable OTA filter for the analog front-ends in wearable devices and bio-sensing.

In the paper [13], the low power 0.65V AMP designed for implantable biomedical application utilized both the native and normal NMOS differential pairs. At the input stage, the native NMOS without using extra masks has the channel formed even with V_{GS} equaling to zero. Hence, the differential stage is still functional for the inputs with a low V_{CM}, which can work with normal pairs for both low and high input conditions. In the proposed work [14] for biomedical signal applications, the researchers designed the OPAMP based on gate-driven MOSFET's technique in which the PMOS transistors are working in the weak-inversion region with higher trans-conductance leading to larger gain. The OTA design has a stack of 3 transistors compared to the conventional 4 stacked transistors

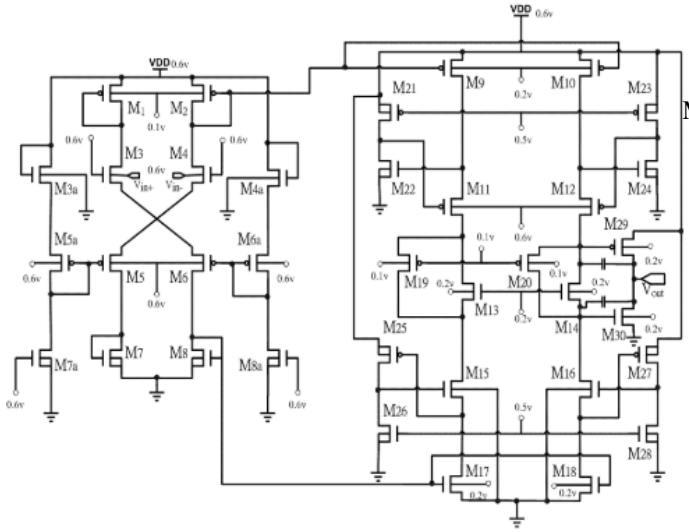

Fig. 2. Schematic of Bulk-Driven (BD) OTA implemented in neural amplifier from [8].

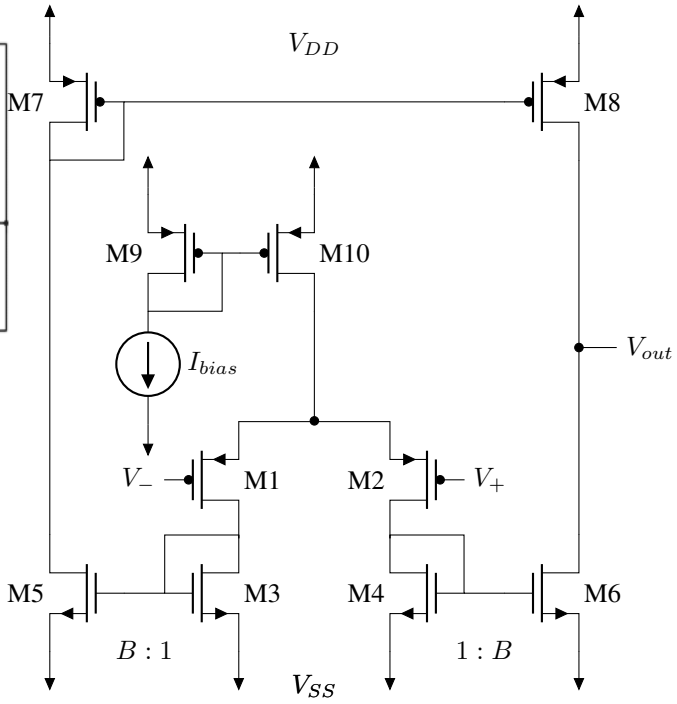

Fig. 3. Schematic of OTA utilized in our amplifier

configuration to obtain a larger output swing. Besides, for a smaller design area overhead, the researchers in [5] argued that active low-frequency suppression techniques can eliminate the need of RC networks or large size feedback capacitors to filter out the unwanted low-frequency contents. Instead, it leveraged two micro-power OTAs including one current mirror OTA and a 2-stage OTA with lead-compensation. The experiments on the final design showed a midband gain of 50dB and input-referred noise of $5.6\mu V_{rms}$.

III. Design Modeling

A. Sub-threshold Conduction

Subthreshold conduction refers to the current through the source and drain of a MOSFET lying in subthreshold region or named weak-inversion region. To operate in this region, the gate-source voltage has to satisfy:

$$V_{GS} \leq V_T + n\frac{kT}{q} \tag{1}$$

In digital design, this subthreshold leakage current is often ideally assumed as zero and the transistor can be considered as cut-off. However, the leakage current follows the equation 2 which is related to the size ratio and gate-source voltage. The subthrehold region conduction has the advantage of saving more power, so it is considered as an efficient operating region and commonly utilized in low power analog circuit design.

$$I_D = \frac{W}{L} I_{D0} \exp(\frac{V_{GS}}{n\frac{kT}{q}}) \tag{2}$$

The factor n depends on the specific CMOS technology, which is usually between 1 and 3. Unlike the normally used transistors operating in the strong inversion region, the subthreshold region transistors have shortages in the speed, accuracy performance and noise response level. However, the energy efficiency is greatly improved while the implementation can still meet the performance requirements. Hence, the largest M_1 and M_2 transistors working at subthreshold region are decided to be utilized in our lower power and frequency design for biomedical applications.

TABLE II
Transistor Dimensions

Device	$W/L(\mu m)$	Region
M1, M2	800/2.5	3
M3, M4	0.375/25	2
M5, M6	1.5/25	2
M7, M8	2.5/20	2
M9, M10	10/10	2

B. Low-Noise Low-Power OTA Design

The Fig.3 shows the schematic of the 2-stage current-mirror OTA utilized in the Electroencephalogram (EEG) signal applications, in which the $8\mu A$ bias current enables the transistors to operate in weak, moderate, or strong inversion regions according to their W/L ratio. This typology achieves larger gain bandwidth, trans-conductance and output impedance with even lower power consumption compared to the traditional OTA design. In order to be symmetric to form the current mirror, the conditions of $M_1 = M_2$, $M_3 = M_4$, $M_5 = M_6$, $M_7 = M_8$, $M_9 = M_{10}$ have to be satisfied. These four pairs of current mirror are used to deliver bias current to each branch and act as active load with each other. The dimensions of transistors is shown in Table II, where the Region 2 means Saturation Region and Region 3 means Sub-threshold Region. The input stage is consist of M_1 and M_2 with differential

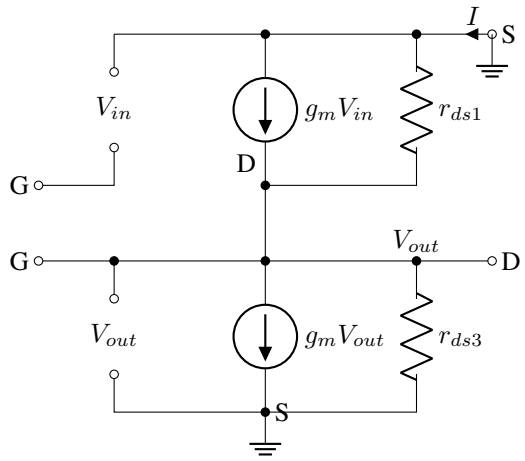

Fig. 4. Small Signal Model for Stage 1 Analysis

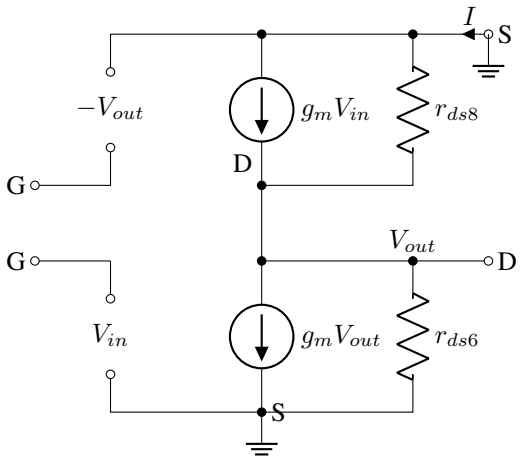

Fig. 5. Small Signal Model for Stage 2 Analysis

structure. M_1, M_2, M_3 and M_4 act as the first stage while M_5, M_6, M_7 and M_8 act as the second stage.

The Flicker noise or called $\frac{1}{f}$ noise is another major concern for a low-noise low-frequency circuit design, which can be eliminated by utilizing large gate area PMOS transistors as input devices. The reason for this consideration is the property of flicker noise is much lower in PMOS than in NMOS, also is inversely proportional to the gate area.

The transconductance is

$$G_m = Bg_{m1} \tag{3}$$

where $B = \frac{(W/L)_6}{(W/L)_4}$

The gain is

$$A_V = G_m r_0 = g_{m1} B r_o = g_{m1} B(r_{ds6} // r_{ds8}) \tag{4}$$

The bandwidth is

$$BW = \frac{1}{2\pi r_o C_L} \tag{5}$$

The gain-bandwidth product is

$$GBW = A_V BW = \frac{G_m}{2\pi C_L} \tag{6}$$

The slew rate is

$$SR = K\frac{I_{bias}}{C_L} \tag{7}$$

C. Small Signal Analysis

1) Stage 1: The small signal circuit for Stage 1 is shown in Fig.4. According to Kirchhoff's Current Law (KCL):

$$\begin{cases} g_{m1}V_{in} + g_{ds1}V_{out} - I = 0 \\ g_{ds3}V_{out} + g_{m3}V_{out} - I = 0 \end{cases} \tag{8}$$

$$\begin{aligned} A &= \frac{V_{out}}{V_{in}} \\ &= \frac{g_{m1}}{g_{m3} + g_{ds3} - g_{ds1}} \\ &\approx \frac{g_{m1}}{g_{m3}} \end{aligned} \tag{9}$$

2) Stage 2: The small signal circuit for Stage 2 is shown in Fig.5. According to Kirchhoff's Current Law (KCL):

$$\begin{cases} -g_{m8}V_{out} + g_{ds8}V_{out} - I = 0 \\ g_{m6}V_{in} + g_{ds6}V_{out} - I = 0 \end{cases} \tag{10}$$

$$\begin{aligned} A &= \frac{V_{out}}{V_{in}} \\ &= -\frac{g_{m6}}{g_{m8} + g_{ds6} - g_{ds8}} \\ &\approx -\frac{g_{m6}}{g_{m8}} \end{aligned} \tag{11}$$

IV. Implementation and Simulation Results

A. AC Analysis

As demonstrated in Fig.6, the amplifier design achieves the midband gain at 43.2dB level with 1.38kHz bandwidth, simulated in the Cadence Analogue design environment. In our design, the load capacitor C_L is set to 3.2 pF to limit the bandwidth and the phase margin is around 48 degree level. The value of phase margin is calculated at the point while the gain of amplifier is at 0 dB, based on the difference between phase lag and -180 degree. Phase margin should be in the range of 30 to 60 and a higher value means a slower and more stable amplifier.

B. Transient Analysis

The transient response and sampling input signals are shown in Fig.7. The bottom two red curves are differential input signals whose amplitudes are 100 μV and frequencies are 1 Hz with 180 degree difference. The output signal swing of the amplifier shows 30 mV. It confirms the effective function of

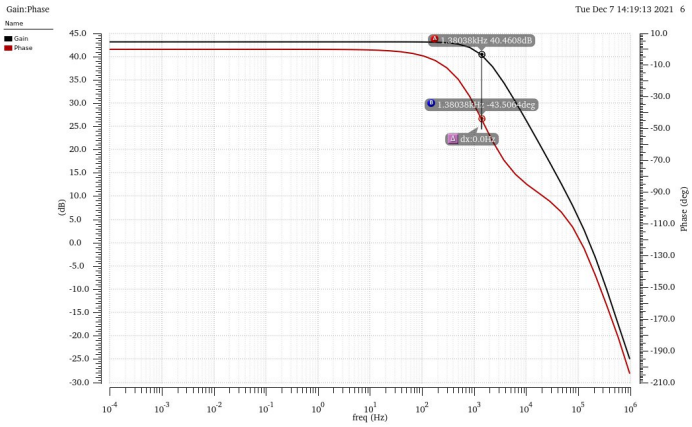

Fig. 6. Gain and Phase of OTA Design

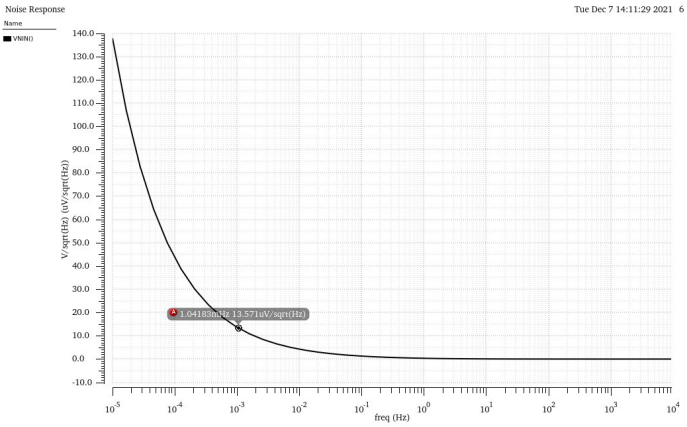

Fig. 8. Input Referred Noise Result

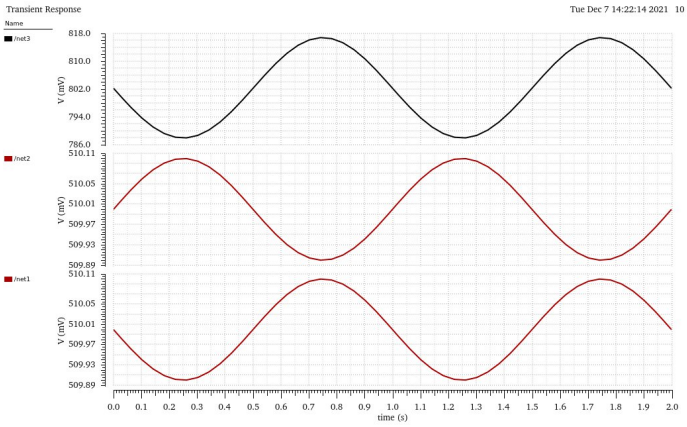

Fig. 7. Transient Response of 100 μV Differential Inputs

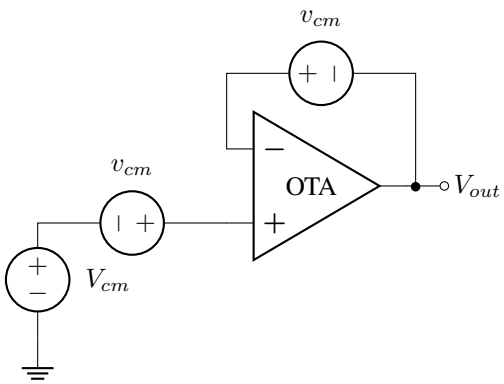

Fig. 9. CMRR Testing Circuit

signal amplification to the 100 μV without significant signal distortion.

C. Noise Analysis

Fig.8 shows the measured input-referred voltage noise spectrum. The thermal noise level is at 120 $nV/\sqrt{Hz}$ while the flicker noise corner occurs at 0.1 mHz. And the integration under this measurement curve at the range of 10μHz to 1.5kHz yields an rms voltage of 4.56 μV_{rms}. The noise response level is acceptable for the low noise circuit design aiming at processing signals at hundreds of micron-volts. Another point worth mentioning is, the 45nm technology library can not simulate the noise very well and the actual flicker noise corner should be at higher frequency in real implementation.

D. Common Mode Rejection Ratio (CMRR)

We leveraged the testing circuit in Fig.9 to obtain the CMRR value, which is a metric to quantify the rejection to the common-mode signals in a differential amplifier. The testing circuit is implemented as negative feedback with unity gain, which provides ac small signal to both noninverting and inverting input nodes and one common mode voltage to the noninverting input. Then we measured the CMRR value of our design as 32.92 dB.

E. Power Supply Rejection Ratio (PSRR)

The testing circuit in Fig.10 is utilized in obtaining the PSRR value, which is a metric to describe the capability of the amplifier to suppress the power supply variations. Similar to the CMRR testing circuit, ac small signal is added to the supply voltage and common mode voltage is added to the noninverting input. We obtained the PSRR value from simulation as 40.27 dB.

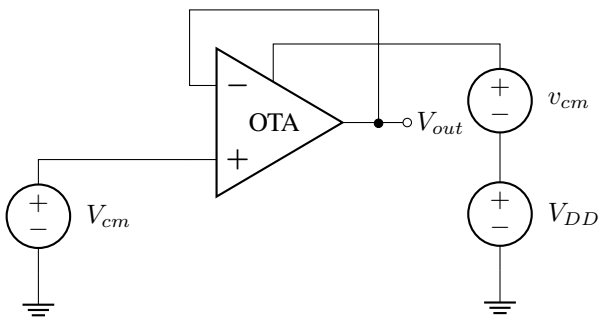

Fig. 10. PSRR Testing Circuit

TABLE III
SIMULATION RESULTS AND COMPARISON OF THE REFERENCE DESIGN

Parameter	This Work	Reference [1]	Reference [15]
Supply Voltage	2.2V	$\pm 2.5V$	$\pm 0.6V$
Supply Current	8 μ A	16 μ A	2 μ A
Gain	43.2dB	40dB	75.47dB
Bandwidth	1.38kHz	9kHz	18.8kHz
Output Noise	4.56 μV_{rms}	2.1 μV_{rms}	$0.91nV^2/Hz$(1mHz)
Power Consumption	88 μW	80 μW	1.24 μW
Technology	45 nm CMOS	1.5 μm CMOS	0.13 μm CMOS

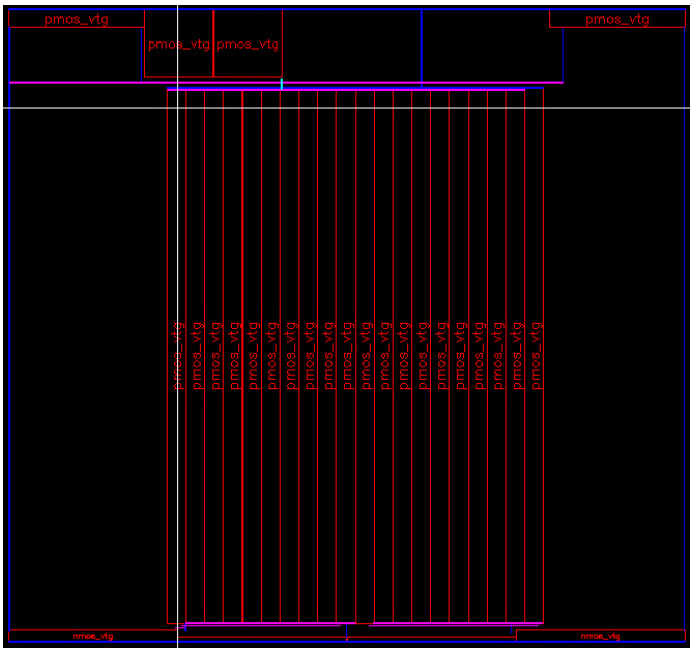

Fig. 11. Layout of OTA implemented for EEG amplifier

F. Reference Results Analysis

With the experimental results in [1] and [15], the fully integrated amplifier designs are compared in Table III. As the fabrication technology improved, the circuit performance is enhanced especially in much lower power consumption. As shown in this table, the proposed design achieved comparable performance to the published works, and realized acceptable performance in terms of input-referred noise level, energy consumption, and midband gain for the target applications.

V. LAYOUT AND EXPERIMENTAL RESULTS

The layout in Fig.11 is drawn using the 45nm CMOS technology library, which has passed the DRC (Design Rule Check, Fig.12) and LVS (Layout Versus Schematic, Fig.13) checks. Because of the size constrains on the transistors in the library, the width of PMOS cannot scale up to 100 μm and we have to use multiplier of 10 PMOS transistors in parallel as one single wide transistor in layout drawing. Wide transistors can provide better gain and noise response level, so we have to consider the trade-off between performance and chip area under low power supply. However, our layout drawing is not very compact and waste many spaces, which needs further optimization. The Table IV shows the measured parameters from layout simulation, including the CMRR, PSRR, chip area, slew rate, and energy consumption. The slew rate represents how fast the amplifier is and how fast the output signal changes. However, the bio-signals are often at really low frequencies and low amplitudes. The parameter should not be our main design concern in this design.

TABLE IV
SIMULATION RESULTS

Parameter	Simulation
Supply Voltage	2.2V
Supply Current	8uA
Gain	43.2dB
Bandwidth	1.38kHz
Input-referred noise	4.56 μV_{rms}
Slew Rate	6.45 $V/\mu s$
CMRR(10uHz$\sim$1.5kHz)	32.92dB
PSRR(10uHz$\sim$1.5kHz)	40.27dB
Power Consumption	88 μW
Area	0.01 mm^2

VI. CONCLUSION

The analog bio-amplifier proposed in this paper achieved mid-band 43.2dB gain to the differential input signals with 1.38kHz bandwidth. From the measured parameters, the basic amplification function and desired low-noise, low-power performance are achieved for the target signal sensing applications. However, the supply voltage should be reduced to 1.1 V to avoid the transistor aging in real implementation using 45nm technology, and more accurate noise simulation should be modeled.

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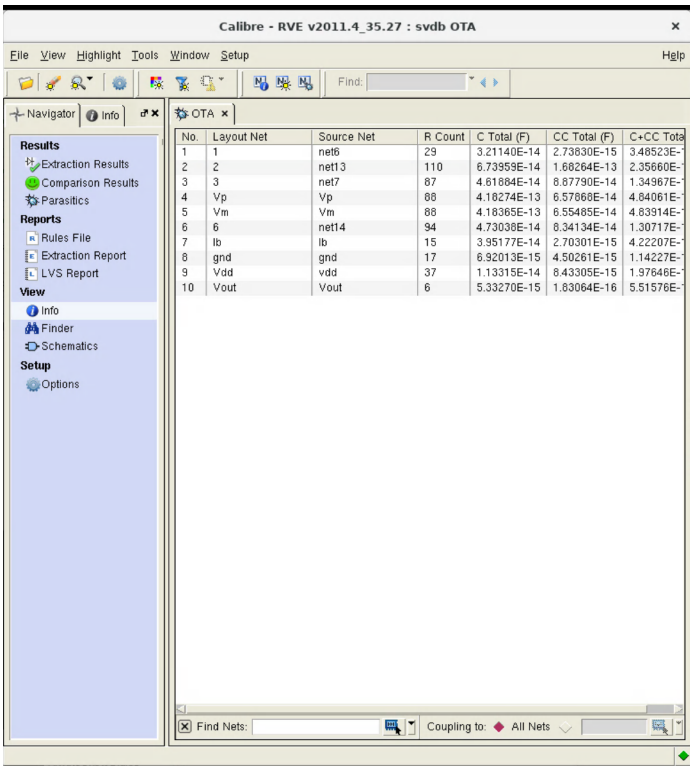

Fig. 12. DRC report

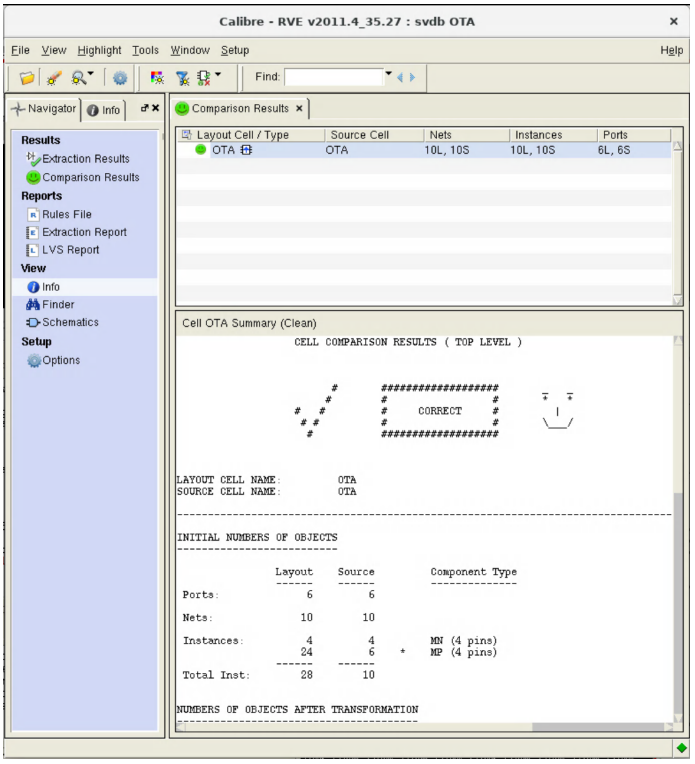

Fig. 13. LVS report