Biomedical Sensing Circuit

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1 Introduction

With the rapid development in micro electromechanical (MEMS) technology in recent decades, the bio-signal acquisition system, which can continuously monitor the patient's physical condition and provide real-time feedback during surgery, can be applied to various clinic areas such as Alzheimer's disease (AD), Parkinson's disease (PD) and Amyotrophic lateral sclerosis (ALS). This kind of technology will make treating the nervous system diseases easier and greatly promote the development of medicine.

Neural related bio-signals can be categorized into many different types according to their own unique amplitude and bandwidth. For example, electroencephalographic (EEG) has an amplitude between 10∼20µV and bandwidth below 100Hz, electrocardiogram (ECG) has an amplitude between 1∼5mV and bandwidth between 0.05∼100Hz, electrocorticographic (ECoG) has an amplitude below 100µV and bandwidth between 0.5∼200Hz, local field potential (LFP) have an amplitude below 5mV and bandwidth below 1Hz, typical action potential or neural spike recorded outside of the cell has an amplitude up to 500µV and bandwidth between 100∼7000Hz, as described in [1]. The amplitude of these bio-signals is too small, for which they need to be amplified first before going through other process like analog-to-digital converter (ADC), analog multiplexer (MUX), then transmitted wireless to external equipment for further analysis to compose a complete bio-signal recording system [2]. In order to detect these biomedical neural signals in extremely micro nerves, the bio-signal acquisition system must be quite small too, which means the power that can be delivered to it will be greatly restricted. Furthermore, because the whole system needs to have direct contact with human tissues for a long time period (approximately five years for replacing the system needs a surgery, which is costly as well as risky) when they are implanted inside, the power dissipated by it should be low enough to protect surrounding tissues from the harm of higher temperature. This application field promotes the development of ultra low power consumption bio-signal acquisition systems. Besides, there is a large DC current offset in the contact surfaces, which has the typical value of 1∼2V. We need to take all these factors into consideration and carefully design a circuit to amplify the bio-signal under all these limitations while achieving low power consumption, low noise level, small chip area, wide working frequency range, high gain level and high reliability.

Jesús Ruiz-Amaya [3] shows us the structure diagram of the bio-signal recording system in Figure 1. First, the bio-signals will be detected in many electrodes, amplified and conditioned. Then extract salient information inside to lower the data rate. Finally the bio-signal will be send through antennas. The power consumption of each amplifier in multiple electrode channel will be monitored and constrained.

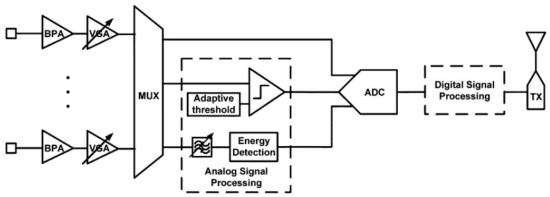

Figure 1: A generic block diagram for a biopotential-recording system from [3].

2 Related Works

2.1 Low Noise Amplifier (LNA)

Many efforts have been made trying to achieve this goal and optimize previous work to get a better performance. There are three different typical topologies of the low noise amplifier, which referring to the Capacitive Feedback Network (CFN), Miller Integrator Feedback Network (MIFN) and Capacitive Amplifier Feedback Network (CAFN), as demonstrated in [4]. Reid R. Harrison [2] adopted the Capacitive Feedback Network (CFN). The MOS-bipolar devices acting as pseudo resistors and large gate area PMOS transistors acting as input devices can minimize the negative impact of the flicker noise ($\frac{1}{f}$ noise). The 1000-channel amplifier experiment result achieves 2.2µVrms input-referred noise over 7.2kHz bandwidth with power dissipated only 80µW and can be arrayed in 13*13mm silicon die using 1.5µm process technology. Benoit Gosselin [5] added an active inverting Miller integrator in the feedback path of a low noise amplifier to remove the DC current offset. The integration time is long enough to suppress low frequency signals, which is realized by high resistance near the origin of the MOS-bipolar device. Wei Zhao [6] put in a differentiator, which can remove DC current offset, and close-loop amplifier, which enables stable gain in the bandwidth. This new proposed low noise amplifier only needs small capacitors, thus the area can be greatly reduced. Woradorn Wattanapanitch [7] proposed using a bandpass filter after the gain stage. It becomes configurable to adjust for different types of bio-signals. It is realized by changing the bias current, thus the output bandwidth can be changed accordingly.

2.2 Operational Transconductance Amplifier (OTA)

Woradorn Wattanapanitch [7] modified the standard folded-cascode topology by biasing the OTA, which results in a great reduction in current going through $M_1 \sim M_{12}$, thus the noise generated by them is largely decreased and can be ignored. This modification lowers the current and the input-referred noise inside of OTA. The noise efficiency factor (NEF) becomes much closer to the theoretical limit. The experiment shows that it can achieve 40.9dB gain in 392mHz∼295Hz with total current only 743nA. However, the use of the source-degeneration resistor makes the area still $0.16mm^2$ even using 0.5µm process technology and increases the supply voltage from 2.5V to 2.8V. Fan Zhang [3] combined the salient features of the closed-loop fully-differential telescopic amplifier (BPA1) and the open-loop single-ended complementary-input amplifier (BPA2) to propose a closed-loop complementary-input amplifier (BPA3). With the use of the power-efficient complementary-input topology in BPA2 and BPA3, they have better performance in power noise reduction.

By analyzing the properties of MOSFET devices, Bulk-Driven (BD) is another commonly used way to operate transistors in the subthreshold region for low power supply with a higher open loop gain, as the typical 0.6V-supply design Figure 2 with 70dB gain demonstrated in [8]. Michael Trakimas and Sammeer Sonkusale [9] also followed this direction to give a two-stage pseudo-differential 65dB gain OTA with improved bulk-mode common-mode feedback (CMFB) circuit, whose self cascode load structure and partial positive feedback give larger signal swing. Another low power amplifier design operating at 1V from [10] used the technique of current driven bulk (CDB) to reduce the threshold voltages of input transistors, which has the performance of 71dB gain and 100dB CMRR. The CDB technique forces a constant current through the transistor bulk terminal, which is analyzed in the project of [11] in 2001. With this method, the researchers tried to bias the bulk as high as possible and alter the voltage of V_{BS}, leading to the possible solution to the conventional dead zone problem. In addition, the 0.6V-supply design in [12] also utilized the mentioned bulk-driven method, and achieved the performance of a voltage gain higher than 60dB as well as 150db CMRR, which is a suitable OTA filter for the analog front-ends in wearable devices and bio-sensing.

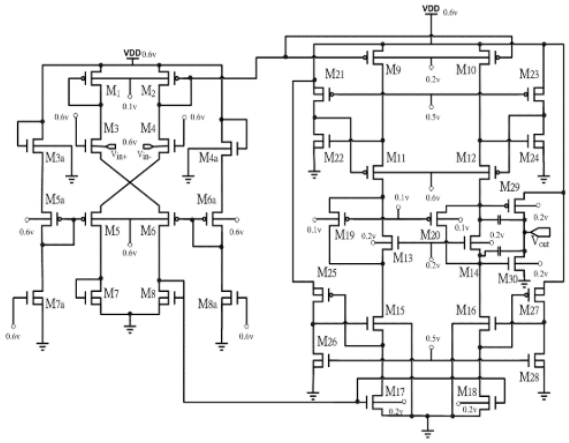

Figure 2: Schematic of Bulk-Driven (BD) OTA implemented in neural amplifier from [8].

In the paper [13], the low power 0.65V AMP designed for implantable biomedical application utilized both the native and normal NMOS differential pairs. At the input stage, the native NMOS without using extra masks has the channel formed even with V_{GS} equaling to zero. Hence, the differential stage is still functional for the inputs with a low V_{CM}, which can work with normal pairs for both low and high input conditions. In the proposed work [14] for biomedical signal applications, the researchers designed the OPAMP based on gate-driven MOSFET's technique in which the PMOS transistors are working in the weak-inversion region with higher trans-conductance leading to larger gain. The OTA design has a stack of 3 transistors compared to the conventional 4 stacked transistors configuration to obtain a larger output swing. Besides, for a smaller design area overhead, the researchers in [5] argued that active low-frequency suppression techniques can eliminate the need of RC networks or large size feedback capacitors to filter out the unwanted low-frequency contents. Instead, it leveraged two micro-power OTAs including one current mirror OTA and a 2-stage OTA with lead-compensation. The experiments on the final design showed a midband gain of 50dB and input-referred noise of 5.6Vrms.

3 Design Modeling

3.1 Schematic of LNA

Figure 3 shows the schematic of the low noise amplifier. Transistors $M_a - M_d$ are MOS-bipolar elements, which are acting as resistors. When $V_{GS} < 0$, all the transistors can be regarded as diode-connected PMOS transistors. When $V_{GS} > 0$, all the transistors can be regarded as bipolar junction transistors (BJT). When the voltage over the transistor is small, the resistance increase pretty fast, which means r_{inc} is extremely large. Because the input voltage may changed rapidly in some points, the voltage over the transistors will be very large. The incremental resistance is lower when in high voltage, thus settle faster in this situation. Taking this factor into account, we use two tandem MOS-bipolar devices to reduce distortion.

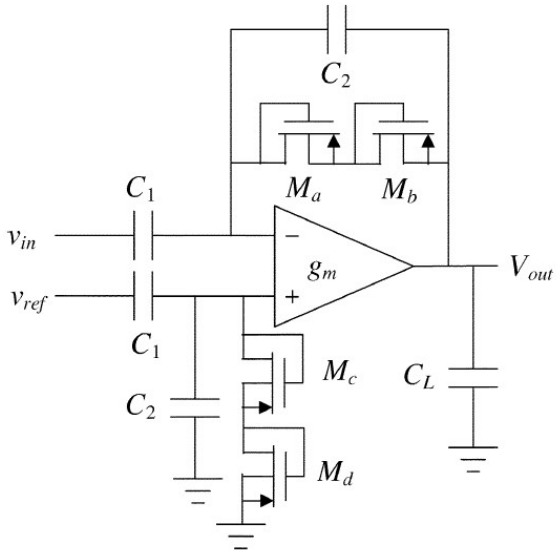

Figure 3: Schematic of neural amplifier in [2].

3.2 Low-Noise Low-Power OTA Design

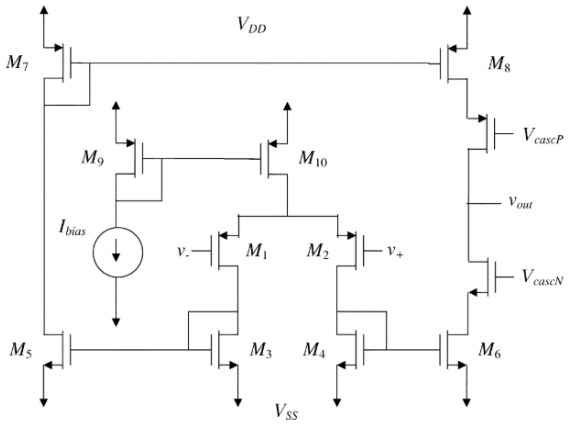

Figure 4: Schematic of current-mirror OTA implemented in neural amplifier in [2].

The Figure 4 from [2] describes the schematic of the current-mirror OTA utilized in the biomedical signal applications, in which the 8µA bias current enables the transistors to operate in weak, moderate, or strong inversion regions according to their W/L ratio. Hence, the modeling analysis focuses on altering the size of transistors, in order to minimize the bioamplifier noise. As described in [2], the inversion coefficient (I_C) parameter for each transistor can be used as the characterization to their operation region, in whose calculation the I_S is the moderate inversion characteristic current and I_D is the drain current.

$$\mathrm{I_C} = \frac{\mathrm{I_D}}{\mathrm{I_S}} \tag{1}$$

$$\mathrm{I_S} = \frac{2\mu \mathrm{C_{ox}} \mathrm{U_T^2}}{\kappa} \cdot \frac{W}{L} \tag{2}$$

In the $\mathrm{I_S}$ computation as Equation 2, the U_T is the thermal voltage and κ is the subthreshold gate coupling coefficient. Then for the low-power circuit design, the transconductance g_m can be estimated by the EKV model using the I_C parameter:

$$\mathrm{g_m} \approx \frac{\kappa \mathrm{I_D}}{\mathrm{U_T}} \cdot \frac{2}{1 + \sqrt{1 + 4 \cdot \mathrm{I_C}}} \tag{3}$$

As demonstrated in the operating point table 5 from [2], the transistors W/L ratio and I_C parameters are decided to operate in the desired region. With the optimal sizing choices of devices, the performance including noise contributions and stability is guaranteed.

Devices	W/L (μm)	I_D (μA)	Inversion Coefficient	g_m/I_D (V^{-1})	V_{EFF} = V_{GS} - V_t (V)
M_1, M_2	800.0/4.0	4.0	0.43	20.6	-0.076
M_3, M_4, M_5, M_6	12.0/44.8	4.0	110	2.5	+0.770
M_7, M_8	6.4/12.8	4.0	171	2.0	+0.960
M_9, M_{10}	20.0/20.0	8.0	171	2.0	+0.960
M_{cascN}	12.0/3.2	4.0	7.8	8.1	+0.200
$M_{casc P}$	6.4/3.2	4.0	43	3.9	+0.481

Figure 5: Operating Point of OTA Transistors for Neural Amplifier

With the aforementioned transistors configurations, the input-referred thermal noise power can be represented as:

$$\overline{\mathrm{v}_{\mathrm{ni,thermal}}^2} = [\frac{16kT}{3\mathrm{g_{m1}}}(1 + 2\frac{g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}})]\Delta f \tag{4}$$

The Flicker noise or called $\frac{1}{f}$ noise is another major concern for a low-noise low-frequency circuit design, which can be eliminated by utilizing large gate area PMOS transistors as input devices. The reason for this consideration is the property of flicker noise is much lower in PMOS than in NMOS, also is inversely proportional to the gate area.

3.3 Noise Efficiency Factor

We want to minimize noise level as well as power consumption, The noise efficiency factor (NEF) is then proposed to describe this tradeoff:

$$\mathrm{NEF} = V_{ni,\mathrm{rms}}\sqrt{\frac{2I_{\mathrm{tot}}}{\pi \cdot U_{\mathrm{T}} \cdot 4kT \cdot \mathrm{BW}}} \tag{5}$$

Where $V_{ni,rms}$ is the input-referred rms noise voltage, I_{tot} is the total amplifier supply current, $UT = \frac{KT}{q}$ is the thermal voltage, BW is the amplifier bandwidth.

Integrate the thermal noise of Equation 4 across the bandwidth BW and assume $g_{m3}, g_{m7} \ll g_{m1}$

$$\mathrm{NEF} = \sqrt{\frac{4I_{\mathrm{tot}}}{3U_{\mathrm{T}}g_{m1}}} = \sqrt{\frac{16}{3U_{\mathrm{T}}}\left(\frac{I_{D1}}{g_{m1}}\right)} \tag{6}$$

where I_{D1} is the drain current through M_1. The goal is to minimize NEF, thus we need to maximize the relative trans-conductance $\frac{g_m}{I_D}$. It can work in deep weak inversion to reach the maximum achievable $\frac{g_m}{I_D}$ of $\frac{\kappa}{U_T}$. We can further maximize $(\frac{W}{L})_1$ to approach the theoretical NEF limit for the Capacitive Feedback Network (CFN) topology low noise amplifier. The typical value of κ is 0.7.

$$\mathrm{NEF} = \sqrt{\frac{4}{\kappa U_{\mathrm{T}}}\left(\frac{I_{D1}}{g_{m1}}\right)} = \sqrt{\frac{4}{\kappa^2}} \approx 2.9 \tag{7}$$

In reality, the NEF will be affected by the $\frac{1}{f}$ noise and parameters of the transistors.

3.4 Reference Results Analysis

From the experimental results in [2] and [15], the fully integrated amplifier designs are compared in table 1. As the fabrication technology improved, the circuit performance is enhanced especially in much lower power consumption.

Table 1: SIMULATION RESULTS AND COMPARISON OF THE REFERENCE DESIGN AMPLIFIER

	Reference [2]	Reference [15]
Supply Voltage	$\pm$ 2.5V	$\pm$ 0.6V
Supply Current	16 μA	2 μA
Gain	39.5dB	75.47dB
Bandwidth	7.2kHz	18.8kHz
Output Noise	2.1 μV_{rms}	$\leq$ 0.91 nV^2/Hz(1mHz)
Power Consumption	80μW	1.24μW
Technology	1.5 μm CMOS	0.13 μm CMOS

4 Project Plan

First, we will work on the OTA schematic and related simulation verification, then report its gain, bandwidth and NEF performance after the layout extraction following the sizes and operating points of transistors in [2]. A more recent project [15] according our literature study shows a comparable gain performance achieved but has much lower power consumption with operations at lower supply voltage. We will try reproduction of their circuit design to compare the simulation results, and further analyze the reasons for the successful optimization.

Next, we will choose the topology of LNA discussed before because the analysis in [4] shows that Capacitive Feedback Network (CFN) achieves the best performance in area and power consumption given the same input-referred noise. After the schematic drawing and layout extraction, the LNA and OTA are combined together to be simulated to test whether the desired function and performance are realized.

Finally, we will compare the simulation results like gain, bandwidth, NEF and other experimental characteristics of our design with the presented reference papers,and give our final layout extraction.

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