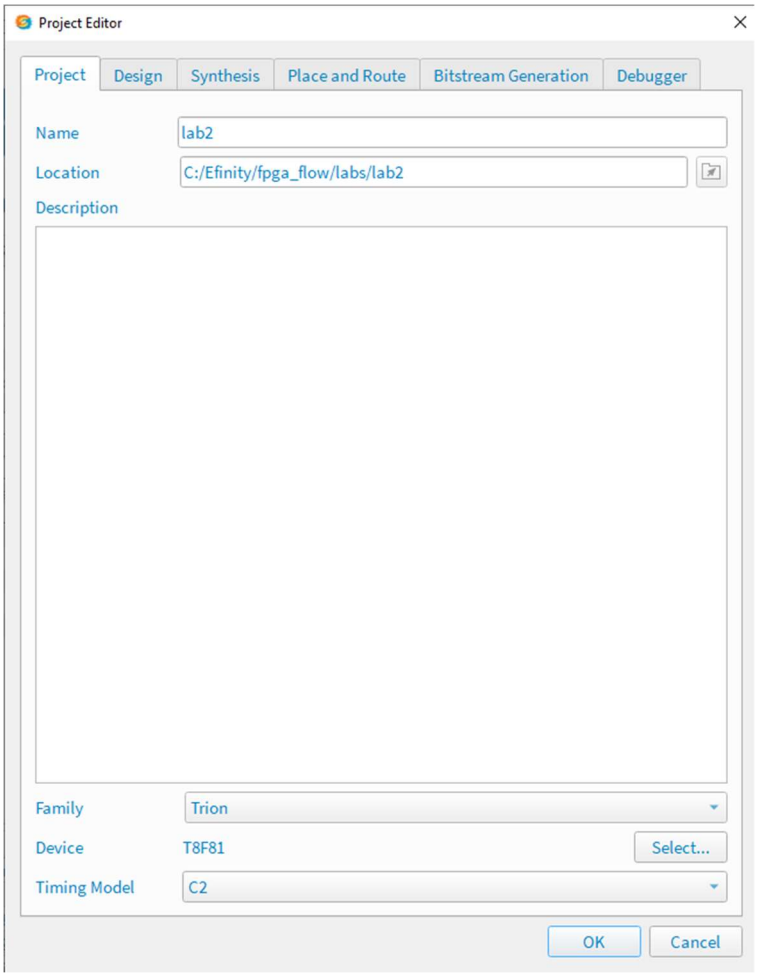
Efinix Design Flow

Steps

Create a Efinity Project

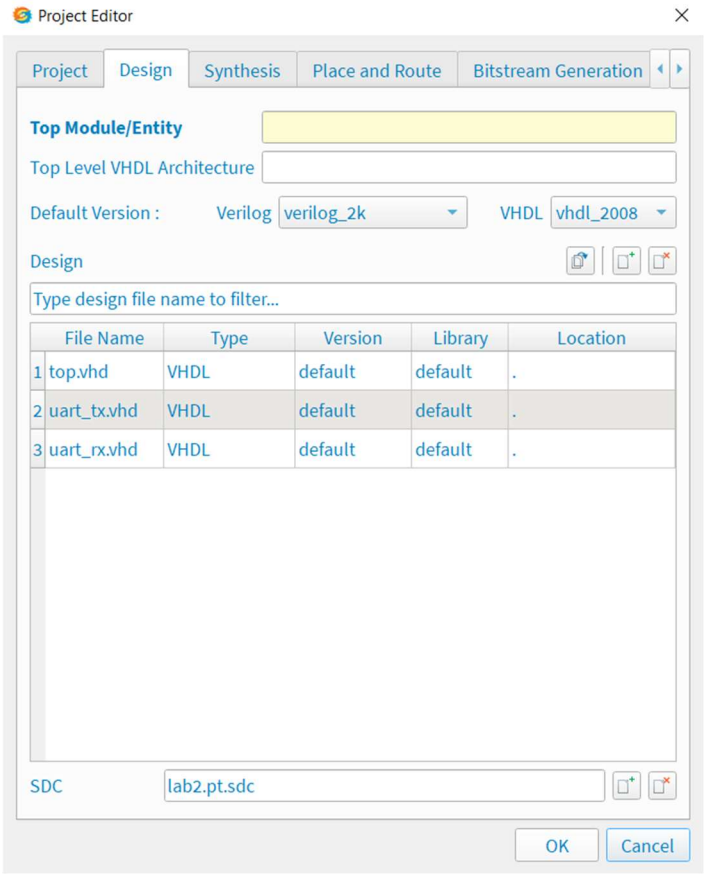
1. Open Efinity by selecting Start > Efinity 2022.1 > Efinity 2022.1.
2. Click File > Create Project… to start the wizard. You will see Project Editor dialog box.
3. Click the Browse button of the *Project location* field of the **New Project** form, browse to **C:/Efinity/fpga_flow/labs/lab2**.
4. Enter lab2 in the Project name field. Make sure that the Family field selected Trion and device field selected the T8F8. Click Design tab.



Project Name and Location entry

5. Enter lab2 in the Top Module/Entity field. Select **vhdl_2008** as the Target Language.

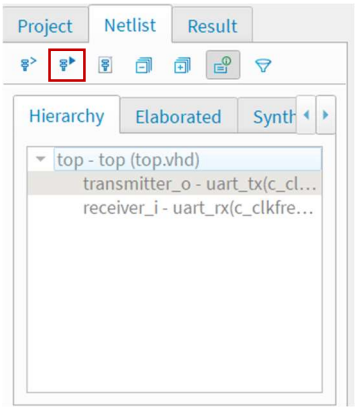
6. Click on the Add design file button and browse to the C:\Efinity\fpga_flow\sources\lab2 directory, select top.vhd, uart_rx.vhd and uart_tx.vhd.
7. Click on the Add SDC file button and browse to the C:\Efinity\fpga_flow\sources\lab2 directory, select lab2.pt.sdc, click **OK**.



Add design and SDC files

Analyze the design source files hierarchy.

1. In the Netlist pane, click the Eleborate all button to analyzing the design source files hierarchy.

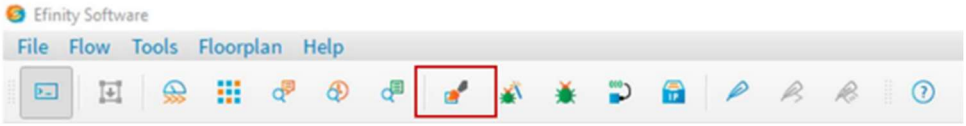


2. Double-click on the top entry to view its content. Notice in the VHDL code, the BAUD_RATE and CLOCK_RATE parameters are defined to be 115200 and 33 MHz respectively as shown in the design diagram. Also notice that the lower level modules are instantiated.

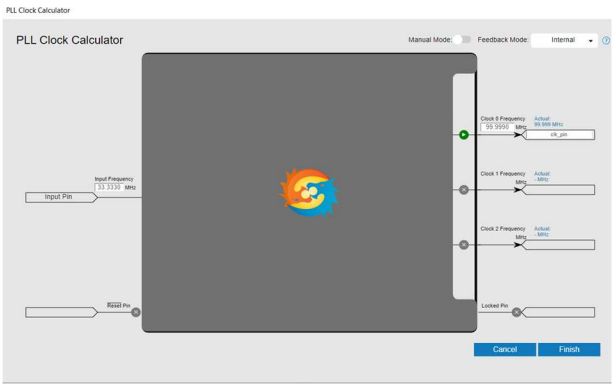
```
entity top is
generic (
c_clkfreq       : integer := 33_333_333;
c_baudrate      : integer := 115_200
);

port (
clk             : in std_logic;
rx_i            : in std_logic;
tx_o            : out std_logic
```

Create the lab2.pt.sdc source.

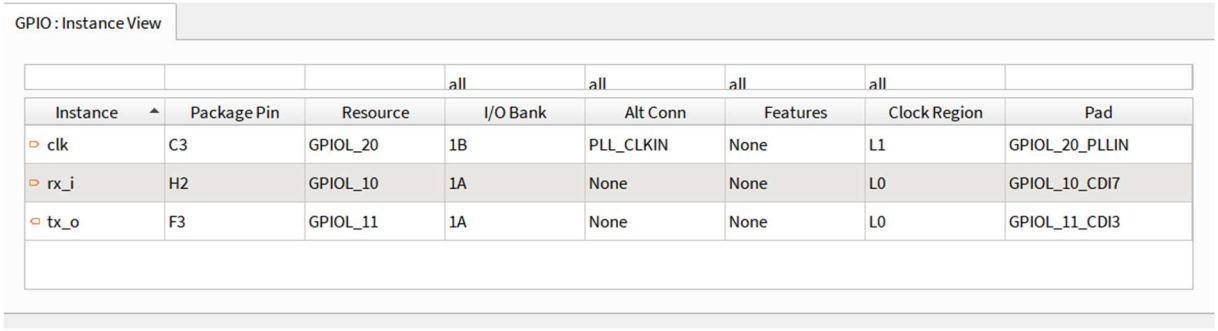
1. Open Efinity Interface Designer.



2. Right click to GPIO and select create block. Enter the name as rx_i and select mode as input.
3. Right click to GPIO and select create block. Enter the name as tx_o and select mode as output.
4. Right click to GPIO and select create block. Enter the name as clk and select mode as input. Select connection type as pll_clkin.
5. Right click to PLL and select create block. Enter the name as clk_pin and click Automated clock calculation. Set input frequency as 33.333 MHz (for xyloni). Enter the name clk_pin and click finish.



6. Click show/hide GPIO Resource Assigner. Enter the resource part according to the datasheet.



			all	all	all	all	
Instance	Package Pin	Resource	I/O Bank	Alt Conn	Features	Clock Region	Pad
clk	C3	GPIOL_20	1B	PLL_CLKIN	None	L1	GPIOL_20_PLLIN
rx_i	H2	GPIOL_10	1A	None	None	L0	GPIOL_10_CDI7
tx_o	F3	GPIOL_11	1A	None	None	L0	GPIOL_11_CDI3

7. Save and check the design then click Generate Efinity constraint file.

Open the lab2.pt.sdc source and analyze the content.

1. In the Project pane, expand the Constraints folder and double-click the lab2.pt.sdc entry to open the file in text mode.

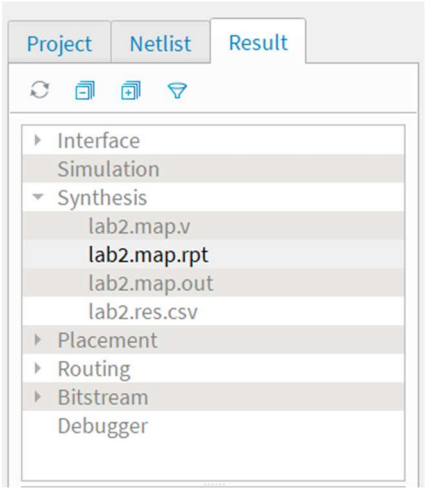
```
1
2 # Efinity Interface Designer SDC
3 # Version: 2022.1.226
4 # Date: 2022-11-11 11:57
5
6 # Copyright (C) 2017 - 2022 Efinix Inc. All rights reserved.
7
8 # Device: T8F81
9 # Project: lab2
0 # Timing Model: C2 (final)
1
2 # PLL Constraints
3 ##################
4 create_clock -period 10.0001 -waveform {5.0001 10.0001} [get_ports {clk_i}]
5
6 # GPIO Constraints
7 ####################
8 # set_input_delay -clock <CLOCK> -max <MAX CALCULATION> [get_ports {clk}]
9 # set_input_delay -clock <CLOCK> -min <MIN CALCULATION> [get_ports {clk}]
0 # set_input_delay -clock <CLOCK> -max <MAX CALCULATION> [get_ports {rx_i}]
1 # set_input_delay -clock <CLOCK> -min <MIN CALCULATION> [get_ports {rx_i}]
2 # set_output_delay -clock <CLOCK> -max <MAX CALCULATION> [get_ports {tx_o}]
3 # set_output_delay -clock <CLOCK> -min <MIN CALCULATION> [get_ports {tx_o}]
```

2. Line 4 creates the period constraint of 10ns with a duty cycle of 50%. The clk is constrained (lines 8, 9). The rx_i is constrained (lines 10, 11). The tx_o is constrained (lines 12, 13).

Synthesize the Design

1. Before performing the synthesis process, we stop the synthesis, placement, routing and bitstream flow by pressing the toogle automated button.
2. Click Synthesis under the dashboard.

3. When the process is completed. Click Result tab and expand Synthesis. Open lab2.map.rpt file as we want to look at the synthesis output before progressing to the placement and routing the stage.




```
### ### Resource Summary (begin) ### ### ###
INPUT  PORTS    :       2
OUTPUT PORTS    :       1

EFX_LUT4        :       71
   1-2  Inputs  :       20
   3    Inputs  :       23
   4    Inputs  :       28
EFX_FF          :       47
EFX_GBUFCE      :       1
### ### Resource Summary (end) ### ### ###
```

Place the Design

1. Click Placement under the dashboard.
2. When the process is completed. Click Result tab and expand Placement. Open lab2.place.rpt file as we want to look at the placement output before progressing to the Routing stage.

```
Family: Trion
Device: T8F81
Top-level Entity Name: lab2
Elapsed time for packing: 0 hours 0 minutes 0 seconds

---------- Resource Summary (begin) ----------
Inputs: 2 / 96 (2.08%)
Outputs: 1 / 113 (0.88%)
Clocks: 1 / 16 (6.25%)
Logic Elements: 85 / 7384 (1.15%)
        LE: LUTs/Adders: 73 / 7384 (0.99%)
        LE: Registers: 47 / 5280 (0.89%)
Memory Blocks: 0 / 24 (0.00%)
Multipliers: 0 / 8 (0.00%)
---------- Resource Summary (end) ----------
```

Route the Design

1. Click Routing under the dashboard.
2. When the process is completed. Click Result tab and expand Routing. Open lab2.timing.rpt file as we want to look at the timing report before progressing to the Bitstream stage.

```
---------- 2. Clock Relationship Summary (begin) ----------

Setup (Max) Clock Relationship
  Launch Clock    Capture Clock   Constraint (ns)     Slack (ns)          Edge
       clk             clk            1.000           -12.951           (R-R)

Hold (Min) Clock Relationship
  Launch Clock    Capture Clock   Constraint (ns)     Slack (ns)          Edge
       clk             clk            0.000            0.642            (R-R)

NOTE: Values are in nanoseconds.

---------- Clock Relationship Summary (end) ---------------
---------- 4. Path Details for Min Critical Paths (begin) ----------

################################################################################
Path Detail Report (clk vs clk)
################################################################################


++++ Path 1 ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

Path Begin     : receiver_i/state[1]_2~FF|CLK
Path End       : receiver_i/state[1]_2~FF|D
Launch Clock   : clk (RISE)
Capture Clock  : clk (RISE)
Slack          : 0.642 (arrival time - required time)
Delay          : 0.460

Logic Level             : 1
Non-global nets on path : 1
Global nets on path     : 0

Launch Clock Path Delay        : 2.502
+ Clock To Q + Data Path Delay : 0.692
---------------------------------------
End-of-path arrival time       : 3.194

Constraint                     : 0.000
+ Capture Clock Path Delay     : 2.502
+ Clock Uncertainty            : 0.050
---------------------------------------
End-of-path required time      : 2.552
```

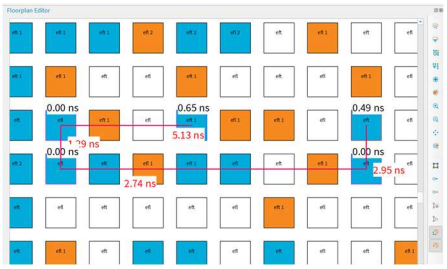
```
---------- 3. Path Details for Max Critical Paths (begin) ----------

################################################################################
Path Detail Report (clk vs clk)
################################################################################


++++ Path 1 ++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

Path Begin     : receiver_i/bittimer[7]~FF|CLK
Path End       : dout[6]_2~FF|CE
Launch Clock   : clk (RISE)
Capture Clock  : clk (RISE)
Slack          : -12.951 (required time - arrival time)
Delay          : 12.668

Logic Level             : 3
Non-global nets on path : 4
Global nets on path     : 0

Launch Clock Path Delay        :  7.006
+ Clock To Q + Data Path Delay : 13.811
---------------------------------------
End-of-path arrival time       : 20.817

Constraint                     : 1.000
+ Capture Clock Path Delay     : 7.006
- Clock Uncertainty            : 0.140
---------------------------------------
End-of-path required time      : 7.866

Launch Clock Path
          name               model name   delay (ns)  cumulative delay (ns) pins on net    location
=============================================================================================================
clk                          inpad        0.000             0.000              0          (0,102)
clk                          inpad        0.420             0.420              2          (0,102)
clk                          net          3.268             3.688              2          (0,102)
   Routing elements:
     Manhattan distance of X:1, Y:24
CLKBUF__0|I                  gbuf         3.318             7.006              2          (1,78)
CLKBUF__0|O                  gbuf         0.000             7.006             48          (1,78)
clk~O                        net          0.000             7.006             48          (1,78)
receiver_i/bittimer[7]~FF|CLK ff          0.000             7.006             48          (11,26)
```

Worst Hold Slack (WHS)

Worst Negative Slack (WNS)

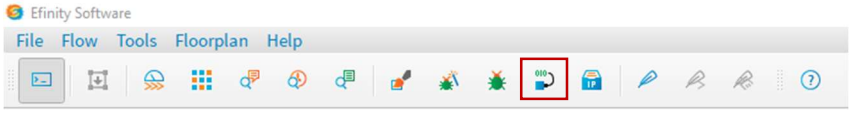
View Floorplan and Show Timing Delays

1. Select Floorplan and click view floorplan.
2. Click Show Timing Path to see timing nets.
3. Click Show Timing Delays to see timing delays.



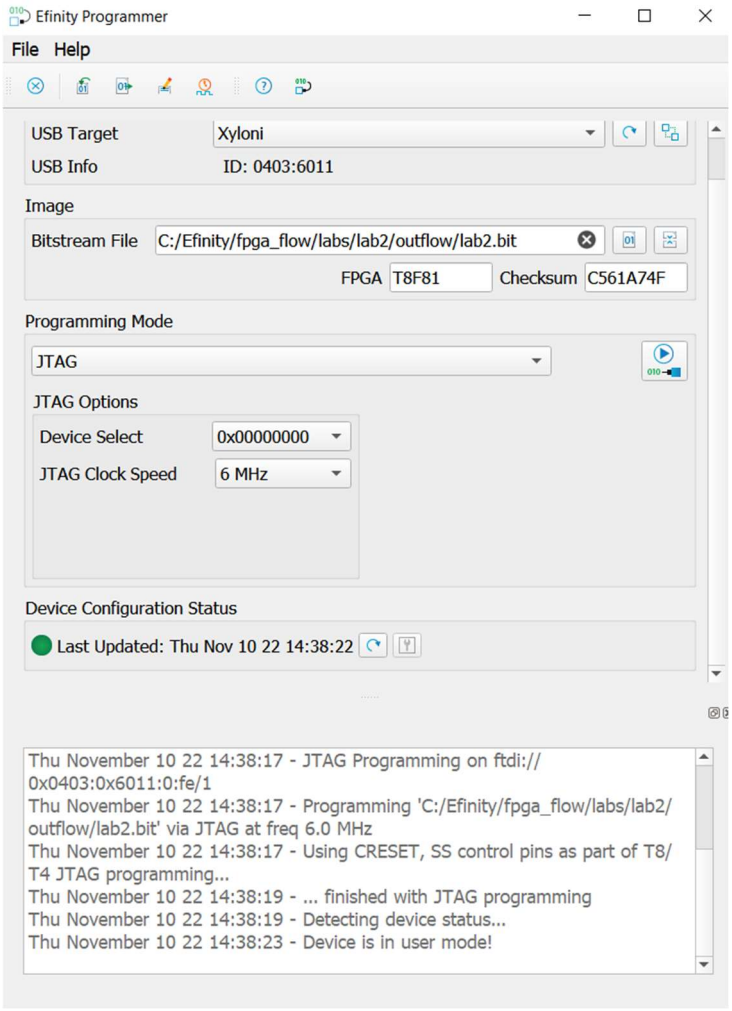
Generate the Bitstream and Verify Functionality

1. Click Bitstream under the dashboard.
2. This process will have generated a lab2.bit file under the Bitstream.
3. Click Open programmer button.



4. Click Refresh USB Targets and select your Xyloni board.
5. Click Select image file button and add lab2.bit file.

6. Under the programming mode select JTAG and click start program button.
7. The Device Configuration Status will lit when the device is programmed.



8. Verify the functionality by install and open the Tera Term. Then select com port click ok.
9. Click Setup>Terminal… and check the Local echo box.
10. Click Setup>Serial port and select speed as 115200 and click new settings.
11. For test the uart communication, write something on the keyboard.
12. When satisfied, power OFF the board.
13. Close the Efinity program by selecting File > Exit.