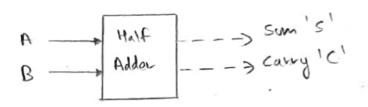
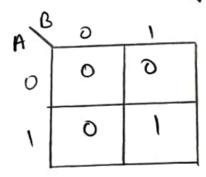
	Experiment - 4			
*	Aim 8- to verify the operation of half adder.			
*	Apparatus 8- Brend board, connecting wires, power supply, IC 7408, IC 7486			
*	Theory &- Half adder is a combinational circuit that performs simple addition of two binary numbers. If we assume A and B as two bits whose addition is to be performed, the block diagram and the truth table for half adder with A, B as impute and Sum, carry as outputs can be tabulated as shown in			
	diagram. The see sum output of the binary addition caused out is similar to that of an Ex-OR operation. While the come Carry output is similar to that of AND operation.			
	the same can be verified with the help of Karnaugh map. SUM = AB' + A'B			
	CARRY = AB			
	If A and B are binary inputs to the half adder, then the logic function to calculate sum S is Ex-OR of A and B and logic function to calculate carry C is AND of A and B.			
	As use knows, that NAND and NOR are called universal gates as any logic system can be implemented using these two, the half adder circuit can also be implemented using them. We know that half adder circuit has one EX-OR gate and one AND gate.			
	implemented using them. We know that half adder circuit has one EX-OR gate and one AND gate.			
(1)				
(8)				
	Teacher's Signature			

Expt. No.	Page No
* bracedure 8-	
1. Construct the circuit as shown in the logic diagram.	
2. Insert the correct IC's on the bread bound.	
3. Whe Vec and ground voltage to all ICS.	
4. Verify the output by toth tuble.	(77)
	(%)
* Result 8- operation of half adder has been verifi	Fled.
& Precautions &	
1. Insert the IC's carefully in the breadboard wi	thout duringing the wives.
2. Switch off the breadboard when not in use.	
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truth table						
Input	<u></u>	Output				
A	B	Sum	Cany			
0	0	0	٥			
٥	1	1	0			
1	0	(٥			
		0	1			





Malf Adder Logic Dingram

