

Monday

STLD → Switching Theory & Logic Design★ Number Systems:

- 1) Decimal Number System  $(\ )_{10} \rightarrow 0-9$
- 2) Binary Number System  $(\ )_2 \rightarrow 0-1$
- 3) Octal Number System  $(\ )_8 \rightarrow 0-7$
- 4) Hexadecimal Number System  $(\ )_{16} \rightarrow 0-9, A, B, C, D, E, F$

$$\begin{array}{ccccccc} A & B & C & D & E & F \\ \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ 10 & 11 & 12 & 13 & 14 & 15 \end{array}$$

Base → RADIX → No. of digits present in the system

★ Conversion:

## (1) A) DECIMAL TO BINARY

Ex1:  $(92)_{10} \rightarrow (?)_2$

2	92	0
2	46	0
2	23	1
2	11	1
2	5	1
2	2	0
	1	

$$(92)_{10} \rightarrow (1011100)_2$$

Ex2:

2	243	1
2	121	1
2	60	0
2	30	0
2	15	1
2	7	1
2	3	1
	1	

$$(243)_{10} \rightarrow (?)_2$$

$$(243)_{10} \rightarrow (11110011)_2$$

Ex3:  $(0.92)_{10} \rightarrow (?)_2$

$$0.92 \times 2 = 1.84 \quad \begin{matrix} & \\ & \swarrow 1 \end{matrix}$$

$$0.84 \times 2 = 1.68 \quad \begin{matrix} & \\ & \swarrow 1 \end{matrix} \quad (0.92)_{10} \rightarrow (0.1110)_2$$

$$0.68 \times 2 = 1.34 \quad \begin{matrix} & \\ & \swarrow 1 \end{matrix}$$

$$0.34 \times 2 = 0.68 \quad \begin{matrix} & \\ & \swarrow 0 \end{matrix}$$

Ex4:  $(11.48)_{10} \rightarrow (?)_2 \quad (11)_{10} \rightarrow (1011)_2$

$$\begin{array}{r} 11.48 \\ \downarrow \\ \begin{array}{r} 2 | 11 \ 1 \\ 2 | 5 \ 1 \\ 2 | 2 \ 0 \\ \hline 1 \end{array} \end{array}$$

$$0.48 \times 2 = 0.96 \quad \begin{matrix} & \\ & \swarrow 0 \end{matrix}$$

$$0.96 \times 2 = 1.92 \quad \begin{matrix} & \\ & \swarrow 1 \end{matrix}$$

$$0.92 \times 2 = 1.84 \quad \begin{matrix} & \\ & \swarrow 1 \end{matrix}$$

$$0.84 \times 2 = 1.68 \quad \begin{matrix} & \\ & \swarrow 1 \end{matrix}$$

$$(0.48)_{10} \rightarrow (0111)_2$$

$$(11.48)_{10} \rightarrow (1011.0111)_2$$

(1) B) BINARY TO DECIMAL:

Most (MSB)  
Significant Bit

(LSB) Least  
Significant Bit

1 0 1 1 1

Ex1:

$2^2$	$2^1$	$2^0$	$2^{-1}$	$2^{-2}$	$2^{-3}$	$2^{-4}$	$2^{-5}$	$2^{-6}$
1	1	1	0	1	1	0	1	1

 $111.011011$ 

$$\begin{aligned}
 (?)_{10} &= 2^2 \times 1 + 2^1 \times 1 + 2^0 \times 1 + 0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 0 \times 2^{-4} \\
 &\quad + 1 \times 2^{-5} + 1 \times 2^{-6} \\
 &= 4 * 2 + 1 + 0 + 1/4 + 1/8 + 0 + 1/32 + 1/64 \\
 &= 7 + 0.25 + 0.125 + 0.03125 + 0.015625 \\
 &= (7.421875)_{10}
 \end{aligned}$$

7/09/22

## Q) A) DECIMAL TO OCTAL

Ex1:  $(79.37)_{10} = (?)_8$

$\frac{8}{8} \overline{)79.37}$	$0.37 \times 8 = 2.96$ $\downarrow$ $0.96 \times 8 = 7.68$ $\downarrow$ $0.68 \times 8 = 5.44$ $\downarrow$ $\Rightarrow (79.37)_{10} \rightarrow (117.275)_8$
$\frac{8}{8} \overline{)91}$	
$\frac{1}{}$	

## B) OCTAL TO DECIMAL

Ex.  $(234.45)_8 \rightarrow (?)_{10}$

$8^2$	$8^1$	$8^0$	$8^{-1}$	$8^{-2}$
2	3	4	.	4 5

$$\begin{aligned}
 &= 2 \times 64 + 3 \times 8 + 4 \times 8^0 + 4 \times 8^{-1} + 5 \times 8^{-2} \\
 &= 128 + 24 + 4 + 0.5 + 0.125 + 0.07 \\
 &= 156.575 \\
 &\Rightarrow (234.45)_8 \rightarrow (156.57)_{10}
 \end{aligned}$$

3) a) DECIMAL TO HEXADECIMAL

$$(234.45)_{10} \rightarrow (?)_{16}$$

16	234	10 ↑	0.45 × 16 = 7.2
	14		7 ↗
			0.2 × 16 = 3.2
			3 ↗
$(EA)_{16}$			

$$(234.45)_{10} \rightarrow (EA.733)_{16}$$

b) HEXADECIMAL TO DECIMAL

$$(D4E.79B)_{16} \rightarrow (?)_{10}$$

$$16^2 \ 16^1 \ 16^0 \quad 16^7 \ 16^6 \ 16^5 \ 16^4 \ 16^3 \\ D \ 4 \ E \ . \ 7 \ 9 \ B$$

$$16^1 = 16$$

$$16^2 = 256$$

$$\begin{aligned} &= D \times 16^2 + 4 \times 16^1 + E \times 16^0 + 7 \times 16^{-1} + 9 \times 16^{-2} + B \times 16^{-3} = 4096 \\ &= 13 \times 16^2 + 4 \times 16^1 + 14 \times 16^0 + 7 \times 16^{-1} \quad 16^4 = 65536 \\ &\quad + 9 \times 16^{-2} + 11 \times 16^{-3} \end{aligned}$$

$$\begin{aligned} &= 3328 + 64 + 14 + 0.4375 + 0.035 + 0.0026 \\ &= 3406 + 0.475 \end{aligned}$$

$$\Rightarrow (D4E.79B)_{16} \rightarrow (3406.475)_{10}$$

4) BINARY TO OCTAL

$(1101110010.001110)_2$



To convert binary number to octal, we need to make groups of 3 digits for integer part decimal points to MSB side and for fractional part decimal to LSB side.

$(\underline{\quad} \underline{\quad} \underline{0} \underline{0} \underline{1} \underline{1} \underline{0} \underline{1} \underline{1} \underline{1} \underline{0} \underline{0} \underline{1} \underline{0} \cdot \underline{0} \underline{0} \underline{1} \underline{1} \underline{1} \underline{0})$

↑  
Decimal point

$$\Rightarrow (1562.16)_{10} =$$

⇒

Binary Table

Decimal No.	Binary No. (8 4 2 1)
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
10	1 0 1 0
11	1 0 1 1
12	1 1 0 0
13	1 1 0 1
14	1 1 1 0
15	1 1 1 1

5) BINARY TO HEXADECIMAL CONVERSION:  
 In this we need to make groups of 4 digits for integer part decimal point to MSB and for fractional part decimal point to LSB.

$\begin{array}{cccccc} 0 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 0 \\ \hline & 3 & & 7 & & 3 & & 8 & & \end{array}$

$$\Rightarrow (372.38)_{10}$$

8/09/22

### \* Binary Arithmetic

#### • ADDITION

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 10$$

$$1 + 1 + 1 = 1 + 10 = 11$$

$$1 + 1 + 1 + 1 = 10 + 10 = 100$$

#### • EX

$$11110.11$$

$$\begin{array}{r} 111 \\ 1110.11 \end{array}$$

$$10011.00$$

$$10011.00$$

$$+ 00010.11$$

$$\underline{110001.11}$$

$$110100.10$$

$$\begin{array}{r} 111 \\ 110001.11 \end{array}$$

$$000010.11$$

$$\underline{110100.10}$$

### SUBTRACTION

$$0 - 0 = 0$$

$$0 - 1 = 1 \text{ with borrow 1}$$

$$1 - 0 = 1$$

$$1 - 1 = 0$$

$$10 = 1 + 1$$

$$10 - 1 =$$

$$1 + 1 - 1 = 1$$

Ex.

$$\begin{array}{r} 111\overset{10}{\cancel{1}}\overset{10}{\cancel{0}}.11 \\ - 10011.00 \\ \hline 01011.1\overset{1}{0}1 \end{array}$$

### MULTIPLICATION

$$0 \times 0 = 0$$

$$0 \times 1 = 0$$

$$1 \times 0 = 0$$

$$1 \times 1 = 1$$

Ex.

$$\begin{array}{r} 11011 \\ \times 101 \\ \hline 111011 \\ 100000 \\ \hline 1101100 \\ \hline 10000111 \end{array}$$

### DIVISION:

$$0 \div 0 =$$

### \*DIVISION

• DIVISION

$$\begin{array}{r}
 1011 \\
 101 ) 110111 \\
 -101 \\
 \hline
 00111 \\
 -101 \\
 \hline
 0101 \\
 -101 \\
 \hline
 000
 \end{array}$$

★ Complements

(1)  $r$ 's complement  $\rightarrow r^m - N$   $r \rightarrow \text{radix}$

(2)  $(r-1)$ 's complement  $\rightarrow r^m - r^m - N$

143.75  $N \rightarrow \text{Number}$

$\downarrow$   $m=2$   $n \rightarrow \text{no. of digits in integer part}$   
 $n=3$   $m \rightarrow \text{no. of digits in fractional part}$

Ex:

Q. Take  $r$ 's complement of  $(143.75)_{10}$

Sol.

$$= 10^3 - 143.75$$

$$= 1000 - 143.75$$

$$= 856.25$$

Direct method 2: for 10's complement  
 $(143.75)$

$$\begin{array}{r}
 999.99 \\
 143.75 \\
 \hline
 856.24 \\
 + 1 \\
 \hline
 856.25
 \end{array}$$

Subtract every digit from 9  
then +1 at the end.

- $(n-1)$ 's complement:

$$\begin{aligned}
 &= n^n - n^{-m} - N \\
 (143.75)_{10} &= 10^3 - 10^{-2} - 143.75 \\
 &= 1000 - 0.01 - 143.75 \\
 &= 1000 - 143.75 \\
 &= 856.24
 \end{aligned}$$

Direct method : 999.99

$$\begin{array}{r}
 9's \text{ complement} \quad 143.75 \\
 \underline{-} \quad \underline{856.24}
 \end{array}$$

- 2's complement

I<sup>st</sup> method:  $(11011.01)_2 \xrightarrow{\text{2's complement}} (2)_{10} - (11011.01)_2$

Step II: convert to Binary

$$\begin{aligned}
 &= (32)_{10} - (11011.01)_2 \\
 &= 100000 - 11011.01 \\
 &= 000100.11
 \end{aligned}$$

~~II<sup>nd</sup> method~~

~~Direct~~

$$\begin{array}{r}
 11011.01 \xrightarrow{1's} 00100.010 \\
 \xrightarrow{2's} \underline{+} \quad \underline{1} \\
 \underline{00100.11}
 \end{array}$$

→ for 2's complement, find the 1's complement  
then add 1 at the end.

- 1's complement.

T<sup>st</sup> memo'd.  $(1011.110)_2 \xrightarrow{1\text{'s complement}} 2^4 - 2^3 - (1011.110)_2$

$$= (16)_{10} - (0.125)_{10} - (1011.110)_2$$

$$= (15.875)_{10} - (1011.110)_2$$

$$\begin{array}{r}
 2 | 15 \ 1 \\
 2 | 7 \ 1 \\
 2 | 3 \ 1 \\
 \hline
 1 \ 1
 \end{array}
 = \begin{array}{l}
 (1111.111)_2 \\
 - (1011.110)_2 \\
 \hline
 0100.001
 \end{array}
 \quad \begin{array}{l}
 0.875 \times 2 = 1.75 \\
 \curvearrowleft 2 \\
 0.75 \times 2 = 1.50 \\
 \curvearrowleft 1 \\
 0.50 \times 2 = 1.0 \\
 \curvearrowleft 1
 \end{array}$$

$$\begin{array}{r}
 1111.111 \\
 - 1011.110 \\
 \hline
 0100.001
 \end{array}$$

12/09/22

- Arithmetic Using Complements:-

Case I: when minuend > subtrahend

I. Subtraction → Using 1's comp

$$\text{Ans: } (1010)_2$$

$$\begin{array}{r} 15 \rightarrow 1111 \text{ minuend} \\ - 0101 \text{ Subtrahend} \\ \hline \text{Ans: } 1010 \end{array}$$

1 1 1 1 ① 1's  
+ 1 0 1 0 Rule  
① 1 0 0 1 if carry comes  
+ 1 → 1  
Ans 1 0 1 0 out in MSB add it to LSB

② In 2's case, carry is neglected.

Example:

$$\begin{array}{r} 11101 \\ - 10001 \\ \hline 01100 \end{array} \quad \begin{array}{r} 11101 \\ + 01110 \\ \hline 10110 \end{array}$$

II. Subtraction - Using 2's comp.

$$\begin{array}{r} 11101 \\ - 10001 \\ \hline 01100 \end{array} \quad \begin{array}{r} 1111 \\ + 01111 \\ \hline 10110 \end{array}$$

neglecting MSB

$$\text{Ans: } (01100)_2$$

Case II: Minuend < subtrahend

Using 1's

$$\begin{array}{r} A \quad 0111 \\ B \quad 1010 \end{array}$$

$$A - B = ?$$

$$\begin{array}{r} 111 \\ 0111 \\ + 0101 \\ \hline 1100 \end{array} \text{ no carry generated}$$

So the answer will be complement of the value  
Answer is  $(-0011)_2$

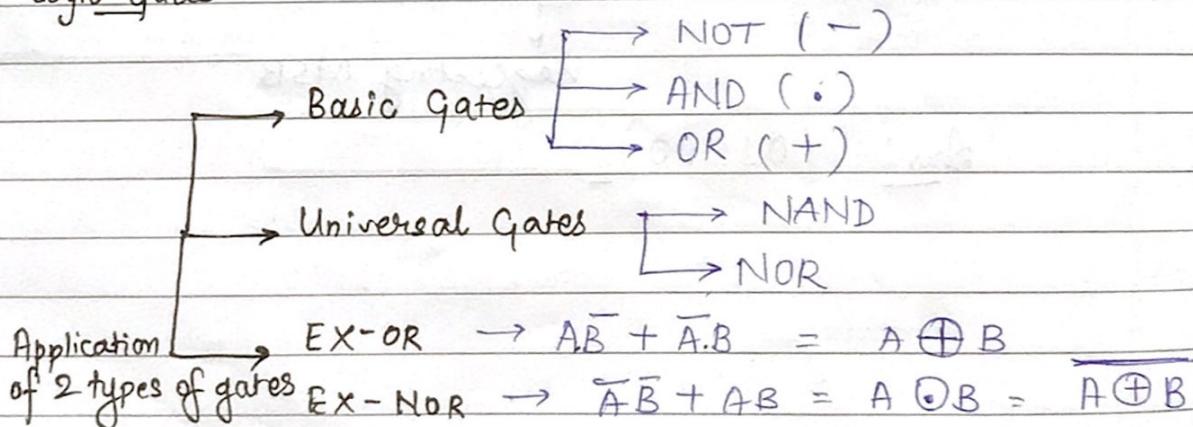
Using 2's

$$\begin{array}{r} A \quad 0111 \\ B \quad 1010 \end{array} \rightarrow \begin{array}{r} 111 \\ 0111 \\ + 0111 \\ \hline 1100 \end{array} \text{ no carry generated}$$

$$\text{Ans: } (-0011)_2$$

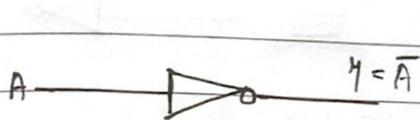
$$\begin{array}{r} 0010 \\ + 1 \\ \hline 1 \end{array}$$

13/09/22 Logic Gates :-



## Basic Gates:-

### ① NOT Gate :-



A	$Y = \bar{A}$
0	1
1	0

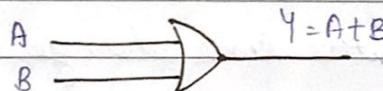
combination =  $2^n$

### ② AND Gate :-



A	B	$Y = A \cdot B$
0	0	0
1	0	0
0	1	0
1	1	1

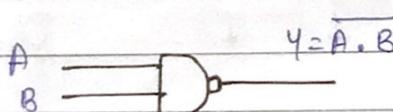
### ③ OR Gate :-



A	B	$Y = A + B$
0	0	0
1	0	1
0	1	1
1	1	1

Universal Gates: These gates can ~~be~~ replace basic gates.

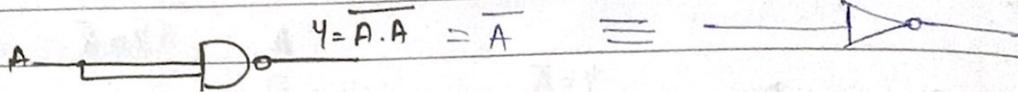
### ① NAND Gate



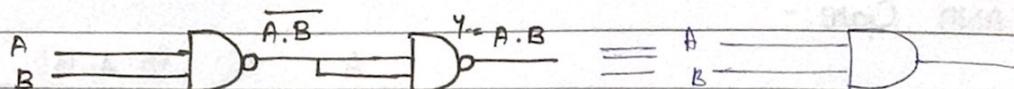
A	B	$Y = \bar{A} \cdot \bar{B}$
0	0	1
0	1	1
1	0	1
1	1	0

Basic gates using NAND gates :-

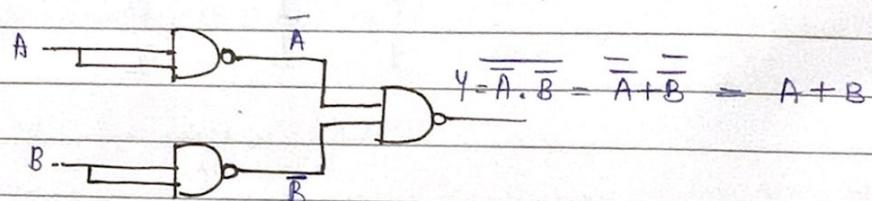
(I) NOT



(II) AND

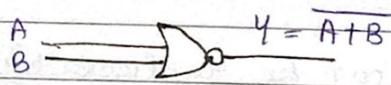


(III) OR



💡 De-Morgan's Theorem: break the line change the sign

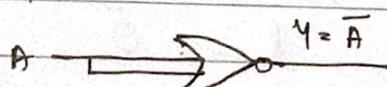
(2) NOR Gate:



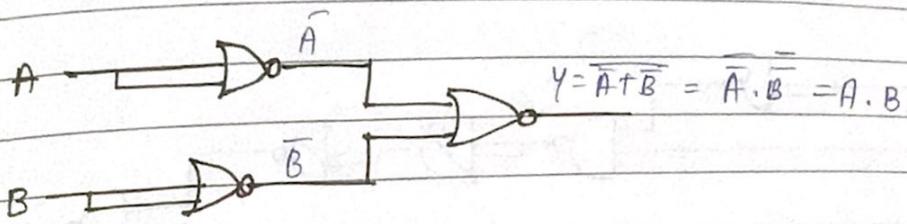
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Basic gates using NOR Gate

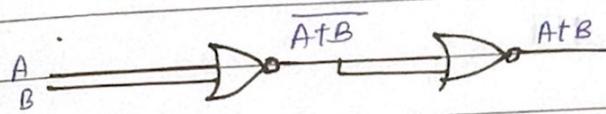
(I) NOT



(II) AND

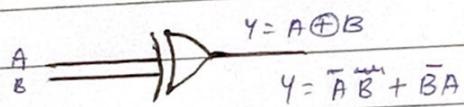


(III) OR



15/09/22

\* EX-OR :-



A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

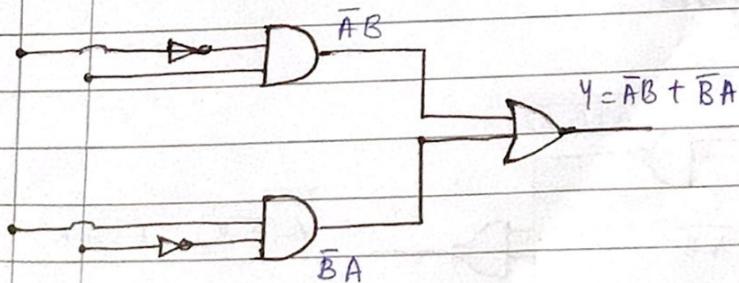
→ when inputs are same XOR is 0

↳ when inputs are opposite XOR is 1

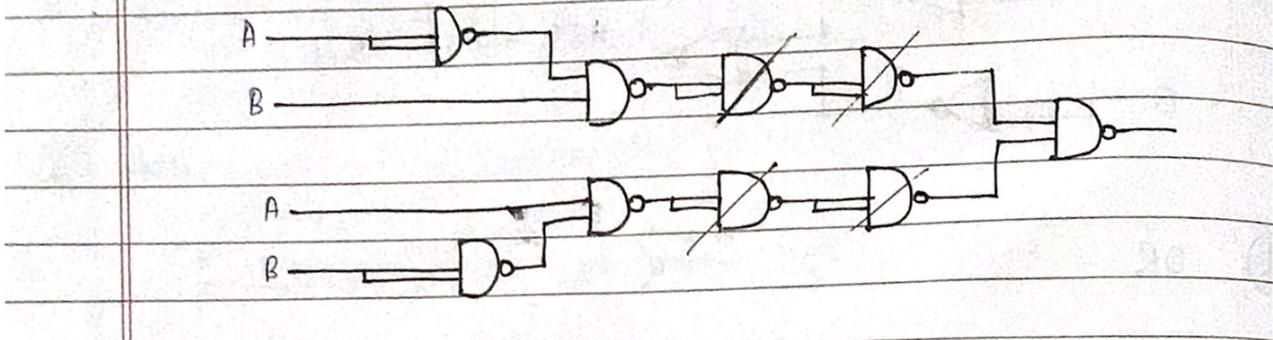
$$\overline{A}B + \overline{B}A$$

Ex-OR  
Working Basic  
gate

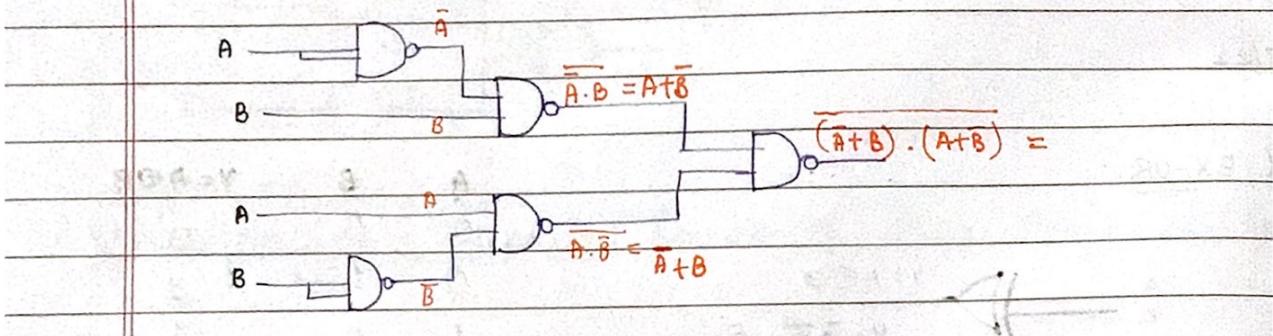
A      B



EX-OR gate using NAND Gate only

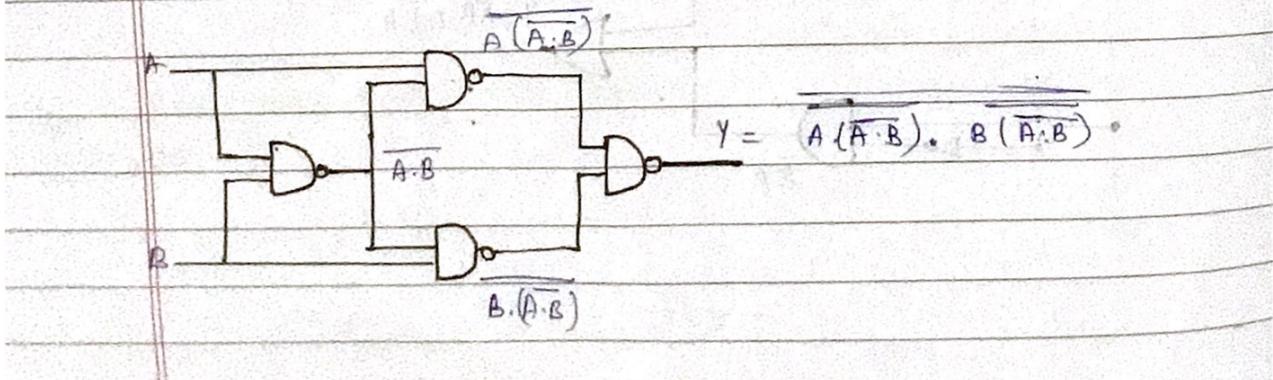


111



$$(\overline{A} + B) \cdot (\overline{A} + \overline{B}) = (\overline{A} + B) + (\overline{A} + \overline{B}) \\ = A \cdot \overline{B} + \overline{A} \cdot B$$

③ Draw the NAND label minimization of XOR gates using minimum gates.



$$\begin{aligned}
 &= \overline{A \cdot (\overline{A} \cdot B)} + \overline{B \cdot (\overline{A} \cdot B)} \\
 &= A \cdot (\overline{A} \cdot \overline{B}) + B \cdot (\overline{A} \cdot \overline{B}) \\
 &= A \cdot (\overline{A} + \overline{B}) + B \cdot (\overline{A} + \overline{B}) \\
 &= A\overline{A} + A\overline{B} + B\overline{A} + B\overline{B} \quad A\overline{A} = 0 \\
 &\quad \downarrow \qquad \qquad \qquad \downarrow \\
 &\quad 0 \qquad \qquad \qquad 0
 \end{aligned}$$

$$A \oplus B = A\overline{B} + \overline{A}\cdot B$$

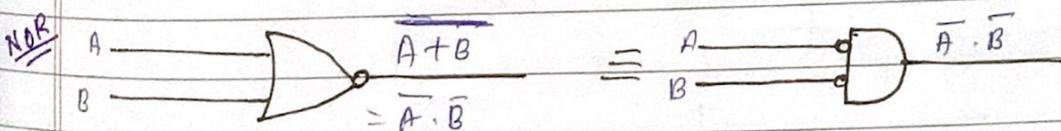
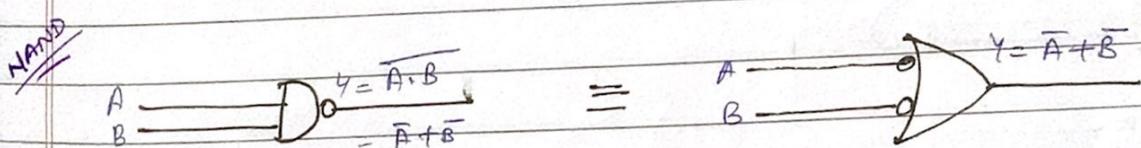
\* EX-NOR :-

$$\begin{aligned}
 &\text{NAND gate: } Y = A \otimes B = \overline{A \oplus B} = \overline{\overline{AB} + \overline{BA}} \\
 &= (\overline{A}\overline{B}) \cdot (\overline{B}\overline{A}) \\
 &= (\overline{A} + \overline{B}) \cdot (\overline{B} + \overline{A}) \\
 &= (\overline{A} + \overline{B}) \cdot (\overline{B} + \overline{A}) \\
 &= A\overline{A} + \overline{A}\overline{B} + AB + B\overline{B} \\
 &\quad \downarrow \qquad \qquad \qquad \downarrow \\
 &\quad 0 \qquad \qquad \qquad 0
 \end{aligned}$$

A	B	$Y = A \otimes B$
0	0	1
0	1	0
1	0	0
1	1	1

$$A \otimes B = \overline{A}\overline{B} + AB$$

16/09/22. Two level NAND/NOR Implementation:-



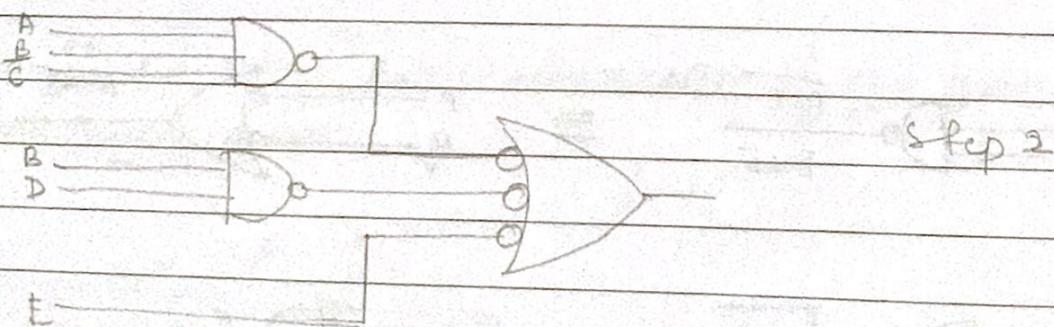
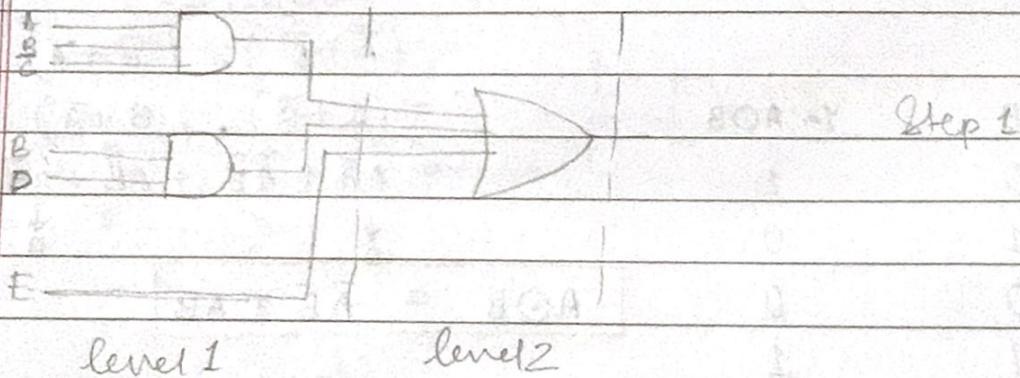
\* AND-OR logic to NAND/NOR logic:

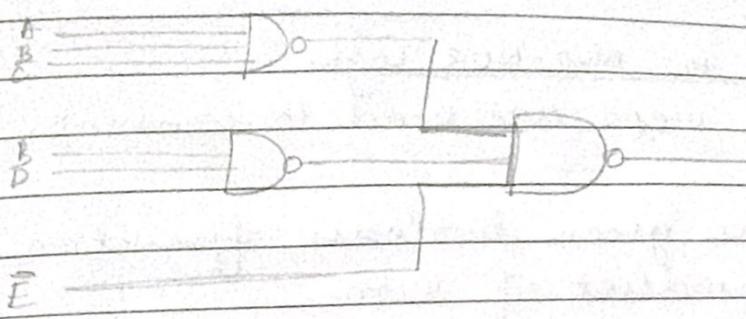
- AND-OR logic to NAND/NAND implementation:

1. Draw and AND-OR logic for the simplified boolean expression.
2. Replace AND gate by NAND gate and OR gate by bubbled OR gate
3. Replace bubbled OR gate by NAND gate

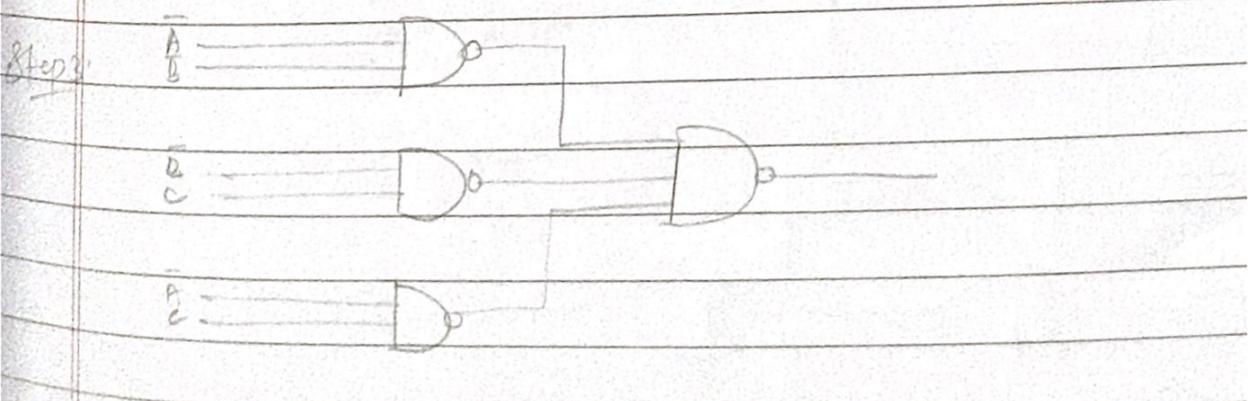
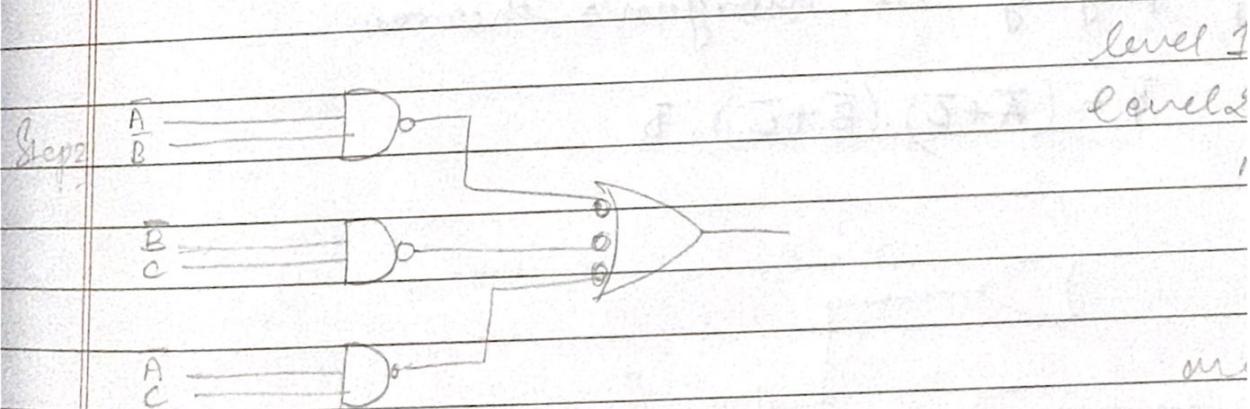
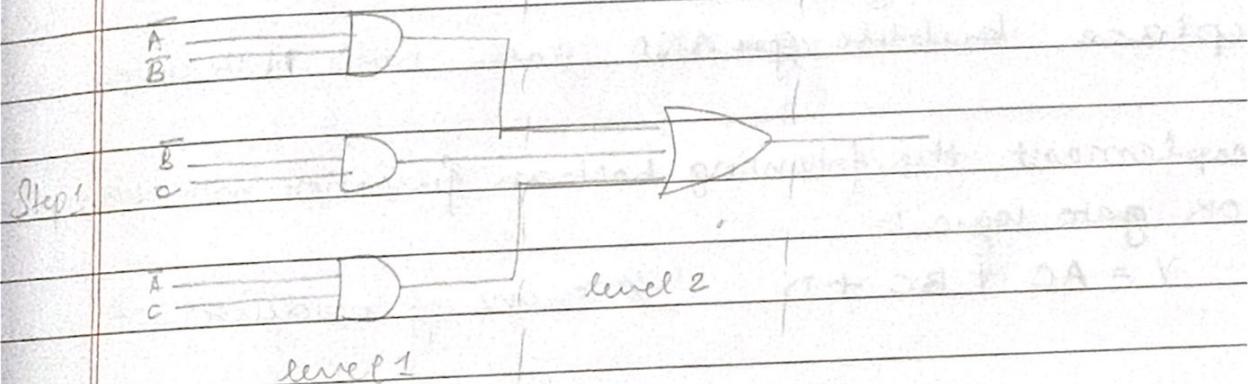
Ex: Implement NAND NAND logic for given expression:-

$$Y = AB\bar{C} + BD + E$$





Ex 2: Implement the boolean function with NAND NAND logic  
 $Y = \overline{A} \cdot \overline{B} + \overline{B} \cdot C + \overline{A} \cdot C$



- OR-AND logic to NOR-NOR logic :-  
The following steps are used to convert,

1. Simplify the given boolean function in the form of product of sum.
2. Draw OR-AND logic circuit for the simplified expression.
3. Replace OR gate by NOR gate and AND gate with bubbled AND gate
4. Replace bubble gate AND gate with NOR gate.

Ex1: Implement the following boolean function with NOR-NOR gate logic :-

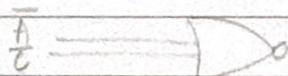
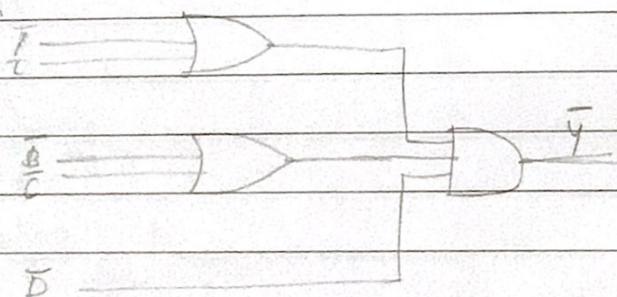
$$Y = AC + BC + D \quad // \text{sum of products (SOP)}$$

Solution:

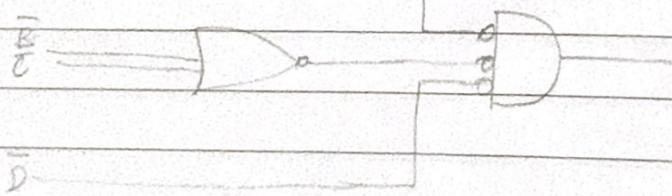
By applying De morgan's theorem

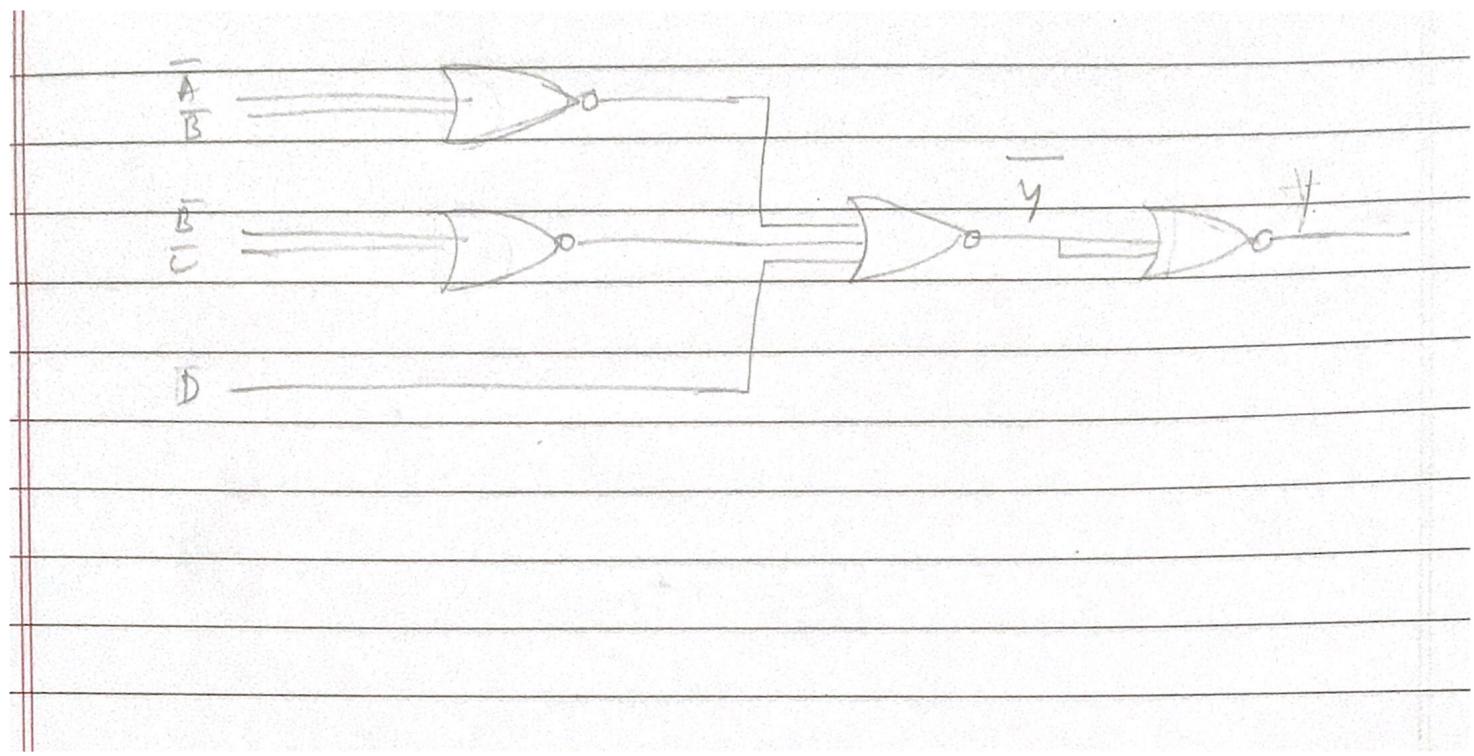
$$\bar{Y} = (\bar{A} + \bar{C}) \cdot (\bar{B} + \bar{C}) \cdot \bar{D}$$

Step 1:-



Step 2:-





19/09/22

### \* Multilevel NAND Implementation:-

The following steps are used to implement :-

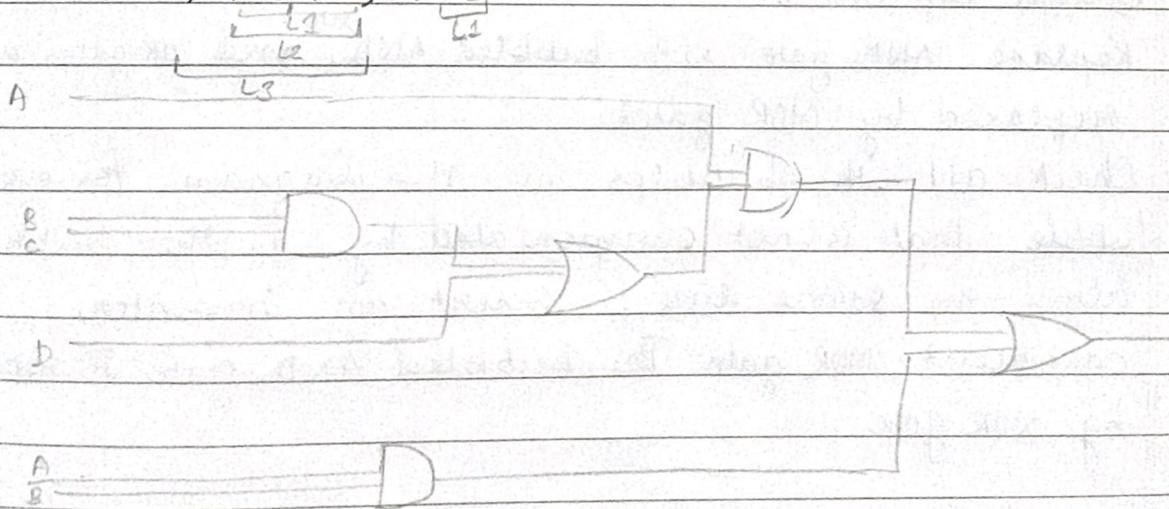
Step 1: Draw the logic circuit using basic gates for the given boolean expression.

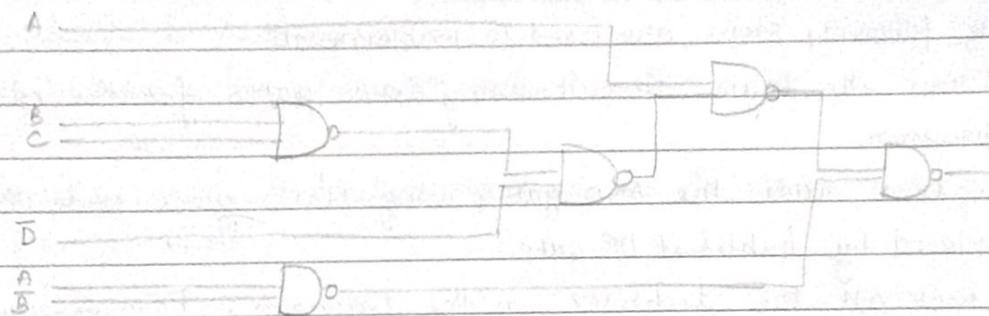
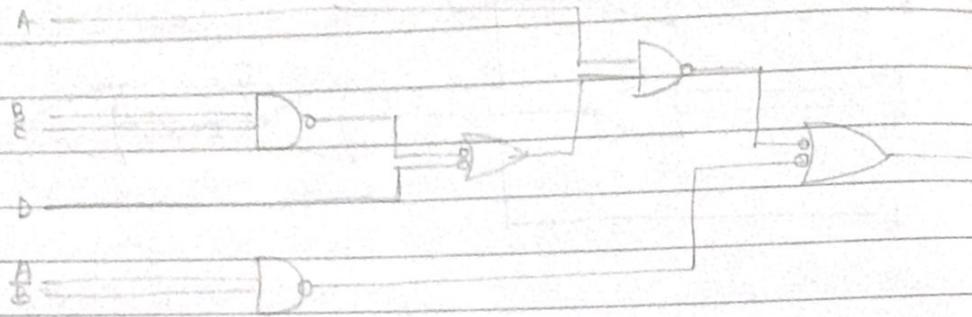
Step 2: Replace all the AND gates using NAND gates and OR gates are replaced by bubbled OR gate.

Step 3: Check all the bubbles in the diagram. For every bubble that is not compensated by another bubble along the same line, Insert a NOT gate and replace it with equivalent NAND gate. The bubbled OR is also replaced by NAND gate.

Q.

$$Y = A \cdot (BC + D) + A\bar{B}$$





### \* Multilevel NOR Implementation :-

The following steps are followed to implement:

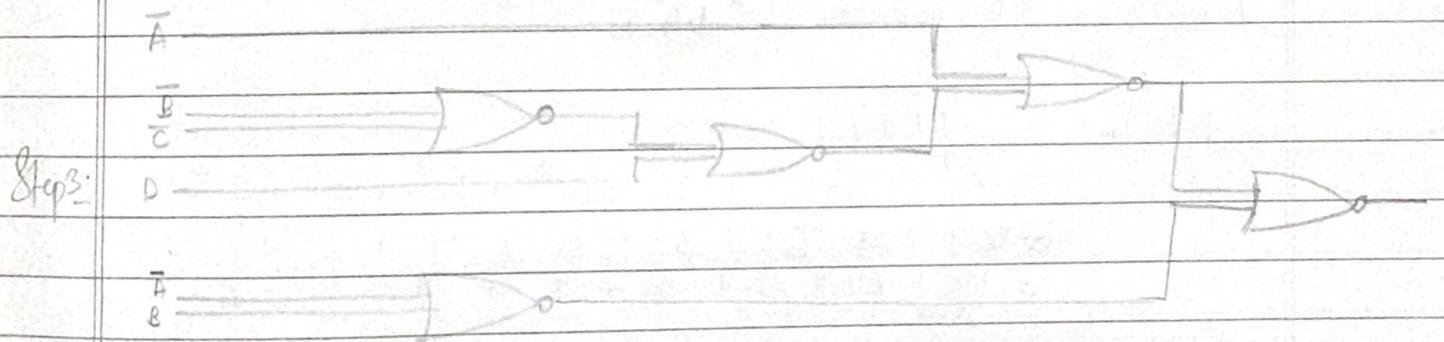
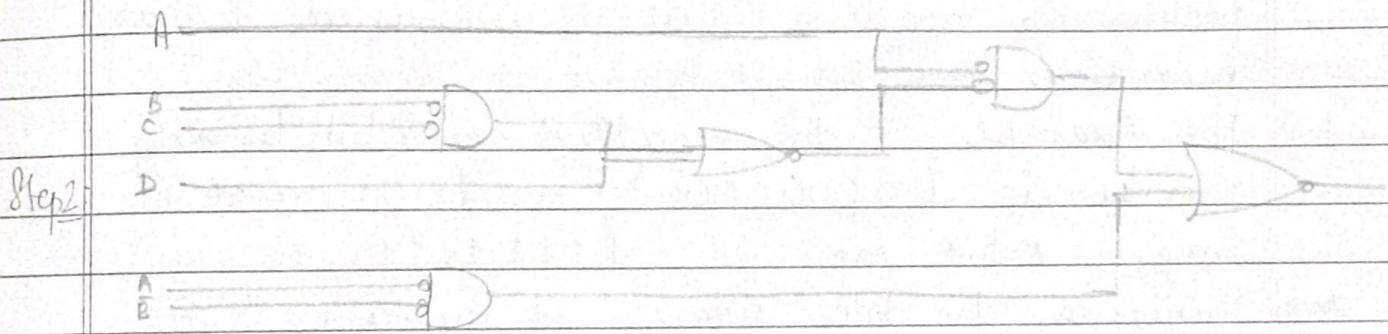
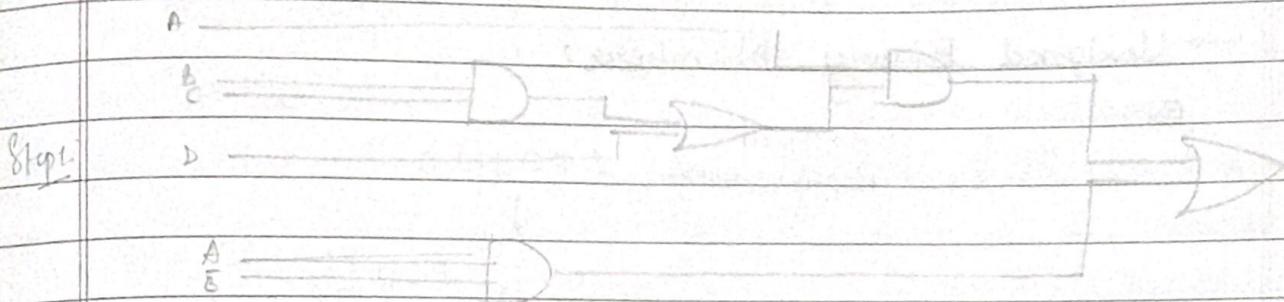
Step 1: Draw the logic diagram using basic gate for the given boolean expression.

Step 2: Replace AND gate with bubbled AND, and OR gates are replaced by NOR gates.

Step 3: Check all the bubbles in the diagram. For every bubble that is not compensated by another bubble along the same line, insert an inverter equivalent NOR gate. The bubbled AND gate is replaced by NOR gate.

Q.  $Y = A(BC + D) + A\bar{B}$

FUN



20/09/22

\* Sign/Magnitude Representation:  
& Unsigned

↪ Unsigned Binary Numbers:

Ex:

$$(22)_{10} \xrightarrow{\text{unsigned Representation}} 100110$$

$$(00010110)_2$$

2	2	0
2	1	1
2	5	1
2	2	0
		4

↪ In some applications, all the data are either positive or negative but in unsigned binary number we forget about + or - sign:

↪ For Example, the smallest 8 bit binary number is  $(00000000)_2$  is  $(00)_2$  and the largest 8 bit no. is  $(11111111)_2$ .

↪ Therefore, the total range of unsigned 8 bit binary no. is from  $(00)_{10}$  to  $(FF)_{10}$ . H represent 16 i.e.  $(0)_{10}$  to  $(255)_{10}$

$$\begin{aligned}(FF)_H &= 11111111 \\&= 2^7 + 2^6 + 2^5 + 2^4 + 2^3 + 2^2 + 2^1 + 2^0 \\&= 128 + 64 + 32 + 16 + 8 + 4 + 2 + 1 \\&= 255\end{aligned}$$

↪ Signed Binary Numbers:

$$+ (89)_{10} \xrightarrow{\text{8 bit Representation}} 01011001$$

Sign Bit

$$-(89)_{10} \xrightarrow{\text{8 bit Representation}} 11011001$$

-ve sign

2	8	1
2	9	0
2	2	0
2	1	1
2	5	1
2	2	0

1 represents -ve  
0 represents +ve

8 bit largest negative no.: 

1	1111111
---	---------

  
largest positive no.: 

0	1111111
---	---------

$-(127)_{10}$

$+(127)_{10}$

- If the data, has positive as well as negative number then the sign binary numbers must be used. The + sign and - sign are represented by 0 and 1 respectively.
- The MSB of the binary no. here, is used to represent the sign and the remaining bits represents the no. Range

→ Range: The signed magnitude numbers range from  $-127$  to  $+127$

### \* Sign One's Complement:

$(-7)_{10}$

Sign Magnitude:

1	0000111
---	---------

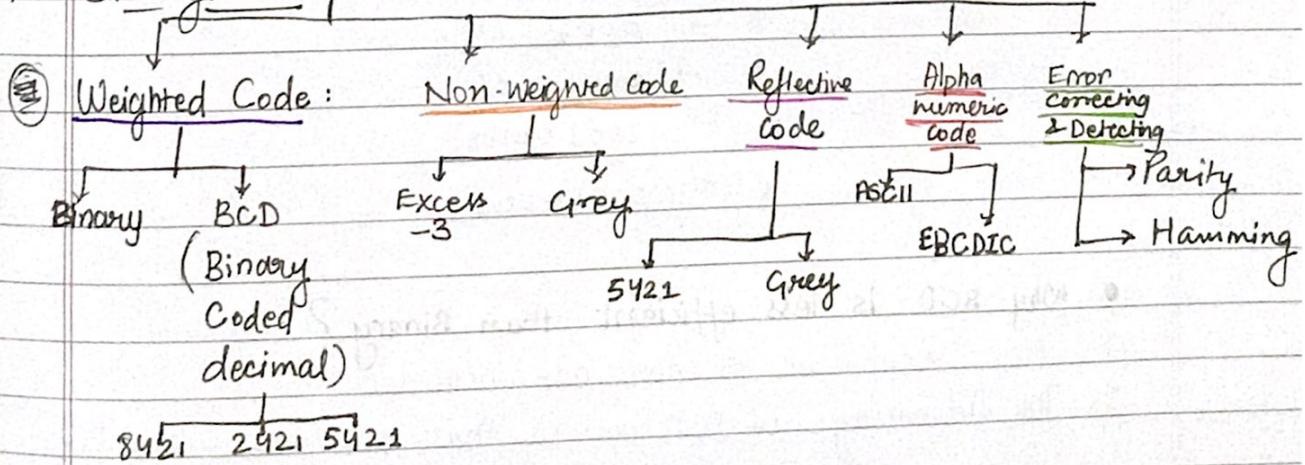
1	1111000
---	---------

Signed 1's complement:

1	1111001
---	---------

Signed 2's complement:

### \* Binary Codes:



① Weighted Code :

→ In weighted codes, each position of the digit represents a specific weight. In 4 bit binary number each digit will have a weight of  $8, 4, 2, 1$  respectively.

A) Binary :

B) Binary Coded Decimal :

→ In this code each decimal digit is represented by a 4 bit binary number. The valid digits ranges from 0 to 9.

• Decimal      BCD code

0            0000

1            0001

2            0010

3            0011

4            0100

5            0101

6            0110

7            0111

8            1000

9            1001

10          X → No 4 bit exists, only 8 bit can

11          X represent this.

12          X → (00010010)

13          X → (00010011)

14          X → (00010010)

15          X → (00010101)

• Why BCD is less efficient than Binary?

1. BCD Arithmetic is more complicated.

2. The Advantage of BCD no. is that the conversion from

decimal to BCD and vice-versa is quite simple.

3. BCD needs more(<sup>bits</sup>digit) to represent in comparison to binary.

● BCD Arithmetic:

Case I: Sum is equal to or less than 9 with carry 0

Ex: Decimal

$$\begin{array}{r} 2 \\ + 6 \\ + 8 \\ \hline 1000 \end{array} \rightarrow (+8)_{BCD}$$

E:

~~Sum  
if sum is~~

Conclusion: If sum less than or equal to 9 with final carry equal to 0 then sum is in proper BCD form and requires no correction.

Case II: Sum is greater than 9 with carry 1

Ex: Decimal

$$\begin{array}{r} 7 \\ + 6 \\ + 13 \\ \hline 01101 \end{array}$$

+ 0110      Add 6 for correction

00010011

1      3

→ VALID NO.

22/09/22

Date \_\_\_\_\_  
Page \_\_\_\_\_

**Case III:** Sum is less than 9 but with carry other than 0, i.e. 1

Decimal	BCD
9	1001
<u>+ 8</u>	<u>1000</u>
<u>17</u>	<u>10001</u>
	+ 0110
	<u>000101101</u>
Add +6 for correction	↓      ↓

Q1. Add  $(57)_{10}$  and  $(26)_{10}$  using BCD arithmetic.  
Sol.

Decimal	BCD
57	0101 0111
<u>26</u>	<u>0010 0110</u>
<u>83</u>	<u>0111 1101</u>
	as this no.
	is considered
	invalid
Add +6 for correction	↓      ↓

Q2. Add  $(83)_{10}$  and  $(34)_{10}$  using BCD arithmetic.

Sol.

Decimal	BCD
83	1000 0011
34	0011 0100
<u>117</u>	<u>1011 0111</u>
+ 0 0110	↓
	1011 1101

Adding + 6       $\begin{array}{r} 1011 \\ + 0110 \\ \hline 00010001 \end{array}$       0111.

for correction       $\begin{array}{r} 00010001 \\ - 0110 \\ \hline 0000 \end{array}$

$\begin{array}{r} 00010001 \\ \downarrow \quad \downarrow \quad \downarrow \\ 1 \quad 1 \quad 1 \end{array}$

Q3. Add  $(569)_{10}$  and  $(687)_{10}$  using BCD arithmetic.

Ans.

Decimal

569

687

1256

Adding + 5

for correction

→ carry is  
1

0101    0110    1001

0110    1000    0111

1011    1111    0000

0110    0110    0110

0001    0010    0101    0110

1    2    5    6

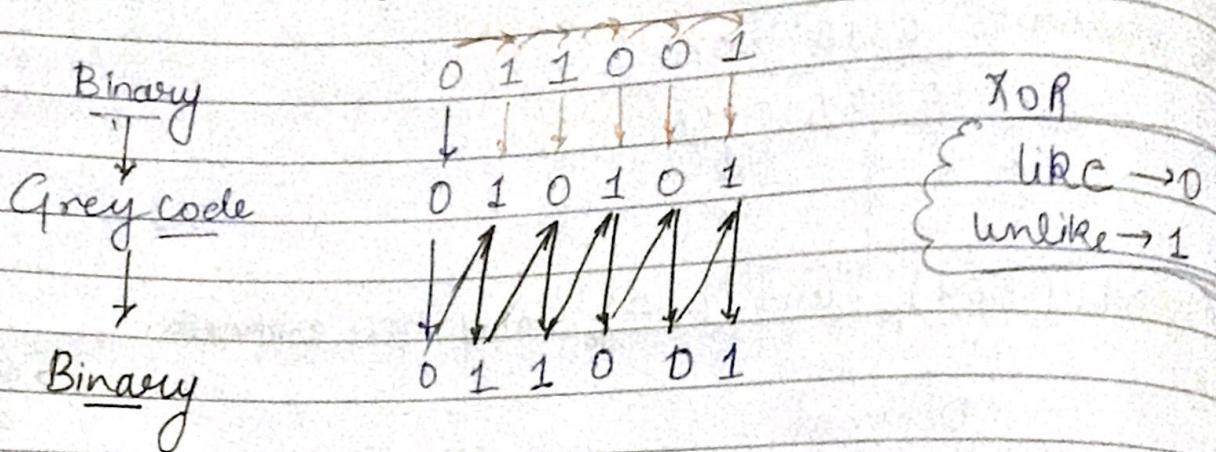
② Non-Weighted code: These codes are not assigned with any weight to each digit position.

Ex: Excess-3 and Grey code

#### A. Excess-3

Decimal	Excess-3
0	0011
1	0100
2	0101
3	0110
4	0111
5	01000
6	1001
7	1010
8	1011
9	1100

B) Grey code :- ① Weighted <sup>Non-</sup> ② Reflective code ③ X-OR implementation



23/09/22

Decimal	Binary	Grey Code	→ generally change in one bit i.e. to get stable condition
0	0000	0000	getting repeated as mirror image
1	0001	0001	stable condition
2	0010	0011	as mirror image
3	0011	0010	We prefer grey code
4	0100	0110	in digital system ∵
5	0101	0111	quad there is only a single bit change
6	0110	0101	single bit change
7	0111	0100	in the grey code
8	1000	1100	for successive binary numbers
9	1001	1101	
10	1010	1111	
11	1011	1110	Mirror image :
12	1100	1010	(0 to $2^n - 1$ ) mirror image
13	1101	1011	( $2^n$ to $2^{n+1} - 1$ )
14	1110	1001	
15	1111	1000	

Grey Code is called Reflective code or Self-complementary code?

- Self Reflecting / Self complementary

~~Ans.~~ Grey codes are called self-reflecting code because the 2 LSBs from 4 to 7 are the mirror image for those from 0 to 3 similarly, the 3 significant bits from 8 to 15 are the mirror images from 0 to 7. In general,  $2^n$  to  $2^{n+1}-1$  are the mirror images of from 0 to  $2^n-1$

## BOOLEAN ALGEBRA

### ★ Basic properties:

1) Commutative law: •  $A + B = B + A$   
                           •  $A \cdot B = B \cdot A$

2) Associative law: •  $(A + B) + C = A + (B + C)$   
                           •  $(A \cdot B) \cdot C = A \cdot (B \cdot C)$

3) Distributive law: •  $A \cdot (B + C) = A \cdot B + A \cdot C$

4) AND law: •  $A \cdot 0 = 0$   
                            $A \cdot 1 = A$   
                            $A \cdot A = A$

$A \cdot \bar{A} = 0$  \*  $\rightarrow$  0

5) OR law: •  $A + 0 = A$   
                            $A + 1 = 1$   
                            $A + A = A$   
                            $A + \bar{A} = 1$   $\rightarrow$  1

6)  $\bar{\bar{A}} = A$

7) Other laws:

1)  $A + AB = A$

2)  $A + \bar{A}B = A + B$

3)  $(A+B)(A+C) = A + BC$

$$\begin{aligned} ① \quad A + AB &= A \cdot (1 + B) \\ &= A \cdot 1 \\ &= A \end{aligned}$$

$$\begin{aligned} ② \quad A + \bar{A}B &= (A + \bar{A})(A + B) \quad \text{shortcut} \\ &= 1(A + B) \\ &= A + B \end{aligned}$$

$$\begin{aligned} ③ \quad (A+B)(A+C) &= A+BC \\ &= A \cdot A + A \cdot C + B \cdot A + BC \\ &= A + A \cdot B + A \cdot C + BC \\ &= A(1+B) + AC + BC \\ &= A \cdot 1 + AC + BC \\ &= A(1+C) + BC \\ &= A \cdot 1 + BC \\ &= A + BC \end{aligned}$$

★ Duality Theorem: Theorem of Boolean algebra

↳ Duality Principle: It states that in a two-valued Boolean algebra, the dual of an algebraic expression can be obtained simply by interchanging AND(.) and OR(+) operators and by replacing ones(1's) by (0's) and zeros(0's) by ones(1's).

$$\begin{aligned} \text{Ex: } A + BC &\Rightarrow A \cdot (B+C) \\ &= A \cdot B + A \cdot C \\ &= A \end{aligned}$$

Q:

Q. Find the dual of the following expression

$$1. A + AB = A \cdot (A+B)$$

Solving,  $= A \cdot A + A \cdot B$   
Dual  $\rightarrow = A \cdot (1+B) = A$

$$2. A + \overline{A}B = A \cdot (\overline{A} + B)$$

$$= A \cdot \overline{A} + A \cdot B$$

$$= \underline{A} + AB$$

$$= \underline{AB}$$

$$3. (A+B)(A+C) = A \cdot (B+C)$$

\* De Morgan's Theorem: combination of two theorems

$$\textcircled{1} \quad \overline{A \cdot B} = \overline{A} + \overline{B} \quad \text{NAND} \equiv \text{Bubble OR}$$

$$\textcircled{2} \quad \overline{A + B} = \overline{A} \cdot \overline{B} \quad \text{NOR} \equiv \text{Bubbled AND}$$

$$\begin{aligned} \text{Q1 Simplify: } Y &= (\overline{AB} + \overline{A} + AB) &= \overline{AB} + \overline{A} + \overline{AB} \\ &= \cancel{\overline{AB}} + \cancel{\overline{A}} + \cancel{AB} \\ &= AB \cdot A \cdot (\overline{A} + \overline{B}) \\ &= AB \cdot (A \cdot \overline{A} + A \cdot \overline{B}) \\ &= AB \cdot A \overline{B} \\ &= A(B\bar{B}) \\ &= A \cdot 0 = 0 \end{aligned}$$

30/09/23

\* Canonical form: (standard form)

$$F(A, B, C) = \overline{AB} + \overline{BC} + ABC \quad // \text{in simplified form}$$

$$\begin{aligned} \hookrightarrow \text{SOP: } &= A\overline{B}(C + \overline{C}) + (\overline{A} + A)\overline{B}\overline{C} + ABC \\ &= A\overline{B}C + A\overline{B}\overline{C} + \overline{A}B\overline{C} + AB\overline{C} + ABC \end{aligned}$$

~~De Morgan's (AB + AC + BC)~~. Convert  $A\overline{B}$  to POS form

$$\hookrightarrow A\overline{B} = (A\overline{B} + C\overline{C})$$

$$\hookrightarrow (A\overline{B} + C)(A\overline{B} + \overline{C})$$

$$= (C + A)(C + \overline{B})(\overline{C} + A)(\overline{C} + \overline{B})$$

$$= (A + C)(\overline{B} + C)(A + \overline{C})(\overline{B} + \overline{C})$$

$$= (A + BB + C)(A\overline{A} + \overline{B} + \overline{C})(A + BB + \overline{C})(A\overline{A} + \overline{B} + \overline{C})$$

$$= (A + C + B)(A + C + \overline{B})(A + \overline{B} + C)(\overline{A} + \overline{B} + C)(A + \overline{C} + B)(A + \overline{C} + \overline{B})$$

$$= (A + \overline{B} + C)(\overline{A} + \overline{B} + \overline{C})$$

$$= (A + B + C)(A + \overline{B} + C)(\overline{A} + \overline{B} + C)(A + B + \overline{C})(\overline{A} + \overline{B} + \overline{C})$$

$$(A + B + \overline{C})$$

### Minterm & Maxterm

0 → False  
1 → True

0 → True  
1 → False

Term	A	B	C	SOP Minterm (m)	(I) Maxterm (M) POS (O)
0	0	0	0	m <sub>0</sub> $\bar{A}\bar{B}\bar{C}$	M <sub>0</sub> A+B+C
1	0	0	1	m <sub>1</sub> $\bar{A}\bar{B}C$	M <sub>1</sub> A+B+ $\bar{C}$
2	0	1	0	m <sub>2</sub> $\bar{A}B\bar{C}$	M <sub>2</sub> A+ $\bar{B}$ +C
3	0	1	1	m <sub>3</sub> $\bar{A}BC$	M <sub>3</sub> A+ $\bar{B}$ + $\bar{C}$
4	1	0	0	m <sub>4</sub> $A\bar{B}\bar{C}$	M <sub>4</sub> $\bar{A}+B+C$
5	1	0	1	m <sub>5</sub> $A\bar{B}C$	M <sub>5</sub> $\bar{A}+B+\bar{C}$
6	1	1	0	m <sub>6</sub> $AB\bar{C}$	M <sub>6</sub> $\bar{A}+\bar{B}+C$
7	1	1	1	m <sub>7</sub> ABC	M <sub>7</sub> $\bar{A}+\bar{B}+\bar{C}$

### SOP and POS expression from Truth Table.

- Ex: HALF ADDER

A	B	Sum (S)	Carry (C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

- Expression in SOP form:

$$S = \bar{A}B + \bar{B}A = A \oplus B \Rightarrow m_1 + m_2$$

$$C = AB \Rightarrow m_3$$

- POS Expression

$$S = (\bar{A}B)(\bar{A}+\bar{B}) \rightarrow M_0 \cdot M_3$$

$$C = (A+B)(A+\bar{B})(\bar{A}+B) \rightarrow M_0 + M_2 \cdot M_1$$

A	B	C	Y	Minterm	Maxterm
0	0	0	0		$M_0$
0	0	1	1	$m_1$	
0	1	0	0		$M_2$
0	1	1	0		$M_3$
1	0	0	1	$m_4$	
1	0	1	0		$M_5$
1	1	0	0		$M_6$
1	1	1	1	$m_7$	

Minterm (1)  $\rightarrow 0 \rightarrow \text{False} \quad 1 \rightarrow \text{True}$

SOP =

$$\begin{aligned} F(A, B, C) &\Rightarrow m_1 + m_4 + m_7 \\ &\Rightarrow \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC \\ &\Rightarrow \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC \end{aligned}$$

POS  $\rightarrow$  Maxterm (0)  $\rightarrow 1 \rightarrow \text{False} \quad 0 \rightarrow \text{True}$

$$F(A, B, C) = M_0 M_2 M_3 M_5 \cancel{M_6}$$

$$\Rightarrow (A+B+C)(A+\bar{B}+C)(A+B+\bar{C})(\bar{A}+\bar{B}+\bar{C})$$

$$(\bar{A}+\bar{B}+\bar{C})$$

$$\Rightarrow (A+B+C)(A+\bar{B}+C)(A+B+\bar{C})(\bar{A}+\bar{B}+\bar{C})(\bar{A}+\bar{B}+C)$$

Q. Simplify the expression given below.

$$Y = AB + AB(\bar{A} + B)$$

$$Y = AB + A\bar{B}\bar{A} + AB\cdot B$$

$$Y = AB + \bar{B} + AB$$

$$\boxed{Y = AB}$$

$\Rightarrow AB$

3/10/22

\* Karnaugh Map (K-Map):

→ As Boolean algebra is limited up to 6 variables

Case I:  $F(A, B) = \bar{A}\bar{B} + AB$

Case I: Using 2 variable SOP 1 → True 0 → False. Minterm

A	B	0	1	0	1
0	0	$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	$AB$
1	1	$A\bar{B}$	$AB$	$\bar{A}B$	$AB$

A	B
0 → 0	0
1 → 0	1
2 → 1	0
3 → 1	1

Case II: Using 3 Variable SOP

Horizontal Orientation:

A	B	C	00	01	11	10
0	0	0	$\bar{A}\bar{B}\bar{C}$	$\bar{A}\bar{B}C$	$\bar{A}BC$	$A\bar{B}\bar{C}$
1	1	1	$ABC$	$A\bar{B}C$	$\bar{A}BC$	$\bar{ABC}$

A	B	C	00	01	11	10
0	0	0	$\bar{A}\bar{B}\bar{C}$	$\bar{A}\bar{B}C$	$\bar{A}BC$	$A\bar{B}\bar{C}$
1	1	1	$ABC$	$A\bar{B}C$	$\bar{A}BC$	$\bar{ABC}$

0	0	0	← 0
0	0	1	← 1
0	1	0	← 2
0	1	1	← 3
1	0	0	← 4
1	0	1	← 5
1	1	0	← 6
1	1	1	← 7

	AC	00	01	11	10
0	B	$\bar{A}\bar{B}C$	$A\bar{B}C$	$A\bar{B}C$	$A\bar{B}C$
1	$\bar{A}B\bar{C}$	$\bar{A}BC$	$ABC$	$ABC$	$ABC$

Vertical Orientation:

	A	0	1
00	B	0	4
01		1	5
11		3	7
10		2	6

Case III Using 4 variables:

	A	B	C	D	AB	CD	00	01	11	10
0 →	0	0	0	0	00		0	1	3	2
1 →	0	0	0	1	01		4	5	7	6
2 →	0	0	1	0	11		12	13	15	14
3 →	0	0	1	1	10		8	9	11	10
4 →	0	1	0	0						
5 →	0	1	0	1						
6 →	0	1	1	0						
7 →	0	1	1	1						
8 →	1	0	0	0						
9 →	1	0	0	1						
10 →	1	0	1	0						
11 →	1	0	1	1						
12 →	1	1	0	0						
13 →	1	1	0	1						
14 →	1	1	1	0						
15 →	1	1	1	1						

Moct'22

	AB	CD
10	1	1
11	1	1
01	1	0
00	0	1

$$(1) \text{ Single - LC's} \quad f_{(A,B,C,D)} = m_0 + m_2 + m_3 + m_4 + m_5 + m_8 + m_7 + m_{11} + m_{12}$$

(S)  
82  
112

A

May 15

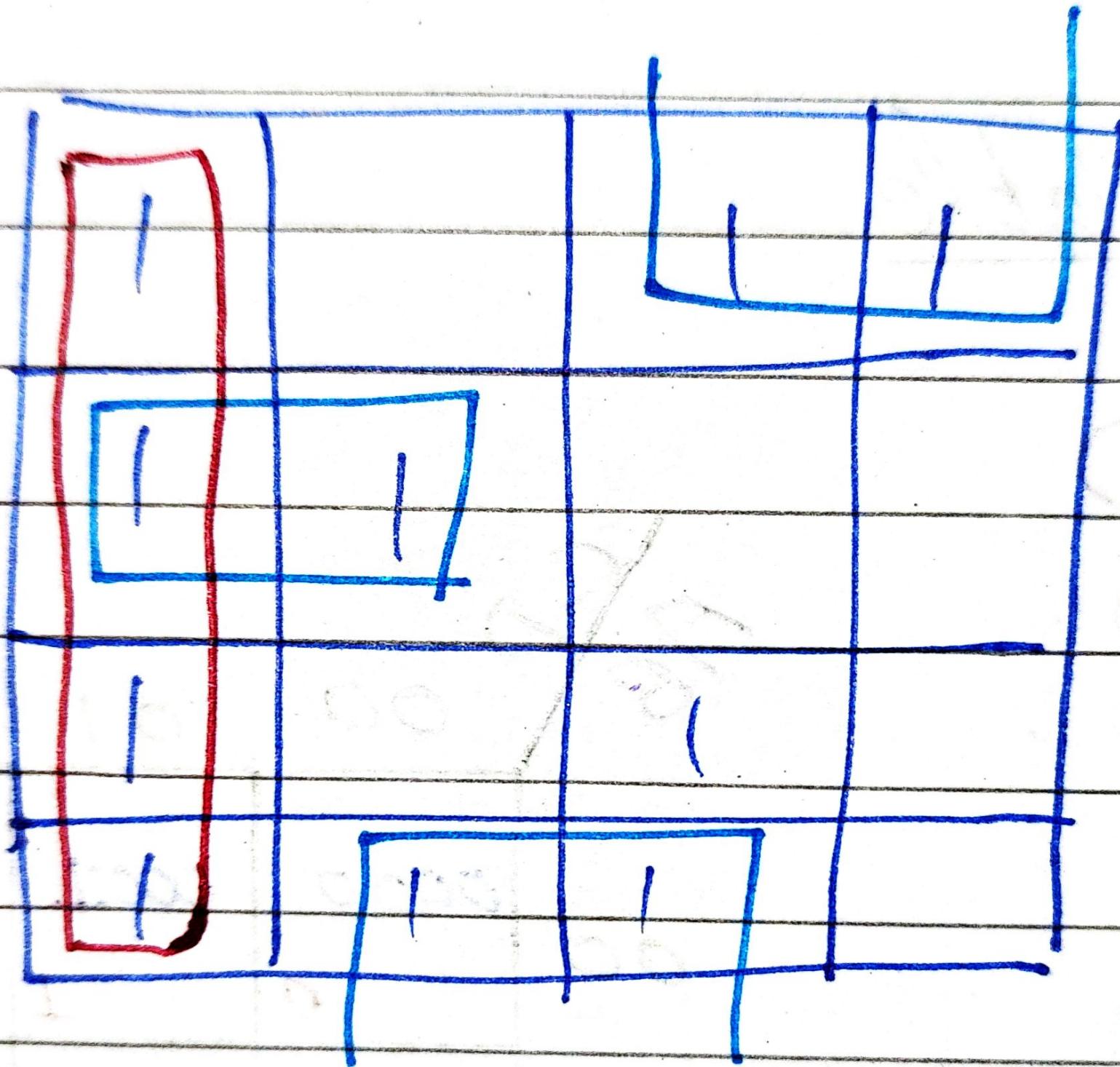
- 162 -

## 3. Grade 4 - part 3

Octate - 8 (1's)

12

10

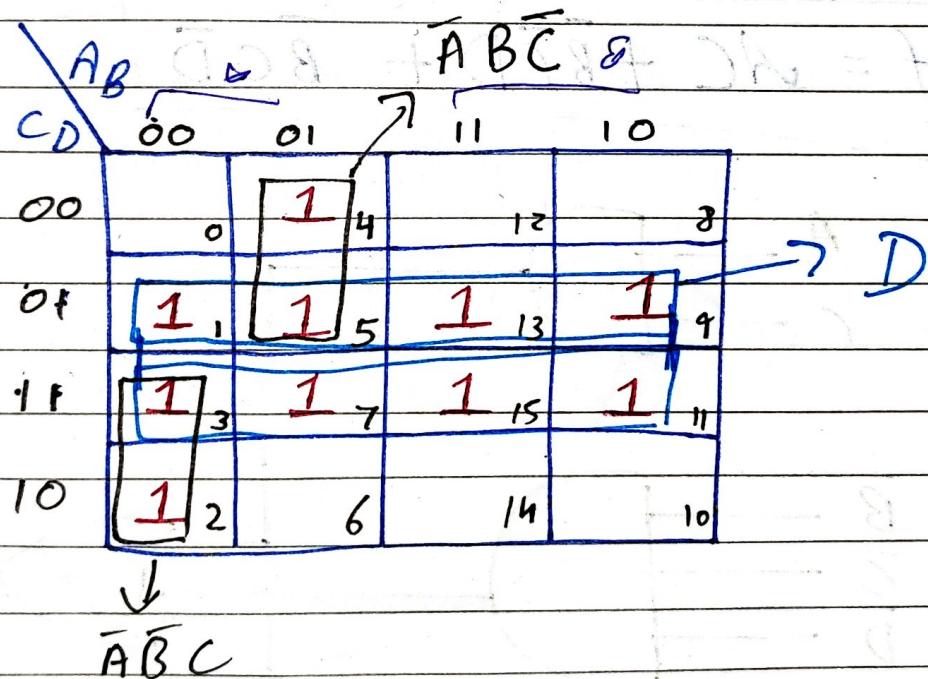


	CD AB	00	01	11	10
00					
01					
11					
10					

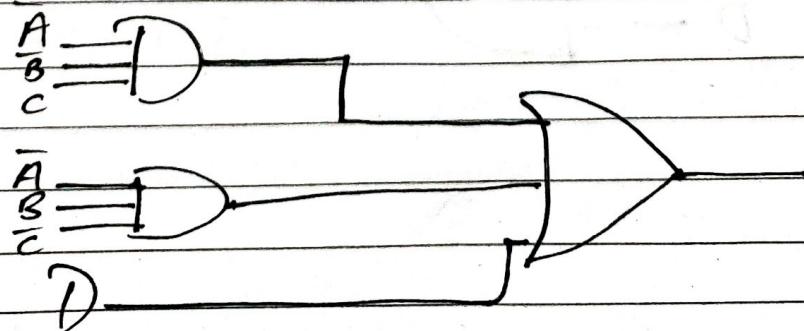
realis.

Q3 Using k-Map Reduce the following expression using Minimum no. of gates.

$$Y = \sum m(1, 2, 3, 4, 5, 7, 9, 11, 13, 15)$$

Ans)

$$f = A'B'C + A'B'C'D + D$$



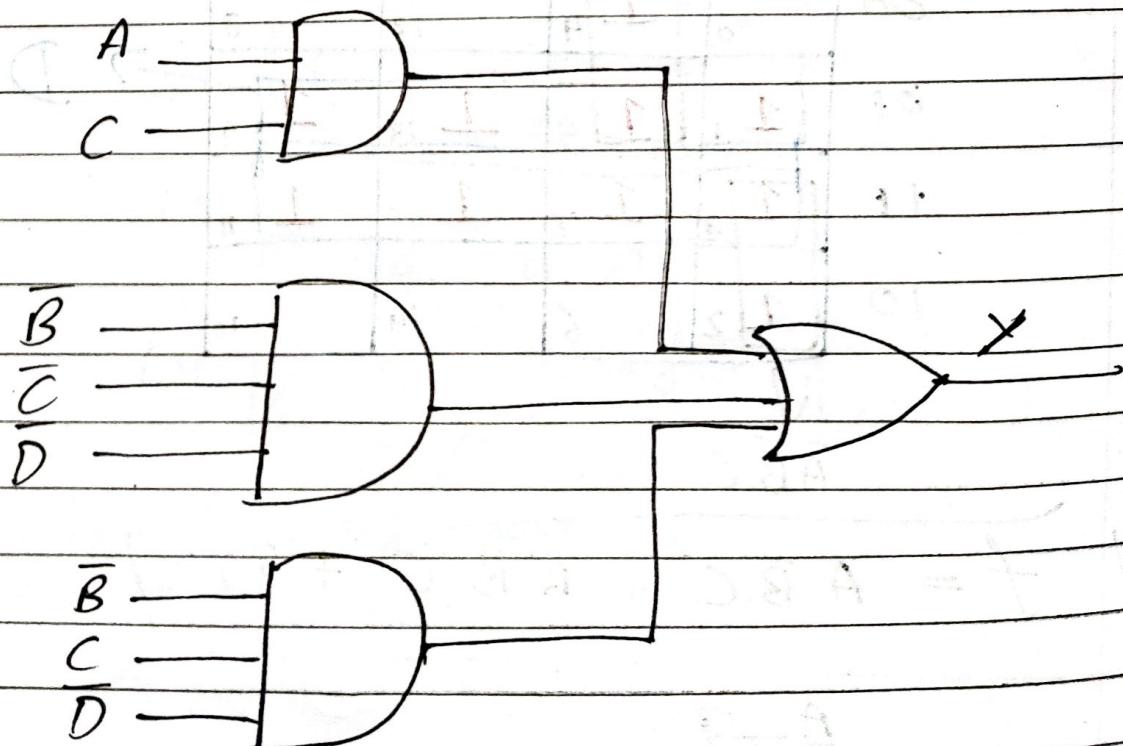
Ques Minimise the following using K-MAP and Realise using Basic Gates.

$$Y = \sum m(1, 2, 9, 10, 11, 14, 15)$$

Ans)

		AB	CD	00	01	11	10	
		CD	00	0	4	12	8	
		01	1	5	13	1	9	
		11	3	7	15	1	11	
		10	12	6	14	1	10	

$$f = AC + \bar{B}\bar{C}D + \bar{B}C\bar{D}$$



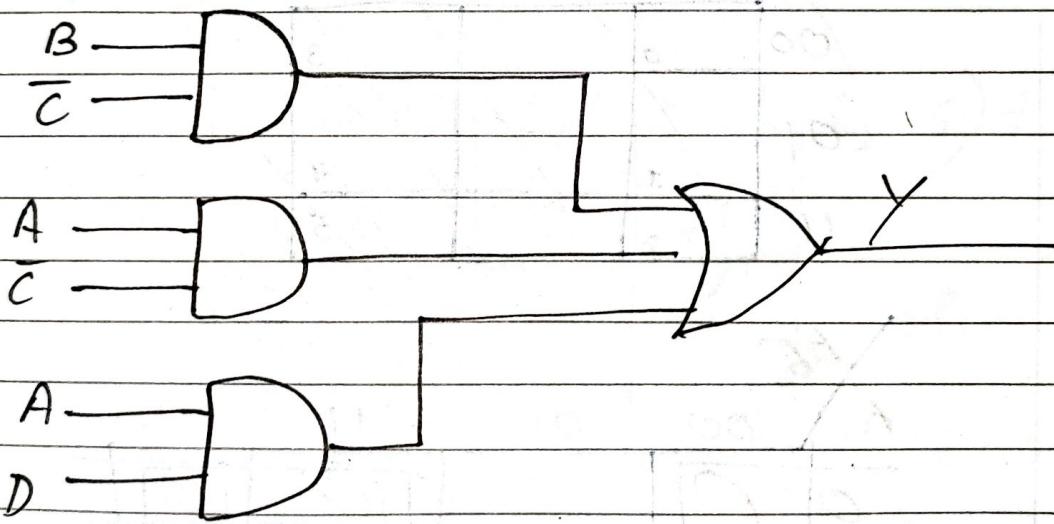
Ques → Minimise the following exp. using K-MAP and Basic Gates.

$$Y = \sum m(4, 5, 8, 9, 11, 12, 13, 15)$$

Ans)

		00	01	11	10
		00	0	1 <sub>4</sub> 1 <sub>2</sub>	1 <sub>8</sub>
		01	1	1 <sub>5</sub> 1 <sub>13</sub>	1 <sub>1</sub>
		11	3	1 <sub>15</sub>	1 <sub>11</sub>
		10	2	6	14
					10

$$Y = BC + AC + AD$$



Ques → Minimise the logic expression:

$$Y = \overline{ABC}D + \overline{AB}CD + \overline{ABC} + \overline{AB}D + A\overline{C} + \overline{B}$$

Ans)

		CD	AB	00	01	11	10
			00	1	1	1	1
			01				1
			11	1	1		
			10	1	1	1	1

$$= \bar{B} + A\bar{C} + \bar{A}B\bar{C}$$

Q) Simplify the following expression using K-map

$$Y = \Sigma M(0, 2, 3, 5, 7)$$

Ans)

		AB	CD	00	01	11
		00	0			3
		01	1			4
		11	2			5

~~BC~~

		AB	CD	00	01	11	10
		00	0	0		0	0
		01	1		0	0	
		11					
		10					

(A+1)

1

$\bar{A} + \bar{C}$

$\bar{B} + \bar{C}$

$$Y = (A+1)(\bar{A}+\bar{C})(\bar{B}+\bar{C})$$

Q→

Minimise The following expression :

$$Y = \prod M(0, 2, 3, 5, 7, 9, 12, 13, 15)$$

Ans

		CD	00	01	11	10
		00	0	4	12	8
		01	1	5	3	9
		11	3	7	15	11
		10	2	6	14	10

Don't Care  $\rightarrow X_{08} d$

$$Y = \sum m(0, 2, 3, 5, 7, 15) +$$

$$d(12, 13, 14)$$

CD	HB	1	1	1	1	$\bar{A}\bar{B}\bar{D}$	$\bar{A}CD$
X	X	1	1	1	X		
X	X				X	$\rightarrow$ NO Need to make pair	

BD

Ques)

Simplify using Don't Care:

$$Y = \sum m(1, 3, 7, 11, 15) + d(0, 2, 5)$$

Ans)

	00	01	11	10
0	0	2	6	4
1	1	3	7	5

06/10/22

Date  
Page

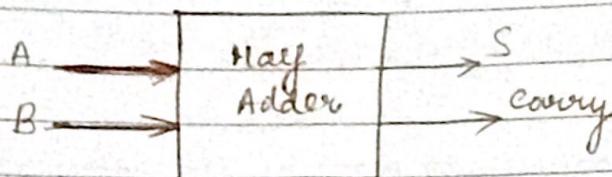
Thursday

- \* Combinational logic Circuit: 1) Adders  
 2) Subtractors  
 3) Code converters  
 4) Magnitude Comparator

 Segmented  
 memory  
 logic gate  
 combinational  
 logic circuit

- \* Adders → Half adder  
 → full adder

- ① Half Adder:



		Input	Output		
		A	B	S	C
		0	0	0	0
		0	1	1	0
		1	0	1	0
		1	1	0	1

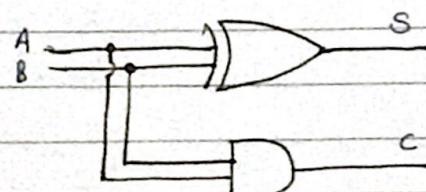
A	B	0	1	A	B	0	1
0	0	1		0	0		
1	1	1		1	1	1	

$$S = A\bar{B} + \bar{A}B$$

$$= A \oplus B$$

$$C = AB$$

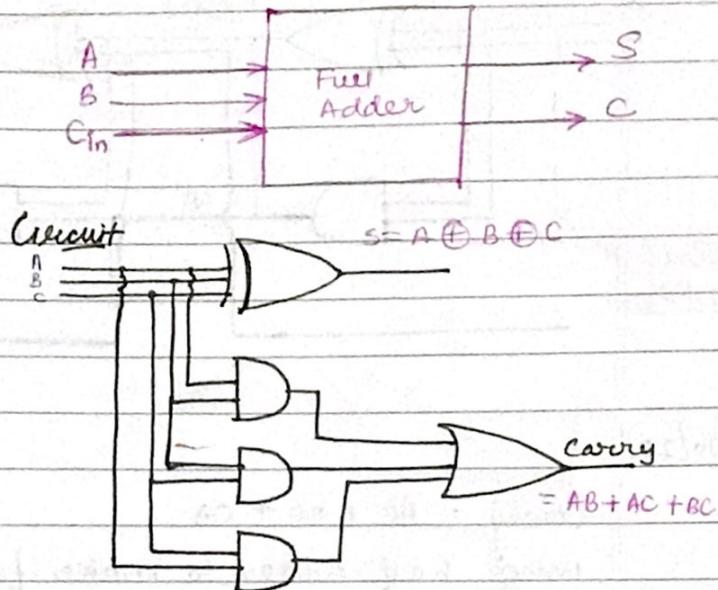
logic



- Drawback of Half Adder: A half adder can add only 2 inputs. However while we add 2 nos. the result may consist carry. This carry needs to be added into successive bits. This can only be done with the help of full adder.

## ★ Full Adder:

Inputs	Outputs			
A	B	C <sub>in</sub>	S	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Sum

BC		00	01	11	10
A	C <sub>in</sub>	0	1	1	0
0	0	0	1	1	0
1	1	1	0	1	1

→ Sum

$$S = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC$$

$$S = \overline{A}\overline{B}C + ABC + \overline{A}B\overline{C} + A\overline{B}\overline{C}$$

$$= C(\overline{A}\overline{B} + AB) + \overline{C}(\overline{A}B + \overline{B}A) \quad \text{using } \overline{AB} + AB = A \oplus B \&$$

$$= C(A \oplus B) + \overline{C}(A \oplus B) \quad \text{using } \overline{\overline{A} \oplus B} = A \oplus B \&$$

$$= C(A \oplus B) + \overline{C}(A \oplus B) \quad \text{using } \overline{A \oplus B} = A \oplus B$$

$$\boxed{S = C \oplus A \oplus B}$$

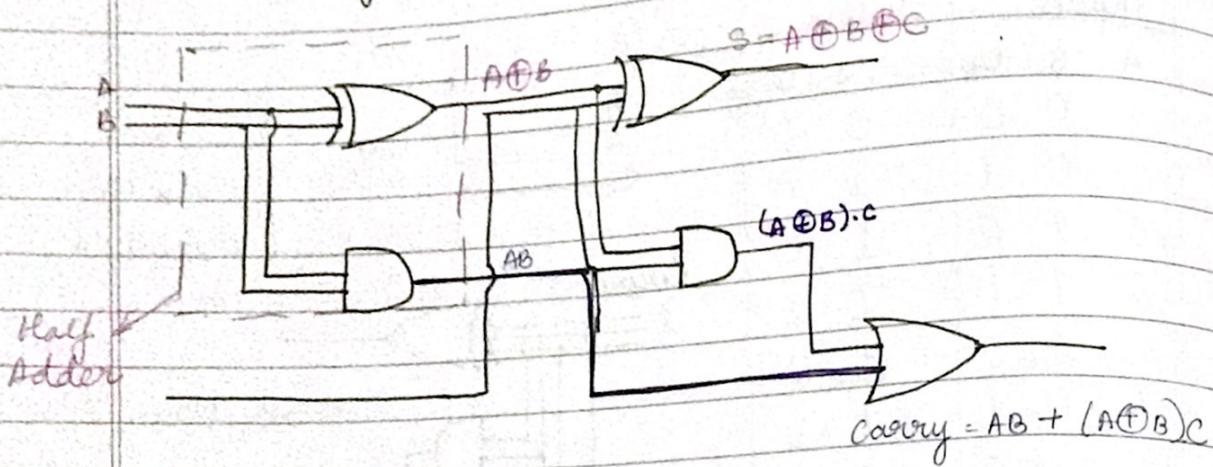
Carry

BC		00	01	10	11
A	C <sub>in</sub>	0	1	1	1
0	0	0	1	1	1
1	1	1	0	1	1

AC → AB

$$C = AC + AB + BC$$

\* Full adder using Half adder:-



10/10/22

$$\text{Carry} = AB + BC + CA$$

using half adder to make full adder

$$\text{we get } \text{Carry} = AB + (A \oplus B)C$$

$$= (\bar{A}B + A\bar{B})C + AB$$

$$= A\bar{B}C + \bar{A}BC + AB(1+C) [1+C=1]$$

$$= A\bar{B}C + \bar{A}BC + AB + ABC$$

$$= A\bar{B}C + (A + \bar{A})BC + AB$$

$$= A\bar{B}C + BC + AB(1+C)$$

$$= AB + ABC + A\bar{B}C + BC$$

$$= AB + AC(B + \bar{B}) + BC$$

$$\boxed{\text{Carry} = AB + AC + BC} \quad (\text{Hence Proved})$$



Subtractors:-

$$0 - 0 = 0$$

$$1 - 0 = 1$$

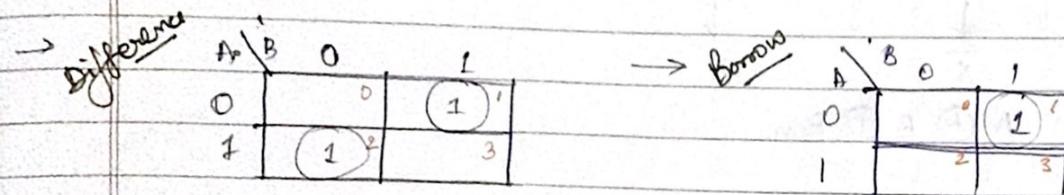
$$0 - 1 = 1 \text{ with borrow}$$

$$1 - 1 = 0$$

\* Half - Subtractor:

→ Truth Table:

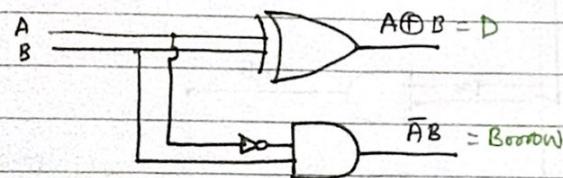
A	B	D	Borrow
0	0	0	0
1	0	1	1
2	1	0	0
3	1	1	0



$$\begin{aligned} D &= A\bar{B} + \bar{A}B \\ &= A \oplus B \end{aligned}$$

$$\text{Borrow} = \bar{A}B$$

logic:  
Diagram

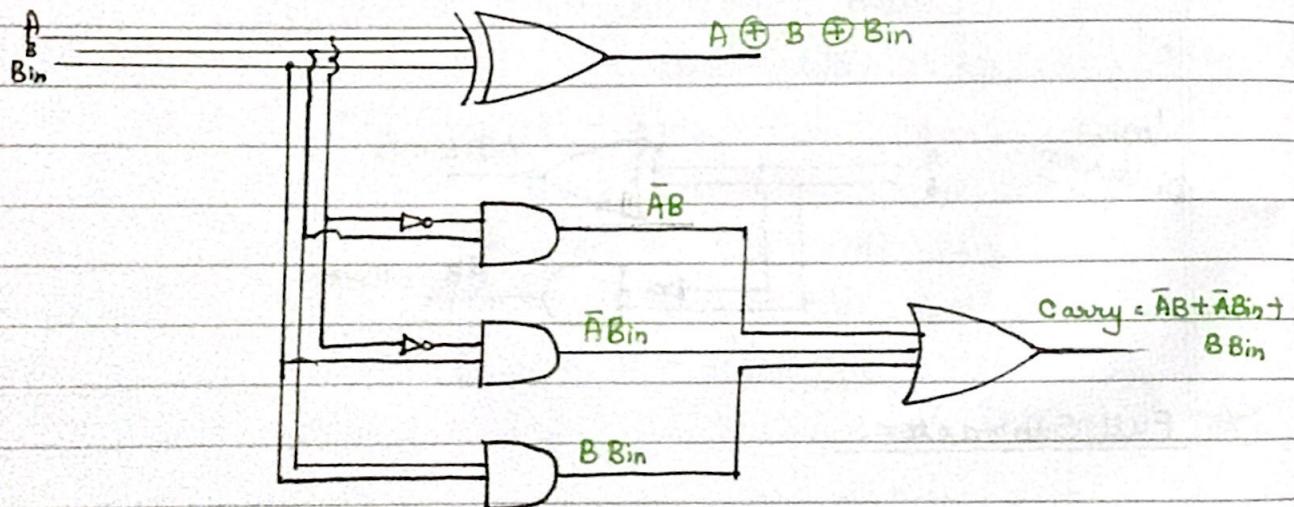


\* Full Subtractor:

A	B	Bin	D	Borrow
0	0	0	0	0
1	0	1	1	1
0	1	0	1	1
0	1	1	0	01
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

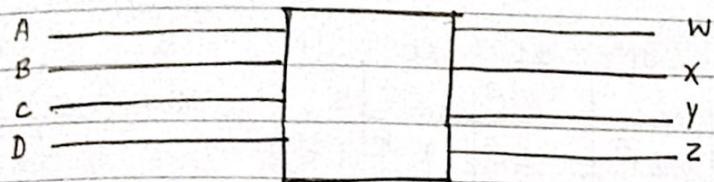
		difference A				Borrow				AB Bin	
		BBin	00	01	11	10	BBin	00	01	11	10
	A	0	1	1	1	1	0	1	1	1	AB
		1	1	1	1	1	1	0	1	1	
D =	$A\bar{B}\bar{B}_{\text{bin}} + \bar{A}\bar{B}B_{\text{bin}} + AB\bar{B}_{\text{bin}} + \bar{A}B\bar{B}_{\text{bin}}$						$\text{Borrow} = \bar{A}B_{\text{bin}} + \bar{A}B + BB_{\text{bin}}$				
=	$(\bar{A}\bar{B} + AB)_{\text{bin}} + (\bar{A}B + A\bar{B})\bar{B}_{\text{bin}}$										
=	$(A \odot B)_{\text{bin}} + (A \oplus B)\bar{B}_{\text{bin}}$										
=	$(A \oplus B)_{\text{bin}} + (A \oplus B)\bar{B}_{\text{bin}}$										
	X		X								
D =	$A \oplus B \oplus B_{\text{bin}}$										

logic design:



11/10/22

Code converter:



A . B . C . D	w x y z
0 0 0 0	0 0 0 0
0 0 0 1	0 0 0 1
0 0 1 0	0 0 1 1
0 0 1 1	0 0 1 0
0 1 0 0	0 1 1 0
0 1 0 1	0 1 1 1
0 1 1 0	0 1 0 1
0 1 1 1	0 1 0 0
1 0 0 0	1 1 0 0
1 0 0 1	1 1 0 1
1 0 1 0	1 1 1 1
1 0 1 1	1 1 1 0
1 1 0 0	1 0 1 0
1 1 0 1	1 0 1 1
1 1 1 0	1 0 0 1
1 1 1 1	1 0 0 0

K-Map:

• For W

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	1 <sup>12</sup>	1 <sup>13</sup>	1 <sup>15</sup>	1 <sup>14</sup>
10	1 <sup>8</sup>	1 <sup>9</sup>	1 <sup>11</sup>	1 <sup>10</sup>

$W = A$

• For X

$\backslash$	AB	CD	00	01	11	10
00	0		1	3	2	
01	14	15	17	16		
11		12	13	15	14	
10	18	19	11	10		

$X = \overline{A}B + A\overline{B} = A \oplus B$

• For Y

$\backslash$	AB	CD	00	01	11	10
00	0	1	1	3	1	2
01	14	15		7	6	
11	12	13		15	14	
10	8	9	1	10	1	10

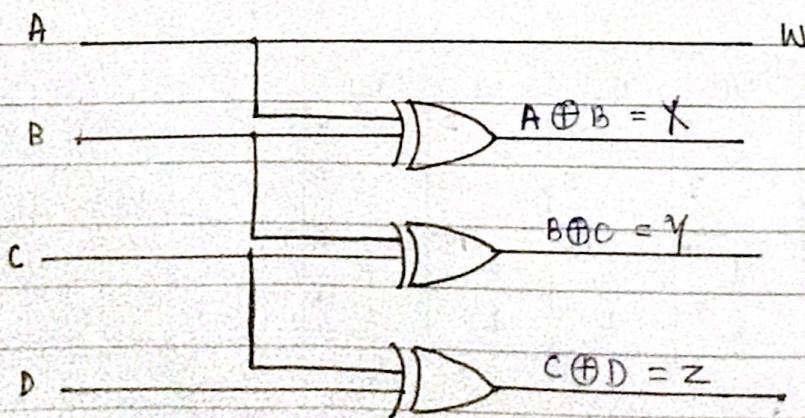
$Y = B\overline{C} + \overline{B}C = B \oplus C$

• For Z

$\backslash$	AB	CD	00	01	11	10
00	0	1	1	3	1	2
01	4	15		7	16	
11	12	13		15	14	
10	8	19		11	10	

$Z = \overline{C}D + C\overline{D} = C \oplus D$

Logic design



★ Magnitude Comparator : (1-bit)

A	B	$X = A < B$	$Y = A = B$	$Z = A > B$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

For X

A	B	0	1
0		1	
1			

For Y

A	B	0	1
0		1	
1			1

For Z

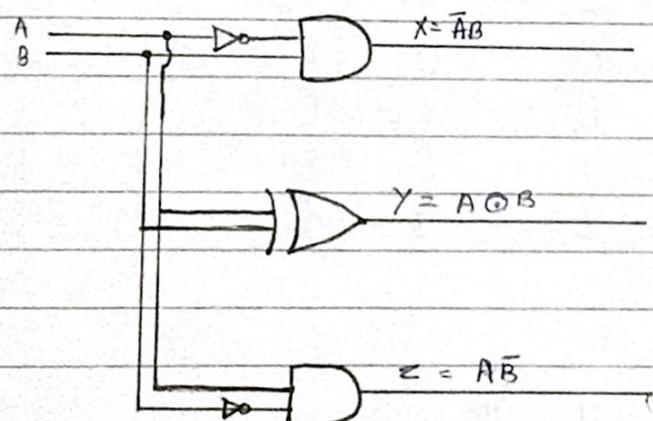
A	B	0	1
0			
1		1	

$$X = \bar{A}B$$

$$Y = \bar{A}\bar{B} + AB \\ = A \oplus B$$

$$Z = A\bar{B}$$

Logic Design



13/10/22

★ 2-bit Magnitude Comparator:-

A	A		B		A → A <sub>1</sub> , A <sub>0</sub>		B → B <sub>1</sub> , B <sub>0</sub>		X A < B	Y A = B	Z A > B
	A <sub>1</sub>	A <sub>0</sub>	B <sub>1</sub>	B <sub>0</sub>	A < B	A = B	B <sub>1</sub>	B <sub>0</sub>			
0	0	0	0	0	0	1	0	0	0	1	0
1	0	0	0	1	1	0	0	1	0	0	0
2	0	0	1	0	1	0	0	0	0	0	0
3	0	0	1	1	1	0	0	1	0	0	0
4	0	1	0	0	0	0	0	0	0	0	1
5	0	1	0	1	0	1	1	0	1	0	0
6	0	1	1	0	1	0	0	1	0	0	0
7	0	1	1	1	1	1	0	1	0	0	0
8	1	0	0	0	0	0	0	0	0	0	1
9	1	0	0	1	0	0	0	1	0	0	1
10	1	0	1	0	0	0	1	0	1	0	0
11	1	0	1	1	01	0	0	1	0	0	0
12	1	1	0	0	0	0	0	0	0	0	1
13	1	1	0	1	0	0	0	1	0	0	1
14	1	1	1	0	0	0	0	0	0	0	1
15	1	1	1	1	1	0	1	1	1	0	0

★ For X

A <sub>1</sub> A <sub>0</sub>		B <sub>1</sub> B <sub>0</sub>		X
00	00	00	00	0
00	01	01	11	1
01	01	11	11	1
11	11	11	11	1
10	10	10	10	1
00	00	00	00	0
00	01	01	11	1
01	01	11	11	1
11	11	11	11	1
10	10	10	10	1

$\bar{A}_1 B_1 + \bar{A}_1 \bar{A}_0 B_0 + \bar{A}_0 B_0 = X$

$\bar{A}C + \bar{A}\bar{B}D + \bar{B}CD = X$

★ For Y

A <sub>1</sub> A <sub>0</sub>		B <sub>1</sub> B <sub>0</sub>		Y
00	00	00	00	0
00	01	01	11	1
01	01	11	11	1
11	11	11	11	1
10	10	10	10	1
00	00	00	00	0
00	01	01	11	1
01	01	11	11	1
11	11	11	11	1
10	10	10	10	1

$\bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + \bar{A}_1 \bar{A}_0 B_0 + A_1 \bar{A}_0 \bar{B}_1 B_0 + A_1 \bar{A}_0 B_1 \bar{B}_0$

\* For Z

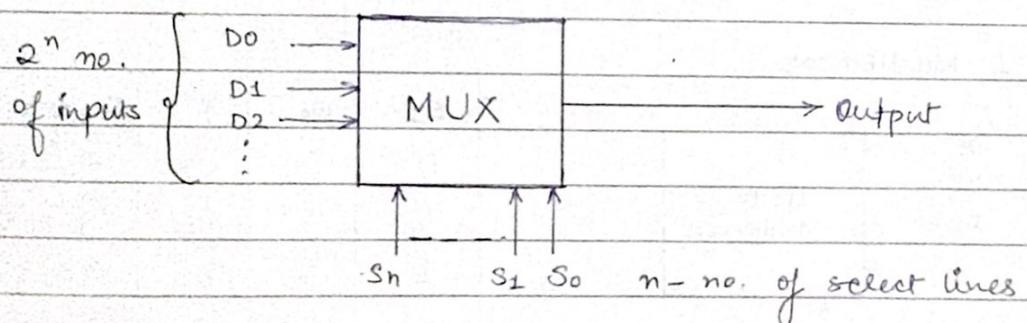
$A_1 A_0 \setminus B_1 B_0$	00	01	11	10	
00	0	1	3	2	$Z = A_1 \bar{B}_1 + A_1 A_0 \bar{B}_0 + A_0 \bar{B}_1 \bar{B}_0$
01	4	5	7	6	
$\cancel{B_0 \bar{B}_1 B_0}$	12	18	10	14	$\rightarrow A_1 A_0 \bar{B}_0$
11	1	9	11	10	
10	8				
					$A_1 \bar{B}_1$

14/10/22

\* Multiplexer / Data Selector:-

Multiplexer is combination device which select one of many data inputs and give single output. The selection of one of input is done by select lines. If there are small n select lines then  $2^n$  inputs can be selected.

→ Advantages of Multiplexer:

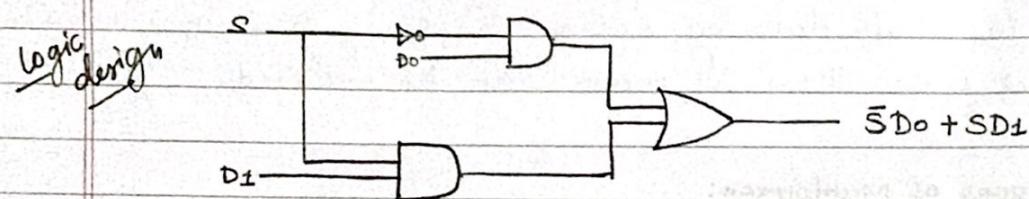
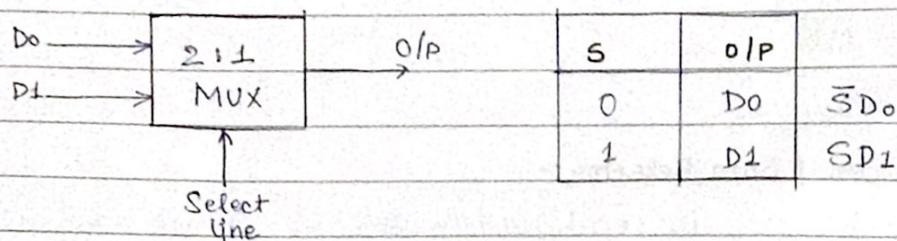


- 1) It reduces the no. of wires
- 2) It reduces the circuit complexity and cost
- 3) We can implement many complex circuit using NAND gate
- 4) It simplifies the logic design
- 5) It doesn't need K-Maps and simplification

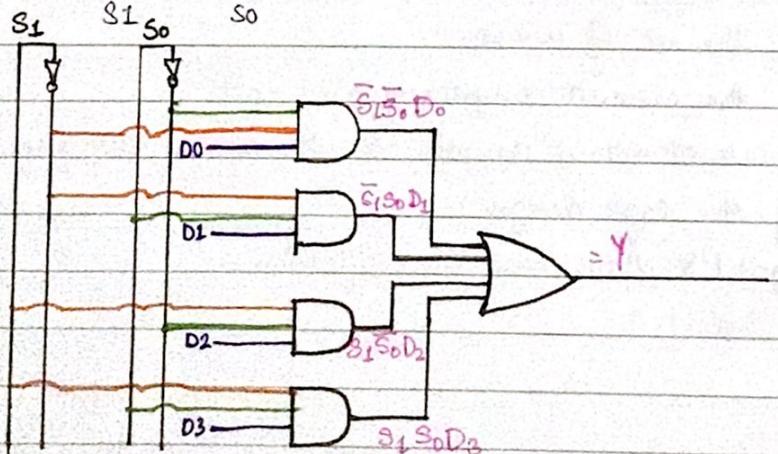
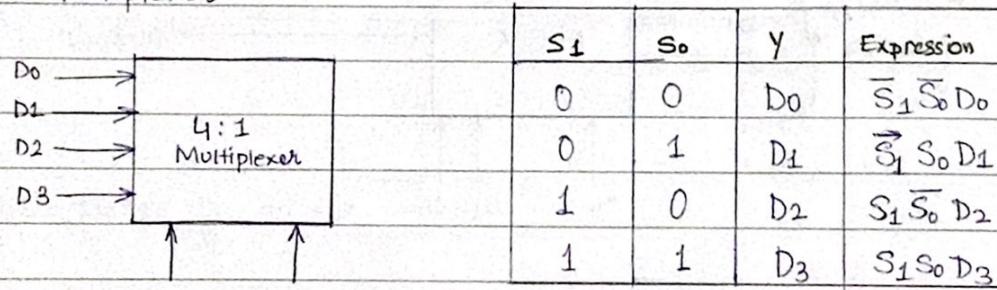
↳ classification of multiplexer

- 1) 2:1 multiplexer
- 2) 4:1 multiplexer
- 3) 8:1 multiplexer
- 4) 16:1 multiplexer

a) 2:1 multiplexer  $\Rightarrow$  2 input - 1 output



b) 4:1 Multiplexer



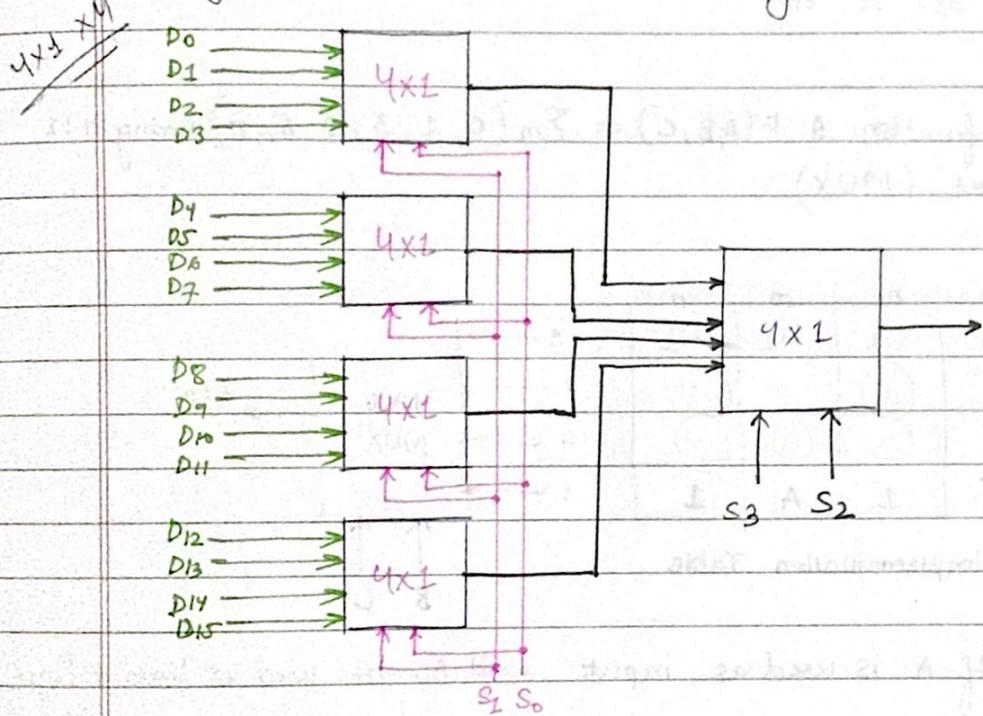
17/10/22

\* Applications of Multiplexer:-

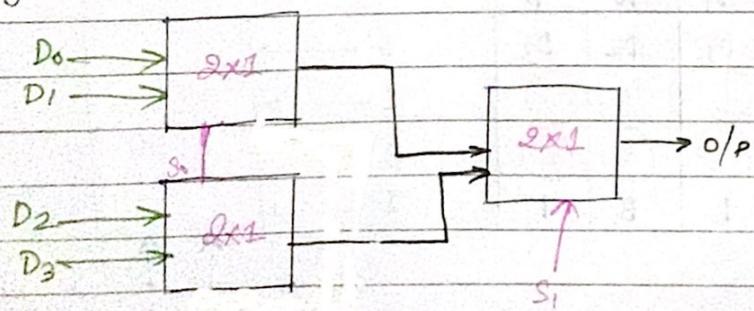
- (1) D/A (Digit to Analog converter)
- (2) As a Data Selector
- (3) In designing combinational circuits
- (4) Parallel to Serial Converter
- (5) Data Acquisition System

\* Multiplexer Trees:

- Q. Design a 16:1 Multiplexer using 4:1 multiplexer.

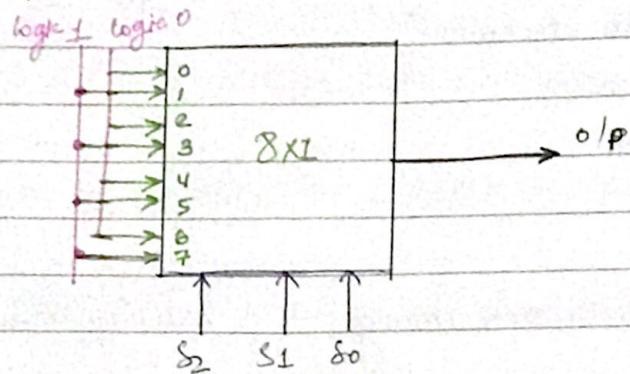


- Q. Design a 4:1 Multiplexer using 2:1 multiplexer



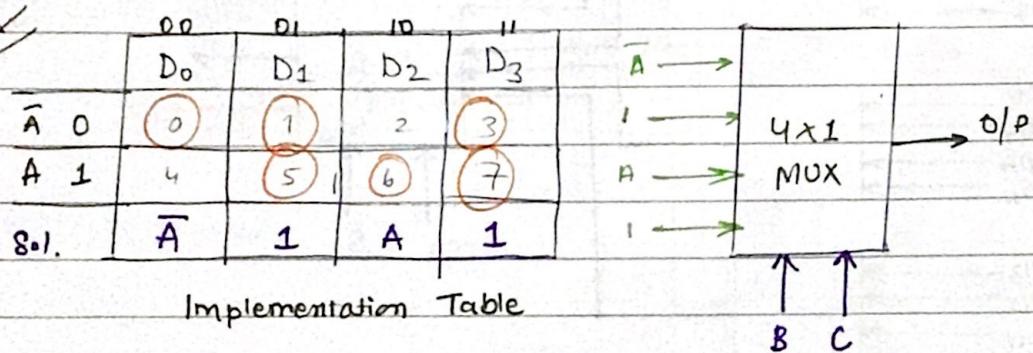
★ Boolean function implementation using Multiplexer

Q1. Implement  $F(A, B, C) = \sum m(1, 3, 5, 7)$  using 8:1 Multiplexers.



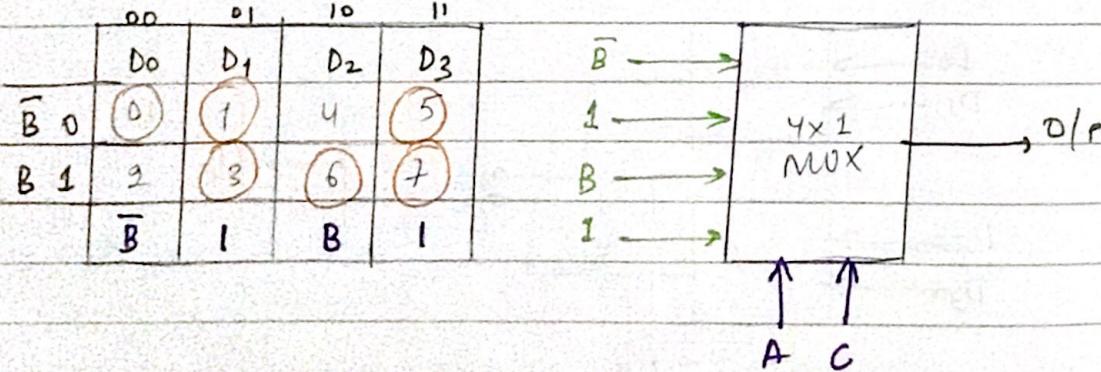
Q2. Implement function  $A F(A, B, C) = \sum m(0, 1, 3, 5, 6, 7)$  using 4:1 Multiplexer. (MUX)

sol.



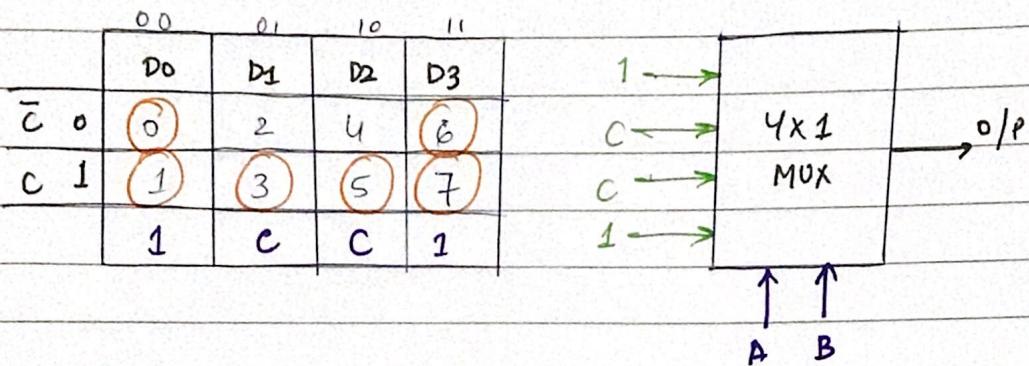
Case I: If A is used as input and BC are used as select lines

Case II: If B is used as input and AC are used as select lines



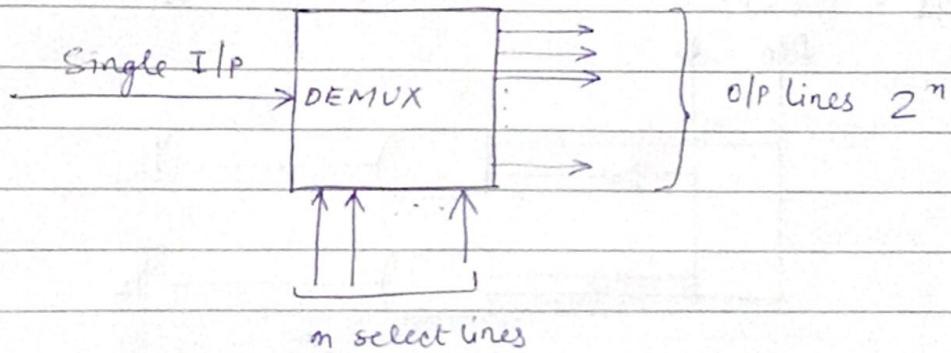
Care III

If C is used as input and AB are used as Select lines.



20/10/22

## \* DEMULTIPLEXER:



- A demultiplexer has a single input, multiple output i.e.  $2^n$  and n select lines. A demultiplexer performs the reverse operation of multiplexer.

- Classification of Demultiplexer:

- 1) 1x2 DEMUX
- 2) 1x4 DEMUX
- 3) 1x8 DEMUX
- 4) 1x16 DEMUX

a) 1x2 DEMUX:

S (select line)	$Y_1$	$Y_2$
0	Din	X
1	X	Din

A block diagram of a 1x2 DEMUX. An input line labeled "S" enters a square "DEMUX" block. Two output lines emerge from the block, labeled " $Y_1$ " and " $Y_2$ ".

Din	S	$Y_1$	$Y_2$
0	0	0	0
1	0	1	0
0	1	0	0
1	1	0	1

K-Map  $Y_1$ 

Din	S	0	1
0			
1		1	

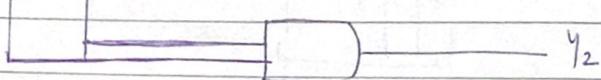
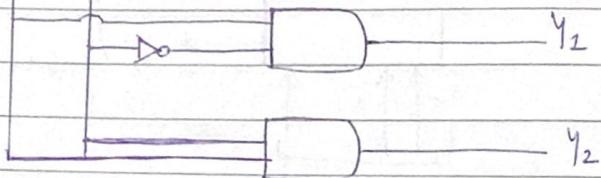
$$Y_1 = D_{in} \bar{S}$$

Din S

K-Map  $Y_2$ 

Din	S	0	1
0			
1			1

$$Y_2 = D_{in} S$$



## b) 1 × 4 DEMUX:

Din	$S_1$	$S_0$	$Y_0$	$Y_1$	$Y_2$	$Y_3$
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

K-map for  $y_0$

Din	$S_1 S_0$	00	01	11	10
0	0				
1	1				

$$Y_0 = \text{Din} \bar{S}_1 \bar{S}_0$$

K-map for  $y_1$

Din	$S_1 S_0$	00	01	11	10
0	0				
1	1		1		

$$Y_1 = \text{Din} \bar{S}_1 S_0$$

K-map for  $y_2$

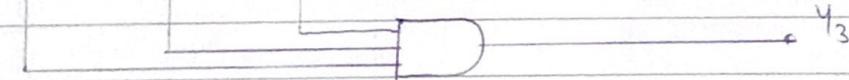
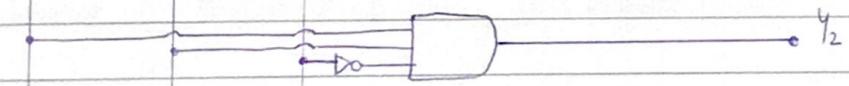
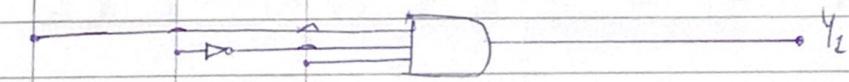
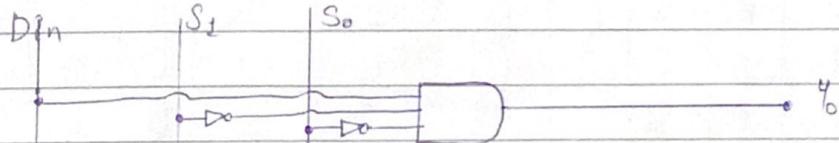
Din	$S_1 S_0$	00	01	11	10
0	0				
1	1				1

$$Y_2 = \text{Din} S_1 \bar{S}_0$$

K-map for  $y_3$

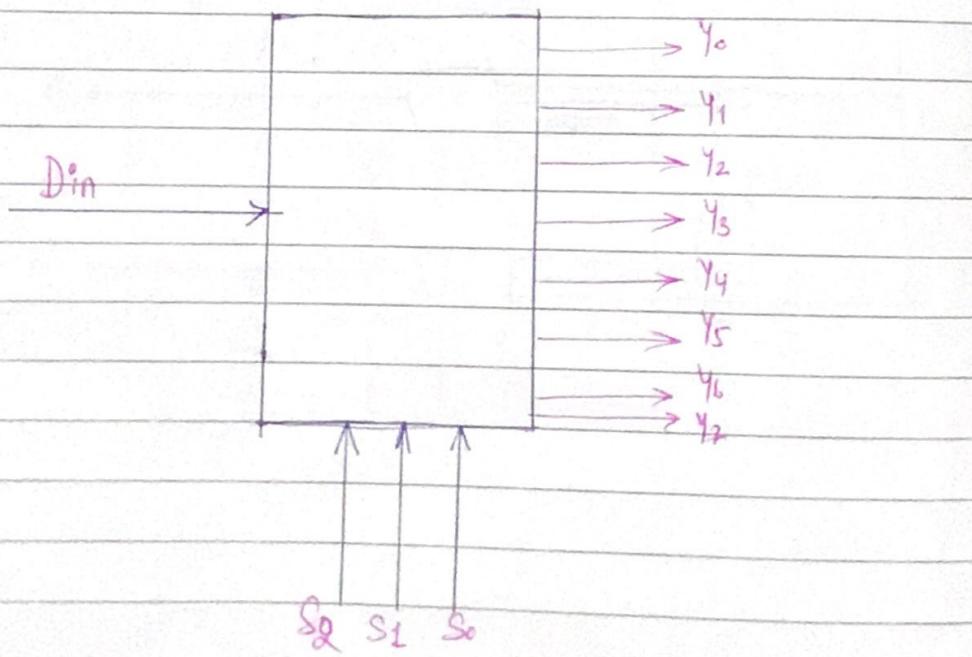
Din	$S_1 S_0$	00	01	11	10
0	0				
1	1		1		

$$Y_3 = \text{Din} S_1 S_0$$



c) 1x8 DEMUX

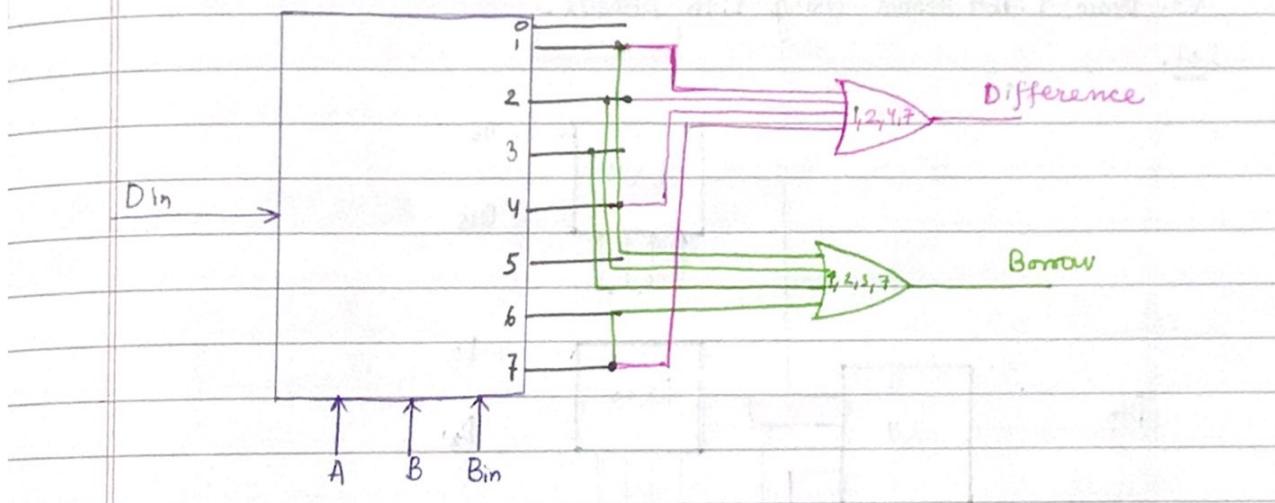
Din	$S_0$	$S_1$	$S_2$	$Y_0$	$Y_1$	$Y_2$	$Y_3$	$Y_4$	$Y_5$	$Y_6$	$Y_7$
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	0	0	0	0
1	1	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	1



07/10/22.

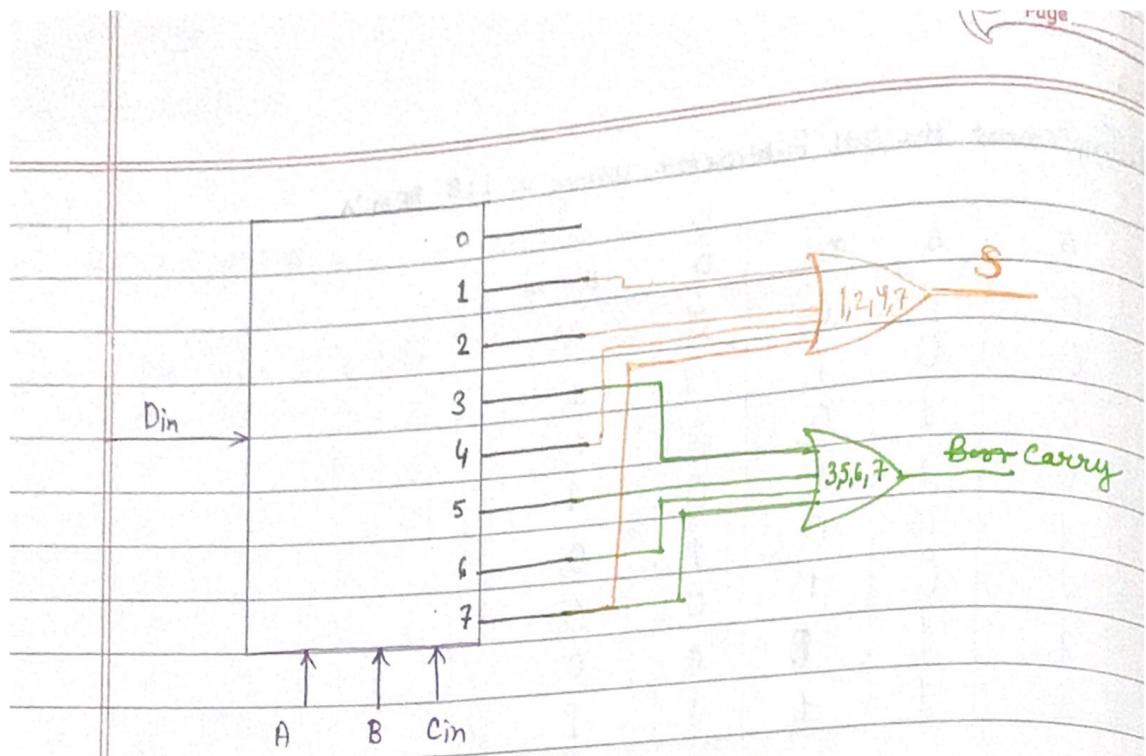
Q. Implement the Full Subtractor using a 1:8 DEMUX

A	B	Bin	D	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



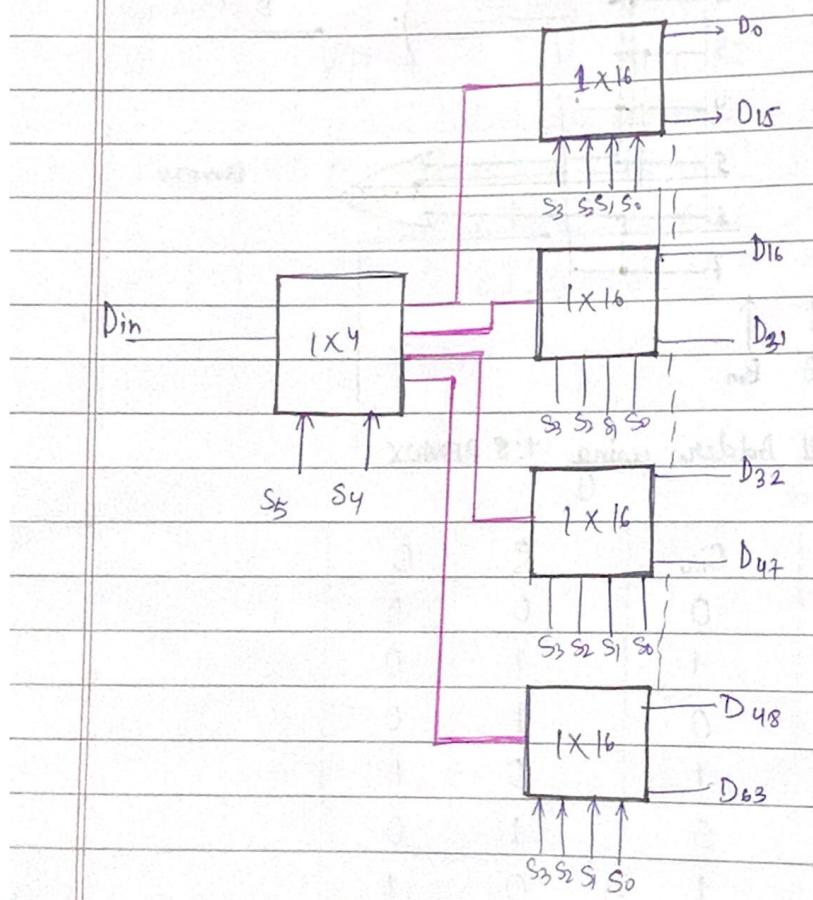
Q2. Implement a full Adder using 1:8 DEMUX

A	B	Cin	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

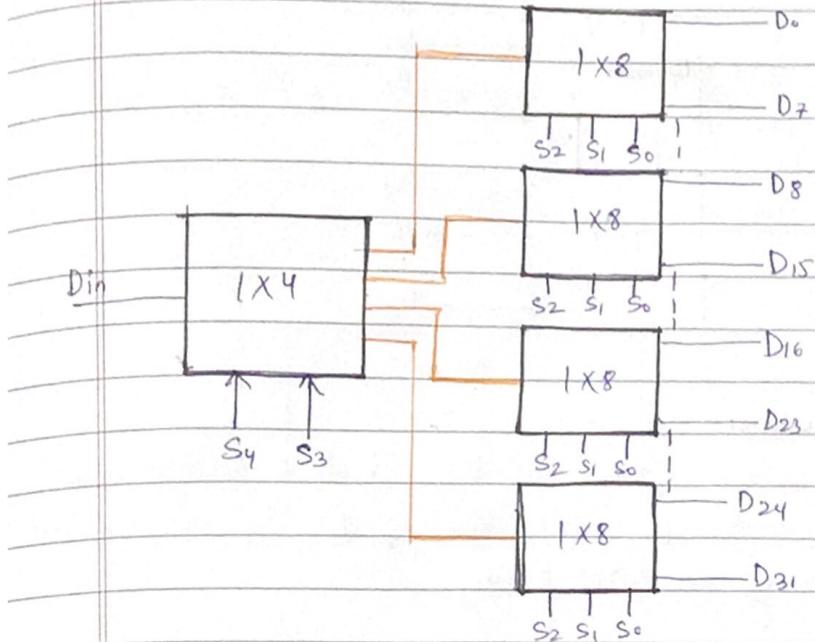


Q3. Draw 1:16 DEMUX Using 1:16 DEMUX.

Sol.



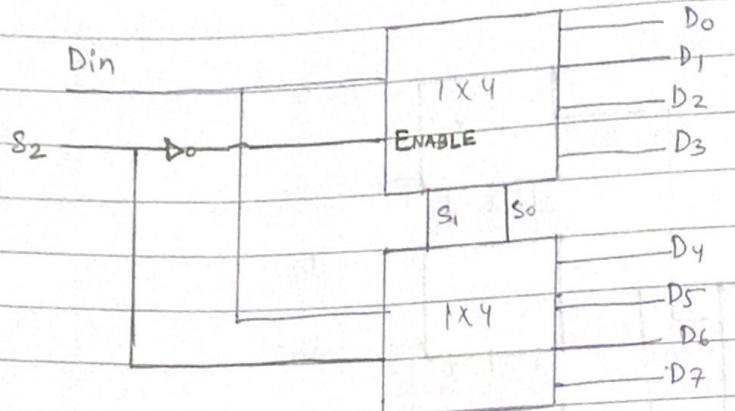
Q4. Draw 1x32 DEMUX using 1:8 DEMUX



Q5. Obtain  $1 \times 8$  DEMUX using  $2, 1:4$  DEMUX.

Sol.

$S_2$	$S_1$	$S_0$	$D_0$	$D_1$	$D_2$	$D_3$	$D_4$	$D_5$	$D_6$	$D_7$
0	0	0	$D_{in}$	0	0	0	0	0	0	0
0	0	1	0	$D_{in}$	0	0	0	0	0	0
0	1	0	0	0	$D_{in}$	0	0	0	0	0
0	1	1	0	0	0	$D_{in}$	0	0	0	0
1	0	0	0	0	0	0	$D_{in}$	0	0	0
1	0	1	0	0	0	0	0	$D_{in}$	0	0
1	1	0	0	0	0	0	0	0	$D_{in}$	0
1	1	1	0	0	0	0	0	0	0	$D_{in}$



28/10/22

\* Parity generator / checker:-

- A parity bit is an additional bit which is added to a binary word in order to make no. of 1's in new form with EVEN parity or ODD parity.

Ex : Message → 1 | 0 | 1 | 0 | 1 | 1

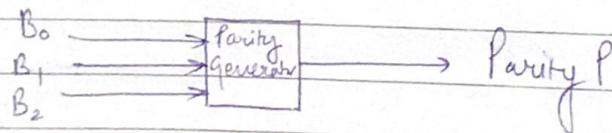
ODD → 1 | 1 | 0 | 1 | 0 | 1 | 1

EVEN → 0 | 1 | 0 | 1 | 0 | 1 | 1

- Parity bits are added in order to detect any error occurring in the process of transmission, the data with parity bits are transmitted by the transmitter. At the receiver, this data is checked for errors.

• Parity Generator:

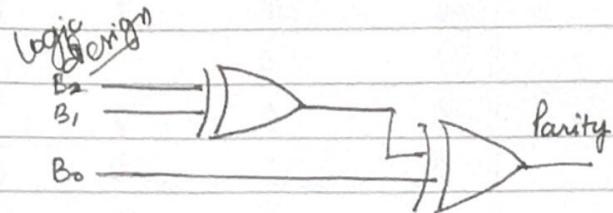
- A parity generator is a device which generates parity bits for even or odd parity.



Q. Design a parity generator using basic gates to generate message with odd parity. Assume the input to be 3 bit binary words.

Sol:

$B_2$	$B_1$	$B_0$	ODD (Parity)
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



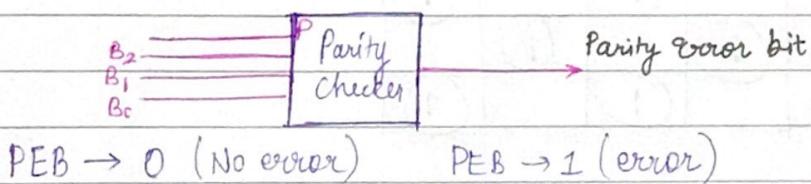
Row 1:  $B_2 \setminus B_1 \setminus B_0$       000    011    110

0	(1)	(1)	(1)
1			

ODD Parity =  $B_2 \oplus B_1 \oplus B_0$

### • Parity checker:

→ At parity checker is used at the receiver side it receives the data at the parity bit and compare it to check the error.



P	$B_2$	$B_1$	$B_0$	Parity (DDD)
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

$PB_2 \backslash B_1 B_0$	00	01	11	10
00	1		1	
01		1		1
11	1		1	
10		1		1

$$\text{Parity} = \bar{P}\bar{B}_2\bar{B}_1\bar{B}_0 + \bar{P}\bar{B}_2B_1B_0 + \bar{P}B_2\bar{B}_1B_0 + \bar{P}B_2B_1\bar{B}_0 + PB_2\bar{B}_1\bar{B}_0 + \\ PB_2B_1B_0 + PB_2\bar{B}_1B_0 + PB_2B_1\bar{B}_0$$

$$= \bar{B}_1\bar{B}_0(\bar{P}\bar{B}_2 + PB_2) + B_1B_0(\bar{P}\bar{B}_2 + PB_2) + \bar{B}_1B_0(\bar{P}B_2 + PB_2) + \\ B_1\bar{B}_0(\bar{P}B_2 + PB_2)$$

$$= (\bar{P}\bar{B}_2 + PB_2)(B_1\bar{B}_0 + B_1B_0) + (\bar{P}B_2 + PB_2)(\bar{B}_1B_0 + B_1\bar{B}_0)$$

$$= (P \odot B_2)(B_1 \odot B_0) + (P \oplus B_2)(B_1 \oplus B_0)$$

$$\textcircled{1} = (\overline{P \oplus B_2})(\overline{B_1 \oplus B_0}) + (P \oplus B_2)(B_1 \oplus B_0) \rightarrow \bar{x}\bar{y} + xy$$

consider

$$X = P \oplus B_2$$

$$Y = B_1 \oplus B_0$$

therefore eq  $\textcircled{1}$  becomes

$$\Rightarrow \bar{x}\bar{y} + xy$$

$$\Rightarrow X \odot Y$$

$$\Rightarrow \overline{X \oplus Y}$$

$$\Rightarrow (\overline{P \oplus B_2}) \oplus (\overline{B_1 \oplus B_0})$$

logic design

