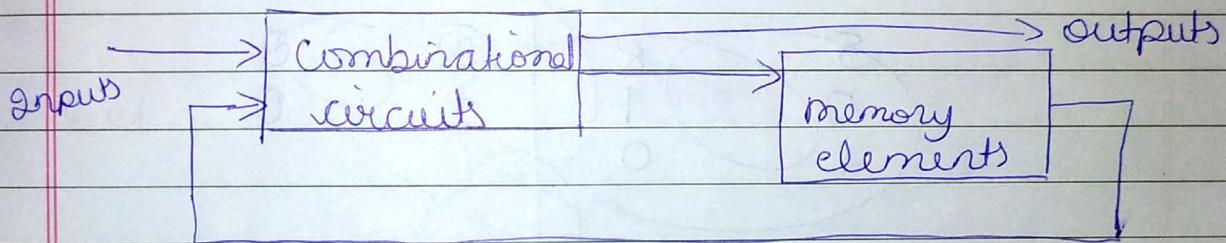


UNIT - II

Sequential logic Circuits

- (i) Output of sequential ckt is dependent on the inputs at that time instant.
- (ii) These do not contain any memory element.
- (iii) Sequential circuits are classified into
 - (i) Synchronous circuits
 - (ii) Asynchronous circuits



Flip Flops

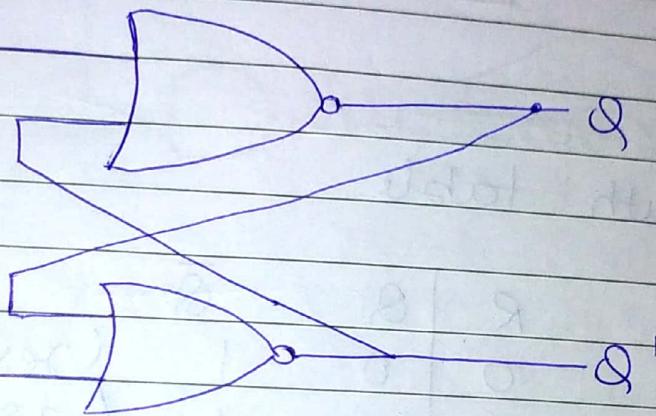
- (i) A device that exhibits two stable states is extremely useful as a memory element in a binary system. Any electrical ckt with this characteristic falls into the category of a device called Flip Flops.
- (ii) Stores one bit of information.
- (iii) The major differences among various types of flip flops are in the no. of inputs they possess.

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* Each flip flop has two outputs, Q , and Q' , and two inputs, set and reset. This type of flip flop is sometimes called a direct-coupled RS flip flop, or SR latch.

Latch with NOR gates

(R) reset



(S) set

Truth table

S	R	Q	\bar{Q}
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

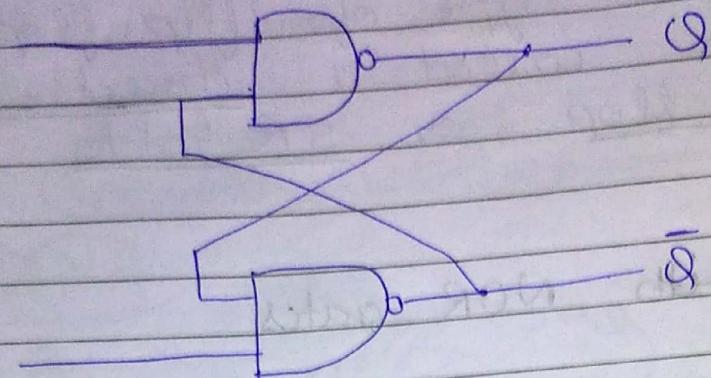
A basic SR latch (direct coupled flip flop) has two useful states.

when $Q = 1$ and $Q' = 0 \rightarrow$ set state (1)

when $Q = 0$ and $Q' = 1 \rightarrow$ clear state (0)

Latch with NAND gate

(S) Set



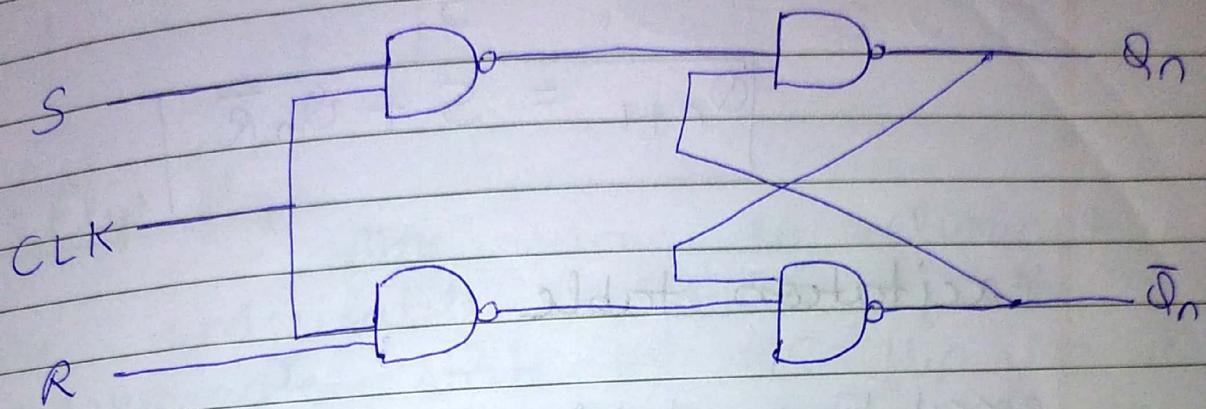
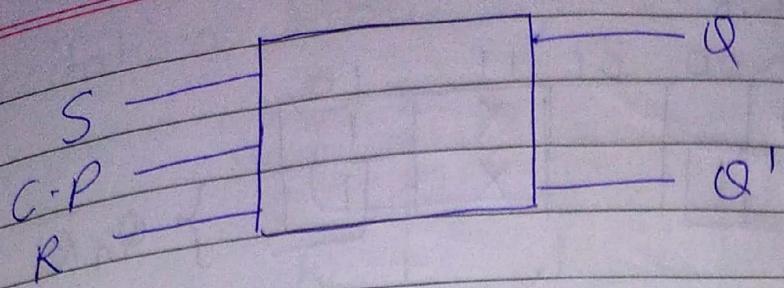
(R) Reset

Truth table

S	R	Q	\bar{Q}	
1	0	0	1	(reset)
1	1	0	1	(no change state)
0	1	1	0	(set)
1	1	1	0	(no change state)
0	0	1	1	boss (undetermined)

Clocked RS flip flop

- (e) RS flip flop has a clock input.
- (o) In clocked RS flip flop the flip flop is activated when the clock signal is high then inputs change the state of flip flop.
- (.) If the clock signal is low then inputs can't affect the flip flop



Truth table

CK	S	R	Q_{n+1}	Q_n
1	0	0	Q_n	x
1	0	1	0	reset x
1	1	0	1	set x
1	1	1	Indeterminate	x

equation for SR flip flop

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	x
1	1	0	x

S.R

Q_n	00	01	11	10	
0	X		X		
1		X		X	$\} Q_n \bar{R}$

S

$$Q_{n+1} = S + Q_n \bar{R}$$

excitation table

excitation table shows that for a particular combination of present state and next state what may be the mandatory input we need to provide.

Truth table of SR flip flop

S	R	P.S		N.S	
		Q_n	Q_{n+1}	Q_n	Q_{n+1}
0	0	X	0	0	1
0	1	X	0	0	0
1	0	X	1	1	1
1	1	X	0	1	1

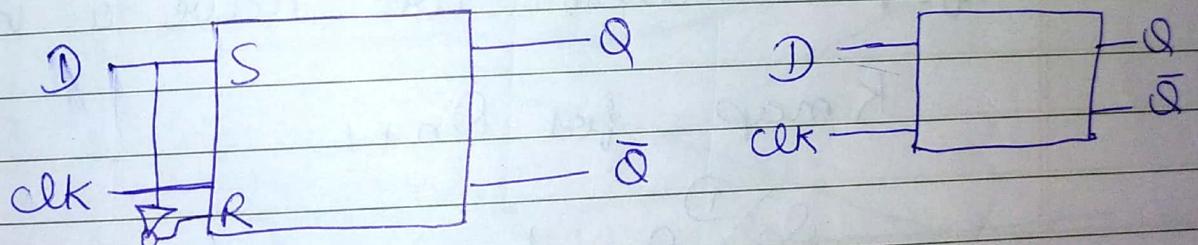
I.D

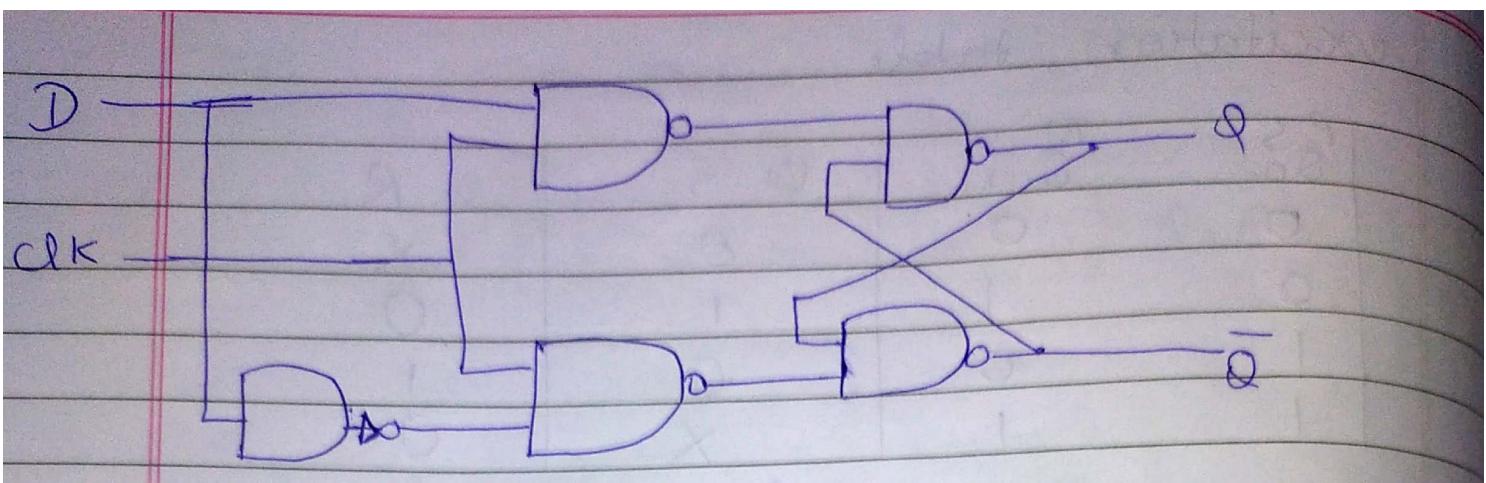
excitation table

$P-S$	$N-S$	$\bar{Q}-S$	R
\bar{S}_n	Q_{n+1}	\bar{Q}	
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D Flip flop

One way to eliminate the undesirable condition of the indeterminate state in RS flip flop is to ensure that inputs S and R are never equal to 1 at the same time. This is done in D flip flop.



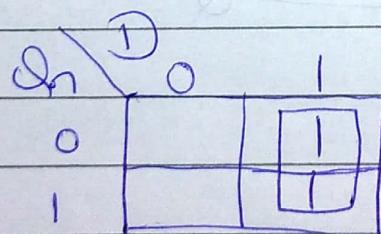


<u>clk</u>	<u>D</u>	<u>Q_{n+1}</u>	<u>Q_n</u>
0	X	Q_n	X
1	0	0	X
1	1	1	X

$S=0, R=0$
 $S=1, R=1$

$S=1, R=1$ is not possible in a flip flop because we have a inverter

K map for Q_{n+1}



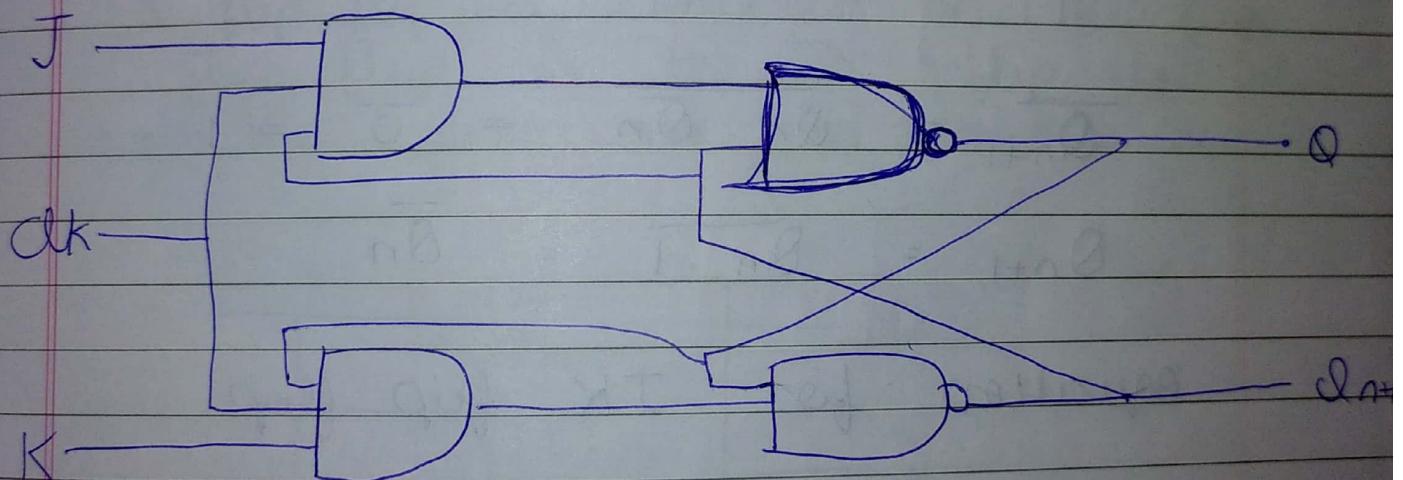
$$\boxed{Q_{n+1} = D}$$

J-K Flip flop

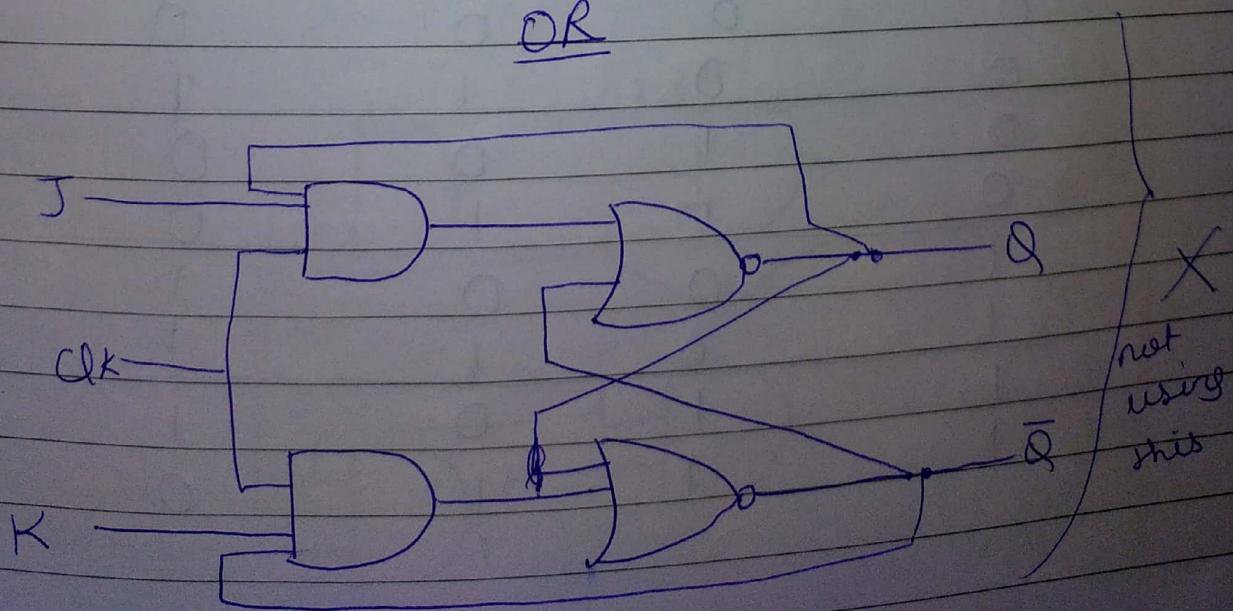
A JK flip flop is a refinement of the RS flip flop in that the indeterminate state of the RS type is defined in the JK type.

Input marked J is for set and the input marked K is for reset.

* To make use of indeterminate condition we are designing JK flip flop.

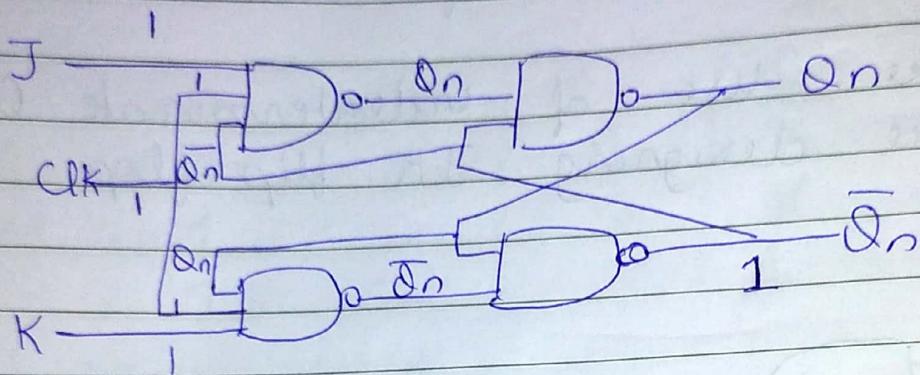


OR



clk	J	K	Q_n	Q_{n+1}
↑	0	0	x	\bar{Q}_n
↑	0	1	x	1
↑	1	0	x	0
↓	1	1	x	\bar{Q}_n
	x	x	x	Q_n

(case (iv) when $J = 1$ and $K = 1$)

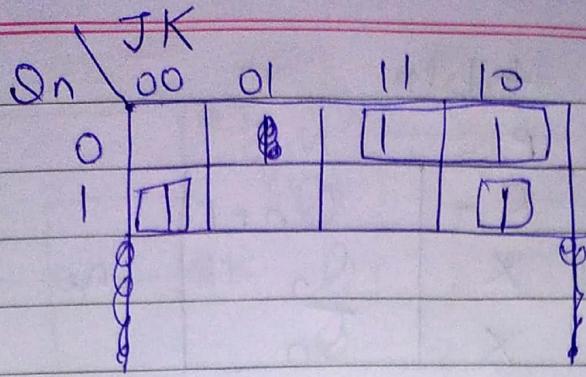


$$\overline{Q_{n+1}} = \overline{Q_n} \cdot \overline{\bar{Q}_n} = \overline{0} = 1$$

$$Q_{n+1} = \overline{Q_n \cdot 1} = \overline{Q_n}$$

equation for JK flip flop

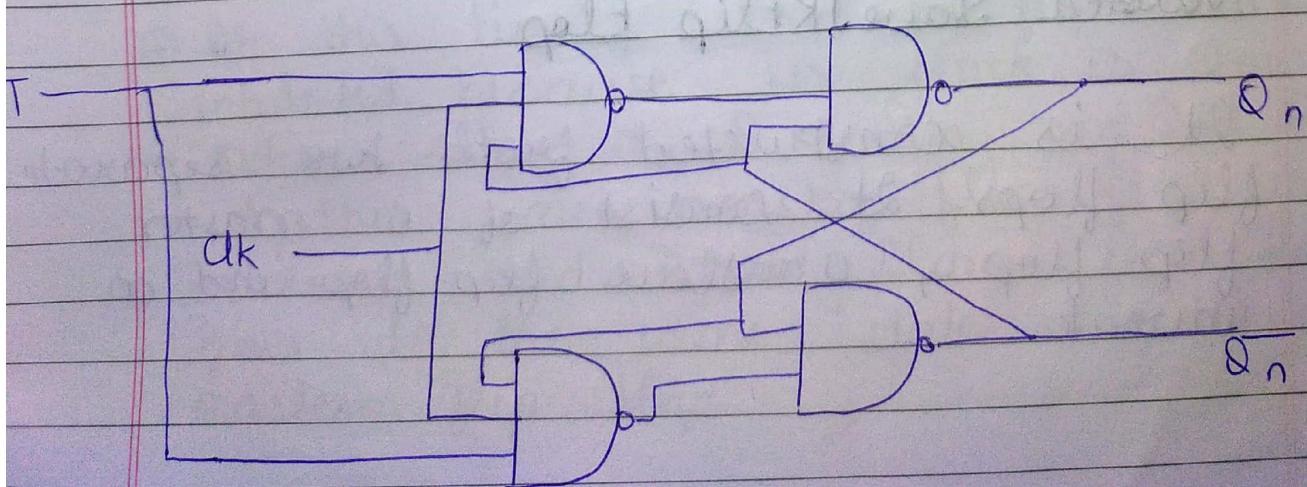
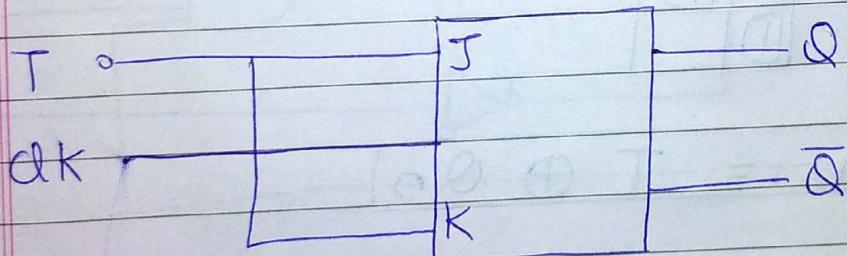
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



$$Q_{n+1} = \overline{Q_n}J + Q_n\bar{K}$$

T Flip Flop

If acts as a toggle switch. If $J = K = 1$, then output is the complement of the previous state q so that the JK flip flop is converted to T flip flop. T flip flop is the JK flip flop when both the inputs are tied together.



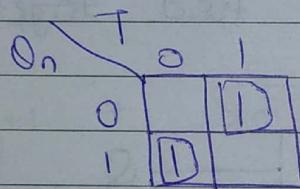
Truth table

		P.S	N.S	
T	Q _n	Q _{n+1}		
0	X	Q _n	no change	
1	X	Q _n		

when T = 1

$$G_1 = Q_n, \quad G_2 = \bar{Q}_n$$

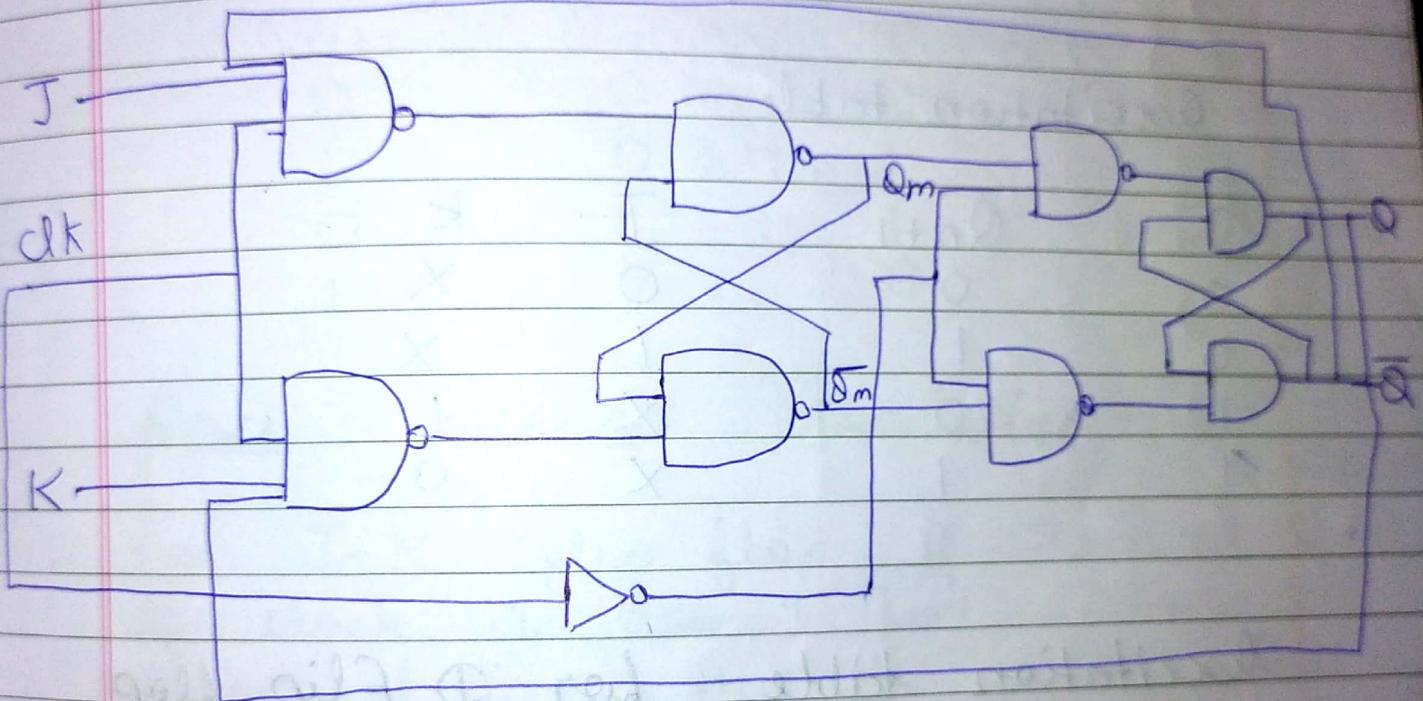
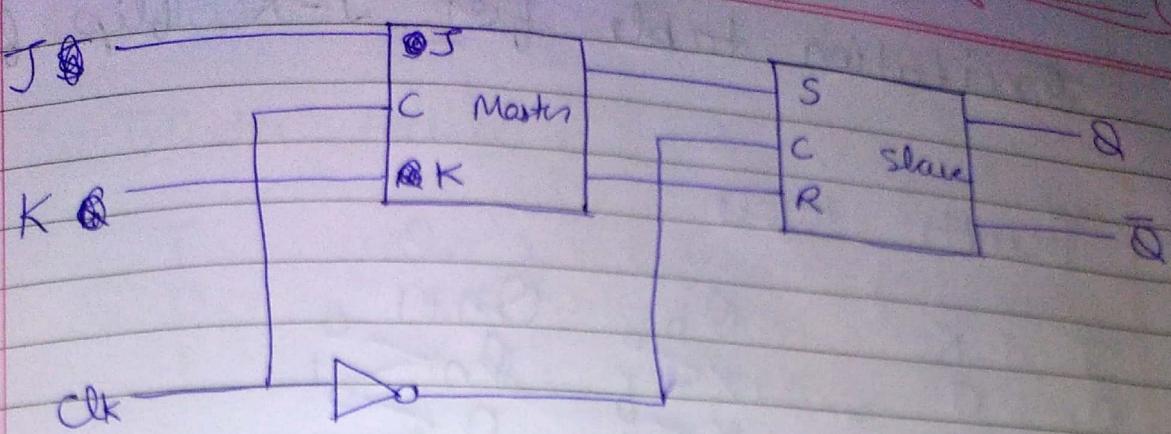
T	Q _n	Q _{n+1}
0	0	0
0	1	1
1	0	1
1	1	0



$$Q_{n+1} = T \oplus Q_n$$

Master Slave JK Flip Flop

It is constructed from two separate flip flops. It consists of a master flip flop, a slave flip flop and an inverter.



- When $\text{clk} = 1$, Q_m and \bar{Q}_m are generated.
 - At this time, second flip flop (slave) is inhibited because its clock is low.
 - When $\text{clk} = 0$, $Q = Q_m$ and $\bar{Q} = \bar{Q}_m$.
 - At this time, master flip flop is inhibited and ~~second~~ slave flip flop goes to the same state as the master flip flop.

Excitation table for J-K flip flop

Truth table

J	K	Q_n	Q_{n+1}
0	0	X	0
0	1	X	1
1	0	X	1
1	1	X	0

Excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation table for D flip flop

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Truth table

D	Q_n	Q_{n+1}
0	X	0
1	X	1

Excitation table for T flip flop

Truth table

T	$Q_n = 0$	Q_{n+1}
0	$X < 1$	$Q_n < 0$
1	$X < 1$	$Q_n < 1$

Excitation table

Q_{n+1}	Q_n	T
0	0	0
1	0	1
0	1	1
1	1	0

Race around conditions

for J-K flip flop if $J = K = 1$ & If clock is ~~on~~ 1 for a long period of time, then Q output will toggle as long as clk is high, which makes the output of the flip flop unstable or uncertain. This problem is called race around condition.

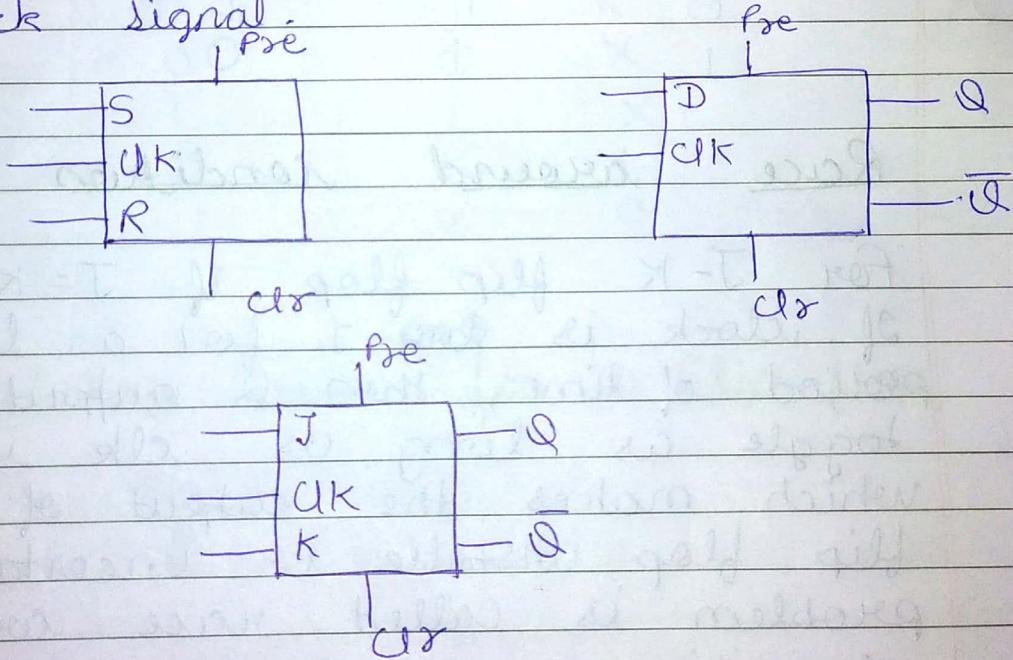
This problem can be avoided by ensuring that the clock logic is "1" only for a short time. This introduce concept of Master Slave JK flip flop.

Synchronous inputs

The normal data inputs to a flip flop (D, S and R, or J and K) are referred to as synchronous inputs because they have an effect on the output (Q and \bar{Q}) with clock signal transitions.

Asynchronous inputs

Asynchronous inputs are preset and clear, they can set or reset the flip flop regardless of the status of clock signal.



When preset is activated, the flip flop will be set ($Q = 1, \bar{Q} = 0$), when clear is activated, the flip flop will be reset ($Q = 0, \bar{Q} = 1$) regardless of any of the synchronous inputs or the clock.

Counters

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A counter is one of the most important subsystems in digital systems. A counter circuit activated by a clock can be used to count the no. of clock cycles. There are two types of counters.

- (1) Synchronous Counter
- (2) Asynchronous Counter.

Binary ripple counter / Asynchronous Counter

In a ripple counter, the flip flop output transitions serves as a source for triggering other flip flops.

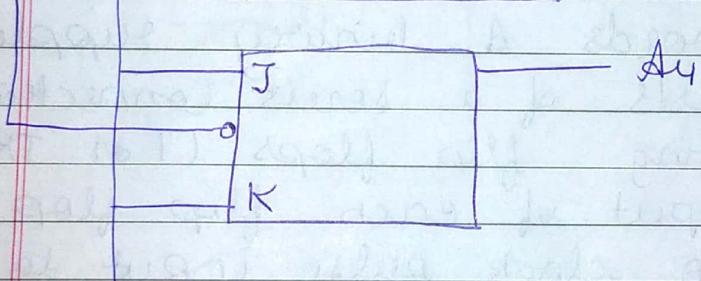
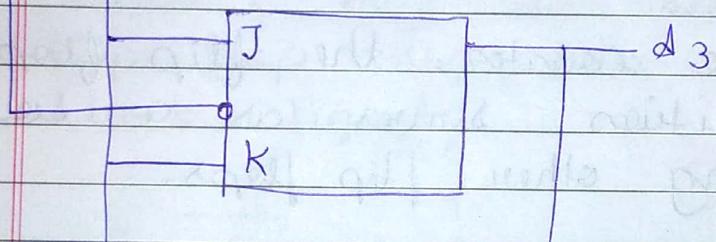
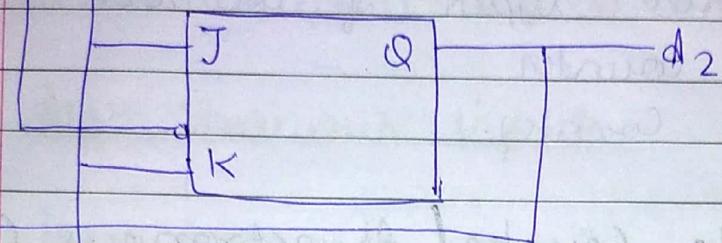
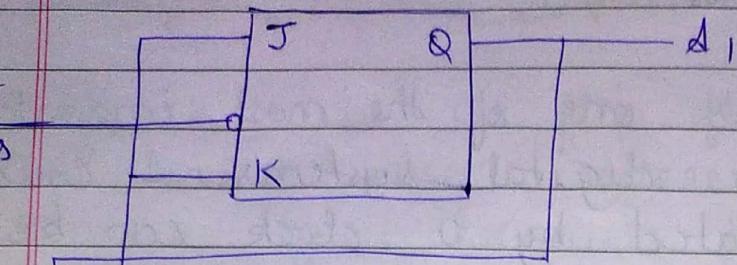
In simple words A binary ripple counter consists of a series connection of complementing flip flops (T or JK type) with the output of each flip flop connected to clock pulse input to the next higher order flip flop.

every time A_1 goes from 1 to 0, it complements A_2 , every time A_2 goes from 1 to 0, it complements A_3 and so on.

2^n states

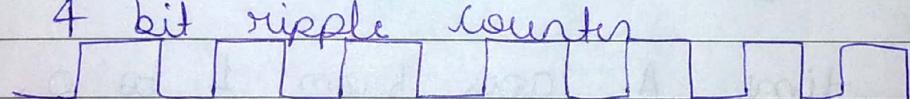
for 4 bit, $2^4 = 16$ states

Count
pulses

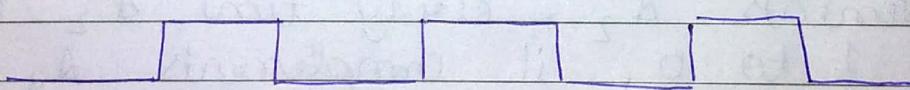


4 bit ripple counter

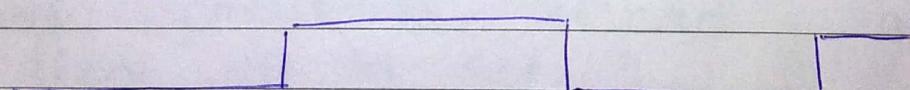
clk



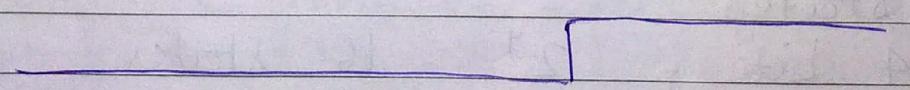
A1



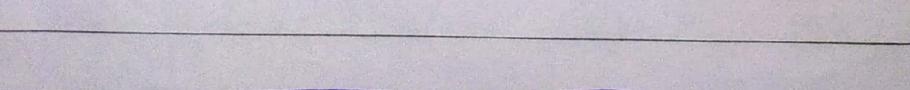
A2



A3



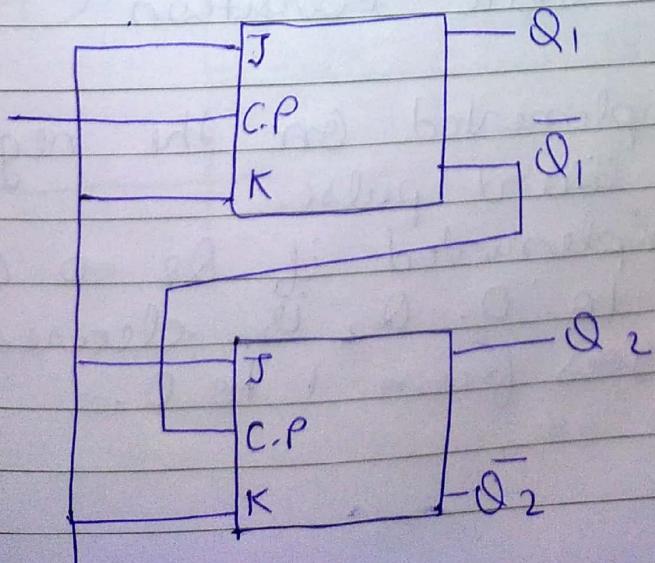
A4



A_4	A_3	A_2	A_1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

A binary counter with a reverse count is called a binary down counter. This is ripple down counter.

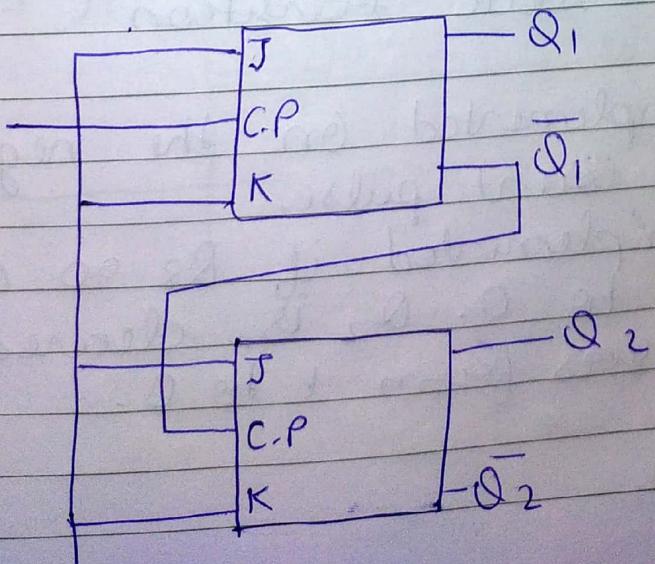
Ripple up counter (2-bit)



A_u	A_3	A_2	A_1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1@	1

A binary counter with a reverse count is called a binary down counter. This is ripple down counter.

Ripple up counter (2-bit)

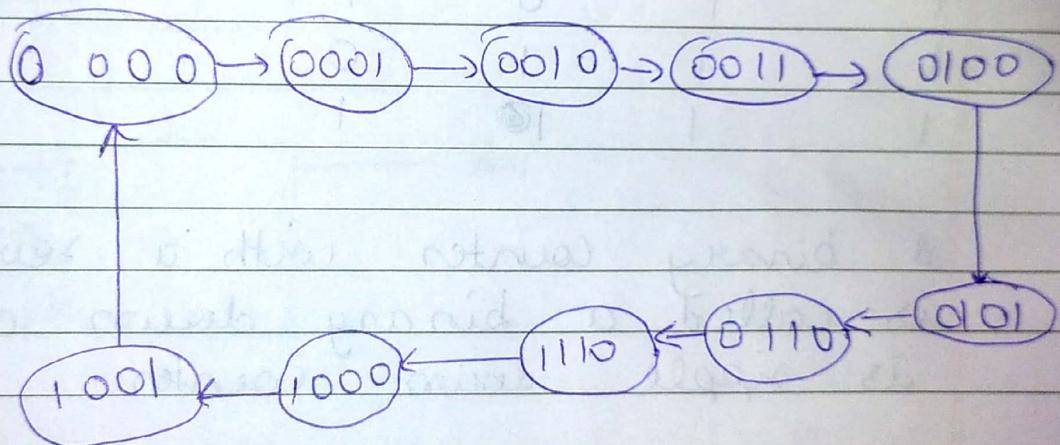


$$2^2 = 4 \text{ states}$$

Q_2	Q_1
0	0
0	1
1	0
1	1

BCD ripple counter

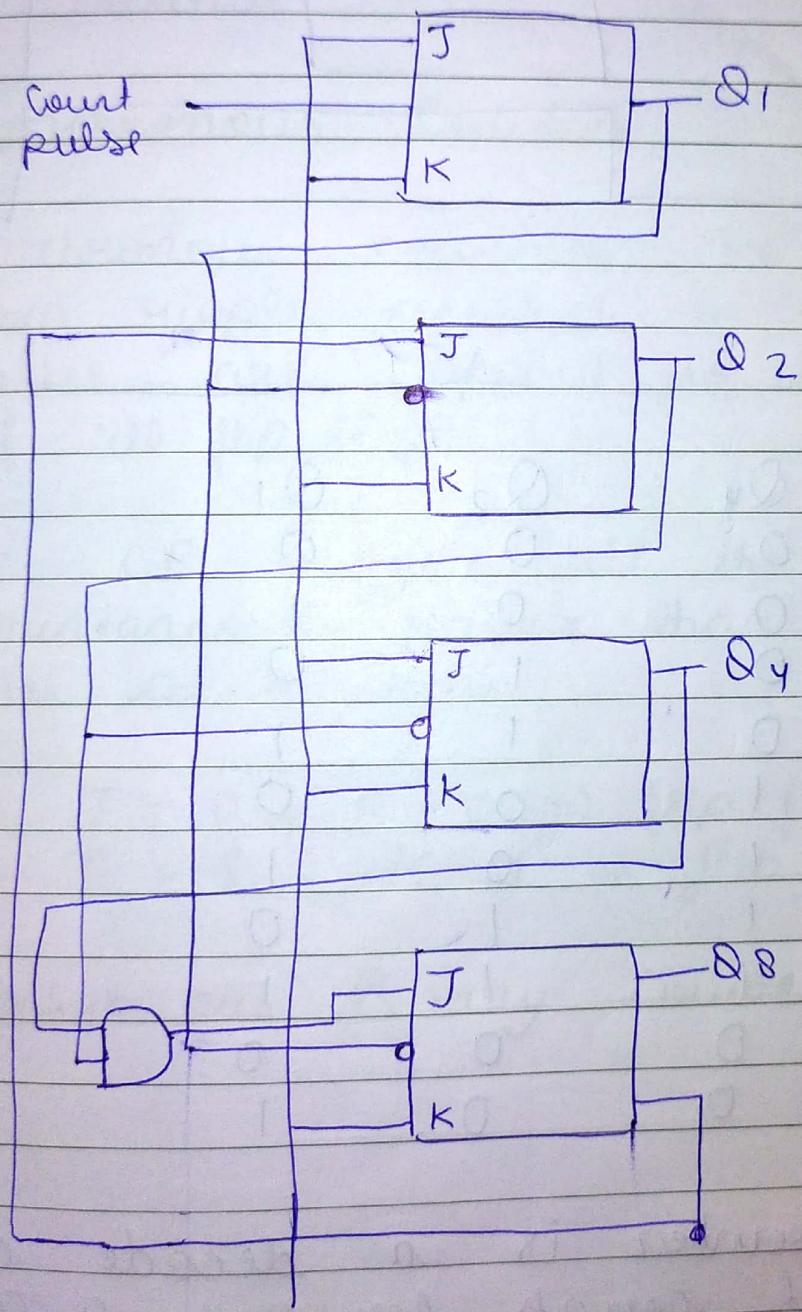
BCD counter follows a sequence of ten states and returns to 0 after the count of 9. Such a counter must have at least four flip flops.



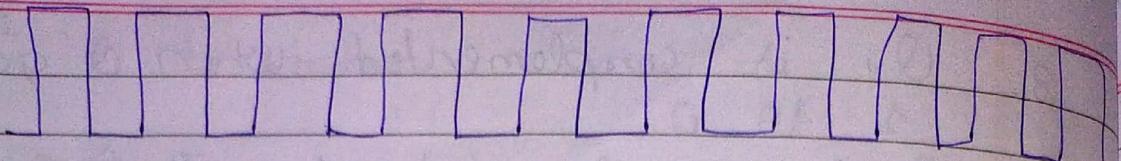
These are the conditions for each flip flop state transition

1. Q_1 is complemented on the negative edge of every count pulse.
2. Q_2 is complemented if $Q_8 = 0$ and Q_1 goes from 1 to 0. Q_2 is cleared if $Q_8 = 1$ and Q_1 goes from 1 to 0.

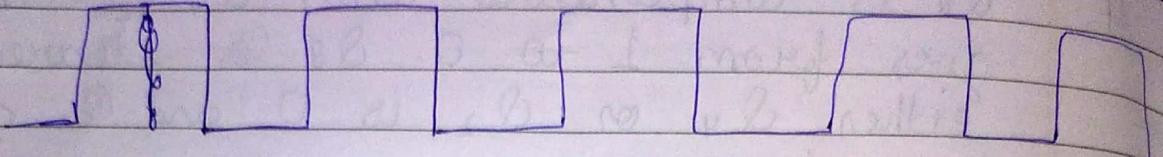
3. Q_4 is complemented when Δ goes from 1 to 0.
4. Q_8 is complemented when $Q_4 Q_2 = 11$ and Q_1 goes from 1 to 0. Q_8 is cleared if either Q_4 or Q_2 is 0 and Q_1 goes from 1 to 0.



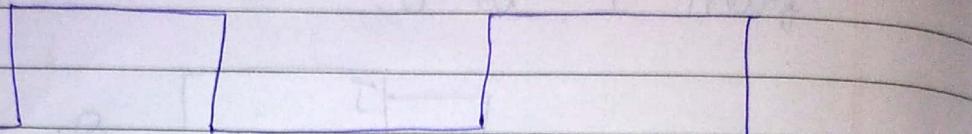
Count Pulse



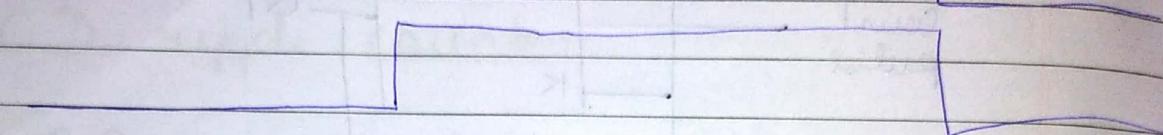
Q_1



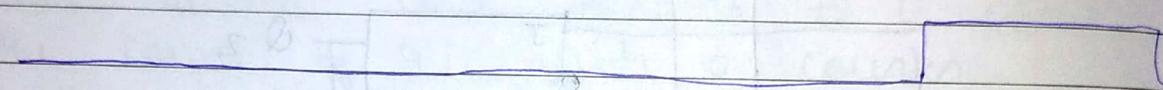
Q_2



Q_4

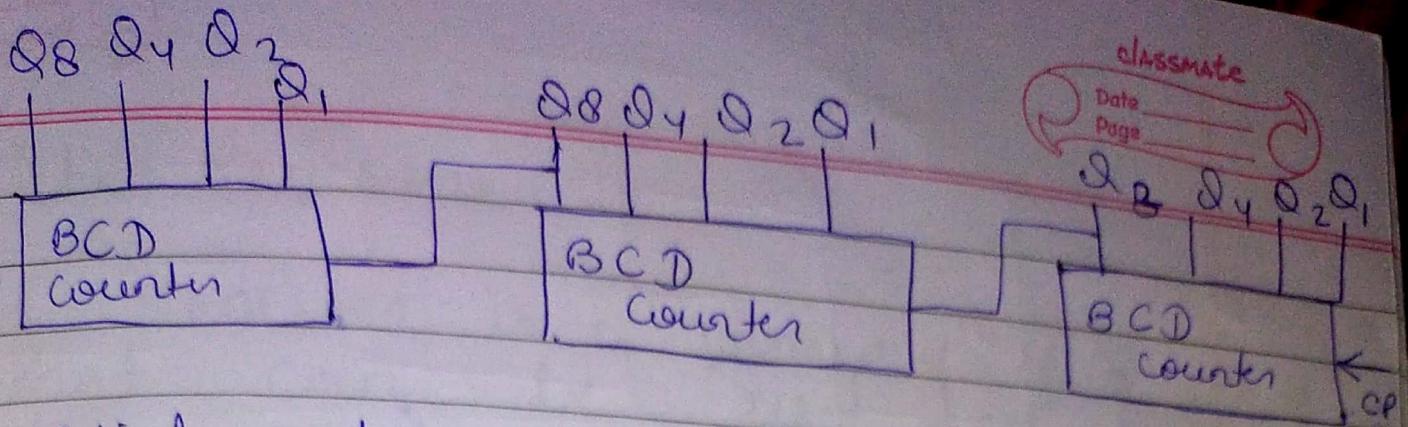


Q_8



Q_8	Q_4	Q_2	Q_1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

BCD counter is a decade counter, since it counts from 0 to 9. To count in decimal from 0 to 99, we need two decade counters. To count for 0 to 999, we need a three decade ~~BCD~~ counter.



Multiple decade counters can be constructed by connecting BCD counters in cascade.

Synchronous Counters

Synchronous counters are distinguished from ripple counters in that clock pulses are applied to the CP inputs of all flip flops.

The CP triggers all the ~~one~~ flip flops simultaneously rather than ripple counters one at a time.

If $J = 0, K = 0 \Rightarrow$ flip flop unchanged
 If $J = 1, K = 1 \Rightarrow$ flip flop complement

Shift Registers

A register is a group of flip flops that can be used to store a binary number. Registers find a variety of applications in digital systems including microprocessors.

If output of each flip flop is connected to the input of adjacent flip flop, then the ckt is called shift register.

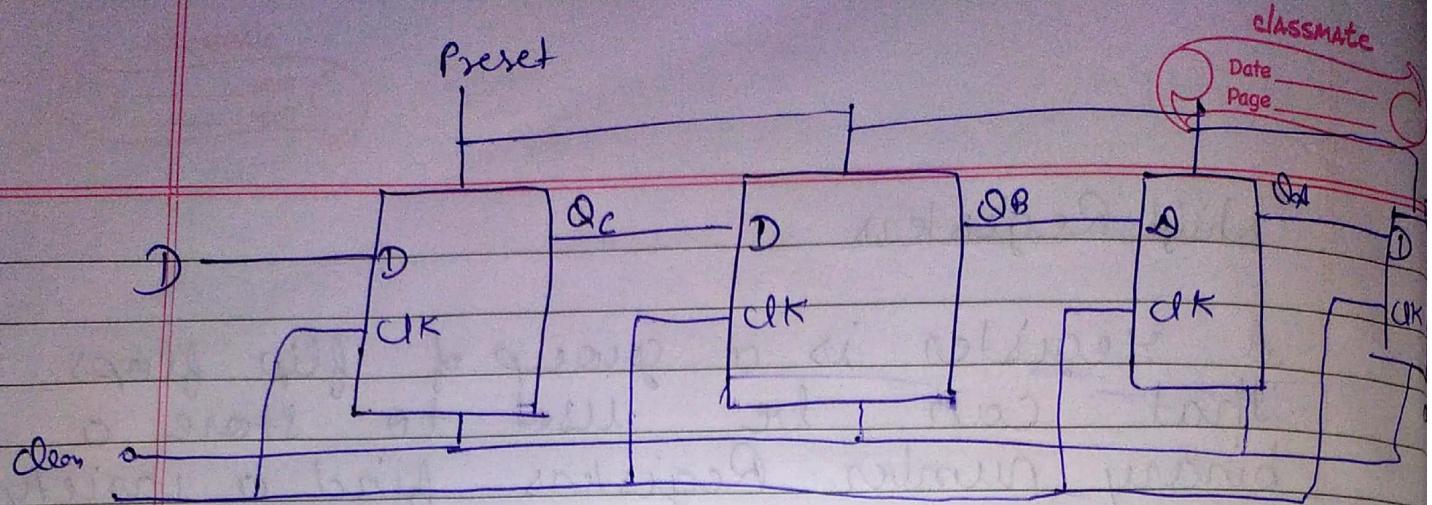
Also used for shifting binary data entered into it from an external source.

Types of Shift registers

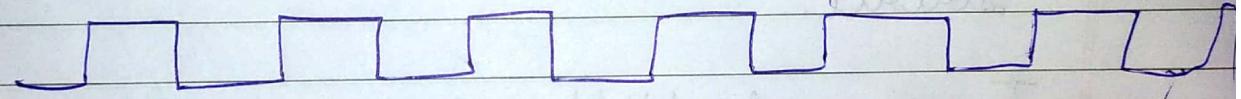
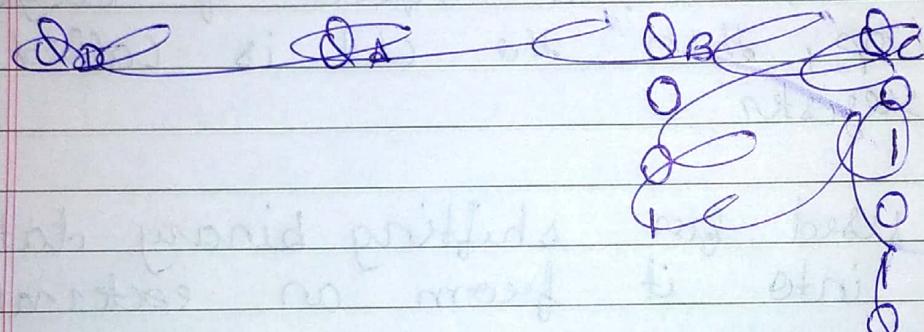
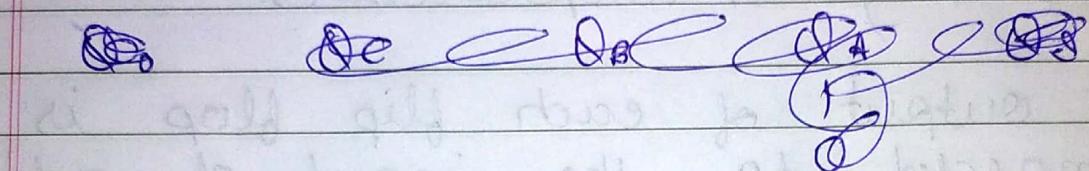
1. serial in serial out
2. serial in parallel out
3. parallel in serial out
4. parallel in parallel out

① Serial in serial out

Input data is applied one bit at a time to the first flip flop in a chain and read out from the last flip flop in chain one bit at a time.



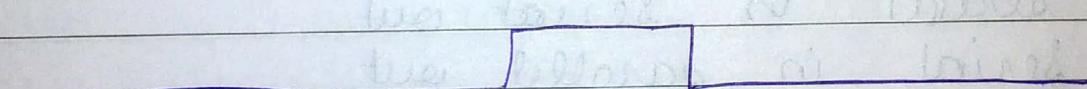
shift test



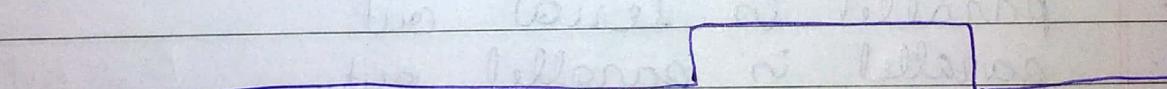
Q_C



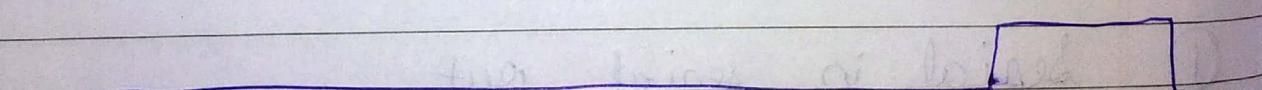
Q_B



Q_A

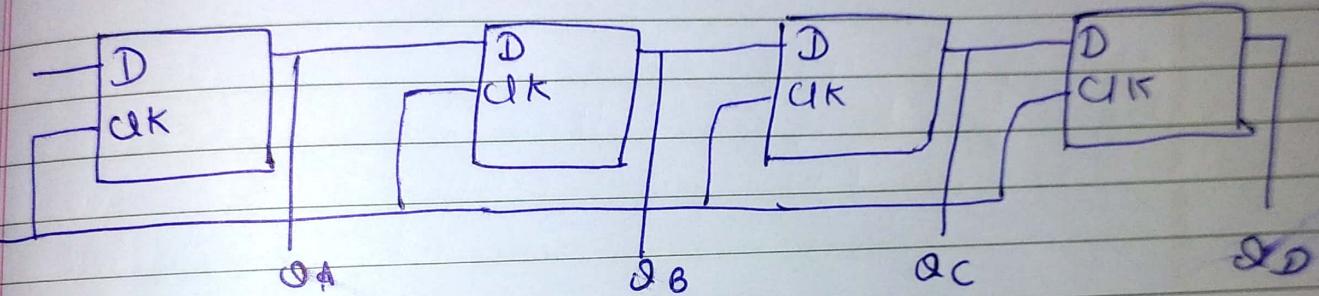


Q_D



Serial in parallel out

Input data is applied one bit at a time to the D input of the first flip flop and read out from the Q output in parallel after a data word is all shifted in.



SYNCHRONOUS COUNTER:

disadv. of ripple Counter : slow speed - ripple action
 Here FFs are clocked simultaneously

Q) Design a 3 bit Synchronous Counter using JK Flip Flops.

$$2^3 = 8 \text{ pulses} \quad (\text{three ffs})$$

flip flop	inputs	output
FF ₀	J ₀ K ₀	Q ₀
FF ₁	J ₁ K ₁	Q ₁
FF ₂	J ₂ K ₂	Q ₂

Flip Flop inputs

Q ₂	Q ₁	Q ₀	J ₀	K ₀	J ₁	K ₁	J ₂	K ₂
0	0	0	1	x	0	x	0	x
0	0	1	x	1	1	x	0	x
0	1	0	1	x	x	0	1	x
0	1	1	x	1	x	1	x	0
0	0	0	1	x	0	x	x	0
1	0	0	1	x	1	x	x	0
1	0	1	x	1	x	0	x	0
1	1	0	1	x	x	1	x	1
1	1	1	x	1	x	1	x	1

$Q_2 Q_1$	00	01	11	10
0	1	1	1	1
1	X	X	X	X

$$J_0 = 1$$

$Q_2 Q_1$	00	01	11	10
0	X	X	X	X
1	1	1	1	1

$K_0 = 1$

$Q_2 Q_1$	00	01	11	10
0	X	X	0	
1	X	X	1	

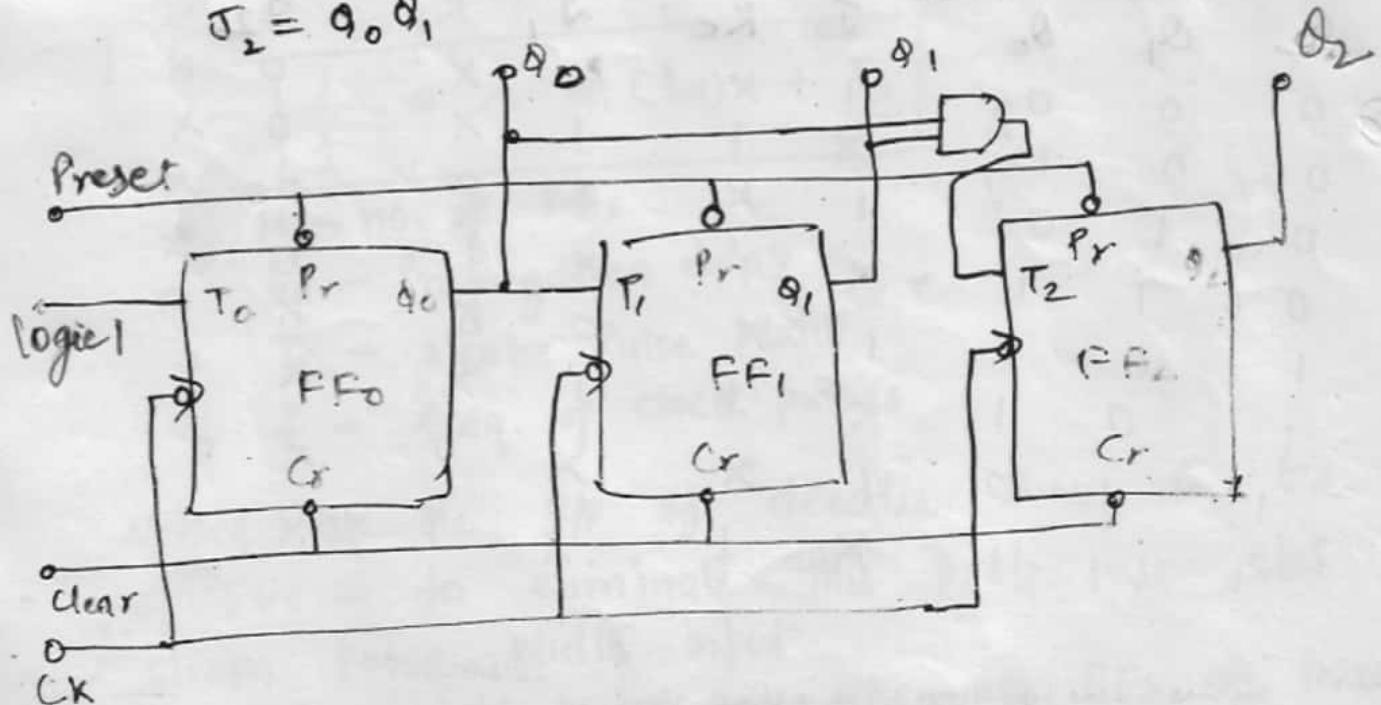
$$S_0$$

$Q_2 Q_1$	00	01	11	10
0	0	0	X	X
1	0	1	X	X

$$J_2 = Q_0 Q_1$$

$Q_2 Q_1$	00	01	11	10
0	X	X	0	0
1	X	(X)	1	0

$$K_{12} = Q_0 Q_1$$



Fan in

Fan in is defined as the maximum number of inputs that a logic gate can accept. If no. of inputs exceed, the output will be undefined or incorrect. It is specified by manufacturer and is provided in the data sheet.

Fan out

The fan out is defined as the maximum no. of inputs (load) that can be connected to the output of a gate without degrading the normal operation. It is calculated from the amount of current available in the output of a gate and the amount of current needed in each input of the connecting gate.