The Comparison of MX25L12835E/36E/45E and MX25L12835F/33F

1. Introduction

This application note compares Macronix MX25L12835E/36E/45E/35F/33F Serial NOR Flash products. The document does not provide detailed information on individual devices, but highlights the similarities and differences among them. The comparison covers the general features, performance, command sets, and device identification numbers.

The information provided in this document is based on datasheets listed in Section 8 *"References"*. Newer versions of the datasheets may override the contents of this document.

2. General Features

2-1. Feature Comparison

The MX25L12835F/33F products provide a feature rich solution to cover legacy products including MX25L12835E/36E/45E.

In addition, they improve the flexibility of device operation with the addition of a new set of Configuration Registers and the Advanced Sector Protection mode.

The Configuration Register sets the number of dummy clock cycles used for fast read operations, the output drive strength, and selects either the top or bottom of memory to be a Block Protect (BP) area.

The MX25L12835E/36E/45E/35F/33F devices support an individual block protection method as an alternative to the grouped block protection provided with Status Register Block Protection (BP) bits. In addition, the MX25L12835F/33F added additional protection features in the Advanced Sector Protection mode that provide higher levels of protection. These higher levels of protection include:

1. Nonvolatile individual sector/block protection.
2. A software locking mechanism to prevent modifications to the nonvolatile protection until the next reset cycle or power-up cycle.
3. A password protection cycle. (only provided by MX25L12835F)

These additional protection features can be used to prevent accidental or deliberate data corruption in protected memory areas.

For the comparisons of MX25L12835F and MX25L12833F, the differences are listed as below:
1. Secured OTP: MX25L12835F/33F have additional 4K-bit/8K-bit secured OTP mode separately.
2. Fast Boot Mode: The fast boot mode is only provided by MX25L12835F.
3. Password Protection: The password protection is only provided by MX25L12835F.

Please refer to the MX25L12835F and MX25L12833F datasheets for more details.

For additional product differences, please refer to the descriptions and comparison tables below.

Table 2-1. Feature Comparison

Part no.		MX25L12835E	MX25L12836E	MX25L12845E	MX25L12835F	MX25L12833F
Technology		110nm	110nm	110nm	75nm	75nm
Density		128Mb	128Mb	128Mb	128Mb	128Mb
VCC		2.7V-3.6V	2.7V-3.6V	2.7V-3.6V	2.7V-3.6V	2.7V-3.6V
Structure						
Fast Read I/O Support	FAST READ (1-1-1)	Yes	Yes	Yes	Yes	Yes
	DREAD (1-1-2)	Yes	Yes	Yes	Yes	Yes
	2READ (1-2-2)	Yes	-	Yes	Yes	Yes
	QREAD (1-1-4)	Yes	Yes	Yes	Yes	Yes
	4READ (1-4-4)	Yes	-	Yes	Yes	Yes
	QPI (4-4-4)	-	-	-	Yes	Yes
DTR		-	-	Yes	-	-
Configurable Dummy Cycles		-	-	-	Yes	Yes
Sector Size		4KB/32KB/64KB	4KB/32KB/64KB	4KB/32KB/64KB	4KB/32KB/64KB	4KB/32KB/64KB
Program Buffer Size		256Byte	256Byte	256Byte	256Byte	256Byte
Secured OTP		4Kb	4Kb	4Kb	4Kb	8Kb
BP Protect		Top	Top	Top	Top/Bottom	Top/Bottom
Software Features						
Read Enhance Mode		Yes	Yes	Yes	Yes	Yes
Wrap-around Read Mode		Yes	-	-	Yes	Yes
S/W Reset Command		Yes	-	-	Yes	Yes
Erase Suspend & Resume		-	-	-	Yes	Yes
Program Suspend & Resume		-	-	-	Yes	Yes
Adjustable Output Driver Strength		-	-	-	Yes	Yes
Fast Boot Mode		-	-	-	Yes	-
Deep Power Down		Yes	Yes	Yes	Yes	Yes
Individual/Volatile Write Protection		Yes	Yes	Yes	Yes	Yes
Individual/Nonvolatile Write Protection		-	-	-	Yes	Yes
Password Protection		-		-	Yes	-
Hardware Features						
Reset# Pin		Yes (16SOP only)	-	-	Yes	Yes
Hold# Pin		Yes	-	-	-	-
Package Solution	8SOP (209mil)	-	-	-	Yes	Yes
	16SOP (300mil)	Yes	Yes	Yes	Yes	Yes
	8WSON (8x6mm^2)	Yes	Yes	Yes	Yes	Yes
	8WSON (6x5mm^2)	-	-	-	Yes	Yes

2-2. Write Protection Comparison

The E version (MX25L12835E/36E/45E) and F version (MX25L12835F/33F) products provide two write protection modes to easily protect sectors from inadvertent changes.

The default mode is Block Protection Mode, utilizing the nonvolatile Block Protection (BP) bits in the Status Register. The BP bits specify which block groups will be protected.

The second mode uses an individual block protection method. This method utilizes a volatile SRAM lock bit assigned to each block (or sector) and controls its protection status. The Gang Block Lock (GBLK) and Gang Block Unlock (GBULK) commands set or clear all SRAM lock bits simultaneously and these commands are identical for both E and F versions. The E and F versions use different commands to control individual SRAM lock bits, and the details are addressed below.

2-2-1 Block Protection (BP) Mode

Both E and F versions use identical Status Register BP bits to specify which group of blocks to be protected. However, their block group sizes are different. The F version has a finer granularity of protection and has the ability to specify whether block protection begins at the top or bottom of memory. This is controlled by the Top/Bottom (TB) bit in the F version's new Configuration Register. The TB default setting is '0' and specifies the top of the memory as shown in **Table 2-2** and *Table 2-3: Block Protection (BP) Comparison (Bottom memory blocks)*.

Table 2-2: Block Protection (BP) Comparison (Top memory blocks)

Status Register Bit				Protected Blocks			
BP3	BP2	BP1	BP0	MX25L12835E/36E/45E		MX25L12835F/33F	
0	0	0	0	None		None	
0	0	0	1	2 blocks	(#254-255)	1 block	(#255)
0	0	1	0	4 blocks	(#252-255)	2 blocks	(#254-255)
0	0	1	1	8 blocks	(#248-255)	4 blocks	(#252-255)
0	1	0	0	16 blocks	(#240-255)	8 blocks	(#248-255)
0	1	0	1	32 blocks	(#224-255)	16 blocks	(#240-255)
0	1	1	0	64 blocks	(#192-255)	32 blocks	(#224-255)
0	1	1	1	128 blocks	(#128-255)	64 blocks	(#192-255)
1	0	0	0	256 blocks	(all)	128 blocks	(#128-255)
1	0	0	1	256 blocks	(all)	256 blocks	(all)
1	0	1	0	256 blocks	(all)	256 blocks	(all)
1	0	1	1	256 blocks	(all)	256 blocks	(all)
1	1	0	0	256 blocks	(all)	256 blocks	(all)
1	1	0	1	256 blocks	(all)	256 blocks	(all)
1	1	1	0	256 blocks	(all)	256 blocks	(all)
1	1	1	1	256 blocks	(all)	256 blocks	(all)

Table 2-3: Block Protection (BP) Comparison (Bottom memory blocks)

Status Register Bit				Protected Blocks	
BP3	BP2	BP1	BP0	MX25L12835F/33F	
0	0	0	0	None	
0	0	0	1	1 block	(#0)
0	0	1	0	2 blocks	(#0-1)
0	0	1	1	4 blocks	(#0-3)
0	1	0	0	8 blocks	(#0-7)
0	1	0	1	16 blocks	(#0-15)
0	1	1	0	32 blocks	(#0-31)
0	1	1	1	64 blocks	(#0-63)
1	0	0	0	128 blocks	(#0-127)
1	0	0	1	256 blocks	(all)
1	0	1	0	256 blocks	(all)
1	0	1	1	256 blocks	(all)
1	1	0	0	256 blocks	(all)
1	1	0	1	256 blocks	(all)
1	1	1	0	256 blocks	(all)
1	1	1	1	256 blocks	(all)

2-2-2 Individual Block Protection Mode

Individual block protection is only effective after executing the WPSEL command. This one-time-use command permanently disables the block group protection method (Status Register BP bits) and activates individual block protection. The WPSEL command is common to both E and F versions. E and F version devices implement individual block protection differently and require different commands. The following sections will discuss both implementations.

2-2-3 Individual Block Protection versus Advanced Sector Protection

The ability to quickly unlock individual blocks is convenient when changes are required, but it also makes the protected areas vulnerable to corrupt or malicious software. To enhance the security of the protection feature, the protection feature, the MX25L12835F and MX25L12833F have added Advanced Sector Protection. Advanced Sector Protection adds nonvolatile protection bits with the ability to lock them until the next reset cycle or power-up cycle. These new features require different commands and the user's application software will need to be modified if the features are desired.

The following sections show the operational differences between E and F version products when using individual sector/block protection.

2-2-4 MX25L12835E/12836E/12845E Individual Block Protection Mode

The Single Block Lock Protection bits are volatile SRAM bits assigned to each protectable sector or block. The bits permit sectors or blocks to be protected individually and independent of any other sector or block. The Single Block Lock Protection bits default to protected mode (set to '1') upon power-up or reset. *Table 2-4: Individually Protectable Sectors/Blocks* illustrates in green, which blocks can be individually protected.

Table 2-4: Individually Protectable Sectors/Blocks

64KB Block #	4KB Sector #	Protectable
255	4095 . . . 4080	16 4KB sectors (lock/unlock)
254	4079 … 4064	254 64KB blocks (lock/unlock)
. . .	. . .	
1	31 . 16	
0	15 . . . 0	16 4KB sectors lock/unlock

Only the sector and block numbers highlighted in green are individually protectable.
The Single Block Lock (SBLK) instruction (36h) enables read only protection for the specified sector or block of memory. Sector selection is made using address bits A23-A12 and only the top and bottom sixteen 4KB sectors can be individually protected. The remaining sectors are grouped into 64KB blocks. Individual 64KB block selection is made using address bits A23-A16. Use the Single Block Unlock (SBULK) instruction (39h) to cancel the individual sector or block protection state.

Figure 2-1: Single Block Lock/Unlock Protection (SBLK/SBULK) Sequence
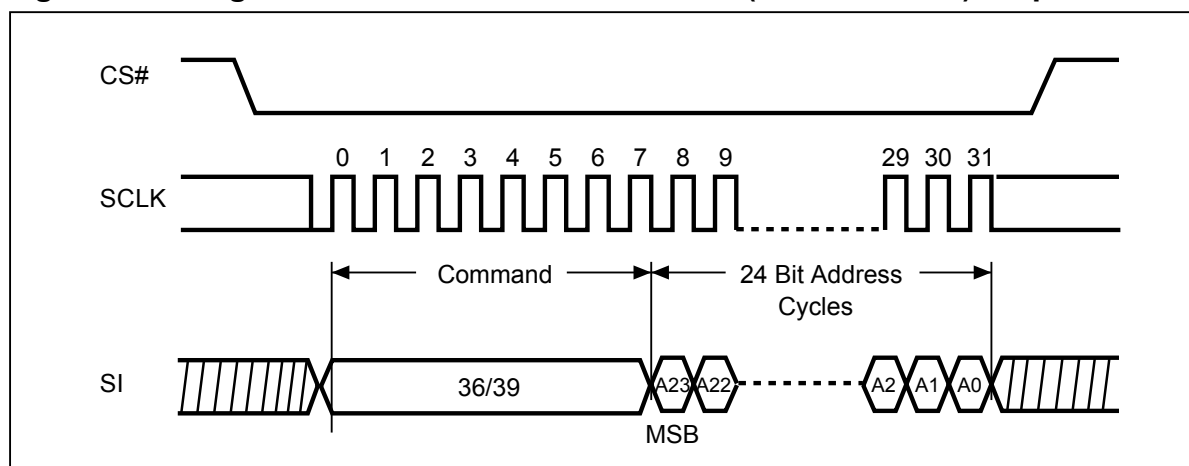
2-2-5 MX25L12835F/33F Advanced Sector Protection Mode

Dynamic Protection Bits (DPB) is volatile and similar in purpose to the Single Block Lock Protection bits used by the E version devices. Nonvolatile Solid Protection Bits (SPB) is a new feature. Each protectable sector or block (*Table 2-4: Individually Protectable Sectors/Blocks*) is assigned one DPB and one SPB. This permits sector or block protection to be specified individually and independent of any other sector or block. The DPB default to the protect state (FFh) upon power-up or reset. They work in conjunction with the nonvolatile SPB. Both DPB and SPB states must be cleared to 00h before the associated sector or block can be modified. The SPB are preset to 00h at the factory and there is no need to modify them if you are only migrating from an E version product to the MX25L12835F/33F. Please refer to the MX25L12835F and MX25L12833F datasheets if you need to use the SPB features.

The SPB protection can also temporary unprotect by solid write protect bit (USPB) feature (only provided by MX25L12835F) to temporarily unprotect the sectors protected by SPB.

To modify the DPB status, issue the DPB Program command (WRDPB) including the target sector or block address and set or clear the DPB protection state. All DPB bits can be quickly unlocked by issuing one Gang Block Unlock (GBULK) command (98h). Sector selection is made using address bits A23-A12 and only the top and bottom sixteen 4KB sectors can be individually protected. The remaining sectors are grouped into 64KB blocks. Individual 64KB block selection is made using address bits A23-A16.

Table 2-5: DPB Register

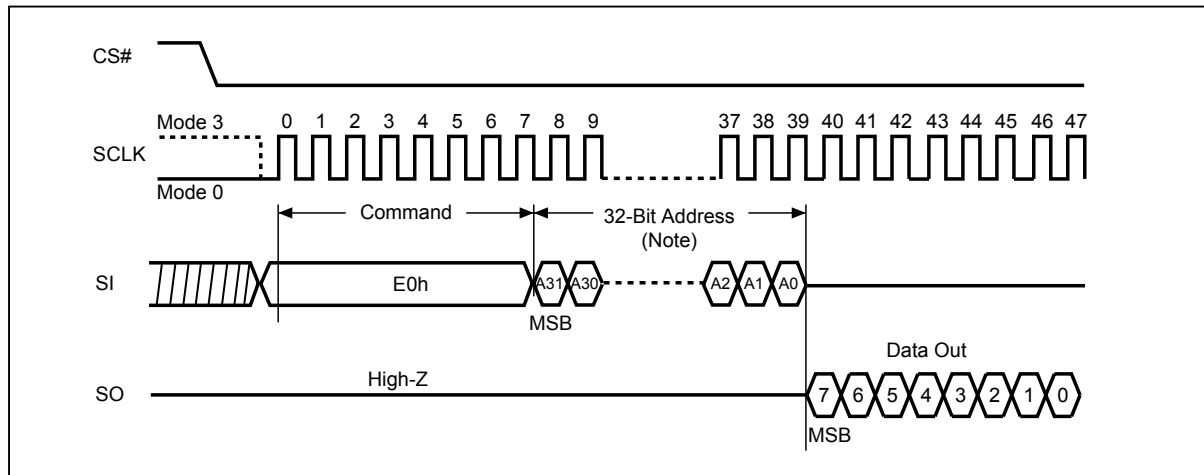| Bit	Description	Bit Status	Default	Type
7 to 0	DPB (Dynamic Protection Bit)	00h= Unprotect Sector / Block FFh= Protect Sector / Block	FFh	Volatile

2-2-5 MX25L12835F/33F Individual Block Protection Mode - Continued

Figure 2-2: Write DPB Register (WRDPB) Sequence
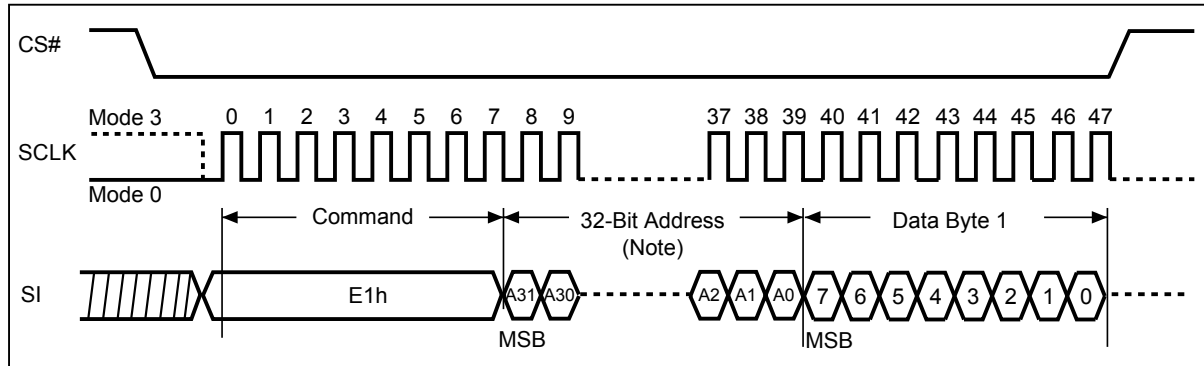
Note: A31-A24 are don't care.

Figure 2-3: Read DPB Register (RDDPB) Sequence

Note: A31-A24 are don't care.

2-2-6 Lock Register

Operating individual sector protection feature on MX25L12835F and MX25L12833F is similar. Both MX25L12835F and MX25L12833F have SPB and DPB to implement individual sector protection feature.

To enhance the security of the protection feature, MX25L12833F provide SPB Lock Down feature, once SPBLKDN (bit 6) is set, SPB bit value cannot be changed again and it is read-only.

The Lock Register has slight difference. Please refer to the comparison table (*Table 2-6: Lock Register Comparison*) and refer to MX25L12835F and MX25L12833F datasheets for more detailed information.

Table 2-6: Lock Register Comparison

	MX25L12835F	MX25L12833F
bit 0	Reserved	Reserved
bit 1	Solid Protection Mode Lock Bit	Reserved
bit 2	Password Protection Mode Lock Bit	Reserved
bit 3	Reserved	Reserved
bit 4	Reserved	Reserved
bit 5	Reserved	Reserved
bit 6	Reserved	SPBLKDN
bit 7-15	Reserved	Reserved

3. Performance Comparison

The MX25L12835F/33F provide higher Fast Read Program/Erase performance, and lower power consumption than the E version ones.

Table 3-1: Read Performance Comparison

Read Performance	MX25L12835E	MX25L12836E	MX25L12845E	MX25L12835F	MX25L12833F
VCC	2.7V-3.6V	2.7V-3.6V	2.7V-3.6V	2.7V-3.6V	2.7V-3.6V
Normal Read (1-1-1)	50MHz	50MHz	50MHz	50MHz	50MHz
FASTREAD (1-1-1)	104MHz	104MHz	104MHz	104MHz* 133MHz**	104MHz* 133MHz**
DREAD (1-1-2)	70MHz	70MHz	-	104MHz* 133MHz**	104MHz* 133MHz**
2READ (1-2-2)	70MHz	-	70MHz	84MHz* 133MHz**	84MHz* 133MHz**
QREAD (1-1-4)	70MHz	70MHz	-	104MHz* 133MHz**	104MHz* 133MHz**
4READ (1-4-4)	70MHz	-	70MHz	84MHz* 133MHz**	84MHz* 133MHz**
QPI (4-4-4)	-	-	-	84MHz* 133MHz**	84MHz* 133MHz**
Double Transfer Rate	-	-	50MHz	-	-
Configurable Dummy Cycles	-	-	-	Yes	Yes

Notes: * *Default*

        ** *Maximum*

Table 3-2: AC Performance Comparison

AC Performance		Condition	MX25L12835E	MX25L12836E	MX25L12845E	MX25L12835F	MX25L12833F
Erase Time	4KB	typ	60ms	60ms	60ms	30ms	25ms
		max.	300ms	300ms	300ms	120ms	120ms
	32KB	typ.	0.5s	0.5s	0.5s	0.15s	0.14s
		max.	2s	2s	2s	0.65s	0.65s
	64KB	typ.	0.7s	0.7s	0.7s	0.28s	0.25s
		max.	2s	2s	2s	0.65s	0.65s
	Chip Erase	typ.	80s	80s	80s	50s	26s
		max.	200s	200s	200s	80s	60s
Program Time	256Byte	typ.	1.4ms	1.4ms	1.4ms	0.5ms	0.33ms
		max.	5ms	5ms	5ms	1.5ms	1.2ms
Clock Low to Output Valid	15pf	max.	8ns	9.5ns	9.5ns	6ns	6ns
	30pf	max.	8ns	12ns	12ns	8ns	8ns

Table 3-3: DC Performance Comparison

DC Performance		MX25L12835E	MX25L12836E	MX25L12845E	MX25L12835F	MX25L12833F
Active Current (max.)	Read (4I/O)	22mA	22mA	22mA	25mA	25mA
	Erase	25mA	25mA	25mA	25mA	25mA
	Program	25mA	25mA	25mA	20mA	20mA
VCC Standby Current		100uA(max.)	100uA(max.)	100uA(max.)	10uA(typ.)/ 50uA(max.)	10uA(typ.)/ 50uA(max.)
Deep Power Down Current		40uA(max.)	40uA(max.)	40uA(max.)	2uA(typ.)/ 20uA(max.)	2uA(typ.)/ 20uA(max.)

Note: *All of the data shown in the table are maximum values unless noted as typical.*
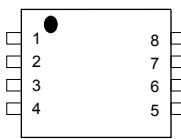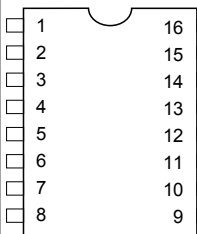
4. Package and Pinout Comparison

shows the common packages and the pinout assignments for the E and F version devices. It has an internal pull-up and can be left floating if it is not used. On the other devices, it is NC/SIO3.
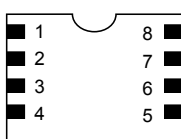
The MX25L12836E and MX25L12845E support the parallel data input/output mode using pins PO[7:0], whereas the MX25L12835E and MX25L12835F/33F flash do not support this mode. This parallel mode is normally only used by external programmers and should not be a problem for in-circuit applications.

The MX25L12835F/33F support the hardware RESET# function in all available packages. RESET# has an internal pull-up and can be left floating if it is not used.

Figure 4-1: Packages and Pinouts

8-PIN SOP (200mil)

MX25L12835F	MX25L12833F		MX25L12835F	MX25L12833F
CS#	CS#	1 ● ... 8	VCC	VCC
SO/SIO1	SO/SIO1	2 ... 7	RESET#/SIO3	RESET#/SIO3
WP#/SIO2	WP#/SIO2	3 ... 6	SCLK	SCLK
GND	GND	4 ... 5	SI/SIO0	SI/SIO0

16-PIN SOP (300mil)

MX25L12835E	MX25L12836E	MX25L12845E	MX25L12835F	MX25L12833F		MX25L12835E	MX25L12836E	MX25L12845E	MX25L12835F	MX25L12833F
HOLD#SIO3	NC/SIO3	NC/SIO3	DNU/SIO3	DNU/SIO3	1 ... 16	SCLK	SCLK	SCLK	SCLK	SCLK
VCC	VCC	VCC	VCC	VCC	2 ... 15	SI/SIO0	SI/SIO0	SI/SIO0	SI/SIO0	SI/SIO0
RESET#	NC	NC	RESET#	RESET#	3 ... 14	NC	PO6	PO6	NC	NC
NC	PO2	PO2	NC	NC	4 ... 13	NC	PO5	PO5	NC	NC
NC	PO1	PO1	NC	NC	5 ... 12	NC	PO4	PO4	NC	NC
NC	PO0	PO0	NC	NC	6 ... 11	NC	PO3	PO3	NC	NC
CS#	CS#	CS#	CS#	CS#	7 ... 10	GND	GND	GND	GND	GND
SO/SIO1	SO/SIO1/PO7	SO/SIO1/PO7	SO/SIO1	SO/SIO1	8 ... 9	WP#/SIO2	WP#/SIO2	WP#/SIO2	WP#/SIO2	WP#/SIO2

8-WSON

MX25L12835E (8x6mm)	MX25L12836E (8x6mm)	MX25L12845E (8x6mm)	MX25L12835F (6x5mm, 8x6mm)	MX25L12833F (6x5mm)		MX25L12835E (8x6mm)	MX25L12836E (8x6mm)	MX25L12845E (8x6mm)	MX25L12835F (6x5mm, 8x6mm)	MX25L12833F (6x5mm)
CS#	CS#	CS#	CS#	CS#	1 ... 8	VCC	VCC	VCC	VCC	VCC
SO/SIO1	SO/SIO1	SO/SIO1	SO/SIO1	SO/SIO1	2 ... 7	HOLD#/SIO3	NC/SIO3	NC/SIO3	RESET#SIO3	RESET#/SIO3
WP#/SIO2	WP#/SIO2	WP#/SIO2	WP#/SIO2	WP#/SIO2	3 ... 6	SCLK	SCLK	SCLK	SCLK	SCLK
GND	GND	GND	GND	GND	4 ... 5	SI/SIO0	SI/SIO0	SI/SIO0	SI/SIO0	SI/SIO0

5. Command Code Comparison

All of the commands are listed in **Table 5-1** below. Most commands are common. Differences are attributted to unsupported or new features.

Table 5-1: Command Code Comparison

Command	Symbol	Description	MX25L12835E	MX25L12836E	MX25L12845E	MX25L12835F	MX25L12833F
ID Read	RDID	Read Identification	9Fh	9Fh	9Fh	9Fh	9Fh
	RES	Read Electronic ID	ABh	ABh	ABh	ABh	ABh
	REMS	Read Electronic Manufacturer & Device ID	90h	90h	90h	90h	90h
	REMS2	2 x I/O Read ID	EFh	EFh	EFh	-	-
	REMS4	4 x I/O Read ID	DFh	DFh	DFh	-	-
	QPIID	QPI ID Read	-	-	-	AFh	AFh
Read	READ	Read Data	03h	03h	03h	03h	03h
	FAST READ	Fast Read	0Bh	0Bh	0Bh	0Bh	0Bh
	2READ	2 x I/O Fast Read	BBh	-	BBh	BBh	BBh
	DREAD	1I 2O Fast Read	3Bh	3Bh	-	3Bh	3Bh
	4READ	4 x I/O Fast Read	EBh	-	EBh	EBh	EBh
	QREAD	1I 4O Fast Read	6Bh	6Bh	-	6Bh	6Bh
	W4READ	4 x I/O Fast Read with 4 dummy clock cycles	E7h	-	-	-	-
	FASTDTRD	Fast DT Read	-	-	0Dh	-	-
	2DTRD	Dual I/O DT Read	-	-	BDh	-	-
	4DTRD	Quad I/O DT Read	-	-	EDh	-	-
	RDSFDP	-	5Ah	5Ah	5Ah	5Ah	5Ah
Erase	SE	Sector Erase	20h	20h	20h	20h	20h
	BE (64K)	Block Erase 64KB	D8h	D8h	D8h	D8h	D8h
	BE (32K)	Block Erase 32KB	52h	52h	52h	52h	52h
	CE	Chip Erase	60h or C7h	60h or C7h	60h or C7h	60h or C7h	60h or C7h
Program	PP	Page Program	02h	02h	02h	02h	02h
	4PP	Quad Page Program	38h	38h	38h	38h	38h
	CP	Continuously Program Mode	ADh	ADh	ADh	-	-
Mode	WREN	Write Enable	06h	06h	06h	06h	06h
	WRDI	Write Disable	04h	04h	04h	04h	04h
	DP	Deep Power Down	B9h	B9h	B9h	B9h	B9h
	RDP	Release from Deep Power Down	ABh	ABh	ABh	ABh	ABh
	EQIO	Enable QPI	-	-	-	35h	35h
	RSTQIO	Reset (Exit) QPI	-	-	-	F5h	F5h
	SBL	Set Burst Length	77h	-	-	C0h	C0h
	WPSEL	Write Protect Selection	68h	68h	68h	68h	68h
	ESRY	Enable SO to Output RY/BY#	70h	70h	70h	-	-
	DSRY	Disable SO to Output RY/BY#	80h	80h	80h	-	-
	ENPLM	Enter Parallel Mode	-	55h	55h	-	-
	EXPLM	Exit Parallel Mode	-	45h	45h	-	-
	HPM	High Performance Mode Enable	-	-	A3h	-	-
	ENSO	Enter Secured OTP	B1h	B1h	B1h	B1h	B1h
	EXSO	Exit Secured OTP	C1h	C1h	C1h	C1h	C1h
	PGM/ERS Suspend	Suspend Program/ Erase	-	-	-	B0h	75h or B0h
	PGM/ERS Resume	Resume Program/ Erase	-	-	-	30h	7Ah or 30h

Table 5-1: Command Code Comparison - Reset/Register/Protection

Command	Symbol	Description	MX25L12835E	MX25L12836E	MX25L12845E	MX25L12835F	MX25L12833F
Reset	NOP	No Operation	00h	-	-	00h	00h
	RSTEN	Reset Enable	66h	-	-	66h	66h
	RST	Reset Memory	99h	-	-	99h	99h
	CLSR	Clear SR Fail Flags	30h	30h	30h	-	-
Register	WRSR	Write Status Register	01h	01h	01h	01h	01h
	RDSR	Read Status Register	05h	05h	05h	05h	05h
	RDSCUR	Read Security Register	2Bh	2Bh	2Bh	2Bh	2Bh
	WRSCUR	Write Security Register	2Fh	2Fh	2Fh	2Fh	2Fh
	RDCR	Read Configuration Register	-	-	-	15h	15h
	RDFBR	Read Fast Boot Register	-	-	-	16h	-
	WRFBR	Write Fast Boot Register	-	-	-	17h	-
	ESFBR	Erase Fast Boot Register	-	-	-	18h	-
Protection	SBLK	Single Block Lock	36h	36h	36h	-	-
	SBULK	Single Block Unlock	39h	39h	39h	-	-
	RDBLOCK	Block Protect Read	3Ch	3Ch	3Ch	-	-
	GBLK	Gang Block Lock	7Eh	7Eh	7Eh	7Eh	7Eh
	GBULK	Gang Block Unlock	98h	98h	98h	98h	98h
	WRLR	Write Lock Register	-	-	-	2Ch	2Ch
	RDLR	Read Lock Register	-	-	-	2Dh	2Dh
	RDPASS	Read Password Register	-	-	-	27h	-
	WRPASS	Write Password Register	-	-	-	28h	-
	PASSULK	Password Unlock	-	-	-	29h	-
	RDSPB	Read SPB Status	-	-	-	E2h	E2h
	WRSPB	SPB bit Program	-	-	-	E3h	E3h
	ESSPB	All SPB bit Erase	-	-	-	E4h	E4h
	SPBLK	SPB Lock Set	-	-	-	A6h	-
	RDSPBLK	Read SPB Lock Register	-	-	-	A7h	-
	RDDPB	Read DPB Register	-	-	-	E0h	E0h
	WRDPB	Write DPB Register	-	-	-	E1h	E1h

6. Device ID Code Comparison

The Manufacturer and Device IDs are not changed, as shown in **Table 6-1**.

Table 6-1: ID Code Comparison

Electronic Identification		MX25L12835E	MX25L12836E	MX25L12845E	MX25L12835F	MX25L12833F
RDID	Manufacturer ID	C2h	C2h	C2h	C2h	C2h
	Type	20h	20h	20h	20h	20h
	Density	18h	18h	18h	18h	18h
RES	Electronic ID	17h	17h	17h	17h	17h
REMS/ REMS2/ REMS4	Manufacturer ID	C2h	C2h	C2h	C2h	C2h
	Device ID	17h	17h	17h	17h	17h

7. Summary

The MX25L12835F/33F is backwards compatible with most of the common commands and features of the earlier E versions.

The MX25L12835F has additional 4K-bit secured OTP mode while MX25L12833F has additional 8K-bit secured OTP mode. Futhermore, MX25L12833F does not provide fast boot mode and password protection.

8. References

Table 8-1 shows the datasheet versions used for comparison in this application note. For the most current Macronix specification, please refer to the Macronix Website at *http://www.macronix.com*

Table 8-1: Datasheet Version

Datasheet	Location	Date Issued	Versions
MX25L12833F	Macronix Website	October 17, 2017	1.0
MX25L12835F	Macronix Website	July 22, 2016	1.6
MX25L12845E	Macronix Website	September 06, 2013	1.9
MX25L12836E	Macronix Website	August 01, 2012	1.7
MX25L12835E	Macronix Website	May 28, 2012	1.3

9. Revision History

Table 9-1: Revision History

Revision No.	Description	Page	Date
Rev. 1	Initial Release	ALL	September 06, 2017
Rev. 2	Updated MX25L12833F Program and Erase values	9, 13	October 17, 2017
Rev. 3	Updated datasheet issued date	13	October 19, 2017
Rev. 4	1. Revised DC Performance Comparison 2. Added "Macronix Proprietary" footnote	9, ALL	July 10, 2018

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