Subrahmanian Hari
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EDUCATION

University of California Santa Cruz, CA 2022-2026
B.S. Computer Engineering
GPA: 3.70

INTEREST

I am looking for internship positions that will provide experience in front-end stages of the SoC-ASIC design flow.

SKILLS

- **Relevant Coursework:** Advanced Python, Computer Architecture I, Logic Design I, Analog Circuit Theory I, Electromagnetism in Physics, ASIC System Design (*in progress*)
- **Programming:** Verilog, Python, C, Java/JS/TS, HTML/CSS, (RISC-V) Assembly, MATLAB
- **Software:** Github, Eagle CAD, LaTeX, Arduino, Onshape, KiCad, Vivado, Synposys VCS, (Ubuntu) Linux
- **Practical:** Surface Mount/Through-hole Soldering, Oscilloscope, Waveform Generator

ACADEMIC POSITIONS

Slugbotics *Control Systems Lead* 2022-2024

- Developed Python handler script to collect and transfer joystick vector packets over ethernet
- Implemented error checking algorithm to safely transfer electronic speed controller instructions over 40 foot wire
- Used hash-map to effectively reduce size of packets over wire in half
- Prototyped physical thruster guards with larger mesh sizes using Onshape CAD

SiliconValley4u *SWE Intern* 2020-2021

- Designed and implemented responsive page designs auto-scaled for multiple aspect ratios using Figma and HTML5
- Implemented file uploading and parsing for on-site resume submission in (Angular) Typescript
- Established user claims hierarchy and user authentication with token validation in Firebase Auth API

PROJECTS

Asynchronous FIFO (Verilog): 2024

- Designed a N-deep parameterized FIFO buffer capable of handling asynchronous access operations between different clock domains
- Utilized synchronizer cells to preserve order of read/writes across domains
- Pointers passed as gray code to minimize meta-stability risk between flop transitions
- Developed comprehensive testbench to ensure correct functionality and performance under various conditions

Single Cycle ALU (Verilog/RISCV32I): 2024

- Designed and implemented a 32-bit signed ALU supporting arithmetic (addition, subtraction), logical (AND, OR, XOR), and shift operations
- Integrated overflow detection and two's complement representation to handle signed integer operations and edge cases like overflow/underflow
- Optimized the ALU using a carry-lookahead adder for faster addition operations by reducing critical path delay
- Verified functionality through directed test-benches and random input simulation

UCSC Catalog Web Scraper (Python): 2023

- Designed a web scraper using Pandas and BeautifulSoup to format UCSC catalog
- Used key and value pair for sorting and dumping into data frame
- Implemented in Discord platform for scalability and ease of use