194083 U
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Assignment - 04

Q1)

1) Size of cache memory = 512 kB
$= 2^{19}$ bytes

memory word size = 4 bytes

In 1 block 4 words = $4 * 4 = 16$ bytes
$= 2^4$

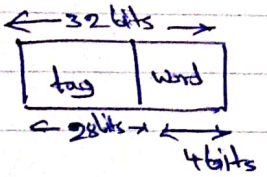
address bus width = 32 bits

No of cache lines = $\frac{512 \times 2^{10}}{16}$

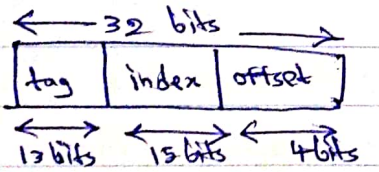
$= \frac{2^{19}}{2^4} = 2^{15}$

$= 32,768$ lines

2) $16 = 2^4$



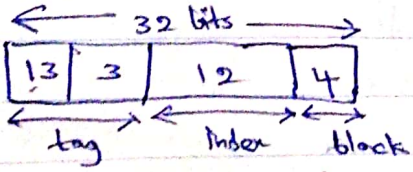
3)



4) No of sets the cache have = $\frac{2^{15}}{2^3}$

$= 2^{12}$

5)



6) 0xB1AC95F9 in binary form

1011 0001 1010 1100 1001 0101 1111 1001

1011 0001 1010 1	100	1001 0101 1111	1001

set number = 1001 0101 1111

Q2) $X = (A*B - C) + (A/C)$

1) stack based instruction set Architecture

```
PUSH A
PUSH B
MUL
PUSH C
SUB
PUSH A
PUSH C
DIV
ADD
POP X
```

2) Accumulator based instruction set Architecture

```
LOAD A
MUL B
SUB C
STORE y
LOAD A
DIV C
ADD y
STORE X
```

3) memory - memory based instruction set architecture

3 operands

```
MUL  X, A, B  ⇒  X = A*B
SUB  X, X, C  ⇒  X = X - C
DIV  y, A, C  ⇒  y = A/C
ADD  X, X, y  ⇒  X = X + y
```

2 operands

```
MOV  X, A  ⇒  X = A
MUL  X, B  ⇒  X = X*B
SUB  X, C  ⇒  X = X - C
MOV  y, A  ⇒  y = A
```

DIV y, c ⇒ y = y/c

ADD X, y ⇒ X = X+y

4. register - register based instruction set architecture

LOAD R1, A

LOAD R2, B

LOAD R3, C

MUL R4, R1, R2 ⇒ R4 = A*B

SUB R4, R4, R3 ⇒ R4 = R4 - C

DIV R5, R1, R3 ⇒ R5 = A/C

ADD R5, R4, R5 ⇒ R5 = R4 + R5

STORE X, R5 ⇒ X = R5

Q3) (-3) * 5

0011 = 3

1100

1

1101 = -3

M = 1101

n	A	Q	q_0	$q_1 q_0$	Action / Comment
4	0000	0101	0	10	Initial values
	0011	0101	0	10	A - M
	0001	1010	1		AQq_0 shift } first cycle
3	1110	1010	1	01	A = A+M
	1111	0101	0		AQq_0 shift } 2nd cycle
2	0010	0101	0	10	A = A-M
	0001	0010	1		AQq_0 shift } 3rd cycle
1	1110	0010	1	01	A = A+M
	1111	0001	0		AQq_0 shift } 4th cycle

Result ⇒ AQ = 11110001 first bit is 1 so negative value

= (-1)(1110001)

result = −0001110

+1

−0001111

(−15)

−3 × 5 = −15

Q4) Fetch - Execute cycle in RTL

Instruction is fetched, decoded and executed

MAR ← PC

MBR ← M[AR]

IR ← MBR

PC ← PC + 1

operand value is fetched, decoded and executed

MAR ← IR

MBR ← M(AR)

AC ← MBR

PC ← PC + 1

After process of ALU

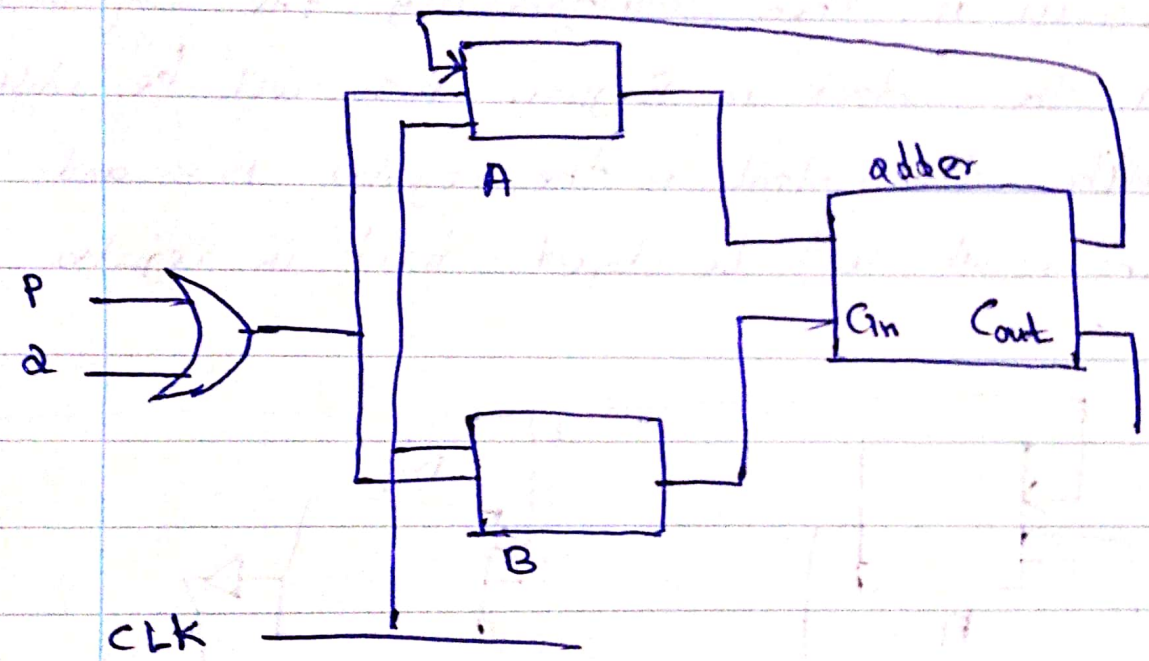
MBR ← AC

M[AR] ← MBR

PC ← PC + 1

2.5)

1. P+Q : A ← A+B if P+Q is true the content in register A is added with the content B register and the result will be stored in register A



2. Q: $A \leftarrow A+B$, $R_1 \leftarrow R1' + R2$

if Q is true then the content in register A will be added to content in register B and then the result will be stored back in register A. Then simultaneously the compliment of the content in Rregister R1 will be added with the content in the register R2 and the result will be stored back in register R1.