DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER VI [CE]
SUBJECT: (CE-610) ADVANCED COMPUTER ARCHITECTURE

Examination	**: First Sessional**	**Seat No**	**: 103**
Date	**: 02/01/2025**	**Day**	**: Thursday**
Time	**:2.30 PM to 3.45 PM**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed. **[12]**

CO6-R a) Convert the decimal number (-94.625) to its IEEE 754 double precision representation. **2**

CO6-U b) Outline the format of the status word register in 8087 and discuss the purpose of individual bits. **2**

CO1-U c) Give the format of the EFLAG register and explain the meaning of the flags used in the protected mode. **2**

CO4-U d) For the given instruction stream in Fig 1. Find out the true dependent and anti-dependent instructions and their respective Registers on which dependency arises. **2**

```
ADD  R5, R0, R1    R5 ← R0 + R1
MUL  R6, R2, R5    R6 ← R2 – R5
SUB  R5, R3, R6    R5 ← R3 – R6
DIV  R6, R5, R4    R6 ← R5 / R4
STR  R6, X         X ← R6
```

Fig 1

CO4-N e) Distinguish between Super-pipelining and Superscalar processors. **2**

CO4-E f) What are the criteria for the classification of Parallel Computer Architectures? **2**

Q.2 Attempt Any Two **[12]**

CO6-E b) Consider the following data items defined as double word (DD) **[6]**
a = 2.5670, b = 3.50 , c = 4.50 , d = 4.0 , x = 3.50 and y = 2.50
Analyze the given 8087 program code snippets in Fig 2 and Fig 3 and report the values of the stack registers after each instruction.

```
fld b
fmul b
fld d
fld a
fmul
fmul c
fsubr
fsqrt
```

Fig 2

```
fld x
fld y
fyl2x
fld d
fsub
f2xm1
fld1
fadd
fld1
fxch
fscale
```

Fig 3

CO1-U b) Illustrate the internal architecture of the 80286 processor and elaborate on the function of each unit. [6]

CO6-C c) Write an ALP to compute roots of quadratic equation using 8087 instructions. If roots are imaginary display message "Roots are imaginary". [6]

Q.3 Answer the following [12]

CO4-A a) The maximum ideal speedup of the pipeline is 5. Let the percentage of unconditional branches in a set of typical programs be 9% and that of conditional branches be 15%. Assume that 85% of the conditional branches are taken in the program. (Branch taken delay = 3 cycles and not taken = 2 cycles)

i. What is the percentage loss of speedup due to the branches? [1]

ii. Extra hardware is used at decode stage to reduce delay cycles to 1 for a branch being taken and 0 cycles for branch being not taken. What is the percentage loss of speedup from ideal case and gain over the previous one? [2]

iii. BTB is used with a prediction accuracy of 91% and the probability of 0.96 that a branch entry would be present in BTB. What is the percentage loss of speedup from ideal case? [3]

CO4-N b) With the help of an example explain how can data parallelism be achieved using dynamic assignment? Discuss the analysis for the scalability of the dynamic assignment method. [6]

OR

CO4-A a) Consider the given instruction stream in Fig 4. Draw the Time-Space diagram for the assignment of instructions to different Processing Elements (PEs), also give the total clock cycles taken to complete the instruction stream over 5 elements of Vector A using [6]

i. Array Processor

ii. Vector Processor

(assume each operation takes 1 clock cycle for processing one element of vector)

```
LD   VR ← A[4:0]
ADD  VR ← VR, 1
MUL  VR ← VR, 2
SUB  VR ← VR, 3
DIV  VR ← VR, 4
ST   A[4:0] ← VR
```

Fig 4

CO4-N b) Discuss the Features, Merits and Demerits of [6]

i. VLIW Architecture

ii. Systolic Architecture

Bloom's Taxonomy levels: R-Remembering, U- Understanding, A-Applying, N-Analyzing, E- Evaluating, C-Creating