DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER III [COMPUTER ENGINEERING]
SUBJECT: (CE318) NAME: DESIGN OF DIGITAL CIRCUITS

Examination : Regular
Date : 08/11/2023
Time : 10:00 to 1:00 pm
Seat No :
Day : Wednesday
Max. Marks : 60

INSTRUCTIONS:

1. Answer each section in a separate answer book.
2. Figures to the right indicate maximum marks for that question.
3. The symbols used carry their usual meanings.
4. Assume suitable data, if required & mention them clearly.
5. Draw neat sketches wherever necessary.

SECTION – I

Q.1 Do as directed. [10]

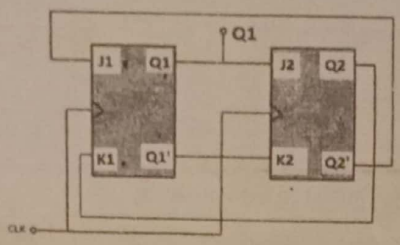
CO1 C (a) Let r denote the number system radix. The only value(s) of r that satisfy the equation $\sqrt{121}_r = 11$, is? [2]

CO2 A (b) Show the advantage of (r-1)'s complement over r's complement with an example. [2]

CO2 E (c) For an n - variable Boolean function how many maximum prime implicants are possible? [2]

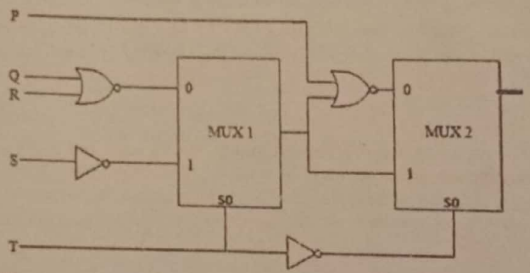
CO3 U (d) The size of the ROM needed to implement a 4 bit multiplier is ? [2]

CO4 N (e) The outputs of the two flip-flops Q1, Q2 in the figure shown are initialized to 0, 0. What is the sequence generated at Q1 upon application of clock signal? [2]



Q.2 Attempt *Any TWO* from the following questions. [10]

CO2 C (a) [5]



For the circuit shown in the above figure, determine the output of MUX 2 with steps. Show applications of the multiplexer.

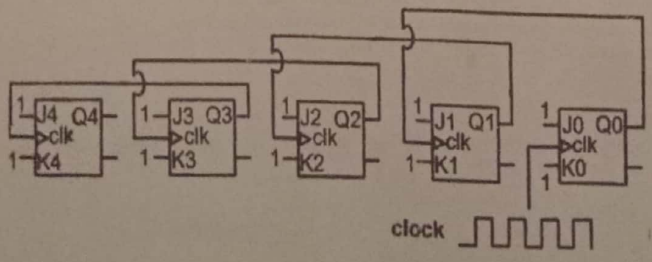
CO2 C (b) Design a 4-to-1 multiplexer using 2-to-4 Decoder. Support with the truth table and boolean expressions. [5]

CO2 C (c) Design a single combinational circuit for converting BCD to 2421 code using encoders and decoders. Also construct the truth table. [5]

Q3. Attempt the following: [10]

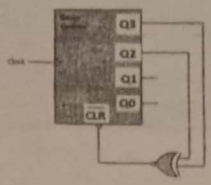
CO3 A (a) Design a mod-6 counter with the sequence 10,11,12,13,14,15 using a binary counter with parallel load MSI. Show the steps with a state table, and a diagram. [5]

CO4 N (b) Show the State table, counting logic, state diagram and timing diagram of the counter shown in the below figure. [5]



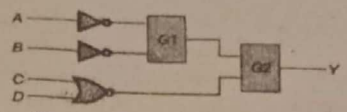
OR

Q3.		**Attempt the following:**		[10]
CO3	A	(a)	Design a 3 -bit Synchronous Counter which can count odd and even sequences in a single circuit based on Mode Input M. Show the steps with a state table, and a diagram.	[5]
CO4	N	(b)	The below figure shows a binary counter with synchronous clear input. Determine the mod counting performed by the counter. Show the State table, counting logic, state diagram and timing diagram of the counter.	[5]



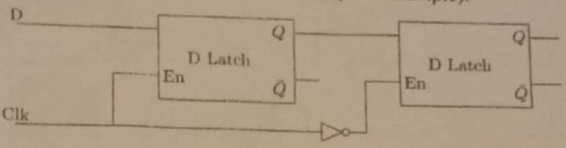
SECTION – II

Q.4		**Do as directed.**		[10]
CO3	N	(a)		[2]



Analyze the circuit shown in the above figure, the output required is Y = AB + C'D'. Determine the gates G1 and G2 which will result in the expression Y.

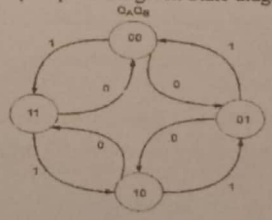
CO3	N	(b)	Analyze the total number of self dual functions with n variables (with example).	[2]
CO1	E	(c)		[2]



Describe the functionality achieved by the circuit shown in the above figure.

CO4	U	(d)	Explain the difference between Flip flop and a latch.	[2]
CO1	A	(e)	Apply the concept of Edge triggering and level triggering with their respective applications.	[2]
Q.5		**Attempt *Any TWO* from the following questions.**		[10]
CO2	C	(a)	Design the circuit which converts a full adder to full-subtractor, derive the equations.	[5]
CO2	C	(b)	Design the circuit for function F = ∑m(0,1,3,7,8). Minimize it using Quine-McCluskey Technique.	[5]
CO2	C	(c)	Design the circuit for F(a,b,c) = a'c + ac' + b'c, showing the total number prime implicants, and Essential prime implicants.	[5]

Q.6		**Attempt the following:**		[10]
CO3	N	(a)	A sequential circuit has two flip flops A and B, two inputs x and y and an output z. The flip flop functions and the circuit output function are as follows: JA = xB + y'B', KA = xy'B', JB = xA', KB = xy' + A, and Z = xyA + x'y'B. Obtain the logic diagram, state table, state diagram, and state equations.	[5]
CO3	C	(b)	Design a synchronous counter using JK flip flop for the given State diagram.	[5]



OR

Q.6		**Attempt the following:**		[10]
CO3	N	(a)	The full adder receives two external inputs x and y; the third input z comes from the output of a D flip flop. The carry output is transferred to the flip flop every clock pulse. The external S output gives the sum of x,y, and z. Obtain the state table and state diagram of the sequential circuit.	[5]
CO3	C	(b)	Design a counter that counts the decimal according to 2421 code using T flip flops, with state table and state diagram.	[5]

Bloom's Taxonomy levels: R-Remembering, U- Understanding, A-Applying, N-Analyzing, E- Evaluating, C-Creating