DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
SECOND SESSIONAL
SUBJECT: (CE-417) COMPUTER SYSTEM ARCHITECTURE

Examination	**: B. Tech Semester-IV**	**Seat No**	**: _____**
Date	**: 07/02/2024**	**Day**	**: Wednesday**
Time	**: 01:00 P.M.-02:15 P.M.**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed. **[12]**

CO4 E (a) Assume a two-level inclusive cache hierarchy, L1 and L2, where L2 is the larger of the two. Consider the following statements. **[2]**

- **S1:** Read misses in a write through L1 cache do not result in writebacks of dirty lines to the L2
- **S2**: Write allocate policy must be used in conjunction with write through caches and no-write allocate policy is used with writeback caches.

Which of the following statement/s is/are true? Justify your answer "Why"?

CO2 A (b) Write an assembly language program to find the GCD of given numbers. **[4]**

CO1 U (c) Using Booth's Algorithm for multiplication, encode the multiplier **-57**. **[1]**

CO1 N (d) What is the worst case for the number of additions/subtractions in Booth's algorithm? Justify. **[1]**

CO1 U (e) How to add three 4-bit numbers using Carry Save Adder? Explain with the help of following 3 unsigned numbers: X=1001; Y=0110; Z=1110. **[2]**

CO1 R (f) How to do addition of two floating point numbers represented in $\mathbf{M * B^E}$ format? Explain with the help of suitable example. **[2]**

Q.2 Attempt *Any Two* of the following questions. **[12]**

CO4 A (a) List out all the cache replacement policies, and explain only LRU. **[3]**

Consider a 2-way set associative cache memory with 4 sets and 8 cache blocks (0-7) and a main memory with 128 blocks (0-127). What memory blocks will be present in the cache after the following sequence of memory block references if LRU policy is used for cache block replacement. **[3]**

Request: 0 5 3 9 7 0 16 55

CO4 N (b) Explain the types of Caches in brief. **[3]**

Consider a system has a WRITE-THROUGH cache with access time of 100ns and hit ratio of 90%. The main memory access time is 500ns. The 70% of memory references are of read operations. Then find the following, **[3]**

1. Average memory access time for read operations only.
2. Average memory access time for Write operations only.
3. Average memory access time for Read-write operations both

CO4 N (c) How the physical address is divided in k-way set associative memory? Show the hardware implementation of it. Consider the size of the physical address space of a processor is 2P bytes. The word length is 2W bytes. The capacity of cache memory is 2N bytes. The size of each cache block is 2M words. Determine the size of TAG field for K-way set cache. **[6]**

Q.3 Attempt the following questions. **[12]**

CO1 A (a) Write algorithm for the Restoring Division Method. Apply it over **11/4**. Show every step of computation. **How to compute -11/4 using 11/4?** **[6]**

CO1 N (b) A CPU is designed to have 58 three-address instructions and 32 two-address instructions and X one-address instructions. The CPU can address a maximum of 16 memory locations. The length of machine code is the same for all instructions. If the list of the machine codes is obtained by using the expanding opcode technique, answer the following questions: **[6]**

i. Determine the maximum number of bits allocated for each address fields. Determine the minimum number of bits allocated for the opcode field of three address instructions. Determine the minimum number of bits allocated for the opcode field of two address instructions.

ii. Determine the length of the machine code. List the Machine codes.

iii. Determine Maximum Value for X.

OR

CO1 A (a) Write algorithm for the Booth's Method of signed multiplication. Apply it over **(-7) * 8**. Show every step of computation. **[6]**

CO1 N (b) i. Consider the IEEE-754 single precision floating point numbers **P=0xC1800000** and **Q=0x3F5C2EF4**. Obtain the product of these numbers (i.e., P × Q), represented in the IEEE-754 single precision format? **[3]**

ii. Explain requirement of **Guard Bit, Round Bit and Sticky bit** with the help of **suitable example**. **[3]**