DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH SEMESTER-3 (CE)
FIRST SESSIONAL
SUBJECT: (CE-308) Design of Digital Circuits

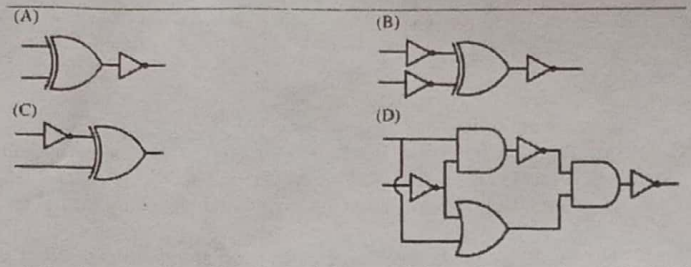
Examination	**: First Sessional**	**Seat No.**	**: 31**
Date	**: 02/08/2023**	**Day**	**: Wednesday**
Time	**: 11.00 AM to 12.15 PM**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 **Do as directed.** **[12]**

R (a) Which one of the following circuits is NOT equivalent to a 2-input XNOR (exclusive NOR) gate? [2]

CO2



CO2 U (b) Consider the following Boolean function of four variables: f(w,x,y,z) = ∑(1,3,4,6,9,11,12,14). Which of the variable(s) is/are not impacting the function? [2]

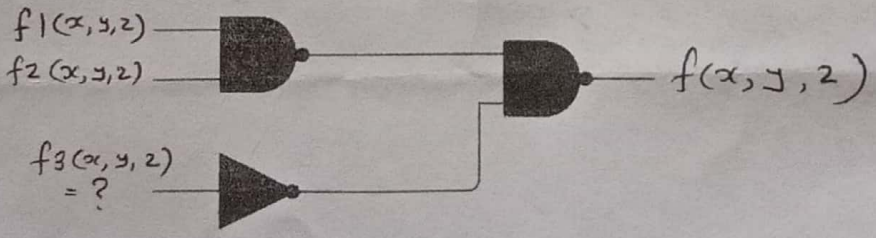
CO2 A (c) How many minimum number of gates are required to implement the Boolean function (BC+D) if we have to use only 2-input NOR gates? Show the circuit. [2]

CO2 A (d) X = 01110 and Y = 11001 are two 5-bit binary numbers represented in two's complement format. Determine the sum of X and Y represented in two's complement format using 6 bits. [2]

CO1 A (e) Consider $(43)_x = (y3)_8$. What could be the possible values of x and y? [2]

R (f) Consider the following logic circuit whose inputs are functions f1,f2, f3 and output is f. [2]

CO1



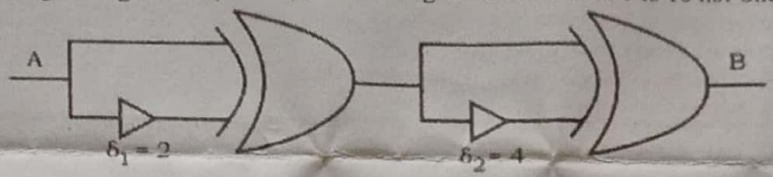
Given that
f1(x, y, z) = ∑(0, 1, 3, 5),
f2(x, y, z) = ∑(6, 7) and
f(x, y, z) = ∑(1, 4, 5), then determine f3.

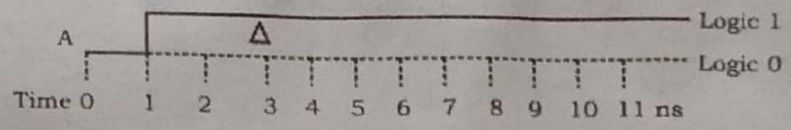
Q.2 Attempt ***Any TWO*** from the following questions. **[12]**

CO2 A (a) Minimize the following boolean functions using algebraic manipulation [6]
F1 = abc'd' + abc'd + ab'c'd + abcd + ab'cd + abcd' + ab'cd'
F2 = AB + (AC)' + AB'C(AB + C)

CO2 A (b) Simplify the function F(a,b,c,d,e,f) = Σ (6,9,13,18,19,25,27,29,45,47,61) by means of the tabulation method. [6]

CO1 U (c) Consider the following circuit composed of XOR gates and non-inverting buffers. The non-inverting buffers have delays δ1=2ns and δ2=4ns as shown in the figure. Both XOR gates and all wires have zero delays. Assume that all gate inputs, outputs, and wires are stable at logic level 0 at time 0. If the following waveform is applied at input A, how many transition(s) (change of logic levels) occur(s) at B during the interval from 0 to 10 ns? Show the output at B. [6]





Q.3 Attempt the following [12]

CO2 A (a) Simplify the below Boolean expression using K-Map and implement with both Universal Gates. [6]
F (A,B,C,D) = A'B'C'D' + AC'D' + B'CD' + A'BCD + BC'D
Note: Both Normal and Complemented inputs are available.

CO2 N (b) Simplify the below Boolean function along with the don't care conditions in both SOP and POS forms. [6]
F (w,x,y,z) = w' (x'y + x'y' + xyz') + x'z' (y + w)
d= w'x (y'z + yz') + wyz

OR

Q.3 Attempt the following [12]

CO2 A (a) Simplify the below function in both SOP and POS form using K Map. [6]
F (A,B,C,D) = (A' + B' + D') (A + B' + C') (A' + B + D') (B + C' + D')

CO2 N (b) Simplify and Implement the below Boolean expression using : [6]
1. No more than 4 NAND gates
2. No more than 3 NOR Gates

F (A,B,C,D) = AB' + ABD + ABD' + A'C'D' + A'BC'