DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER VI [CE]
SUBJECT: (CE-610) ADVANCED COMPUTER ARCHITECTURE

Examination	**: Third Sessional**	**Seat No**	**: 103**
Date	**: 20/03/2025**	**Day**	**: Thursday**
Time	**: 2.30 PM to 3.45 PM**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed. **[12]**

CO2-R a) Fill in the blanks **2**

i. The TSS descriptor is stored only in the _____.
ii. The maximum size of the I/O permission bit map is _____.
iii. In TSS descriptor minimum value of LIMIT is _____
iv. Address of branch instruction is stored in _____.

CO2-N b) State true or false and justify: Busy bit prevents reloading of an active task in 80386. **2**

CO2-U c) Explain the concept of hyper-threading. **2**

CO3-U d) What is the cost of a parallel algorithm, and under what conditions is a parallel algorithm considered cost-optimal? **2**

CO3-C e) Design a pseudocode algorithm to compute the OR of n bits using a Common CRCW PRAM model. **2**

CO3-E f) Consider two 5x5 matrices A and B interconnected as mesh network. If a matrix multiplication algorithm is run on this mesh network **2**

i. In how many steps would this algorithm end?
ii. In which step processor $P_{4,3}$ would compute the value $C_{4,3}$?

Q.2 Attempt Any Two **[12]**

CO2-U b) i. Explain the NT (Nested Task) flag in the 80386 processor. How does it affect task switching in a multitasking environment? **[3]**

ii. What is IO Permission Bitmap? Draw and explain it with proper diagram. **[3]**

CO2-A b) Explain how task switching occurs in the 80386 processor using Direct method and Task Gate. Provide necessary diagrams and examples where applicable. **[6]**

CO2-N c) i. Draw the format of IDT and give the steps followed when an interrupt occurs using an Interrupt Gate. **[3]**

ii. Suppose an exception handler needs to switch to a new privileged task using a Task Gate in the IDT. Describe how the IDT entry would differ and how the CPU performs the task switch. **[3]**

Q.3 Answer the following questions **[12]**

CO3-C a) i. Consider an unsorted sequence of 16 numbers given by S = < 37, 12, 54, 06, 45, 72, 08, 60, 03, 33, 26, 67, 15, 71, 47, 09 >. Create a bitonic sorting network for S to produce a sorted sequence in ascending order. Leaving first and last stage draw the detailed network for the intermediate stages. **[6]**

CO3-N ii. Analyze the network created in (i) to give the recurrence relation for the depth of the network. Use this recurrence relation to find the depth of the network. **[2]**

CO3-C b) Consider two sorted sequences given by S1 = < 02, 03, 06, 08 > and S2 = <01, 04, 05, 07 >. Create an Odd-Even Merging network OEM (4, 4). Give the recurrence relation for calculating the depth of the network. **[4]**

OR

CO3-C a) Consider an unsorted sequence of 16 numbers given by S = < 33, 31, 02, 05, 18, 16, 01, 04, 09, 08, 07, 63, 72, 03, 91, 23> Create an Odd – Even Merge sorting network for n=16 to produce a sorted sequence in ascending order. Leaving the last stage draw the detailed network for the rest of the stages. Give the depth and the size of the network. **[8]**

CO3-C b) Consider a bitonic sequence given by S = < 06, 08, 12, 37, 45, 54, 60, 72, 71, 67, 47, 33, 26, 15, 09, 03> Create a bitonic merging network to produce the sorted sequence in ascending order. **[4]**

Bloom's Taxonomy levels: R-Remembering, U- Understanding, A-Applying, N-Analyzing, E- Evaluating, C-Creating