DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
THIRD SESSIONAL
SUBJECT: (CE-417) COMPUTER SYSTEM ARCHITECTURE

Examination	**: B.Tech Semester-IV**	**Seat No**	**: _____**
Date	**: 20/03/2024**	**Day**	**: Wednesday**
Time	**: 01:00 P.M.-02:15 P.M.**	**Max. Marks**	**: 36**

INSTRUCTIONS:

1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed. **[12]**

CO3 E (a) Identify the 8085 instruction from information of Timing Diagram: Instruction Size is 1-Byte. It has 2 Machine cycles: Opcode Fetch, Memory Write. Justify. **[2]**

CO3 A (b) Calculate the timing delay for the following code. Assume the frequency of the microprocessor is 4 MHz. **[2]**

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        MVI B, 0AH; 7 T-states
REPEAT: DCR B; 4 T-states
        JNZ REPEAT; 7/10 T-states
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CO3 R (c) Explain disadvantage of strobe method. Which method is used for overcoming the issue? **[2]**

CO2 U (d) What is structural Hazard in the pipelined system? Give suitable example and write possible solution for the structural hazard. **[2]**

CO2 A (e) Consider Instruction Pipeline with 4 stages each with combinational circuit only. Buffer registers are required between each stage and at the end of last stage. Delays for the stages are 5,6,11,8ns respectively. Delay for buffer register is 1ns. Find out the speedup of the pipeline. **[2]**

CO2 N (f) Compare and contrast Hardwired and Microprogrammed Control Unit. **[2]**

Q.2 Attempt *Any Two* of the following questions. **[12]**

CO3 A (a) Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. Assume that for 20% of the total page faults, a dirty page has to be written back to disk before the required page is read from disk. TLB update time is negligible. What is the average memory access time in ns? **[6]**

CO3 N (b) Analyze different modes of IO transfer. Suppose DMA is employed in two modes 1)Cycle Stealing Mode 2)Burst Mode. Transfer of bus control from CPU to I/O or I/O to CPU takes 300ns. Assume the system in which bus cycle takes 700ns and one of the I/O device has a data transfer rate of 50KB/sec and employs DMA. Data are transferred one byte at a time. Find the time taken for the I/O device to transfer a block of 100 bytes in both the modes. **[6]**

CO3 A (c)
i. How hard disk is designed? Explain the designing of it. **[2]**
ii. Consider a disk with 8 platters having 16384 cylinders, and 64 sectors per track. A file size of 42797 KB is needed to be stored with starting location of file is <1200,9,40>. Determine the cylinder number of last sector of the file. **[4]**

Q.3 Attempt the following questions. **[12]**

CO2 U (a) i. Considering control hazards in the pipeline, explain how branch delay can be reduced from 3-Cycle to 1-Cycle? **[2]**

ii. What is Branch Target Buffer? How can that be used with 2-bit dynamic branch predictor to reduce branch delay? **[4]**

CO2 A (b) Consider Micro-programmed Control Unit which supports 240 instructions, each of which on an average takes 16 Micro-operations. They support 16 flag conditions and 150 control signals. Find out the length of Micro-Instruction and size of the Control Memory for each of the following control unit design strategy: **[6]**

i. Horizontal Micro-programming.
ii. Vertical Micro-programming.
iii. Control signals are divided into 5 mutually exclusive groups, each group having 30, 60, 12, 40, 8 control signals respectively.

OR

CO2 N (a) Consider the sequence of machine instructions using R0 to R8 registers: **[6]**

MUL R5, R0, R1;**R5=R0*R1**
DIV R6, R2, R3; **R6=R2/R3**
ADD R7, R5, R6; **R7=R5+R6**
SUB R8, R7, R4; **R8=R7-R4**

This sequence of instructions is to be executed in a pipelined instruction processor with the following 5 stages: (1) Instruction Fetch (IF) (2) Decode (ID), (3) Operand Fetch (OF), (4) Perform Operation (PO) and (5) Write back the Result (WB).
The IF, ID, OF and WB stages take 1 clock cycle each for any instruction.
The PO stage takes 1 clock cycle for ADD or SUB instruction, 3 clock cycles for MUL instruction and 5 clock cycles for DIV instruction.
The pipelined processor uses operand forwarding from the PO stage to the OF stage. Find out the number of clock cycles taken for the execution of the above sequence of instructions. **Show the detailed space-time diagram for the execution of above sequence.**

CO2 C (b) Consider the following state diagram.

i. Is it Mealy machine or Moore Machine? Why? **[1]**

ii. Assume **One-Hot Encoding** technique is used, how many flipflops are required to implement the control unit? Write equations for obtaining next states of flipflops. Write equations for obtaining output control signals C_0 C_1,C_2,C_3,C_4,C_5. **[4]**

iii. If you have used Classical Method for Control unit design, how many flipflops are required to implement the control unit? **[1]**