**DHARMSINH DESAI UNIVERSITY, NADIAD**
**FACULTY OF TECHNOLOGY**
**FIRST SESSIONAL**
**SUBJECT: (CE-417) COMPUTER SYSTEM ARCHITECTURE**

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| **Examination** | **: B. Tech Semester-IV** | **Seat No** | **: _____** |
| **Date** | **: 03/01/2024** | **Day** | **: Wednesday** |
| **Time** | **: 01:00 P.M.-02:15 P.M.** | **Max. Marks** | **: 36** |

**INSTRUCTIONS:**

1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

**Q.1 Do as directed.** **[12]**

**CO1 C** (a) Design Full Subtractor at Gate Level. **[2]**

**CO2 A** (b) A block of 5 bytes of data is stored at 2050H onwards. Transfer the data to the location 2080H in the **reverse order**. Write 8085 instructions for the same. **[4]**

**CO1 N** (c) Consider the statement **Z=X+Y**, where **X, Y and Z** are the Memory Addresses. Assume Simple Accumulator based CPU Architecture. **[2]**

Write Assembly instructions to implement **Z=X+Y** using following different ways:

**Way 1**: Load/Store Architecture based instructions.

**Way 2:** Instructions can refer Single Memory Address.

**CO2 E** (d) Consider the following instructions of 8085. Assume all the flags are RESET initially. **[2]**

```
MVI A, 80H
MVI B, 88H
XRA A
SUB B
```

Write the status of Carry and Zero flag after each instruction. Justify your answer.

**CO1 U** (e) What is $(1111\ 1110)_2$ in decimal, assuming following two cases: **[1]**

**Case 1**: It is 8-bit unsigned number.

**Case 2:** It is 8-bit signed number represented using 2's Complement.

**CO1 A** (f) Check for Overflow flag while adding following 8-bit signed numbers:**7F H and 02 H**. Justify your answer. **[1]**

**Q.2 Attempt *Any Two* of the following questions.** **[12]**

**CO2 N** (a) i. Explain Instruction format for each of the addressing modes. **[4]**

ii. Consider a processor that can address 50 instruction operations uniquely, it has 30 different general-purpose registers. A 32-bit instruction word has an opcode, two register operands and one immediate operand. Determine how many bits of immediate data can be given as an input in the instruction word. **[2]**

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| **CO2** | **N** | | i. Explain the Architecture of IAS Machine. | **[3]** |
| | | | ii. Show the steps of Instruction Cycle of **SUB X** instruction of **IAS** Machine clearly. | **[3]** |
| **CO2** | **N** | (c) | Derive the formula for speedup parameter in context of a non-pipelined and pipelined system. Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Calculate the speed up achieved in this pipelined processor. | **[6]** |

**Q.3 Attempt the following questions.** **[12]**

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|---|---|---|---|---|
| **CO1** | **A** | (a) | i. Represent following 8 bytes in Little-Endian and Big-Endian Architectures respectively. Assume Memory is byte addressable and starting address is 2500H. Number consisting of 8 Bytes is 2F 56 12 7D 9A BC FF A0 H. | **[2]** |
| | | | ii. Convert following number to IEEE-754 Single precision format: **$(-192.75)_{10}$** . | **[3]** |
| | | | iii. Do XS-3 Addition of following BCD: **7+ 4** | **[1]** |
| **CO2** | **U** | (b) | i. Write Addressing Modes for the following instructions:<br>MOV A,M; CMA; LDA 4500H ; MVI C, 34H; MOV D,A.<br>Here **;** is used to separate instructions of 8085. | **[3]** |
| | | | ii. Differentiate IO Mapped IO and Memory Mapped IO. | **[1.5]** |
| | | | iii. Derive the Minimum representable number in the Denormalized representation for IEEE-754 format. | **[1.5]** |

**OR**

| | | | | |
|---|---|---|---|---|
| **CO1** | **A** | (a) | i. Explain step by step BCD Addition over following 8-bit numbers: **78H + 89H.** | **[3]** |
| | | | ii. Convert following number to IEEE-754 Single precision format: **$(192.75)_{10}$** | **[3]** |
| **CO2** | **U** | (b) | i. Explain CPU behavior with suitable diagram. | **[3]** |
| | | | ii. Encode a binary message 1110 into the hamming code. Assume that transmission of the hamming code contains 1 bit error. **Do this by changing any 1 bit of the hamming code obtained**. Show how the receiver will detect single error in this case. | **[3]** |