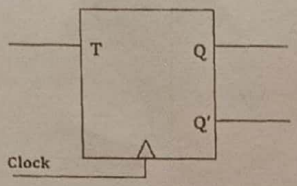
DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
THIRD SESSIONAL
SUBJECT: (CE-308) Design of Digital Circuits

Examination	**: B.Tech Semester III**	**Seat No.**	**:**
Date	**: 11-10-2023**	**Day**	**: Wednesday**
Time	**: 9:15 AM to 10:30 AM**	**Max. Marks**	**: 36**

INSTRUCTIONS:
1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q1 **Do as directed.** **[12]**

CO3 A (a) Q of the T flip-flop is zero. Clock transition from __ to __ when T = __ will ensure flip-flop output Q' to have zero value. [2]



CO3 U (b) The flip-flop(s) which has not any invalid states is/are _____ [2]
(a) SR (b) JK (c) D (d) T

CO3 U (c) Why is state reduction important? [2]
(a)To save time of the designer (b)To reduce number of flip-flops
(c)To make the circuit attractive (d)To identify identical states
(e) To reduce complex states (f)All of these

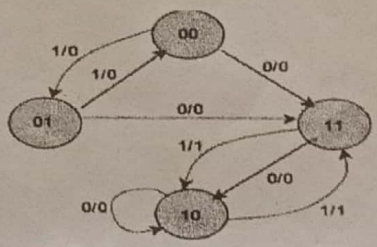
CO4 E (d) If a counter having 10 FFS is initially at 0, what count will it hold after 2060 pulses ? - Justify your answer. [2]

CO4 U (e) Mention any two applications of Shift Register. [2]

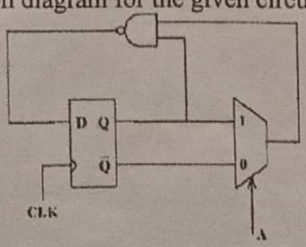
CO4 N (f) The content of a 4 bit register is 1101. The register is shifted 6 times to the right with serial input being 101101. What will be the final content of the register? Explain your answer. [2]

Q2 **Attempt Any TWO from the following:** **[12]**

CO3 C (a) Design an optimal sequential circuit for the following state diagram using JK flip-flop(s). [6]



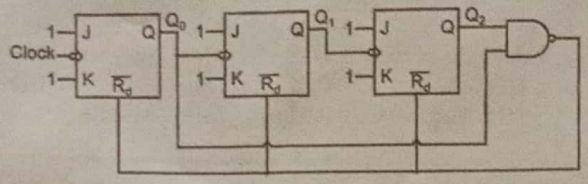
CO3 C (b) (i) How many SR flip-flops will be required to implement the following counter? Justify your answer. [6]
00 – 11 – 00 – 01 – 10 – 00 – 11 – 00 – 11 – 00 – 01 – 10 – 00 – 11 .....
(ii) Draw state transition diagram for the given circuit.



CO3 C (c) Design a counter for the sequence: 0,1,3,2,4,5,2,7 and repeat. Use SR flip-flops. [6]

Q3. **Attempt the following:** [12]

CO4 E (a) The circuit shown consists of J-K flip-flops, each with an active low asynchronous reset input (denoted by R_d'). Determine the counting sequence of the same, supporting it with the timing diagram. [6]

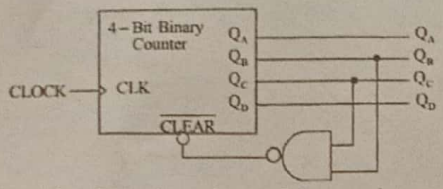


CO4 C (b) Create a Mod 2N synchronous counter. Show the counting logic, state diagram, state table and timing diagram. [6]

OR

Q3. **Attempt the following:** [12]

CO4 E (a) A mod-n counter using a synchronous binary up-counter with synchronous clear input (Synchronous clear is synchronized with the clock. It waits for a clock pulse to Reset FF output.) is shown in the figure. [6]



Determine the value of "n", and evaluate the counting sequence performed by the counter, supporting it with the timing diagram.

CO4 C (b) Design a Mod 5 asynchronous down counter that counts the sequence 7-6-5-4-3 using positive edge triggering as well as with negative edge triggering. [6]