Signoff timing analysis – workshop

Lab 1

Output:

```
  Delay    Time   Description
---------------------------------------------------------
  25.00   25.00   clock tau2015_clk (fall edge)
   0.00   25.00   clock network delay (ideal)
   0.00   25.00 v f1/CLK_N (sky130_fd_sc_hd__dfbbn_2)
   0.51   25.51 ^ f1/Q (sky130_fd_sc_hd__dfbbn_2)
   0.03   25.55 v u2/Y (sky130_fd_sc_hd__inv_1)
  22.41   47.96 ^ u3/Y (sky130_fd_sc_hd__inv_1)
   0.00   47.96 ^ out (out)
          47.96   data arrival time

  50.00   50.00   clock tau2015_clk (rise edge)
   0.00   50.00   clock network delay (ideal)
   0.00   50.00   clock reconvergence pessimism
 -30.00   20.00   output external delay
          20.00   data required time
---------------------------------------------------------
          20.00   data required time
         -47.96   data arrival time
---------------------------------------------------------
         -27.96   slack (VIOLATED)
```

```
Startpoint: inp1 (input port clocked by tau2015_clk)
Endpoint: f1 (falling edge-triggered flip-flop clocked by tau2015_clk)
Path Group: tau2015_clk
Path Type: max
```

Day 2- Lab 2:

Liberty File

•The .lib file is an ASCII representation of the timing and power parameters associated with any cell in a particular semiconductor technology

•The .lib file contains timing models and data to calcumax

•I/O delay paths

•Timing check values

•Interconnect delays

Understanding Liberty File

```
library (name_of_library)
technology ( cmos ) ;

delay_model      : table_lookup;
date : "date_of_creation)" ;
revision : revision_number ;
time_unit : "1ns" ;
leakage_power_unit : "1pW" ;
voltage_unit : "1V" ;
pulling_resistance_unit : "1kohm" ;
current_unit : "1uA" ;
capacitive_load_unit(1.000,ff) ;

nom_voltage      : 1.200000;
nom_temperature : 125.0;
nom_process : 1.000;
```

Name of Library

Name of Technology

Units

```
operating_conditions("TYPICAL") {
    process :   1.0;
    temperature :   125;
    voltage :   1.2;
```

PVT – Process, Voltage and Temperature

Minimum delay library

```
roopa.patavardhan@sta-workshop-05:~$ git clone https://github.com/vikkisachdeva/openSTA_sta_workshop
fatal: destination path 'openSTA_sta_workshop' already exists and is not an e
roopa.patavardhan@sta-workshop-05:~$ git clone https://github.com/vikkisachde
fatal: destination path 'openSTA_sta_workshop' already exists and is not an e
roopa.patavardhan@sta-workshop-05:~$ ls
Desktop    Downloads  Pictures  Templates  openSTA_sta_workshop
Documents  Music      Public    Videos     thinclient_drives
roopa.patavardhan@sta-workshop-05:~$ cd openSTA_sta_workshop/
roopa.patavardhan@sta-workshop-05:~/openSTA_sta_workshop$ ls
vlsideepdive_openSTA_labs
roopa.patavardhan@sta-workshop-05:~/openSTA_sta_workshop$ cd vlsideepdive_ope
roopa.patavardhan@sta-workshop-05:~/openSTA_sta_workshop/vlsideepdive_openSTA
lab1  lab2  lab3  lab4  lab5  lab6  lab7  sky130_fd_sc_hd__tt_025C_1v80.lib
roopa.patavardhan@sta-workshop-05:~/openSTA_sta_workshop/vlsideepdive_openSTA
roopa.patavardhan@sta-workshop-05:~/openSTA_sta_workshop/vlsideepdive_openSTA
change1.spef  run.log  simple.sdc   simple.v        simple_min.lib
roopa.patavardhan@sta-workshop-05:~/openSTA_sta_workshop/vlsideepdive_openSTA
```

simple_min.lib

File Edit Search Options Help

```
/*
 * Library File Format
 * Copyright (c) 2011, Synopsys, Inc. and others. All Righ
 */
library ("contest_min") {
  delay_model : table_lookup ;
  time_unit : "1ps" ;
  voltage_unit : "1V" ;
  current_unit : "1mA" ;
  leakage_power_unit : 1uW ;
  capacitive_load_unit(1,ff);
  pulling_resistance_unit : "1kohm" ;
  default_fanout_load : 1.0 ;
  default_inout_pin_cap : 0.0 ;
  default_input_pin_cap : 0.0 ;
  default_output_pin_cap : 0.0 ;
  slew_lower_threshold_pct_rise : 20.0 ;
  slew_lower_threshold_pct_fall : 20.0 ;
  slew_upper_threshold_pct_rise : 80.0 ;
```

```
  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock tau2015_clk (rise edge)
   0.00    0.00   clock network delay (ideal)
   5.00    5.00 v input external delay
   0.00    5.00 v inp1 (in)
   3.33    8.33 ^ u1/Y (sky130_fd_sc_hd__nand2_1)
   0.08    8.41 v u4/Y (sky130_fd_sc_hd__nor2_1)
   0.00    8.41 v f1/D (sky130_fd_sc_hd__dfbbn_2)
           8.41   data arrival time

  25.00   25.00   clock tau2015_clk (fall edge)
   0.00   25.00   clock network delay (ideal)
   0.00   25.00   clock reconvergence pessimism
          25.00 v f1/CLK_N (sky130_fd_sc_hd__dfbbn_2)
  -0.31   24.69   library setup time
          24.69   data required time
---------------------------------------------------------
          24.69   data required time
          -8.41   data arrival time
---------------------------------------------------------
          16.27   slack (MET)
```

Lab 2

Find all the cells in simple_max.lib.

```
roopa.patavardhan@sta-workshop-05:~/openSTA_sta_workshop/vlsideepdive_openSTA_labs/lab2$ grep -c "cell" simple_max.lib
1775
roopa.patavardhan@sta-workshop-05:~/openSTA_sta_workshop/vlsideepdive_openSTA_labs/lab2$ grep  "cell" simple_max.lib
/* Begin cell: INV_X1 */
  cell ("INV_X1") {
        cell_fall ("delay_outputslew_template_7X8") {
        cell_rise ("delay_outputslew_template_7X8") {
/* End cell: INV_X1 */
/* Begin cell: INV_X2 */
  cell ("INV_X2") {
        cell_fall ("delay_outputslew_template_7X8") {
        cell_rise ("delay_outputslew_template_7X8") {
/* End cell: INV_X2 */
/* Begin cell: INV_X3 */
  cell ("INV_X3") {
        cell_fall ("delay_outputslew_template_7X8") {
        cell_rise ("delay_outputslew_template_7X8") {
/* End cell: INV_X3 */
/* Begin cell: INV_X4 */
  cell ("INV_X4") {
        cell_fall ("delay_outputslew_template_7X8") {
        cell_rise ("delay_outputslew_template_7X8") {
/* End cell: INV_X4 */
/* Begin cell: INV_X6 */
```

Find all the pins of the cell NAND2_X1 in simple_max.lib

```
/* Begin cell: NAND2_X1 */
  cell ("NAND2_X1") {
    pin ("o") {
      direction : output ;
      capacitance : 0.0 ;
      max_capacitance : 6.40 ;
      min_capacitance : 0.00 ;
      timing() {
      pin ("a") {
        capacitance : 1.00 ;
        direction : input ;
      }
/* End pin */
      pin ("b") {
        capacitance : 1.00 ;
        direction : input ;
      }
/* End pin */
  }
/* End cell: NAND2_X1 */
```

What difference you see between NAND2_X1 and NAND3_X1

```
/* Begin cell: NAND2_X1 */
  cell ("NAND2_X1") {
    pin ("o") {
      direction : output ;
      capacitance : 0.0 ;
      max_capacitance : 6.40 ;
      min_capacitance : 0.00 ;
      timing() {
        cell_fall ("delay_outputslew_template_7X8") {
         index_1 ("0.00,0.50,1.00,2.00,4.00,8.00,16.00") ;
         index_2 ("5.00,30.00,50.00,80.00,140.00,200.00,300.00,500.00") ;
         values (\
         "39.096, 47.1, 53.496, 63.096, 80.616, 94.38, 113.064, 142.992",\
         "45.348, 53.352, 59.748, 69.348, 87.852, 102.852, 123.108, 155.208",\
         "51.6, 59.604, 66, 75.6, 94.644, 110.808, 132.576, 166.8",\
         "64.104, 72.096, 78.504, 88.104, 107.304, 125.508, 150.132, 188.436",\
         "89.1, 97.104, 103.5, 113.1, 132.3, 151.5, 181.164, 227.04",\
         "139.104, 147.096, 153.504, 163.104, 182.304, 201.504, 233.496, 292.176",\
         "239.1, 247.104, 253.5, 263.1, 282.3, 301.5, 333.504, 397.5"\
         );
      pin ("a") {
        capacitance : 1.00 ;
        direction : input ;
      }
/* End pin */
      pin ("b") {
        capacitance : 1.00 ;
        direction : input ;
      }
/* End pin */
  }
/* End cell: NAND2_X1 */
```

NAND3_X1:

```
'* Begin cell: NAND3_X1 */
  cell ("NAND3_X1") {
    pin ("o") {
      direction : output ;
      capacitance : 0.0 ;
      max_capacitance : 4.27 ;
      min_capacitance : 0.00 ;
      timing() {
        cell_fall ("delay_outputslew_template_7X8") {
         index_1 ("0.00,0.33,0.67,1.33,2.67,5.33,10.67") ;
         index_2 ("5.00,30.00,50.00,80.00,140.00,200.00,300.00,500.00") ;
         values (\
      }
/* End pin */
    pin ("a") {
        capacitance : 1.00 ;
        direction : input ;
      }
/* End pin */
    pin ("b") {
        capacitance : 1.00 ;
        direction : input ;
      }
/* End pin */
    pin ("c") {
        capacitance : 1.00 ;
        direction : input ;
      }
/* End pin */
  }
/* End cell: NAND3_X1 */
```

Exercise: output

Log file data:

run.log

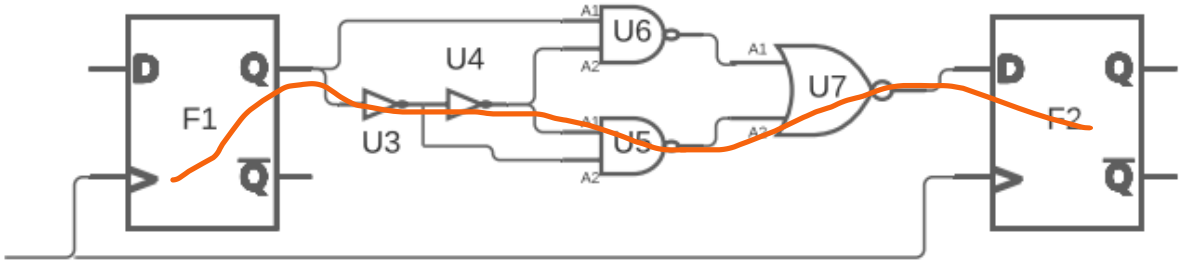
File Edit Search Options Help

```
OpenSTA 2.3.1 3c3f8f61fd Copyright (c) 2021, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type `show_copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show_warranty'.
Startpoint: inp1 (input port clocked by tau2015_clk)
Endpoint: f1 (rising edge-triggered flip-flop clocked by tau2015_clk)
Path Group: tau2015_clk
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock tau2015_clk (rise edge)
   0.00    0.00   clock network delay (ideal)
   5.00    5.00 ^ input external delay
   0.00    5.00 ^ inp1 (in)
 113.95  118.95 v u1/o (NAND2_X1)
 119.78  238.73 ^ u4/o (NOR2_X1)
   8.32  247.05 ^ f1/d (DFF_X80)
         247.05   data arrival time
```

```
  50.00   50.00   clock tau2015_clk (rise edge)
   0.00   50.00   clock network delay (ideal)
   0.00   50.00   clock reconvergence pessimism
          50.00 ^ f1/ck (DFF_X80)
  -1.50   48.50   library setup time
          48.50   data required time
-----------------------------------------------------------
          48.50   data required time
        -247.05   data arrival time
-----------------------------------------------------------
        -198.55   slack (VIOLATED)
```

Day 3:

Lab exercise:



On executing the code with

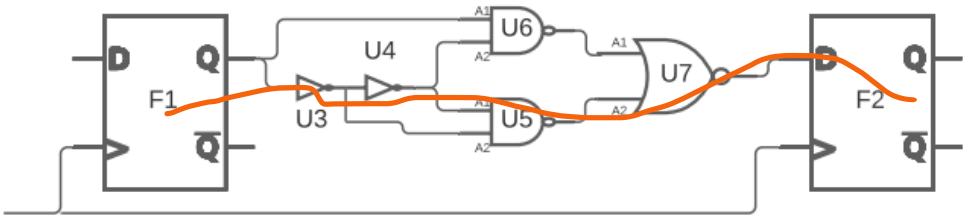
```
Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net)
Path Group: clk_net
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (DFFR_X2)
 141.53  141.53 ^ F1/Q (DFFR_X2)
   8.51  150.04 v U3/ZN (INV_X1)
   7.82  157.86 ^ U4/ZN (INV_X1)
   6.63  164.49 v U5/ZN (NAND2_X2)
```

```
   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock network delay (ideal)
   0.00    1.00   clock reconvergence pessimism
           1.00 ^ F2/CK (DFFR_X2)
 -30.22  -29.22   library setup time
         -29.22   data required time
-----------------------------------------------------------
         -29.22   data required time
        -188.10   data arrival time
-----------------------------------------------------------
        -217.32   slack (VIOLATED)
```

report_checks –from F1/CK -endpoint_count100

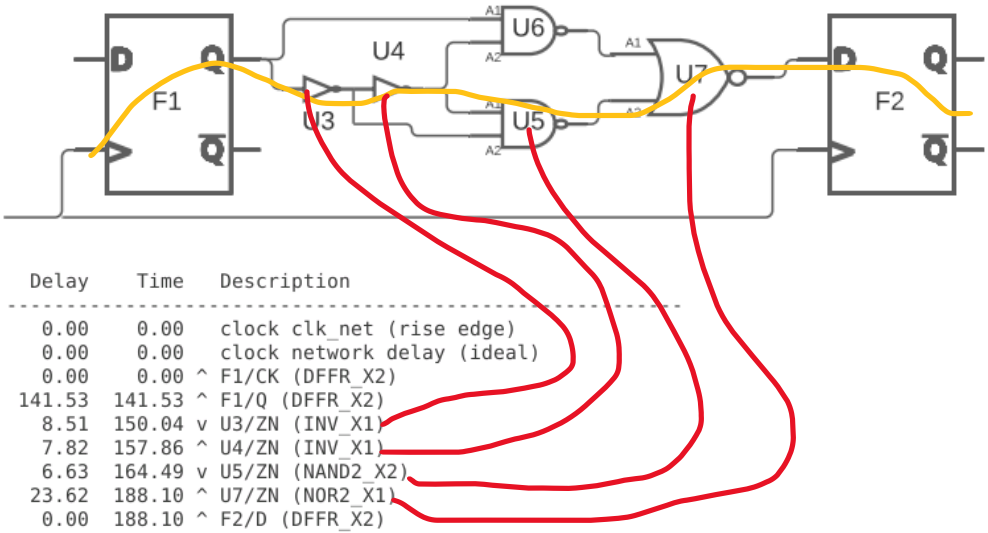
```
File  Edit  Search  Options  Help
read_liberty s27_Late.lib
read_verilog s27.v
link_design s27
read_sdc s27.sdc
report_checks -from F1/CK -endpoint_count 100
```

Path1:



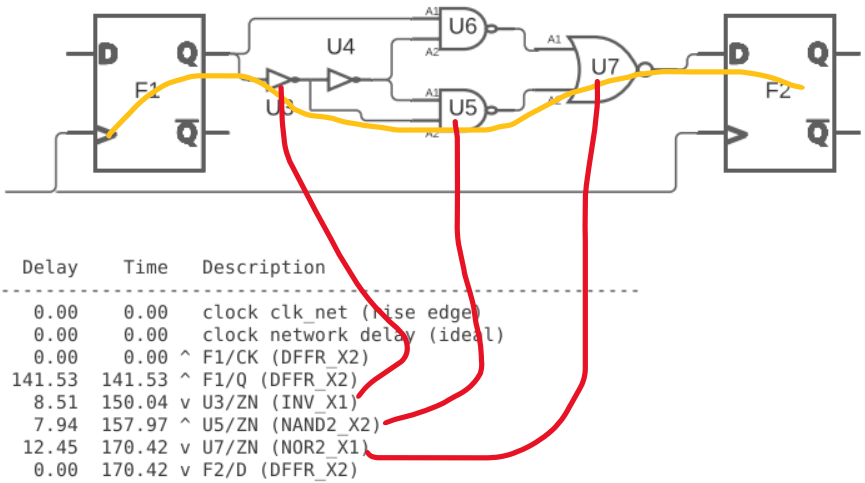

```
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net)
Path Group: clk_net
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (DFFR_X2)
 141.53  141.53 ^ F1/Q (DFFR_X2)
   8.51  150.04 v U3/ZN (INV_X1)
   7.82  157.86 ^ U4/ZN (INV_X1)
   6.63  164.49 v U5/ZN (NAND2_X2)
  23.62  188.10 ^ U7/ZN (NOR2_X1)
   0.00  188.10 ^ F2/D (DFFR_X2)
         188.10   data arrival time

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock network delay (ideal)
   0.00    1.00   clock reconvergence pessimism
           1.00 ^ F2/CK (DFFR_X2)
 -30.22  -29.22   library setup time
         -29.22   data required time
---------------------------------------------------------
         -29.22   data required time
        -188.10   data arrival time
```

Path2:



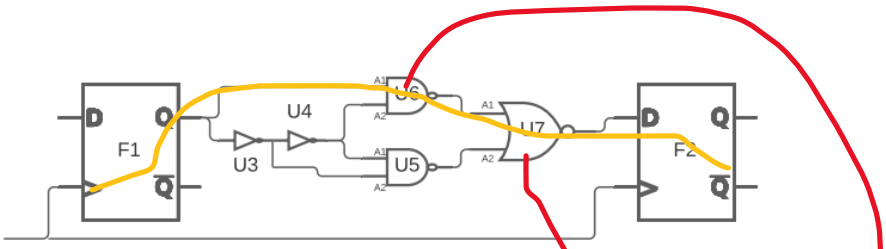

```
  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (DFFR_X2)
 141.53  141.53 ^ F1/Q (DFFR_X2)
   8.51  150.04 v U3/ZN (INV_X1)
   7.82  157.86 ^ U4/ZN (INV_X1)
   6.63  164.49 v U5/ZN (NAND2_X2)
  23.62  188.10 ^ U7/ZN (NOR2_X1)
   0.00  188.10 ^ F2/D (DFFR_X2)
         188.10   data arrival time

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock network delay (ideal)
   0.00    1.00   clock reconvergence pessimism
           1.00 ^ F2/CK (DFFR_X2)
 -30.22  -29.22   library setup time
         -29.22   data required time
---------------------------------------------------------
         -29.22   data required time
        -188.10   data arrival time
---------------------------------------------------------
        -217.32   slack (VIOLATED)
```

Path3:



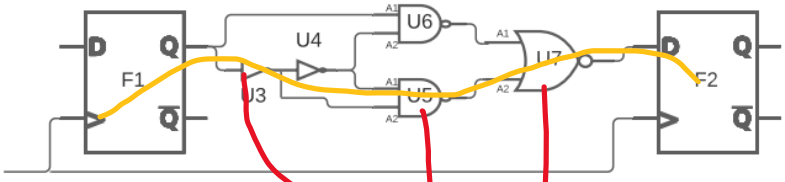

```
  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (DFFR_X2)
 141.53  141.53 ^ F1/Q (DFFR_X2)
   8.51  150.04 v U3/ZN (INV_X1)
   7.94  157.97 ^ U5/ZN (NAND2_X2)
  12.45  170.42 v U7/ZN (NOR2_X1)
   0.00  170.42 v F2/D (DFFR_X2)
         170.42   data arrival time

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock network delay (ideal)
   0.00    1.00   clock reconvergence pessimism
           1.00 ^ F2/CK (DFFR_X2)
 -31.13  -30.13   library setup time
         -30.13   data required time
---------------------------------------------------------
         -30.13   data required time
        -170.42   data arrival time
---------------------------------------------------------
        -200.55   slack (VIOLATED)
```

PATH4:



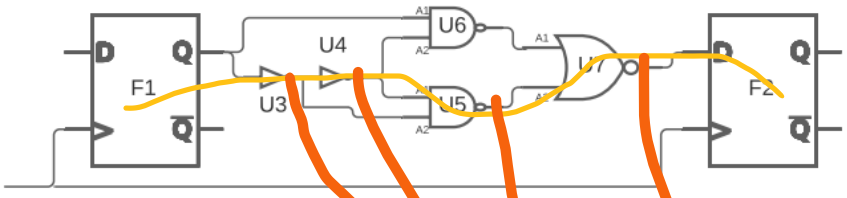
Delay	Time	Description
0.00	0.00	clock clk_net (rise edge)
0.00	0.00	clock network delay (ideal)
0.00	0.00 ^	F1/CK (DFFR_X2)
141.53	141.53 ^	F1/Q (DFFR_X2)
6.66	148.19 v	U6/ZN (NAND2_X2)
16.66	164.85 ^	U7/ZN (NOR2_X1)
0.00	164.85 ^	F2/D (DFFR_X2)
	164.85	data arrival time
1.00	1.00	clock clk_net (rise edge)
0.00	1.00	clock network delay (ideal)
0.00	1.00	clock reconvergence pessimism
	1.00 ^	F2/CK (DFFR_X2)
-30.22	-29.22	library setup time
	-29.22	data required time
	-29.22	data required time
	-164.85	data arrival time
	194.06	slack (VIOLATED)

PATH 5:



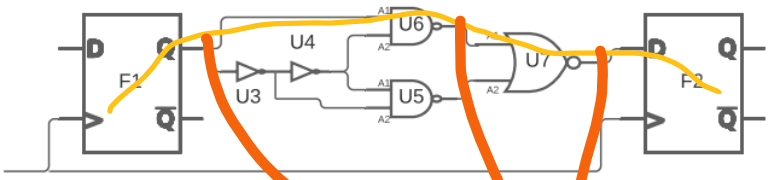
0.00	0.00	clock clk_net (rise edge)
0.00	0.00	clock network delay (ideal)
0.00	0.00 ^	F1/CK (DFFR_X2)
114.19	114.19 v	F1/Q (DFFR_X2)
7.15	121.34 ^	U3/ZN (INV_X1)
9.53	130.87 v	U5/ZN (NAND2_X2)
23.62	154.48 ^	U7/ZN (NOR2_X1)
0.00	154.48 ^	F2/D (DFFR_X2)
	154.48	data arrival time
1.00	1.00	clock clk_net (rise edge)
0.00	1.00	clock network delay (ideal)
0.00	1.00	clock reconvergence pessimism
	1.00 ^	F2/CK (DFFR_X2)
-30.22	-29.22	library setup time
	-29.22	data required time
	-29.22	data required time
	-154.48	data arrival time
	-183.70	slack (VIOLATED)

PATH 6:




```
  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (DFFR_X2)
 114.19  114.19 v F1/Q (DFFR_X2)
   7.15  121.34 ^ U3/ZN (INV_X1)
   8.96  130.30 v U4/ZN (INV_X1)
   5.34  135.63 ^ U5/ZN (NAND2_X2)
  12.45  148.08 v U7/ZN (NOR2_X1)
   0.00  148.08 v F2/D (DFFR_X2)
         148.08   data arrival time

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock network delay (ideal)
   0.00    1.00   clock reconvergence pessimism
           1.00 ^ F2/CK (DFFR_X2)
 -31.13  -30.13   library setup time
         -30.13   data required time
---------------------------------------------------------
         -30.13   data required time
        -148.08   data arrival time
---------------------------------------------------------
        -178.20   slack (VIOLATED)
```

PATH 7:




```
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ F1/CK (DFFR_X2)
 114.19  114.19 v F1/Q (DFFR_X2)
   5.39  119.57 ^ U6/ZN (NAND2_X2)
  10.20  129.77 v U7/ZN (NOR2_X1)
   0.00  129.77 v F2/D (DFFR_X2)
         129.77   data arrival time

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock network delay (ideal)
   0.00    1.00   clock reconvergence pessimism
           1.00 ^ F2/CK (DFFR_X2)
 -31.13  -30.13   library setup time
         -30.13   data required time
---------------------------------------------------------
         -30.13   data required time
        -129.77   data arrival time
---------------------------------------------------------
        -159.90   slack (VIOLATED)
```

DAY 4:

Gating techniques illustrated is ‘Active Low Clock Gating’

Contents of run.tcl

```
File  Edit  Search  Options  Help
read_liberty ../sky130_fd_sc_hd__tt_025C_1v80.lib
read_verilog s27.v
link_design s27
read_sdc -echo s27.sdc
check_setup -verbose
report_checks -to [get_pins clkgate/*]
```

On executing the command

sta run.tcl–exit | tee run.log

```
roopa.patavardhan@sta-workshop-05:~/openSTA_sta_workshop/vlsideepdive_openSTA_labs/lab6$ sta run.tcl -exit|tee run.log
OpenSTA 2.3.1 3c3f8f61fd Copyright (c) 2021, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type `show_copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type `show_warranty'.
create_clock -period 1 -name clk_net [get_ports clk_net]
set_input_delay 0 -min -rise [get_ports G1] -clock clk_net
set_input_delay 0 -min -fall [get_ports G1] -clock clk_net
set_input_delay 0 -max -rise [get_ports G1] -clock clk_net
set_input_delay 0 -max -fall [get_ports G1] -clock clk_net
set_input_transition 5 -min -rise [get_ports G1]
set_input_transition 5 -min -fall [get_ports G1]
set_input_transition 5 -max -rise [get_ports G1]
set_input_transition 5 -max -fall [get_ports G1]
set_input_delay 0 -min -rise [get_ports G2] -clock clk_net
set_input_delay 0 -min -fall [get_ports G2] -clock clk_net
set_input_delay 0 -max -rise [get_ports G2] -clock clk_net
set_input_delay 0 -max -fall [get_ports G2] -clock clk_net
set_input_transition 5 -min -rise [get_ports G2]
set_input_transition 5 -min -fall [get_ports G2]
```

```
set_input_transition 5 -min -rise [get_ports reset_net]
set_input_transition 5 -min -fall [get_ports reset_net]
set_input_transition 5 -max -rise [get_ports reset_net]
set_input_transition 5 -max -fall [get_ports reset_net]
set_input_delay 0 -min -rise [get_ports G3] -clock clk_net
set_input_delay 0 -min -fall [get_ports G3] -clock clk_net
set_input_delay 0 -max -rise [get_ports G3] -clock clk_net
set_input_delay 0 -max -fall [get_ports G3] -clock clk_net
set_input_transition 5 -min -rise [get_ports G3]
set_input_transition 5 -min -fall [get_ports G3]
set_input_transition 5 -max -rise [get_ports G3]
set_input_transition 5 -max -fall [get_ports G3]
set_input_delay 0 -min -rise [get_ports G0] -clock clk_net
set_input_delay 0 -min -fall [get_ports G0] -clock clk_net
set_input_delay 0 -max -rise [get_ports G0] -clock clk_net
set_input_delay 0 -max -fall [get_ports G0] -clock clk_net
set_input_transition 5 -min -rise [get_ports G0]
set_input_transition 5 -min -fall [get_ports G0]
set_input_transition 5 -max -rise [get_ports G0]
set_input_transition 5 -max -fall [get_ports G0]
set_output_delay -2.1 -min -rise [get_ports G17] -clock clk_net
set_output_delay -2.1 -min -fall [get_ports G17] -clock clk_net
set_output_delay -1.2 -max -rise [get_ports G17] -clock clk_net
set_output_delay -1.2 -max -fall [get_ports G17] -clock clk_net
set_load -pin_load 4 [get_ports G17]
set_clock_gating_check -setup 1.0 -hold 0.5 [get_clocks clk_net]
```

```
Startpoint: F1 (rising edge-triggered flip-flop clocked by clk_net)
Endpoint: clkgate (rising clock gating-check end-point clocked by clk_net)
Path Group: clk_net
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock network delay (propagated)
   0.00    0.00 ^ F1/CLK (sky130_fd_sc_hd__dfbbp_1)
   1.08    1.08 ^ F1/Q (sky130_fd_sc_hd__dfbbp_1)
   0.05    1.12 v U3/Y (sky130_fd_sc_hd__inv_1)
   0.05    1.18 ^ U4/Y (sky130_fd_sc_hd__inv_1)
   0.05    1.22 v U6/Y (sky130_fd_sc_hd__nand2_1)
   0.08    1.30 ^ U7/Y (sky130_fd_sc_hd__nor2_1)
```

```
   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock network delay (propagated)
   0.00    1.00   clock reconvergence pessimism
           1.00 ^ clkgate/CLK (sky130_fd_sc_hd__dlclkp_4)
  -0.37    0.63   library setup time
           0.63   data required time
---------------------------------------------------------
           0.63   data required time
          -1.30   data arrival time
---------------------------------------------------------
          -0.67   slack (VIOLATED)
```

LAB 4: Async Pin Checks:

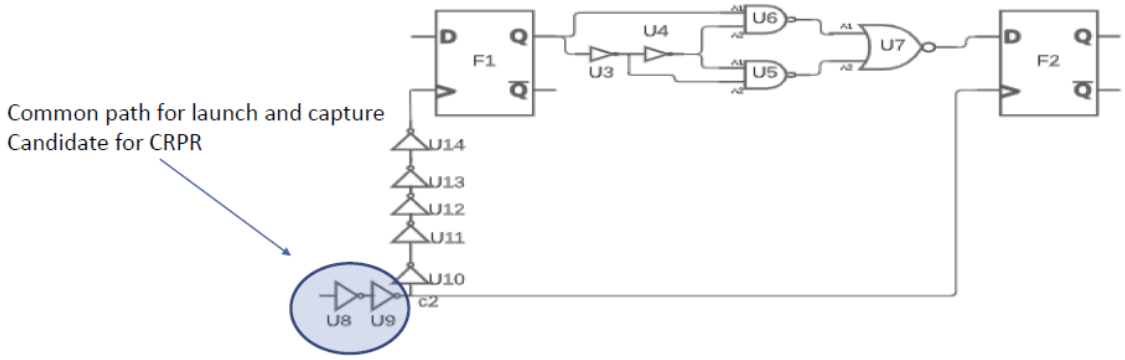
```
module s27 ( G1,G2,clk_net,reset_net,G3,G0,G17);

//Start PIs
input G0;
input G1;
input G2;
input G3;
input clk_net,reset_net;

//Start POs
output G17;

wire n1,n2,n3,n4,n5,n6,n7,n8,n9;
wire rst_sync;
// Reset Synchronizer
sky130_fd_sc_hd__dfbbp_1 SYNC1 (.D(1'b1), .CLK(clk_net), .RESET_B(rst),
.Q(n1),.SET_B(1'b1));
sky130_fd_sc_hd__dfbbp_1 SYNC2 (.D(n1), .CLK(clk_net), .RESET_B(rst), .Q(rst_sync));

// Functional Register
sky130_fd_sc_hd__dfbbp_1 R1 (.D(G0), .CLK(clk_net), .RESET_B(rst_sync),
.Q(G17),.SET_B(1'b1));
endmodule
```

run.tcl file
read_liberty ../sky130_fd_sc_hd__tt_025C_1v80.lib
read_verilog s27.v
link_design s27
read_sdc s27.sdc
check_setup -verbose
report_checks -to R1/RESET_B

on executing
sta run.tcl–exit | tee run.log

```
  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock network delay (ideal)
   0.00    0.00 ^ SYNC2/CLK (sky130_fd_sc_hd__dfbbp_1)
   0.47    0.47 ^ SYNC2/Q (sky130_fd_sc_hd__dfbbp_1)
   0.00    0.47 ^ R1/RESET_B (sky130_fd_sc_hd__dfbbp_1)
           0.47   data arrival time

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock network delay (ideal)
   0.00    1.00   clock reconvergence pessimism
           1.00 ^ R1/CLK (sky130_fd_sc_hd__dfbbp_1)
  -0.07    0.93   library recovery time
           0.93   data required time
---------------------------------------------------------
           0.93   data required time
          -0.47   data arrival time
---------------------------------------------------------
           0.46   slack (MET)


roopa.patavardhan@sta-workshop-05:~/openSTA_sta_workshop/vlsideepdive_openSTA_la
bs/lab7$
```

Day5: Common Path Pessimism Removal(CPPR)



```
 module s27 (G1,G2,clk_net,reset_net,G3,G0,G17);

//Start PIs
input G0;
input G1;
input G2;
input G3;
input clk_net,reset_net;

//Start POs
output G17;

wire n1,n2,n3,n4,n5,n6,n7,n8,n9;
DFFR_X2 F1 (.D(G0), .CK(c4), .Q(n1));
INV_X1 U3 (.A(n1), .ZN(n2));
INV_X1 U4 (.A(n2), .ZN(n3));
NAND2_X2 U6 (.ZN(n4), .A1(n1), .A2(n3));
NAND2_X2 U5 (.ZN(n5), .A1(n3), .A2(n2));
NOR2_X1 U7 (.ZN(n6), .A1(n4), .A2(n5));
DFFR_X2 F2 (.D(n6), .CK(c2), .Q(G17));

//Clock Paths
wire c1,c2,c3,c4_1,c4_2,c4_3,c4;
CLKBUF_X2 U8 (.A(clk_net), .Z(c1));
CLKBUF_X2 U9 (.A(c1), .Z(c2));
CLKBUF_X2 U10 (.A(c2), .Z(c3));
CLKBUF_X2 U11 (.A(c3), .Z(c4_1));
CLKBUF_X2 U12 (.A(c4_1), .Z(c4_2));
CLKBUF_X2 U13 (.A(c4_2), .Z(c4_3));
CLKBUF_X2 U14 (.A(c4_3), .Z(c4));
endmodule
```

sta run.tcl–exit | tee out.txt

```
Endpoint: F2 (rising edge-triggered flip-flop clocked by clk_net)
Path Group: clk_net
Path Type: max

  Delay    Time   Description
---------------------------------------------------------
   0.00    0.00   clock clk_net (rise edge)
   0.00    0.00   clock source latency
   0.00    0.00 ^ clk_net (in)
  34.84   34.84 ^ U8/Z (CLKBUF_X2)
  35.15   69.99 ^ U9/Z (CLKBUF_X2)
  34.85  104.84 ^ U10/Z (CLKBUF_X2)
  34.84  139.68 ^ U11/Z (CLKBUF_X2)
  34.84  174.53 ^ U12/Z (CLKBUF_X2)
  34.84  209.37 ^ U13/Z (CLKBUF_X2)
  34.71  244.08 ^ U14/Z (CLKBUF_X2)
   0.00  244.08 ^ F1/CK (DFFR_X2)
 141.54  385.62 ^ F1/Q (DFFR_X2)
   8.51  394.12 v U3/ZN (INV_X1)
   7.82  401.94 ^ U4/ZN (INV_X1)
   6.63  408.57 v U5/ZN (NAND2_X2)
  23.62  432.19 ^ U7/ZN (NOR2_X1)
   0.00  432.19 ^ F2/D (DFFR_X2)

   1.00    1.00   clock clk_net (rise edge)
   0.00    1.00   clock source latency
   0.00    1.00 ^ clk_net (in)
  31.53   32.53 ^ U8/Z (CLKBUF_X2)
  31.80   64.32 ^ U9/Z (CLKBUF_X2)
   0.00   64.32 ^ F2/CK (DFFR_X2)
 -30.23   34.09   library setup time
          34.09   data required time
---------------------------------------------------------
          34.09   data required time
        -432.19   data arrival time
---------------------------------------------------------
        -398.10   slack (VIOLATED)


roopa.patavardhan@sta-workshop-05:~/openSTA_sta_workshop/vlsideepdive_openSTA_la
bs/lab4$
```