Time delay Calculation.

for Example

255.

```
        MVI C, FFH      → 7T.
Loop    DCR C           4T      when C=0 then 10T
        JNZ Loop        10/7T → when C≠0 then 7T.
```

This Loop will Execute until value of C becomes Zero.

$T_{delay} = T_O + T_L$

T_O = delay outside the loop.

T_L = delay of the Loop.

$T_L = (T_{IL} \times N) - 3)T$

T_{IL} → T States Inside Loop

N → No. of Decimal No. System

- Why -3? because in JNZ total No. of T-States required when C=0 then 10 & when C≠0 then 7T States are req'.
  So -3 for the Gap.
- That means loop will be running for 255 times.
- Outside Loop is only 1 instruction.

  then T_O = 7T States

  T_{IL} = 14T States

  $T_L = ((14 \times 255) - 3)T = 3567T$

$T_{delay} = 3567T + 7T$

$= 3574T \quad = 3574 \times 0.5\mu S = 1787\mu S$

Suppose $f = 2MHz$

$T = \frac{1}{f} = 0.5\mu S$

$1MHz = 10^{-6}$

Total time required is = 1787 μS. for Executing this Second.

(1) Now we can see we have taken max. possible value FF. Then also we are getting only 1787 μS

(2) If we want to ~~Calculate~~ time delay in case of Single Register then we use Register pair

Delay Using a Register Pair

Note:- DCX instruction does not affect ZF.

```
        LXI B, 1000H      10T
Loop    DCX B             6T
        MOV A, C          4T
        ORA B             4T
        JNZ Loop          10T
```

$T_D = 10T$

$T_L = ((24 \times 4096) - 3T$

$= 98301T$

$T_{delay} = 98311T$

1000 − 0001 = 0FFF

A = FF, B = 0F

0000 0000 + 0001 0000 = 0

JNZ ⇒ Z = 0FFE

FE 0F

0000 1111 (A = 0F)

0 F

AC = 0, CY = 0

(*) Delay by using Nested Loop Structure

```
        MVI B, 10      → 7T
Loop2   MVI C, FF      → 7T
Loop1   DCR C          → 4T
        JNZ Loop1      → 10/7T
        DCR B          → 4T
        JNZ Loop2      → 10/7T
```

for Loop1 → we have calculated = 3567T

for Loop2

T_{L_1} = 1783.5nS.

~~3567 T~~

$T_{L_2} = 56(T_{L_1} + 21.T\ States) \times 0.5$

$= 56(1783.5nS + 10.5nS$

$= 100.46ms.$

(*) Why delay is needed?

- The delay will be used in diffrent places to Simulate clocks, or Counters or Someother area.
- when the delay Subroutine is executed, the up does not Execute Other tasks. for the delay we are using the instruction execution time.
  Executing Same instructions in Loop, the delay is generated
- Counters are used to keep track of events. Time delay are important in Setting up Reasonbly accurate timing between two events.

(3)

- If we don't go use mov A, C & ORA B then Loop will go on infinite times.
- So to Set Zero flag we use move A, C & ORA B
- Max value we can take is ffff

  1000 − B = 0FFF.
- ORA B :- is used to Zero flag OR operation between A & B.
- In case of DCX & INX we required 6T not 4T.

  TO = 10T

  TL = (24 × 4096) − 3) T = 98301T

  Tdelay = 98311T -

  T = 0·5

  = 98311 × 0·5 =

Memory Interfacing

- We know the µp uses inside to access data and code which are stored in a memory location, and this access of memory done by memory interfacing that is RAM & ROM.

Difference b/w I/O Mapped & Memory Mapped.

	memory mapped I/O	I/o mapped I/O
1	I/O treated as memory	I/O is treated I/O
2	16 bit addressing	8 bit addressing.
3	more Decoder Hardware is Required	Less Decoder Hardware is required
4	can address 64 K Location	can address 256 Locations
5	memory Instruction are used	Special Instructions are IN, OUT
6	Memory Control Signals ($\overline{MEMW}$, $\overline{MEMR}$)	Special Control Signals are used ($\overline{IOR}$, $\overline{IOW}$)
7	Arithmetic & Logic operations Can be performed on data	Arithmetic and logic operations Can not be performed on data.
8	Data transfer b/w registers & memory	Data transfer b/w Acc and I/p

Memory Interfacing.

- we can perform Read & WR operation.

$\frac{2^n \times n}{2^n \text{ diff loc}}$

each loc. is of n-bits

$\overline{WR}$ → Data is coming up to memory

~~RD~~ → 2048 → Total No of Registers

8 → Size of Register each

group of Registers = Memory.

- Erasable Programble Memory.

(*) How to interface up with memory.

(1) Determine 8085 address line which are connected to the memory chip by using formula

memory capacity = $2^{\text{address Lines}}$.

(2) Remining address line of 8085 are connected to decoder. output of decoder is connected to CE which enable memory chip.

(3) Generate control Signal. It will enable output buffer.

645.

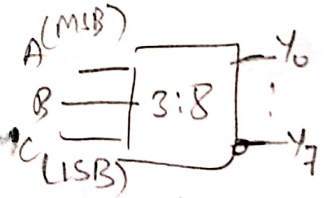
$A_0 - A_{11}$ = 4096×1024 (memory Capacity)

Size of Register → 8 bit

↓

4096

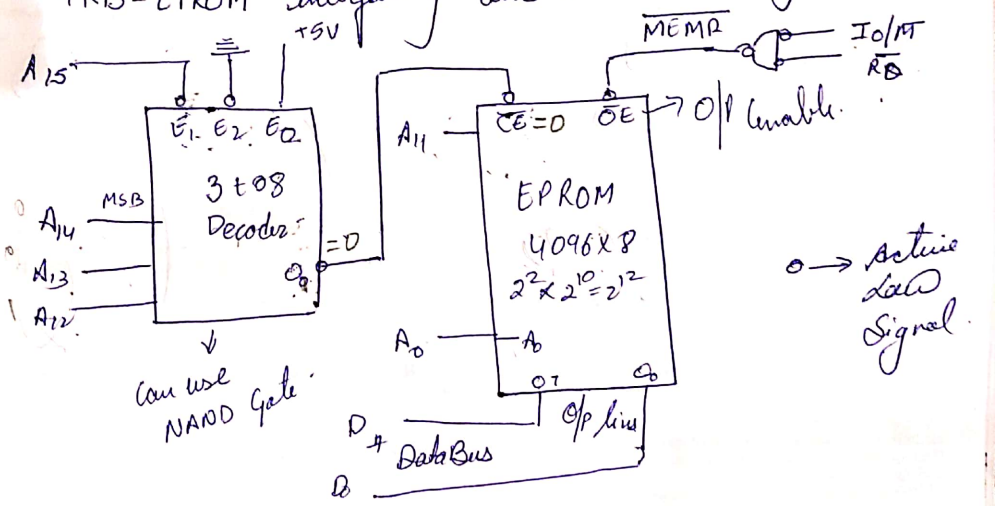
$2^2 \times 2^{10} = A_0 - A_{11}$

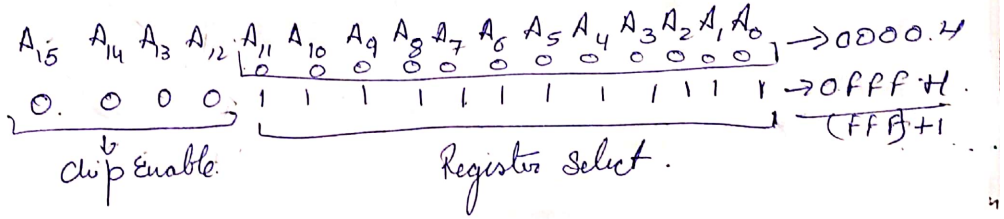


A	B	C	Y_0	...	Y_7
0	0	0	0	1	1
0	0	1	1	0	1
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Memory Interfacing

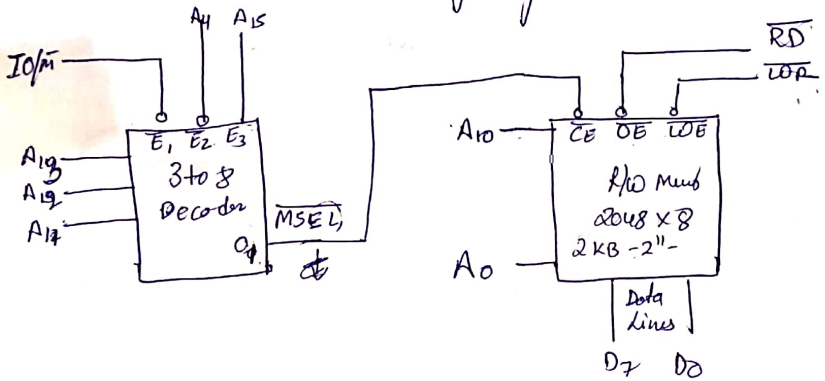
4KB-EPROM interfacing and address decoding





- Decoder means 3 input & output if O_0 is Zero then 000 will be value of A_{12} & A_{13} and A_4 & so on.
- A_{15} → Enable Line.
- When Decoder will work :- When $\bar{E}_1$ is = 0, $\bar{E}_2 = 0$ & $E_3 = 1$
- Generate Control Signal by $IO/\bar{M}$ & $\bar{RD}$
-

2KB - RAM interfacing and address decoding



A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0000
					1	1	1	1	1	1	1	1	1	1	1	07FF

- For $\overline{RD}$ & $\overline{WR}$ IO/$\overline{M}$ Should be Zero.
- when this decoder will work when $\overline{E_1} = 0$ $E_2 = 0$ $E_3 = 1$
- Add are determining with O_1

0000
07FF
+1