VLSI SYSTEM DESIGN

PROJECT

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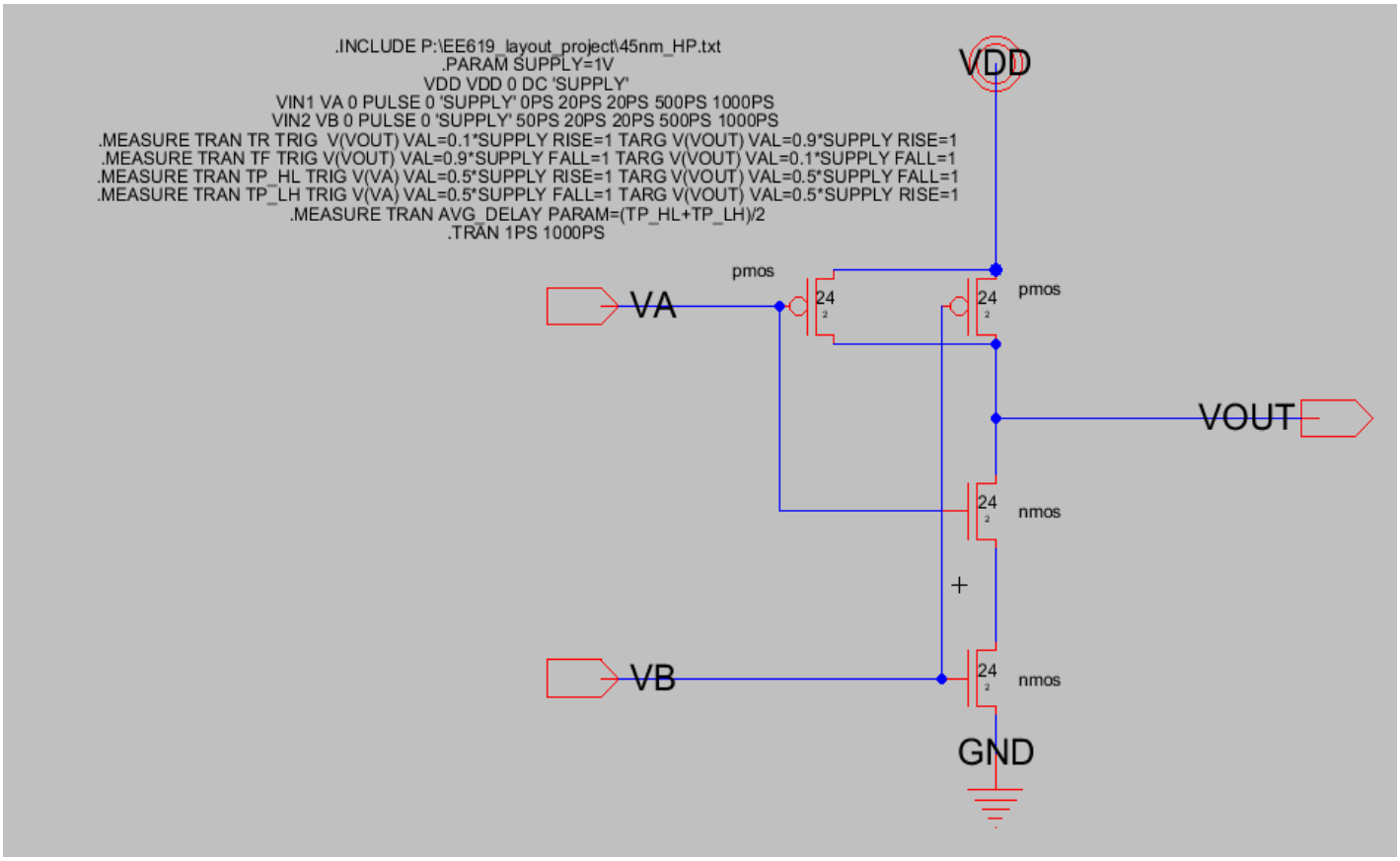
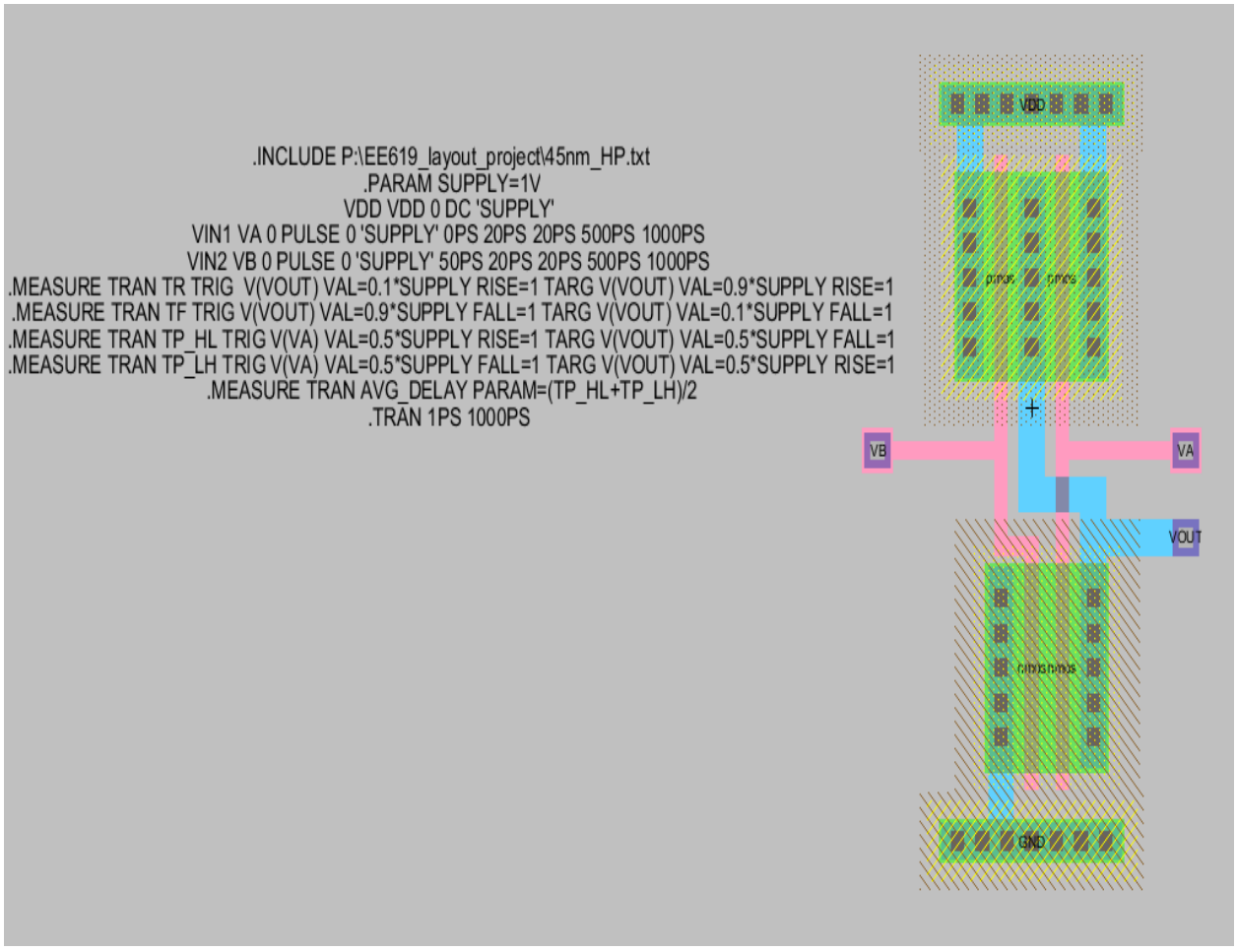
2 INPUT NAND GATE

SCHEMATIC



To Drive the 50fF and 5fF capacitors, and to get equal rise and fall time we have chosen the above sizes for the schematic and layout.

LAYOUT



DRC LOG

```
================================54================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 11 networks
Checking cell 'CMOS_NAND2{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.034 secs)
```

LVS LOG

```
Hierarchical NCC every cell in the design: cell 'CMOS_NAND2{sch}'  cell 'CMOS_NAND2{lay}'
Comparing: CMOS_NAND2:CMOS_NAND2{sch} with: CMOS_NAND2:CMOS_NAND2{lay}
  exports match, topologies match, sizes not checked in 0.001 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.002 seconds.
```

DELAY

FANOUT SCHEMATIC LAYOUT

	TPHL (ps)	TPLH (ps)	TPHL (ps)	TPHL (ps)
S5 fF	64.1	12.3	64.3	12.4
50 fF	125.9	58.6	126.0	58.7

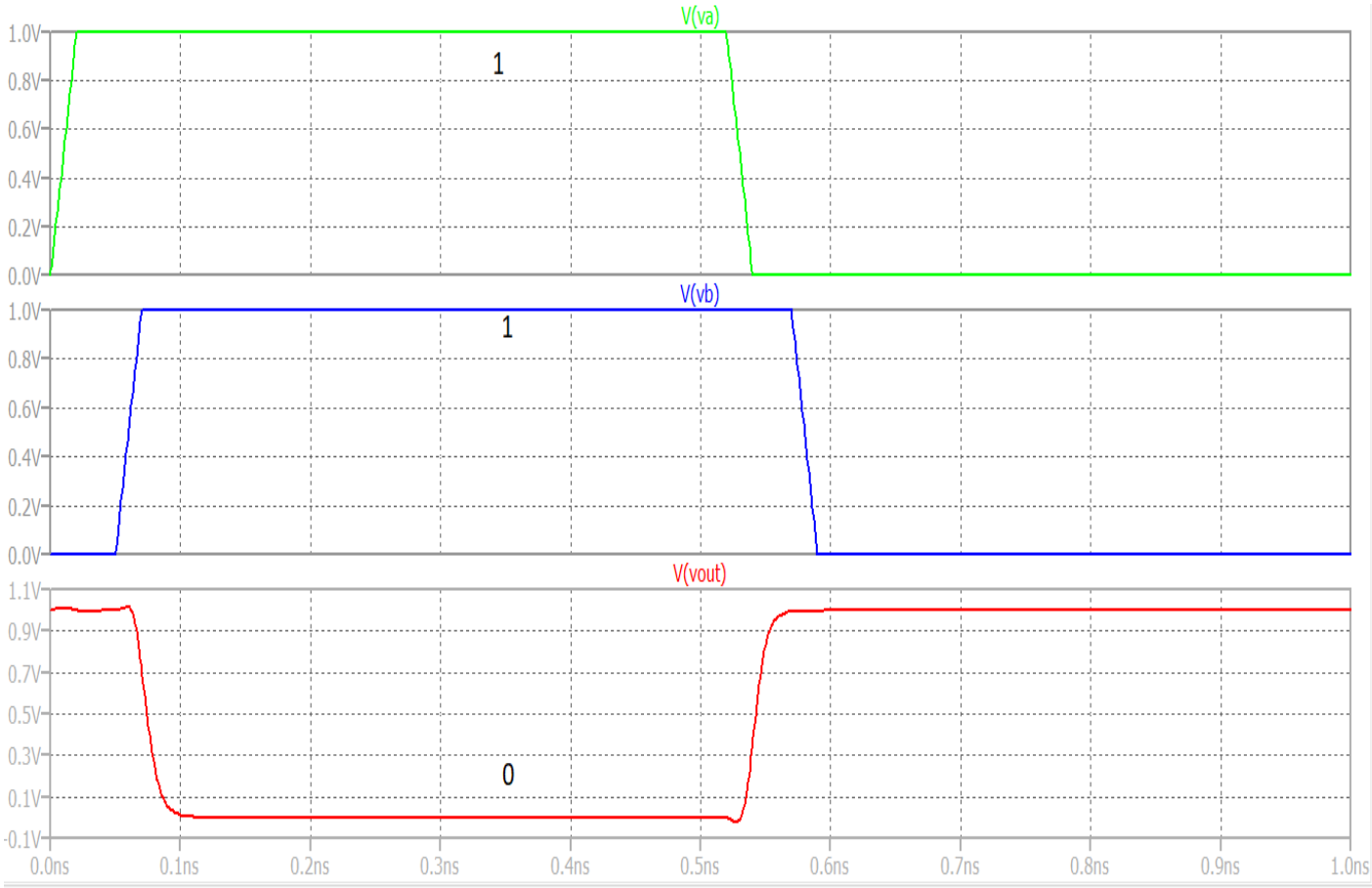
Power consumption

	SCHEMATIC (uW)	LAYOUT (uW)
5fF	7.38	7.50
50fF	52.70	52.83

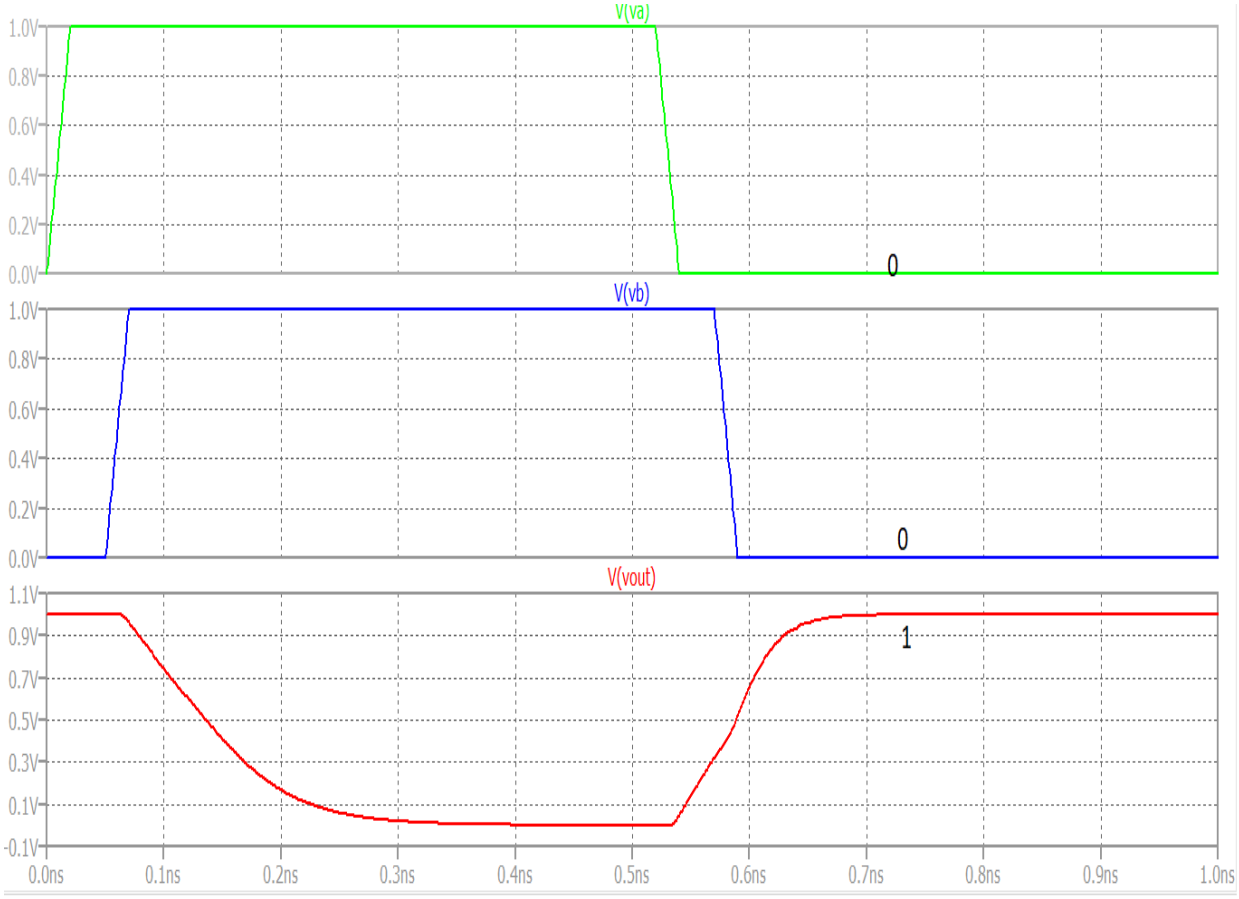
WAVEFORMS

FROM SCHEMATIC

FOR 5fF LOAD

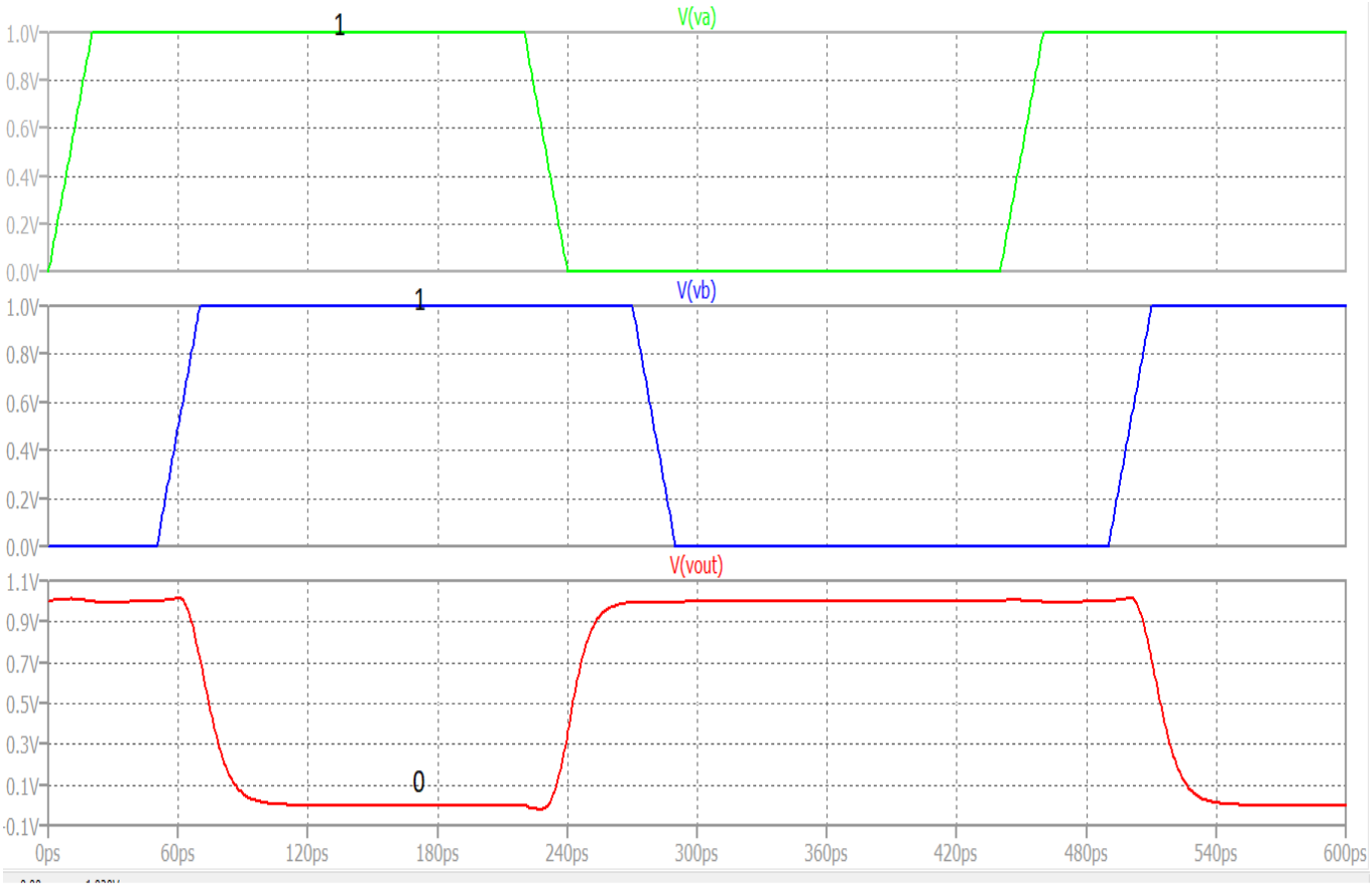


FOR 50fF LOAD

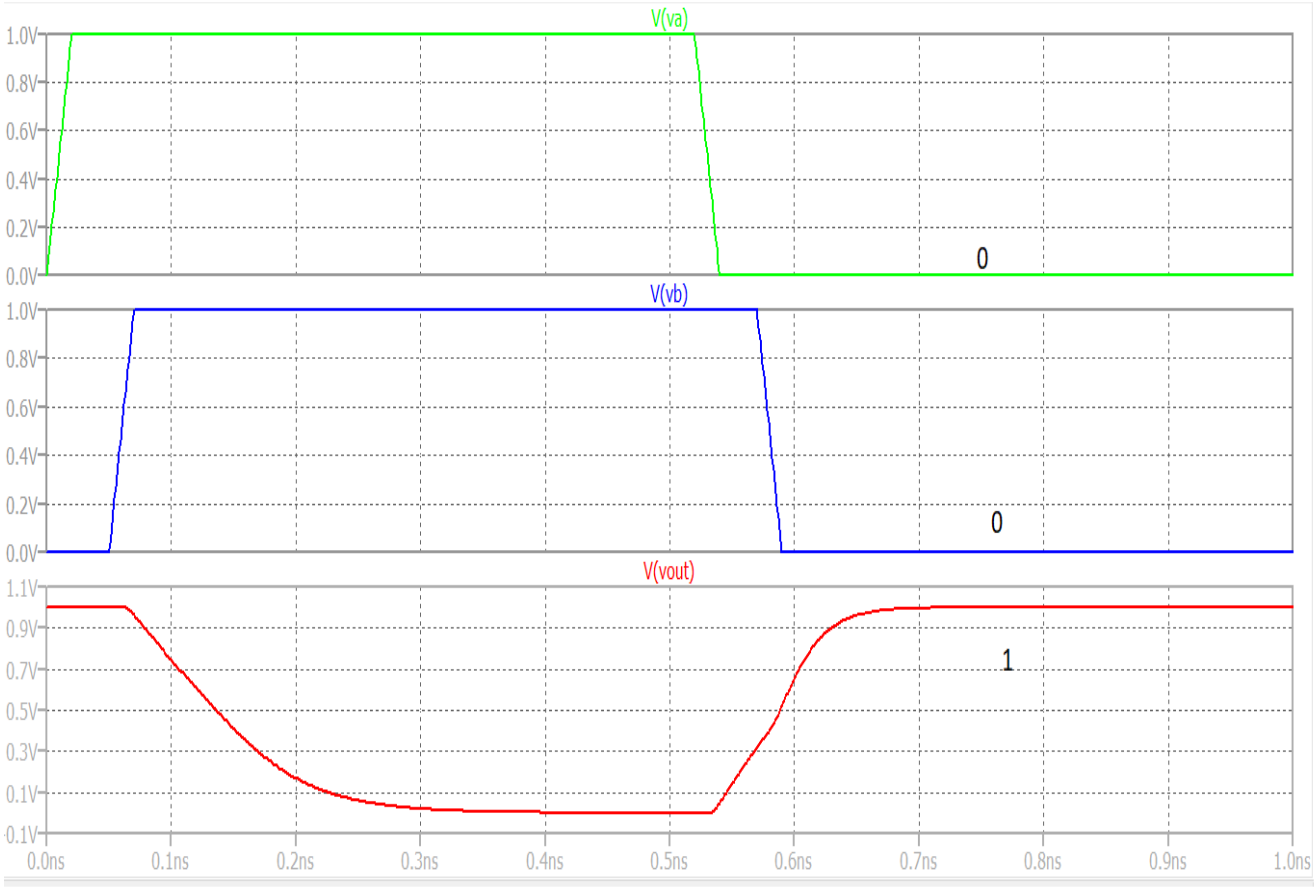


FROM LAYOUT

FOR 5fF LOAD

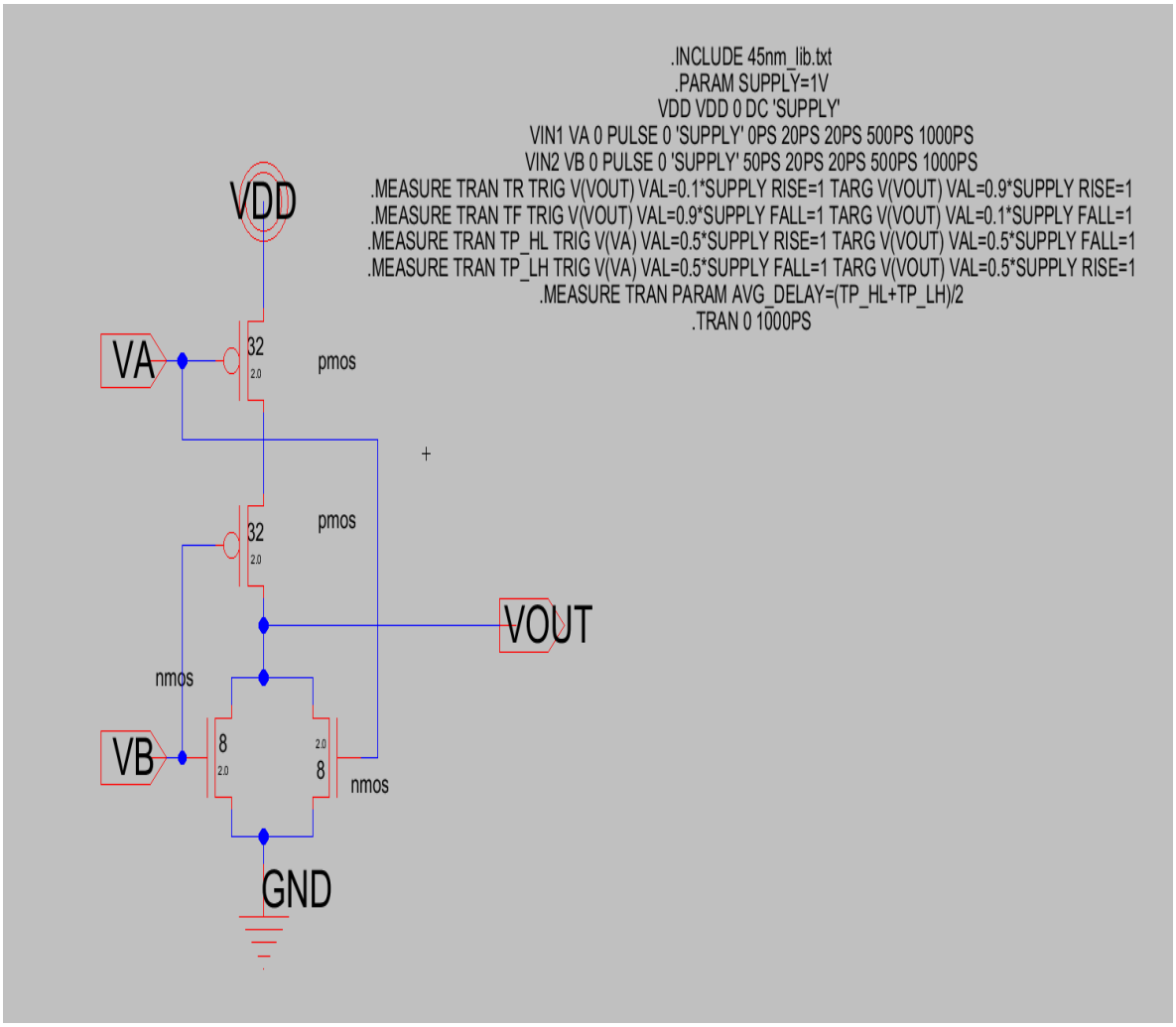


FOR 50fF LOAD



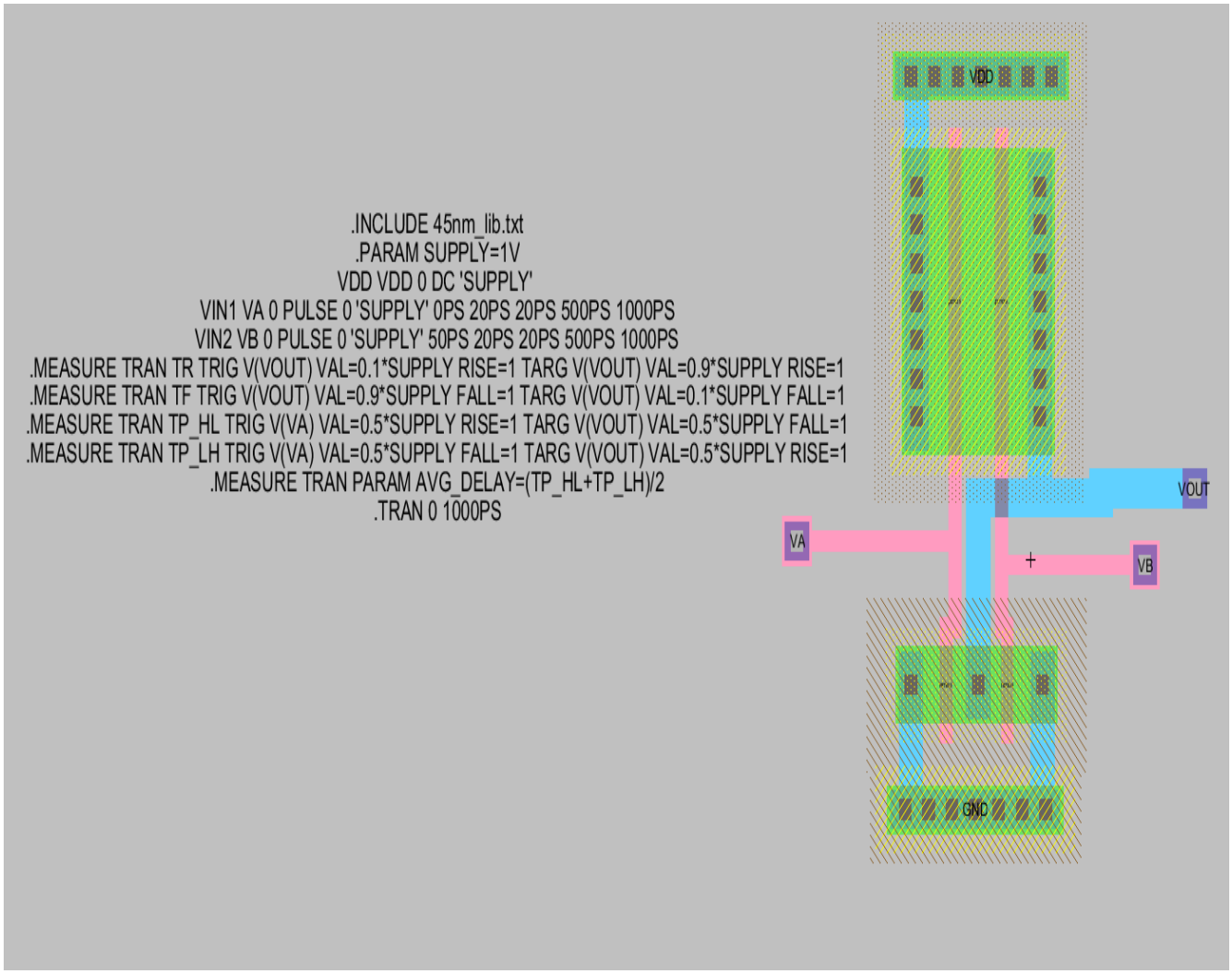
2 INPUT NOR GATE

SCHEMATIC



To Drive the 50fF and 5fF capacitors, and to get equal rise and fall time we have chosen the above sizes for the schematic.

LAYOUT


.INCLUDE 45nm_lib.txt
.PARAM SUPPLY=1V
VDD VDD 0 DC 'SUPPLY'
VIN1 VA 0 PULSE 0 'SUPPLY' 0PS 20PS 20PS 500PS 1000PS
VIN2 VB 0 PULSE 0 'SUPPLY' 50PS 20PS 20PS 500PS 1000PS
.MEASURE TRAN TR TRIG V(VOUT) VAL=0.1*SUPPLY RISE=1 TARG V(VOUT) VAL=0.9*SUPPLY RISE=1
.MEASURE TRAN TF TRIG V(VOUT) VAL=0.9*SUPPLY FALL=1 TARG V(VOUT) VAL=0.1*SUPPLY FALL=1
.MEASURE TRAN TP_HL TRIG V(VA) VAL=0.5*SUPPLY RISE=1 TARG V(VOUT) VAL=0.5*SUPPLY FALL=1
.MEASURE TRAN TP_LH TRIG V(VA) VAL=0.5*SUPPLY FALL=1 TARG V(VOUT) VAL=0.5*SUPPLY RISE=1
.MEASURE TRAN PARAM AVG_DELAY=(TP_HL+TP_LH)/2
.TRAN 0 1000PS
VDD
VOUT
VA
VB
GND

DRC LOG

```
==================================409==================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 11 networks
0 errors and 0 warnings found (took 0.003 secs)
```

LVS LOG

```
------------------------------411------------------------------
Hierarchical NCC every cell in the design: cell 'NOR_22104012:2NOR2_22104012{sch}'  cell 'NOR_22104012:2NOR2_22104012{lay}'
Comparing: NOR_22104012:2NOR2_22104012{sch} with: NOR_22104012:2NOR2_22104012{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.002 seconds.
```

DELAY

FANOUT SCHEMATIC LAYOUT

	TPHL (ps)	TPLH (ps)	TPHL (ps)	TPHL (ps)
5 fF	22.88	65.23	11.99	1
50 fF	90.90	141.98	86.48	58.7

Power consumption

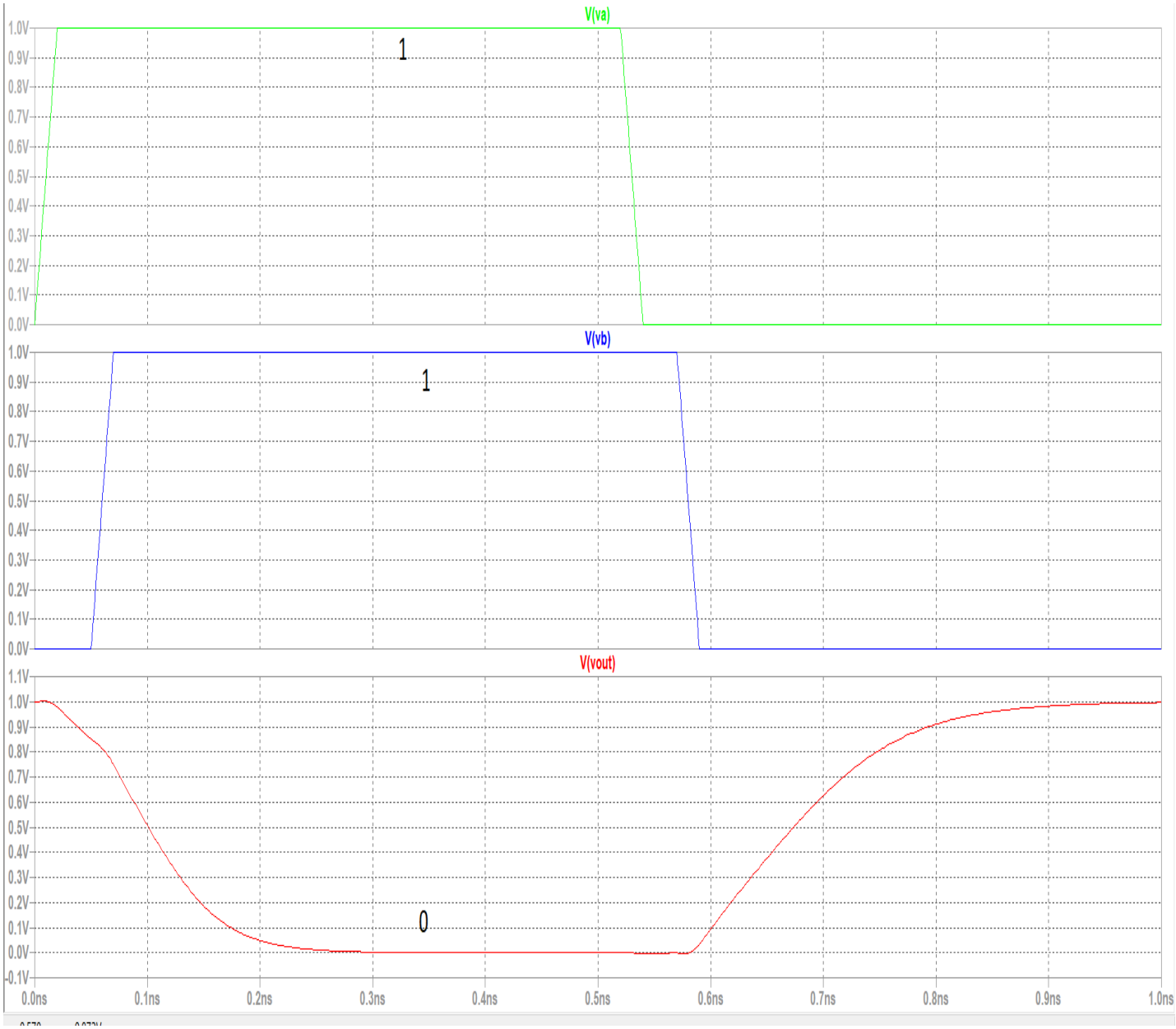
	SCHEMATIC (uW)	LAYOUT (uW)
5fF	6.87	6.89
50fF	51.98	52.07

WAVEFORMS

FROM SCHEMATIC

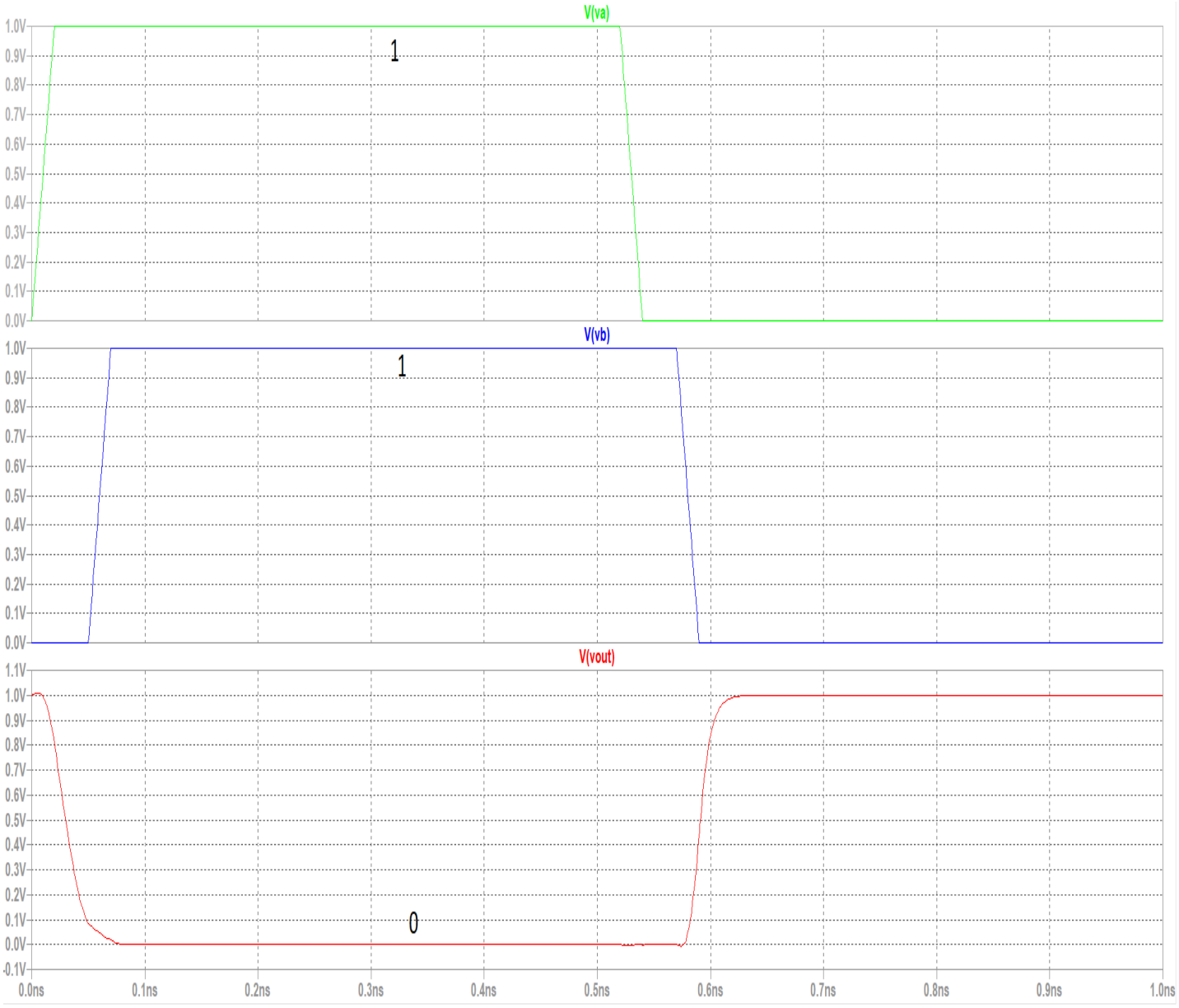
FOR 5fF

FOR 50fF

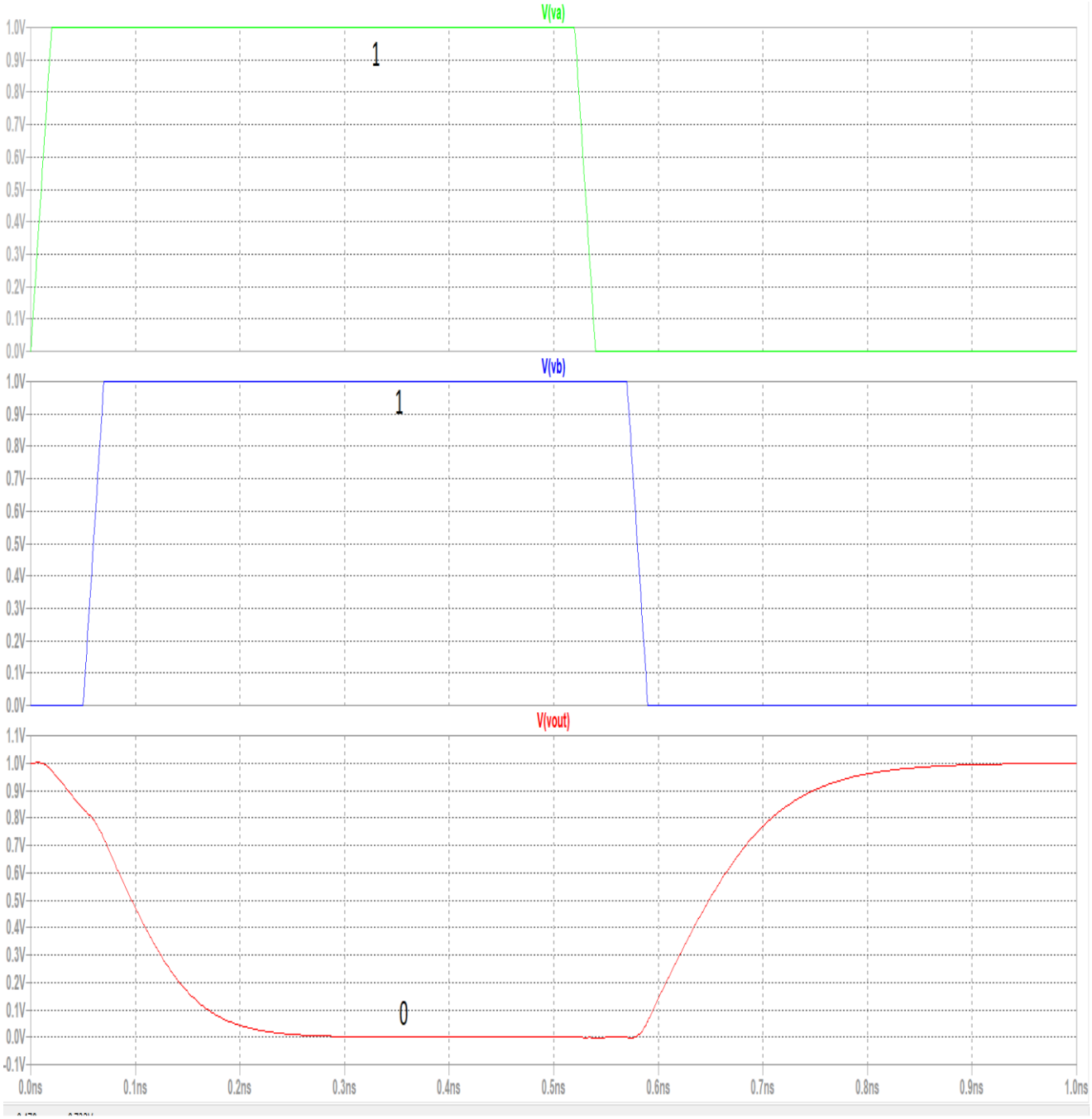

V(va)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
1
V(vb)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
1
V(vout)
1.1V
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
-0.1V
0
0.0ns
0.1ns
0.2ns
0.3ns
0.4ns
0.5ns
0.6ns
0.7ns
0.8ns
0.9ns
1.0ns

FROM LAYOUT

FOR 5fF



FOR 50fF


V(va)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
1
V(vb)
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
1
V(vout)
1.1V
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
-0.1V
0
0.0ns
0.1ns
0.2ns
0.3ns
0.4ns
0.5ns
0.6ns
0.7ns
0.8ns
0.9ns
1.0ns