

# DAY3: COMBINATIONAL AND SEQUENTIAL OPTIMISATION

## Combinational Logic Optimisations:

Activities XDot Sep 27 19:47

root@kuna-Acer-One-14-Z2-493: /home/kuna/Deskto...

```
fxtpt_1".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__sed
fxtpt_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__sed
fxtpt_4".
ABC: Library "sky130_fd_sc_hd__tt_025C_1v80" from "/home/kuna/Desktop/VLSI
/sky130RTLDesignAndSynthesisWorkshop/verilog_files/./lib/sky130_fd_sc_hd__
tt_025C_1v80.lib" has 324 cells (94 skipped: 63 seq; 13 tri-state; 18 no
func; 0 dont_use; 0 with 2 outputs; 0 with 3+ outputs). Time = 0.15 s
ec
ABC: Memory = 19.52 MB. Time = 0.15 sec
ABC: Warning: Detected 9 multi-output cells (for example, "sky130_fd_sc_hd__
fa_1").
ABC: Warning: The network is combinational (run "fraig" or "fraig_sweep").
ABC: abc 07> echo "ABC_DONE"

5.1.2. Re-integrating ABC results.
ABC RESULTS: sky130_fd_sc_hd__or2_0 cells: 1
ABC RESULTS: internal signals: 0
ABC RESULTS: input signals: 2
ABC RESULTS: output signals: 1
Removing temp directory.
Removing global temp directory.

yosys> show

6. Generating Graphviz representation of design.
Writing dot description to '/root/.yosys_show.dot'.
Dumping module opt_check2 to page 1.
Exec: { test -f '/root/.yosys_show.dot.pid' && fuser -s '/root/.yosys_show
.dot.pid' 2> /dev/null; } || { echo $$ >&3; exec xdot '/root/.yosys_show.d
ot'; } 3> '/root/.yosys_show.dot.pid' &

yosys> 
```

yosys\_show.dot - Dot Viewer

```
graph LR
    a((a)) --> A
    b((b)) --> B
    subgraph opt_check2 [opt_check2]
        direction LR
        A[A] --- B[B] --- X[X]
        label "$84 sky130_fd_sc_hd__or2_0"
    end
    X --> y((y))
```

Activities XDot Sep 27 20:00

root@kuna-Acer-One-14-Z2-493: /home/kuna/Deskto...

```
fxtpt_1".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__sed
fxtpt_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__sed
fxtpt_4".
ABC: Library "sky130_fd_sc_hd__tt_025C_1v80" from "/home/kuna/Desktop/VLSI
/sky130RTLDesignAndSynthesisWorkshop/verilog_files/./lib/sky130_fd_sc_hd__
tt_025C_1v80.lib" has 324 cells (94 skipped: 63 seq; 13 tri-state; 18 no
func; 0 dont_use; 0 with 2 outputs; 0 with 3+ outputs). Time = 0.15 s
ec
ABC: Memory = 19.52 MB. Time = 0.15 sec
ABC: Warning: Detected 9 multi-output cells (for example, "sky130_fd_sc_hd__
fa_1").
ABC: Warning: The network is combinational (run "fraig" or "fraig_sweep").
ABC: abc 07> echo "ABC_DONE"

10.1.2. Re-integrating ABC results.
ABC RESULTS: sky130_fd_sc_hd__and3_1 cells: 1
ABC RESULTS: internal signals: 1
ABC RESULTS: input signals: 3
ABC RESULTS: output signals: 1
Removing temp directory.
Removing global temp directory.

yosys> show

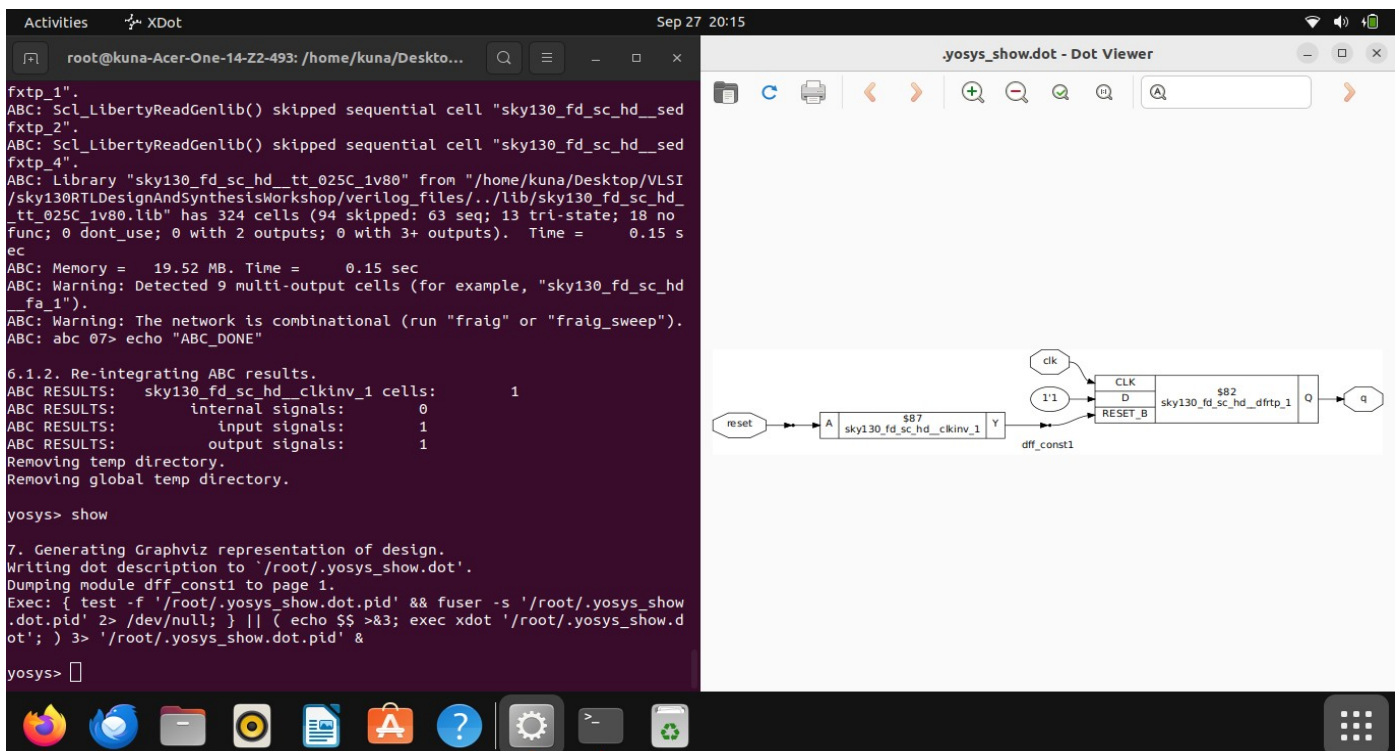
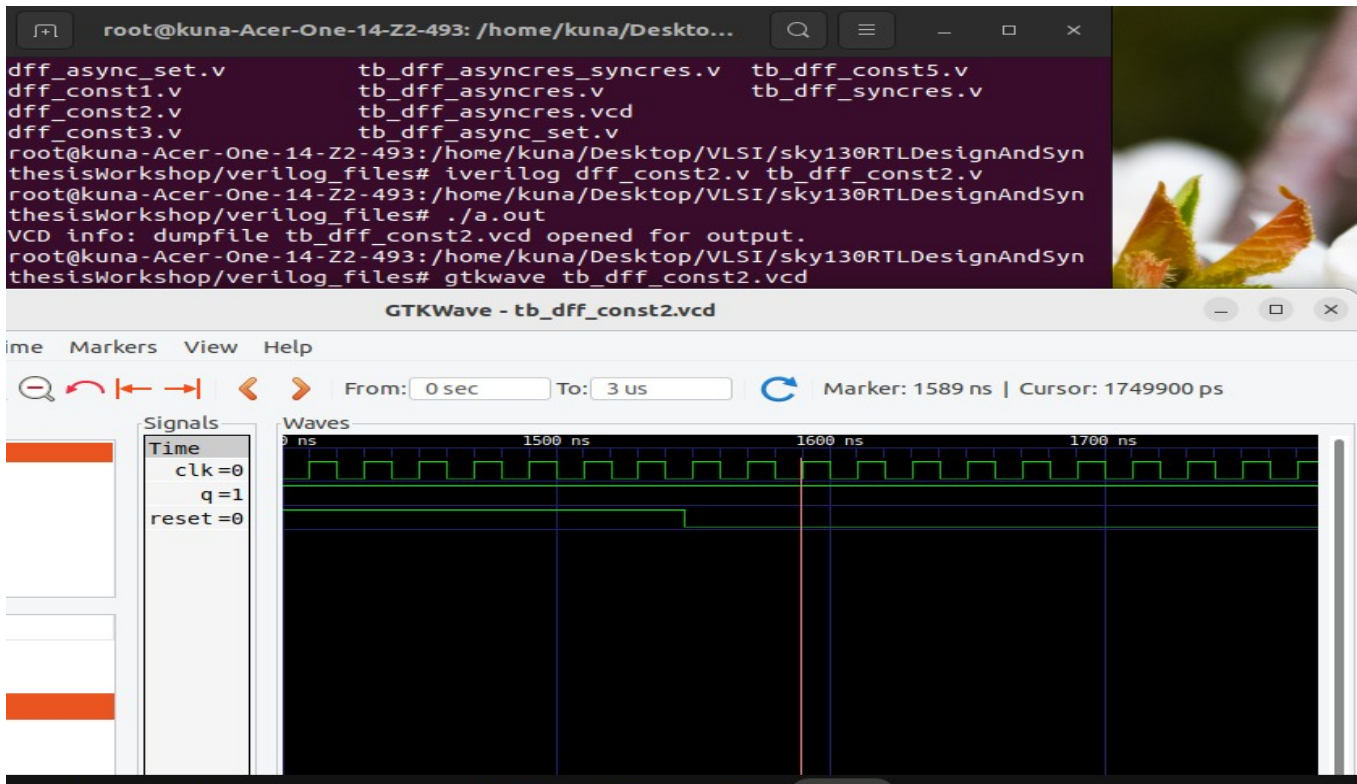
11. Generating Graphviz representation of design.
Writing dot description to '/root/.yosys_show.dot'.
Dumping module opt_check3 to page 1.
Exec: { test -f '/root/.yosys_show.dot.pid' && fuser -s '/root/.yosys_show
.dot.pid' 2> /dev/null; } || { echo $$ >&3; exec xdot '/root/.yosys_show.d
ot'; } 3> '/root/.yosys_show.dot.pid' &

yosys> 
```

yosys\_show.dot - Dot Viewer

```
graph LR
    b((b)) --> A
    c((c)) --> B
    a((a)) --> C
    subgraph opt_check3 [opt_check3]
        direction LR
        A[A] --- B[B] --- C[C] --- X[X]
        label "$172 sky130_fd_sc_hd__and3_1"
    end
    X --> y((y))
```

# Sequential Logic Optimisations:





Activities XDot Sep 27 20:24

root@kuna-Acer-One-14-Z2-493: /home/kuna/Desktop...

```

fxtp_1".
ABC: Scl_LibertyReadGenLib() skipped sequential cell "sky130_fd_sc_hd__sed
fxtp_2".
ABC: Scl_LibertyReadGenLib() skipped sequential cell "sky130_fd_sc_hd__sed
fxtp_4".
ABC: Library "sky130_fd_sc_hd__tt_025C_1v80" from "/home/kuna/Desktop/VLSI
/sky130RTLDesignAndSynthesisWorkshop/verilog_files/./lib/sky130_fd_sc_hd__
tt_025C_1v80.lib" has 324 cells (94 skipped: 63 seq; 13 tri-state; 18 no
func; 0 dont_use; 0 with 2 outputs; 0 with 3+ outputs). Time = 0.15 s
ec
ABC: Memory = 19.52 MB. Time = 0.15 sec
ABC: Warning: Detected 9 multi-output cells (for example, "sky130_fd_sc_hd__
fa_1").
ABC: Warning: The network is combinational (run "fraig" or "fraig_sweep").
ABC: abc 07> echo "ABC_DONE"

12.1.2. Re-integrating ABC results.
ABC RESULTS: sky130_fd_sc_hd__clkinv_1 cells: 2
ABC RESULTS: internal signals: 0
ABC RESULTS: input signals: 1
ABC RESULTS: output signals: 2
Removing temp directory.
Removing global temp directory.

yosys> show

13. Generating Graphviz representation of design.
Writing dot description to '/root/.yosys_show.dot'.
Dumping module dff_const3 to page 1.
Exec: { test -f '/root/.yosys_show.dot.pid' && fuser -s '/root/.yosys_show
.dot.pid' 2> /dev/null; } || { echo $$ >&3; exec xdot '/root/.yosys_show.d
ot'; } 3> '/root/.yosys_show.dot.pid' &

yosys>

```

.yosys\_show.dot - Dot Viewer

The diagram shows a combinational network. It starts with a 'reset' signal that branches into two paths. One path goes through a cell labeled 'sky130\_fd\_sc\_hd\_\_clkinv\_1' (A) to produce 'clk'. The other path goes through a cell labeled 'sky130\_fd\_sc\_hd\_\_clkinv\_1' (A) to produce 'sky130\_fd\_sc\_hd\_\_clkinv\_1'. The 'clk' signal is connected to the 'CLK' input of a multi-output cell 'sky130\_fd\_sc\_hd\_\_dtt\_1' (Q). The 'sky130\_fd\_sc\_hd\_\_clkinv\_1' signal is connected to the 'RESET\_B' input of the same cell. The output of this cell is 'q1', which is connected to the 'CLK' input of another multi-output cell 'sky130\_fd\_sc\_hd\_\_dtt\_2' (Q). The output of this second cell is 'q', which is connected to the 'SET\_B' input of the same cell. The output of this third cell is 'q', which is connected to the 'SET\_B' input of the same cell. The output of this third cell is 'q', which is connected to the 'SET\_B' input of the same cell. The output of this third cell is 'q', which is connected to the 'SET\_B' input of the same cell.

## Seq optimisation unused outputs:

root@kuna-Acer-One-14-Z2-493: /home/kuna/Desktop...

```

Time spent: 409% 4x abc (0 sec), 166% 4x read_liberty (0 sec), ...
root@kuna-Acer-One-14-Z2-493: /home/kuna/Desktop/VLSI/sky130RTLDesignAndSyn
thesisWorkshop/verilog_files# iverilog dff_const3.v tb_dff_const3.v
root@kuna-Acer-One-14-Z2-493: /home/kuna/Desktop/VLSI/sky130RTLDesignAndSyn
thesisWorkshop/verilog_files# ./a.out.v
-bash: ./a.out.v: No such file or directory
root@kuna-Acer-One-14-Z2-493: /home/kuna/Desktop/VLSI/sky130RTLDesignAndSyn
thesisWorkshop/verilog_files# ./a.out
VCD info: dumpfile tb_dff_const3.vcd opened for output.
root@kuna-Acer-One-14-Z2-493: /home/kuna/Desktop/VLSI/sky130RTLDesignAndSyn
thesisWorkshop/verilog_files# gtkwave tb_dff_const3.vcd

```

GTKWave - tb\_dff\_const3.vcd

Markers View Help

From: 0 sec To: 3 us Marker: 1550 ns | Cursor: 1645400 ps

Signals

- Time
- reset=0
- q=0
- clk=1

Waves

The timing diagram shows three signals: 'reset', 'q', and 'clk'. The 'reset' signal is a single pulse at the beginning of the simulation. The 'q' signal is a single pulse that occurs after the 'reset' signal. The 'clk' signal is a periodic square wave that starts at 1400 ns and continues until 1700 ns.

```
Activities XDot Sep 27 20:38
root@kuna-Acer-One-14-Z2-493: /home/kuna/Desktop...

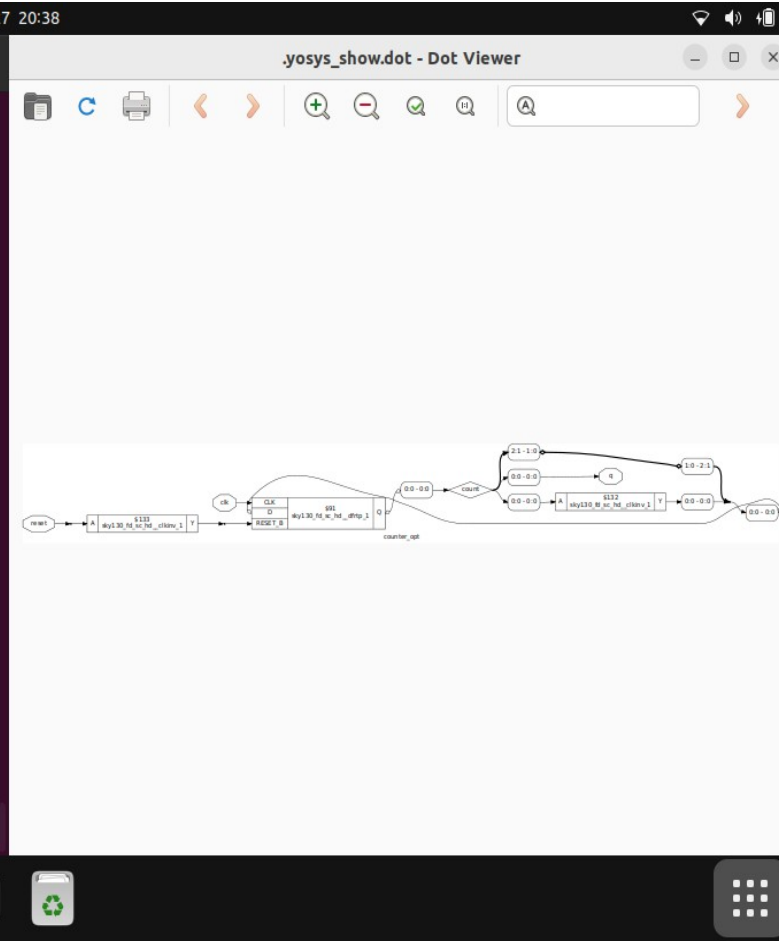
fxtpt_1".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__sed
fxtpt_2".
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ABC: Library "sky130_fd_sc_hd__tt_025C_1v80" from "/home/kuna/Desktop/VLSI
/sky130RTLDesignAndSynthesisWorkshop/verilog_files/./lib/sky130_fd_sc_hd__
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func; 0 dont_use; 0 with 2 outputs; 0 with 3+ outputs). Time = 0.15 s
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fa_1").
ABC: Warning: The network is combinational (run "fraig" or "fraig_sweep").
ABC: abc 07> echo "ABC_DONE"

5.1.2. Re-integrating ABC results.
ABC RESULTS: sky130_fd_sc_hd__clkinv_1 cells: 2
ABC RESULTS: internal signals: 0
ABC RESULTS: input signals: 2
ABC RESULTS: output signals: 2
Removing temp directory.
Removing global temp directory.

yosys> show

6. Generating Graphviz representation of design.
Writing dot description to '/root/.yosys_show.dot'.
Dumping module counter_opt to page 1.
Exec: { test -f '/root/.yosys_show.dot.pid' && fuser -s '/root/.yosys_show
.dot.pid' 2> /dev/null; } || { echo $$ >&3; exec xdot '/root/.yosys_show.d
ot'; } 3> '/root/.yosys_show.dot.pid' &

yosys> 
```



```
Activities XDot Sep 27 20:52
root@kuna-Acer-One-14-Z2-493: /home/kuna/Desktop...

fxtpt_1".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__sed
fxtpt_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__sed
fxtpt_4".
ABC: Library "sky130_fd_sc_hd__tt_025C_1v80" from "/home/kuna/Desktop/VLSI
/sky130RTLDesignAndSynthesisWorkshop/verilog_files/./lib/sky130_fd_sc_hd__
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ABC: abc 07> echo "ABC_DONE"

5.1.2. Re-integrating ABC results.
ABC RESULTS: sky130_fd_sc_hd__clkinv_1 cells: 2
ABC RESULTS: internal signals: 0
ABC RESULTS: input signals: 2
ABC RESULTS: output signals: 2
Removing temp directory.
Removing global temp directory.

yosys> show

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yosys> 
```

