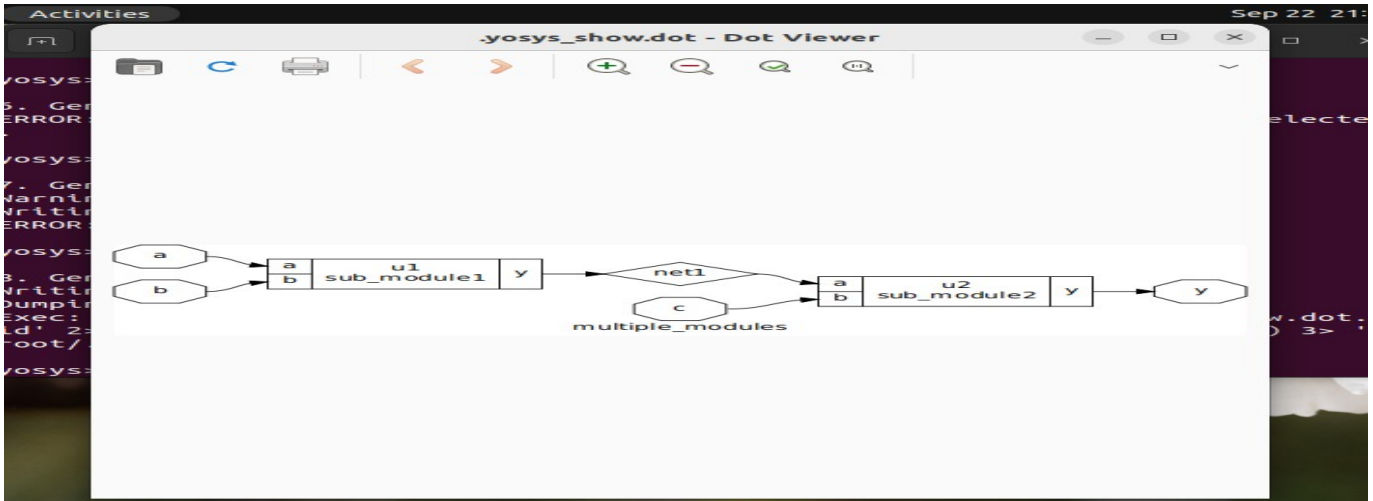


DAY2:TIMING LIBS, HIERARCHIAL VS FLAT SYNTHESIS AND EFFICIENT FLOP CODING STYLE

HIERARCHICAL VS FLAT SYNTHESIS:



```
root@kuna-Acer-One-14-Z2-493: /home/kuna/Desktop/VLSI/...
/* Generated by Yosys 0.57+153 (git sha1 6b3a7e244, g++ 11.4.0-1ubuntu1~22.04.2
-fPIC -O3) */

module multiple_modules(a, b, c, y);
    input a;
    wire a;
    input b;
    wire b;
    input c;
    wire c;
    output y;
    wire y;
    wire net1;
    sub_module1 u1 (
        .a(a),
        .b(b),
        .y(net1)
    );
    sub_module2 u2 (
        .a(net1),
        .b(c),
        .y(y)
    );
endmodule
```

```
root@kuna-Acer-One-14-Z2-493: /home/kuna/Desktop/VLSI/...
3.3.1. Executed ABC.
Extracted 0 gates and 0 wires to a netlist network with 0 inputs and 0 outputs.
Removing temp directory.
Removing global temp directory.

yosys> write_verilog -noattr multiple_modules_hier.v

4. Executing Verilog backend.

4.1. Executing BMUXMAP pass.

4.2. Executing DEMUXMAP pass.
Dumping module '\multiple_modules'.
Dumping module '\sub_module1'.
Dumping module '\sub_module2'.

yosys> !vim multiple_modules_hier.v

5. Shell command: vim multiple_modules_hier.v

[3]+  Stopped                  yosys
root@kuna-Acer-One-14-Z2-493: /home/kuna/Desktop/VLSI/sky130RTLDesignAndSynthesis
workshop/verilog_files#
```

FLATTEN HIER SYNTHESIS:

The terminal window shows the following commands and output:

```
4.3.2. Re-integrating ABC results.
ABC RESULTS: sky130_fd_sc_hd_or2_0 cells: 1
ABC RESULTS: internal signals: 0
ABC RESULTS: input signals: 2
ABC RESULTS: output signals: 1
Removing temp directory.
Removing global temp directory.
yosys> flatten

5. Executing FLATTEN pass (flatten design).
Deleting now unused module sub_module1.
Deleting now unused module sub_module2.
<suppressed ~2 debug messages>

yosys> write_verilog -noattr multiple_modules_flat.v

6. Executing Verilog backend.
6.1. Executing BMUXMAP pass.
6.2. Executing DEMUXMAP pass.
Dumping module `multiple_modules'.

yosys> show

7. Generating Graphviz representation of design.
Writing dot description to '/root/.yosys_show.dot'.
Dumping module multiple_modules to page 1.
Exec: { test -f '/root/.yosys_show.dot.pid' && fuser -s '/root/.yosys_show
.dot.pid' 2> /dev/null; } || { echo $$ >&3; exec xdot '/root/.yosys_show.d
ot'; } 3> '/root/.yosys_show.dot.pid' &
yosys>
```

The Dot Viewer shows a Graphviz diagram representing the flattened design, with nodes and edges illustrating the logic flow.

Flops and Flop coding styles : Asynchronous reset:

The terminal window shows the following commands and output:

```
thesisWorkshop/verilog_files# ls *dff*
dff_ares.net.v          dff_const3.v          tb_dff_async_set.v
dff_asyncres_net.v      dff_const4.v          tb_dff_const1.v
dff_asyncres_syncre.v   dff_const5.v          tb_dff_const2.v
dff_asyncres.v          dff_net.v             tb_dff_const3.v
dff_async_set.v         dff_syncre.v          tb_dff_const4.v
dff_const1.v           tb_dff_asyncres_syncre.v tb_dff_const5.v
dff_const2.v           tb_dff_asyncres.v      tb_dff_syncre.v
root@kuna-Acer-One-14-Z2-493: /home/kuna/Desktop/VLSI/sky130RTLDesignAndSyn
thesisWorkshop/verilog_files# iverilog dff_asyncres.v tb_dff_asyncres.v
root@kuna-Acer-One-14-Z2-493: /home/kuna/Desktop/VLSI/sky130RTLDesignAndSyn
thesisWorkshop/verilog_files# ./a.out
VCD info: dumpfile tb_dff_asyncres.vcd opened for output.
root@kuna-Acer-One-14-Z2-493: /home/kuna/Desktop/VLSI/sky130RTLDesignAndSyn
thesisWorkshop/verilog_files# gtkwave tb_dff_asyncres.vcd
```

The GTKWave window shows the waveform for the asynchronous reset circuit, with signals like `async_reset`, `clk`, `d`, and `q` visible.

The terminal window shows the following commands and output:

```
fxtpt.1".
ABC: Scl_LibertyReadGenLib() skipped sequential cell "sky130_fd_sc_hd_sed
fxtpt.2".
ABC: Scl_LibertyReadGenLib() skipped sequential cell "sky130_fd_sc_hd_sed
fxtpt.4".
ABC: Library "sky130_fd_sc_hd_tt_025C_1v80" from "/home/kuna/Desktop/VLSI
/sky130RTLDesignAndSynthesisWorkshop/verilog_files/./lib/sky130_fd_sc_hd
_tt_025C_1v80.lib" has 324 cells (94 skipped: 63 seq; 13 tri-state; 18 no
func; 0 dont_use; 0 with 2 outputs; 0 with 3+ outputs). Time = 0.15 s
ec
ABC: Memory = 19.52 MB. Time = 0.15 sec
ABC: Warning: Detected 9 multi-output cells (for example, "sky130_fd_sc_hd
_fa_1").
ABC: Warning: The network is combinational (run "fraig" or "fraig_sweep").
ABC: abc 07> echo "ABC_DONE"

7.1.2. Re-integrating ABC results.
ABC RESULTS: sky130_fd_sc_hd_clkinv_1 cells: 1
ABC RESULTS: internal signals: 0
ABC RESULTS: input signals: 1
ABC RESULTS: output signals: 1
Removing temp directory.
Removing global temp directory.

yosys> show

8. Generating Graphviz representation of design.
Writing dot description to '/root/.yosys_show.dot'.
Dumping module dff_asyncres to page 1.
Exec: { test -f '/root/.yosys_show.dot.pid' && fuser -s '/root/.yosys_show
.dot.pid' 2> /dev/null; } || { echo $$ >&3; exec xdot '/root/.yosys_show.d
ot'; } 3> '/root/.yosys_show.dot.pid' &
yosys>
```

The Dot Viewer shows a logic diagram for the asynchronous reset circuit, with components like `sky130_fd_sc_hd_clkinv_1` and `sky130_fd_sc_hd_dfftp_1` visible.

OPTIMISATIONS:

Activities XDot Sep 27 19:16

root@kuna-Acer-One-14-Z2-493: /home/kuna/Deskto...

```
7 wire bits
2 public wires
7 public wire bits
2 ports
7 port bits

6.26. Executing CHECK pass (checking for obvious problems).
Checking module mul2...
Found and reported 0 problems.

yosys> abc -liberty ../lib/sky130_fd_sc_hd_tt_025C_1v80.lib

7. Executing ABC pass (technology mapping using ABC).

7.1. Extracting gate netlist of module '\mul2' to '<abc-temp-dir>/input.blif'...
Don't call ABC as there is nothing to map.

7.1.1. Executed ABC.
Extracted 0 gates and 0 wires to a netlist network with 0 inputs and 0 outputs.
Removing temp directory.
Removing global temp directory.

yosys> show

8. Generating Graphviz representation of design.
Writing dot description to '/root/.yosys_show.dot'.
Dumping module mul2 to page 1.
Exec: { test -f '/root/.yosys_show.dot.pid' && fuser -s '/root/.yosys_show.dot.pid' 2> /dev/null; } || ( echo $$ >&3; exec xdot '/root/.yosys_show.dot'; ) 3> '/root/.yosys_show.dot.pid' &

yosys> 
```

.yosys_show.dot - Dot Viewer

```
graph LR
    a{{a}} --> mul2[2:0 - 3:1<br/>0 -> 0:0]
    mul2 --> y{{y}}
```

Activities XDot Sep 27 19:21

root@kuna-Acer-One-14-Z2-493: /home/kuna/Deskto...

```
9 wire bits
2 public wires
9 public wire bits
2 ports
9 port bits

11.26. Executing CHECK pass (checking for obvious problems).
Checking module mult8...
Found and reported 0 problems.

yosys> abc -liberty ../lib/sky130_fd_sc_hd_tt_025C_1v80.lib

12. Executing ABC pass (technology mapping using ABC).

12.1. Extracting gate netlist of module '\mult8' to '<abc-temp-dir>/input.blif'...
Don't call ABC as there is nothing to map.

12.1.1. Executed ABC.
Extracted 0 gates and 0 wires to a netlist network with 0 inputs and 0 outputs.
Removing temp directory.
Removing global temp directory.

yosys> show

13. Generating Graphviz representation of design.
Writing dot description to '/root/.yosys_show.dot'.
Dumping module mult8 to page 1.
Exec: { test -f '/root/.yosys_show.dot.pid' && fuser -s '/root/.yosys_show.dot.pid' 2> /dev/null; } || ( echo $$ >&3; exec xdot '/root/.yosys_show.dot'; ) 3> '/root/.yosys_show.dot.pid' &

yosys> 
```

.yosys_show.dot - Dot Viewer

```
graph LR
    a{{a}} --> mult8[2x 2:0 - 5:0]
    mult8 --> y{{y}}
```