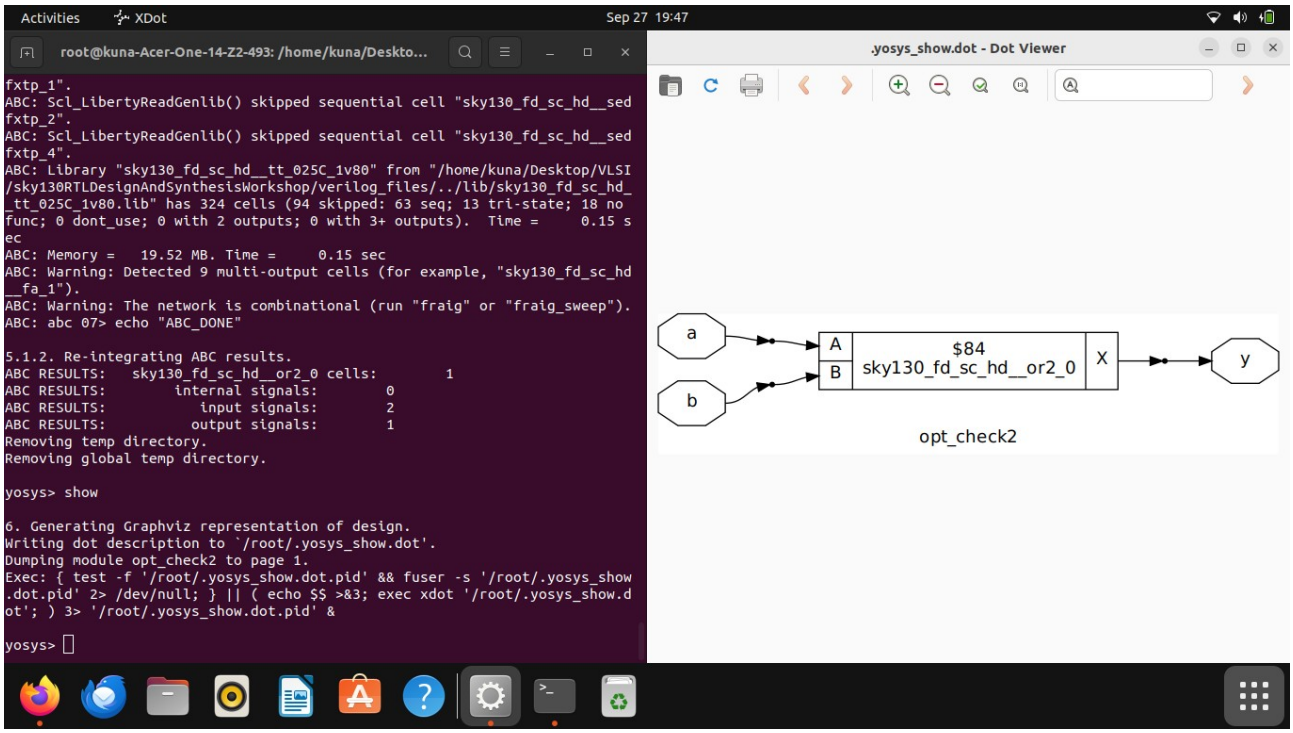
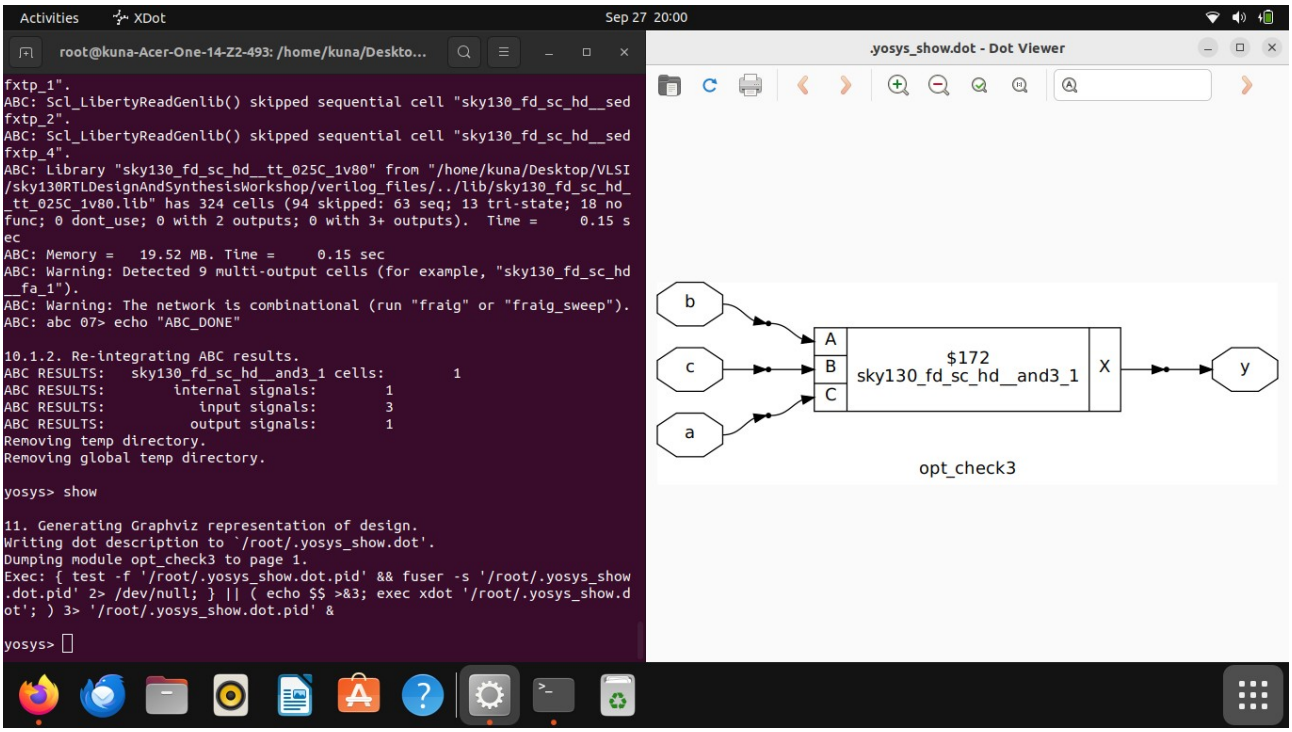
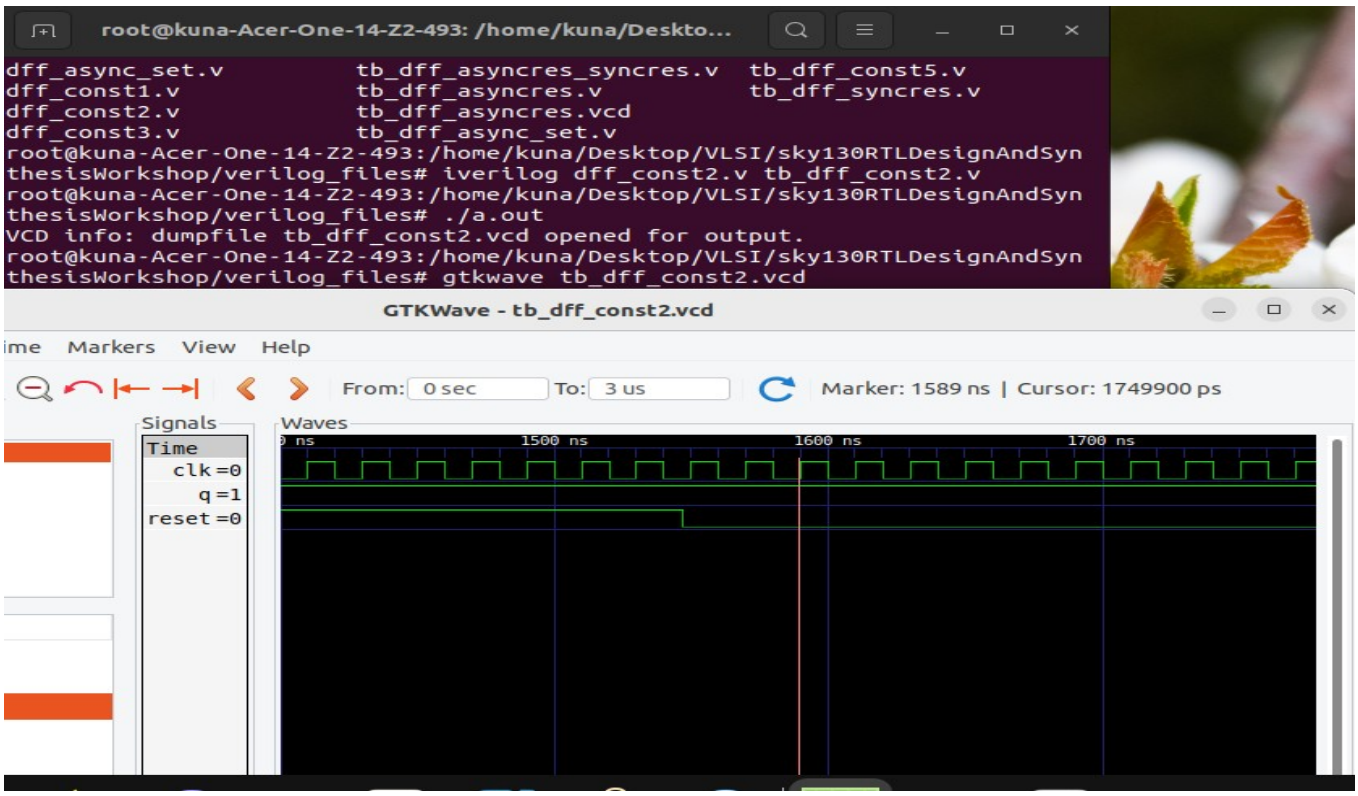
DAY3: COMBINATIONAL AND SEQUENTIAL OPTIMISATION

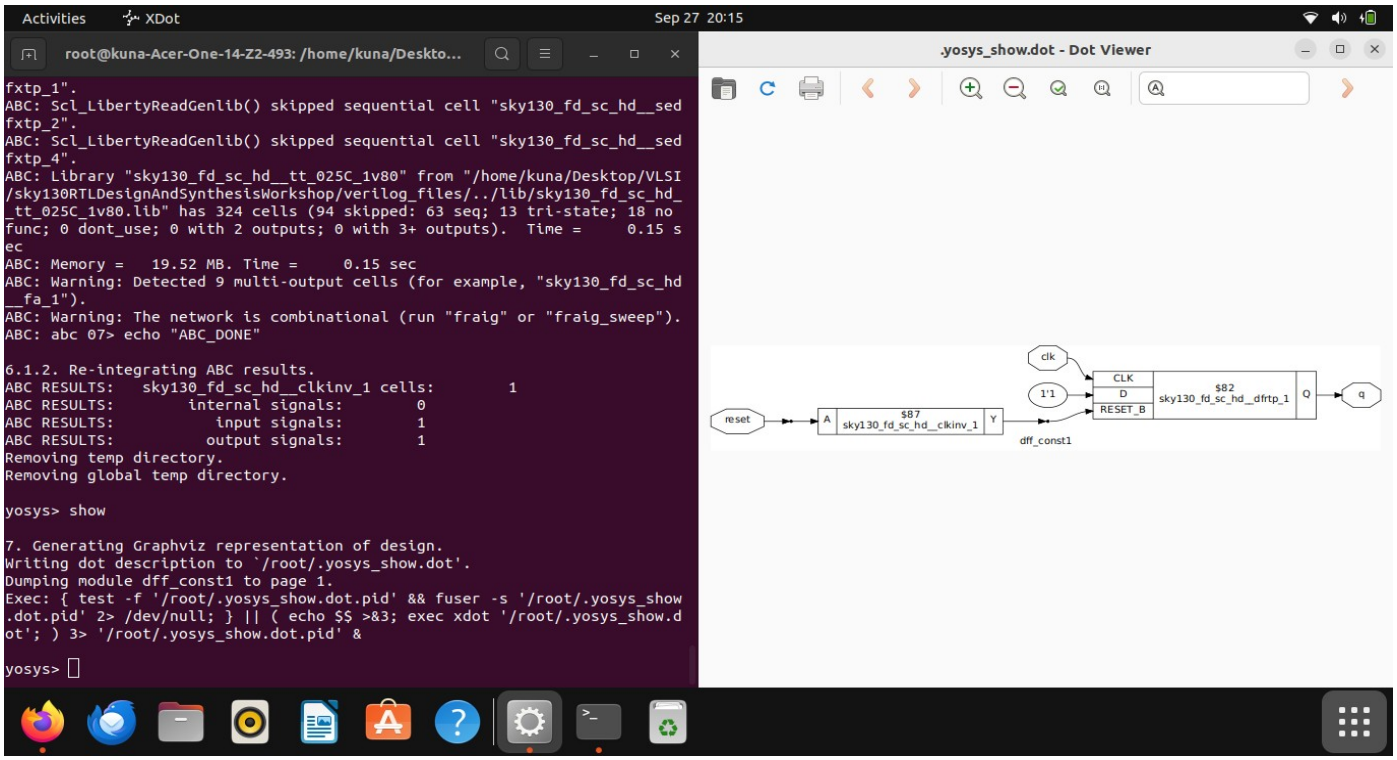
Combinational Logic Optimisations:

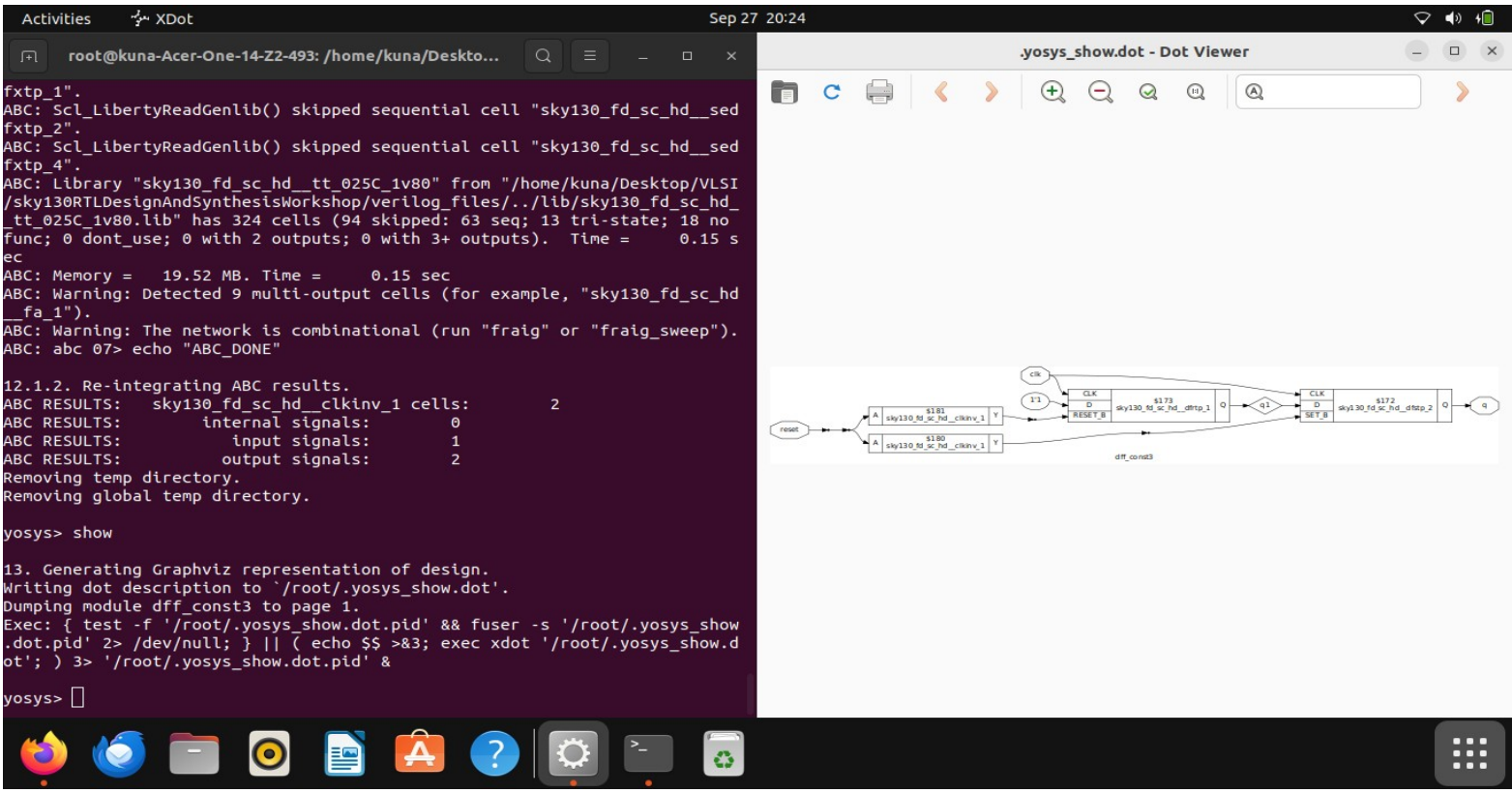




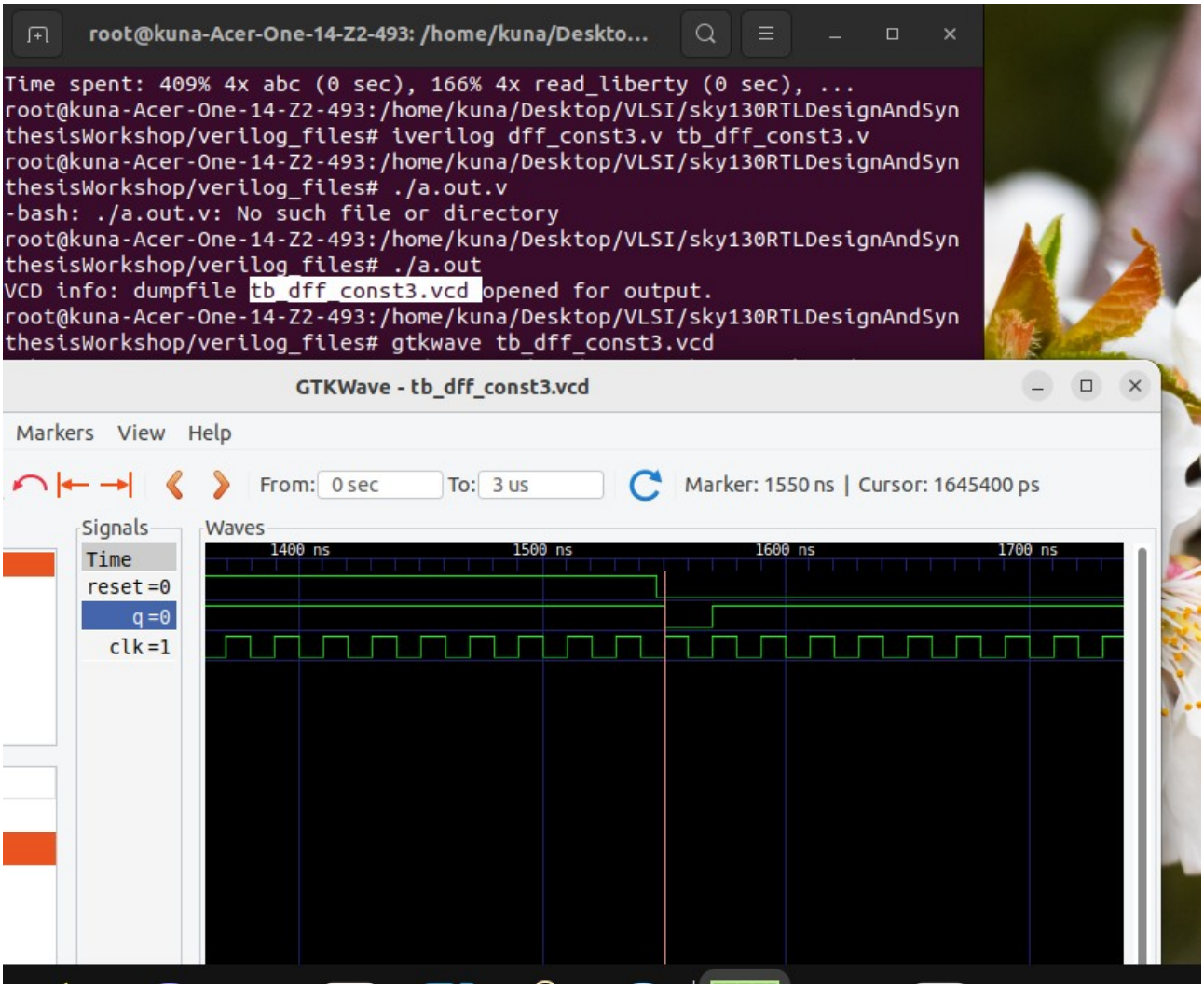
Sequential Logic Optimisations:







Seq optimisation unused outputs:

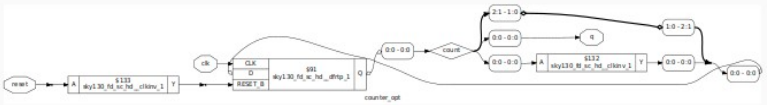


Activities XDot Sep 27 20:38

root@kuna-Acer-One-14-Z2-493: /home/kuna/Deskto...

```
fxtp_1".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__sed
fxtp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__sed
fxtp_4".
ABC: Library "sky130_fd_sc_hd__tt_025C_1v80" from "/home/kuna/Desktop/VLSI
/sky130RTLDesignAndSynthesisWorkshop/verilog_files/../lib/sky130_fd_sc_hd_
_tt_025C_1v80.lib" has 324 cells (94 skipped: 63 seq; 13 tri-state; 18 no
func; 0 dont_use; 0 with 2 outputs; 0 with 3+ outputs).  Time =     0.15 s
ec
ABC: Memory =   19.52 MB. Time =     0.15 sec
ABC: Warning: Detected 9 multi-output cells (for example, "sky130_fd_sc_hd
__fa_1").
ABC: Warning: The network is combinational (run "fraig" or "fraig_sweep").
ABC: abc 07> echo "ABC_DONE"

5.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__clkinv_1 cells:        2
ABC RESULTS:        internal signals:        0
ABC RESULTS:           input signals:        2
ABC RESULTS:          output signals:        2
Removing temp directory.
Removing global temp directory.

yosys> show

6. Generating Graphviz representation of design.
Writing dot description to `/root/.yosys_show.dot'.
Dumping module counter_opt to page 1.
Exec: { test -f '/root/.yosys_show.dot.pid' && fuser -s '/root/.yosys_show
.dot.pid' 2> /dev/null; } || ( echo $$ >&3; exec xdot '/root/.yosys_show.d
ot'; ) 3> '/root/.yosys_show.dot.pid' &

yosys>
```

.yosys_show.dot - Dot Viewer



Activities XDot Sep 27 20:52

root@kuna-Acer-One-14-Z2-493: /home/kuna/Deskto...

fxtp_1".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__sed
fxtp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__sed
fxtp_4".
ABC: Library "sky130_fd_sc_hd__tt_025C_1v80" from "/home/kuna/Desktop/VLSI
/sky130RTLDesignAndSynthesisWorkshop/verilog_files/../lib/sky130_fd_sc_hd_
_tt_025C_1v80.lib" has 324 cells (94 skipped: 63 seq; 13 tri-state; 18 no
func; 0 dont_use; 0 with 2 outputs; 0 with 3+ outputs). Time =   0.15 s
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ABC: Memory =   19.52 MB. Time =   0.15 sec
ABC: Warning: Detected 9 multi-output cells (for example, "sky130_fd_sc_hd
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ABC: Warning: The network is combinational (run "fraig" or "fraig_sweep").
ABC: abc 07> echo "ABC_DONE"

5.1.2. Re-integrating ABC results.
ABC RESULTS: sky130_fd_sc_hd__clkinv_1 cells: 2
ABC RESULTS: internal signals: 0
ABC RESULTS: input signals: 2
ABC RESULTS: output signals: 2
Removing temp directory.
Removing global temp directory.

yosys> show

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Writing dot description to `/root/.yosys_show.dot'.
Dumping module counter_opt to page 1.
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.dot.pid' 2> /dev/null; } || (echo $$ >&3; exec xdot '/root/.yosys_show.d
ot';) 3> '/root/.yosys_show.dot.pid' &

yosys>

.yosys_show.dot - Dot Viewer