Designs ran on ASAP7 PDK Platform – Test 2

*All the documentation is also drafted in my Github Forked Repository >> **7nmcontest** branch >> **7nmdesigncontest.md** file.*

https://github.com/KunalKokate/OpenROAD-flow-scripts/tree/7nmcontest

AIM:

To improve the timing parameters below by making changes in CTS script:

1. Overall Performance Elapsed Runtime
2. CPU User Time
3. CTS Elapsed Seconds to run CTS Stage

All the parameters to look are highlighted in **bold**.

Description:

In this document, the idea is to modify the OpenROAD scripts for improvement of CTS timings. I plan to improve the overall runtime for a design by modifying the Clock Tree Synthesis TCL script.
To do so, I have updated the **scripts/cts.tcl** file to improve the **Overall Performance Elapsed Runtime, CPU User Time**, and **CTS Elapsed Seconds to run CTS Stage**

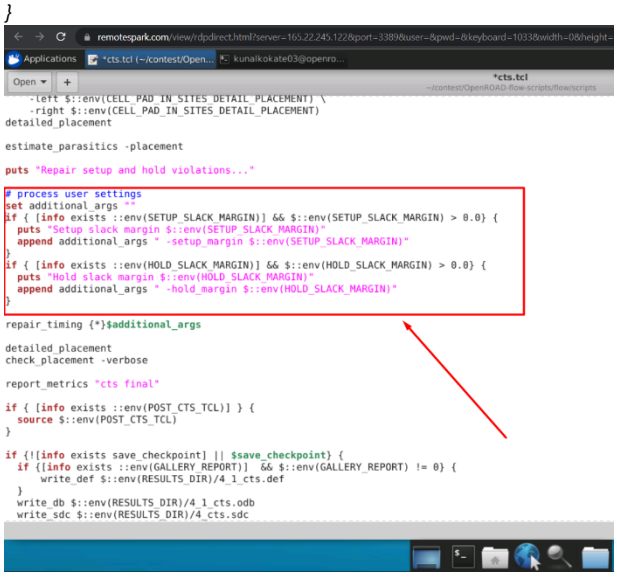
Steps taken:

- Goto OpenROAD-flow-scripts/flow/scripts
- Gedit cts.tcl
- Updated the process user settings if loop with for loop.
  And saved the file.

Before:

Code –

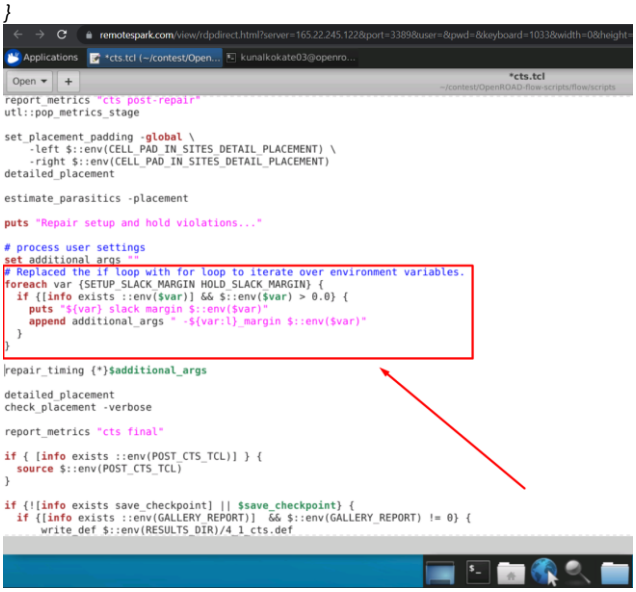
```
if { [info exists ::env(SETUP_SLACK_MARGIN)] && $::env(SETUP_SLACK_MARGIN)
> 0.0} {
  puts "Setup slack margin $::env(SETUP_SLACK_MARGIN)"
  append additional_args " -setup_margin $::env(SETUP_SLACK_MARGIN)"
}
if { [info exists ::env(HOLD_SLACK_MARGIN)] && $::env(HOLD_SLACK_MARGIN)
> 0.0} {
  puts "Hold slack margin $::env(HOLD_SLACK_MARGIN)"
  append additional_args " -hold_margin $::env(HOLD_SLACK_MARGIN)"
}
```



After:

Code –

```
foreach var {SETUP_SLACK_MARGIN HOLD_SLACK_MARGIN} {
  if {[info exists ::env($var)] && $::env($var) > 0.0} {
    puts "${var} slack margin $::env($var)"
    append additional_args " -${var:l}_margin $::env($var)"
  }
}
```



This code uses a **foreach** loop to iterate over the environment variables **SETUP_SLACK_MARGIN** and **HOLD_SLACK_MARGIN**. Inside the loop, it checks if the variables exist and their values are greater than 0.0. If they do, it prints a message and appends

their values to the additional_args variable using the append command. Note that ${var:l} converts the first letter of the variable name to lowercase and appends the string _margin to it.

This code eliminates the need for separate **if statements**, and thus simplifies the code.

After making the changes and saving the file. I ran the same designs again to see the improvement in the timings as illustrated below:

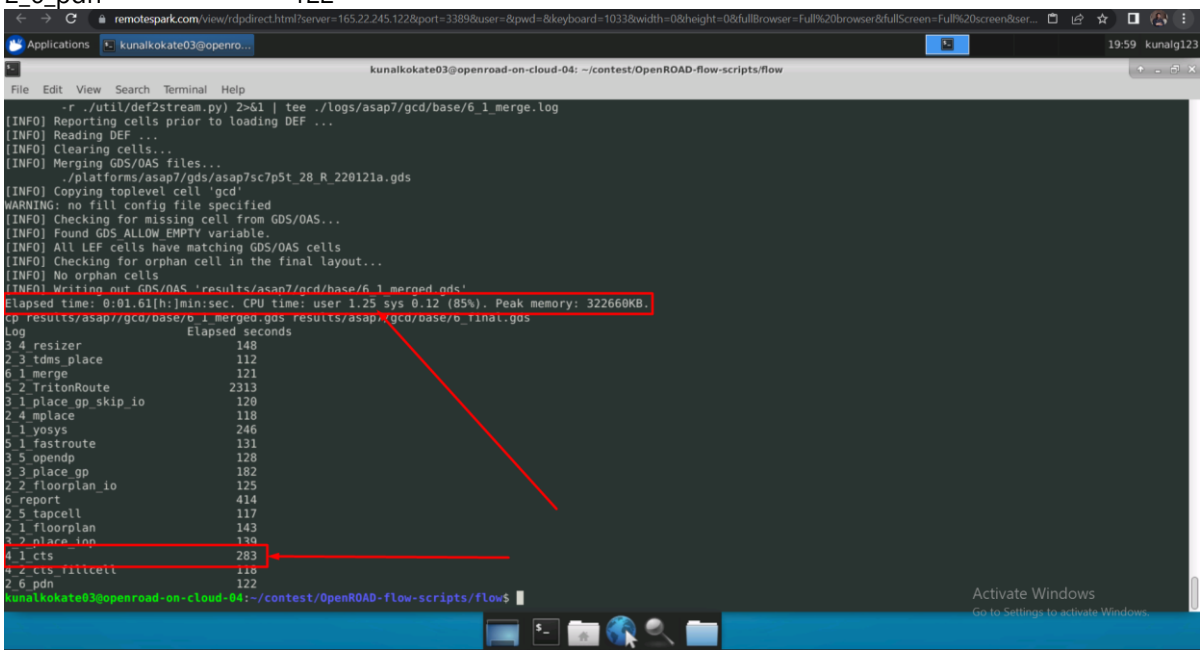
TEST 2: Runtimes of all the designs after modifying the CTS TCL Script in ORFS

GCD Design

Overall Performance time

Elapsed time: 0:01.61[h:]min:sec. CPU time: user **1.25** sys 0.12 (85%). Peak memory: 322660KB.
cp results/asap7/gcd/base/6_1_merged.gds results/asap7/gcd/base/6_final.gds

Log	Elapsed seconds
3_4_resizer	148
2_3_tdms_place	112
6_1_merge	121
5_2_TritonRoute	2313
3_1_place_gp_skip_io	120
2_4_mplace	118
1_1_yosys	246
5_1_fastroute	131
3_5_opendp	128
3_3_place_gp	182
2_2_floorplan_io	125
6_report	414
2_5_tapcell	117
2_1_floorplan	143
3_2_place_iop	139
4_1_cts	**283**
4_2_cts_fillcell	118
2_6_pdn	122



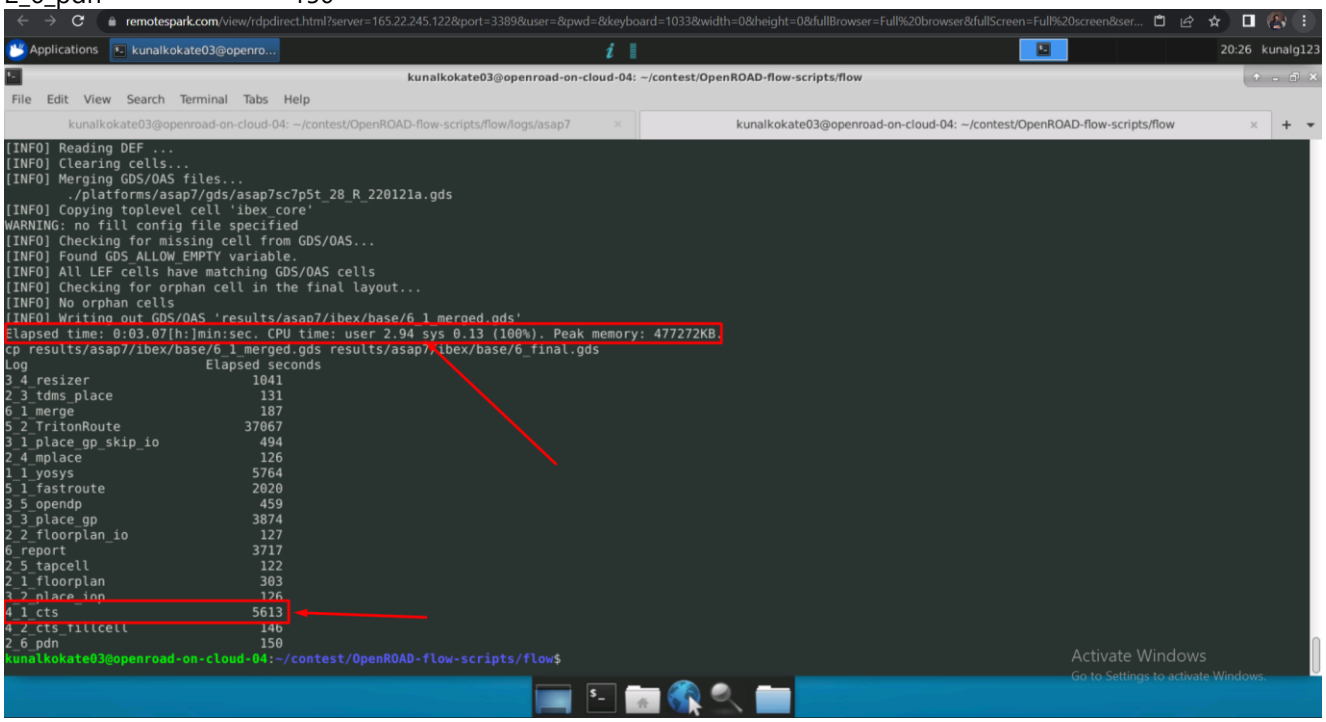
Timing report from 4_1_cts.log

Elapsed time: 0:04.43[h:]min:sec**. CPU time: user 4.36** sys 0.06 (99%). Peak memory: 197336KB.

IBEX Design

Elapsed time: 0:03.07[h:]min:sec. **CPU time: user 2.94** sys 0.13 (100%). Peak memory: 477272KB.
cp results/asap7/ibex/base/6_1_merged.gds results/asap7/ibex/base/6_final.gds

Log	Elapsed seconds
3_4_resizer	1041
2_3_tdms_place	131
6_1_merge	187
5_2_TritonRoute	37067
3_1_place_gp_skip_io	494
2_4_mplace	126
1_1_yosys	5764
5_1_fastroute	2020
3_5_opendp	459
3_3_place_gp	3874
2_2_floorplan_io	127
6_report	3717
2_5_tapcell	122
2_1_floorplan	303
3_2_place_iop	126
4_1_cts	**5613**
4_2_cts_fillcell	146
2_6_pdn	150



Timing report from 4_1_cts.log

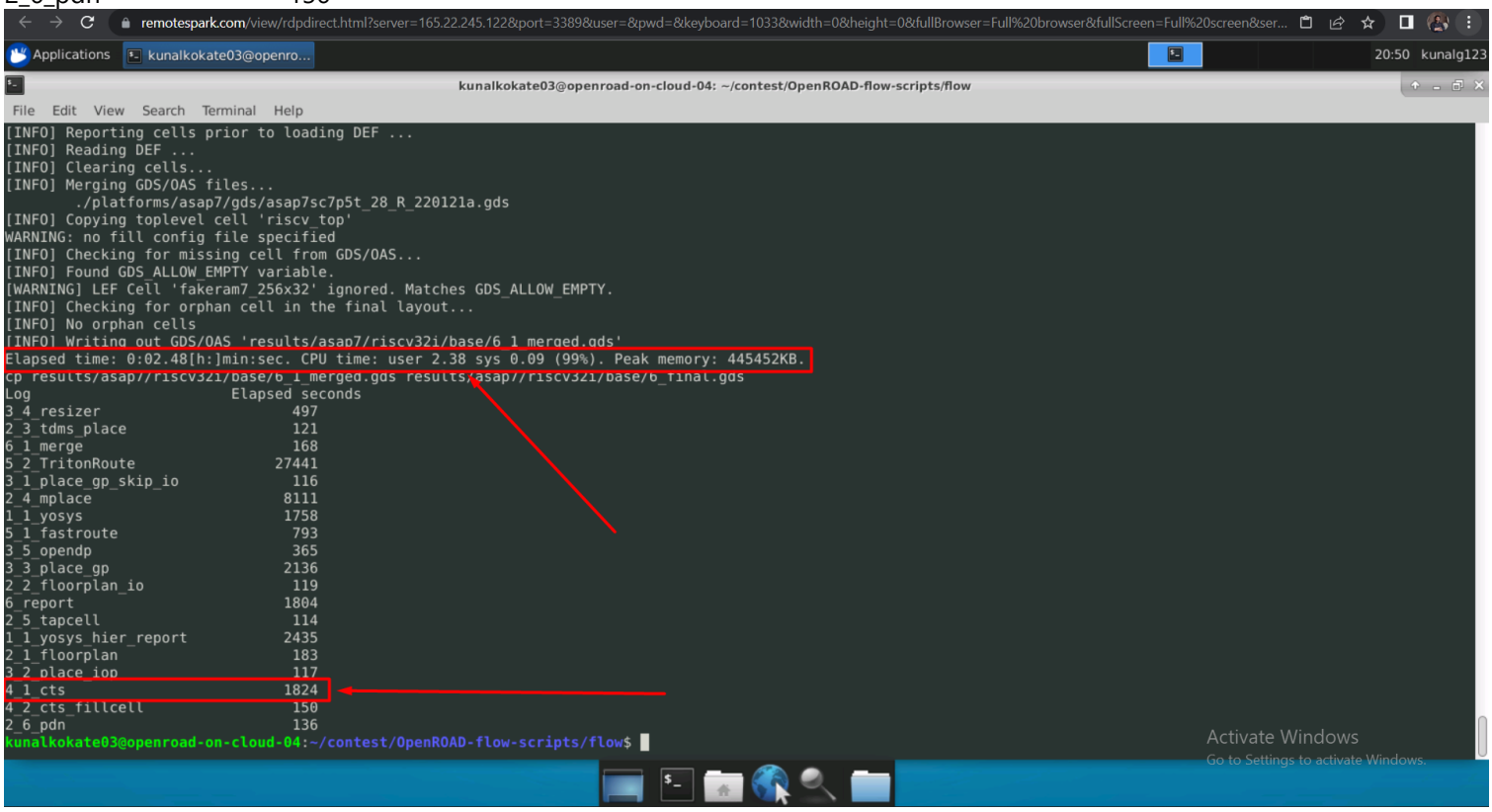
Elapsed time: 1:33.33[h:]min:sec. **CPU time: user 93.20** sys 0.13 (100%). Peak memory: 297076KB

RISCV32i Design

Elapsed time: 0:02.48[h:]min:sec. **CPU time: user 2.38** sys 0.09 (99%). Peak memory: 445452KB.

cp results/asap7/riscv32i/base/6_1_merged.gds results/asap7/riscv32i/base/6_final.gds

Log	Elapsed seconds
3_4_resizer	497
2_3_tdms_place	121
6_1_merge	168
5_2_TritonRoute	27441
3_1_place_gp_skip_io	116
2_4_mplace	8111
1_1_yosys	1758
5_1_fastroute	793
3_5_opendp	365
3_3_place_gp	2136
2_2_floorplan_io	119
6_report	1804
2_5_tapcell	114
1_1_yosys_hier_report	2435
2_1_floorplan	183
3_2_place_iop	117
4_1_cts	**1824**
4_2_cts_fillcell	150
2_6_pdn	136



Timing report from 4_1_cts.log

Elapsed time: 0:30.24[h:]min:sec. **CPU time: user 30.12** sys 0.11 (99%). Peak memory: 296780KB.