

# Designs ran on ASAP7 PDK Platform- Test 1

All the documentation is also drafted in my Github Forked Repository >> **7nmcontest** branch >>  
**7nmcontest.md** file

<https://github.com/KunalKokate/OpenROAD-flow-scripts/tree/7nmcontest>

## AIM:

To improve the timing parameters below by making changes in CTS script:

1. Overall Performance Elapsed Runtime
2. CPU User Time
3. CTS Elapsed Seconds to run CTS Stage

All the parameters to look are highlighted in **bold**.

## Description:

This document reflects the default performance runtimes of current designs without any changes made. I plan to improve the overall runtime for a design by modifying the **Clock Tree Synthesis TCL script**.

I have documented my changes in another document (*Test2 of all the designs.docx*) to compare the run times for all the designs.

## TEST 1: Runtimes of all the default designs of ORFS

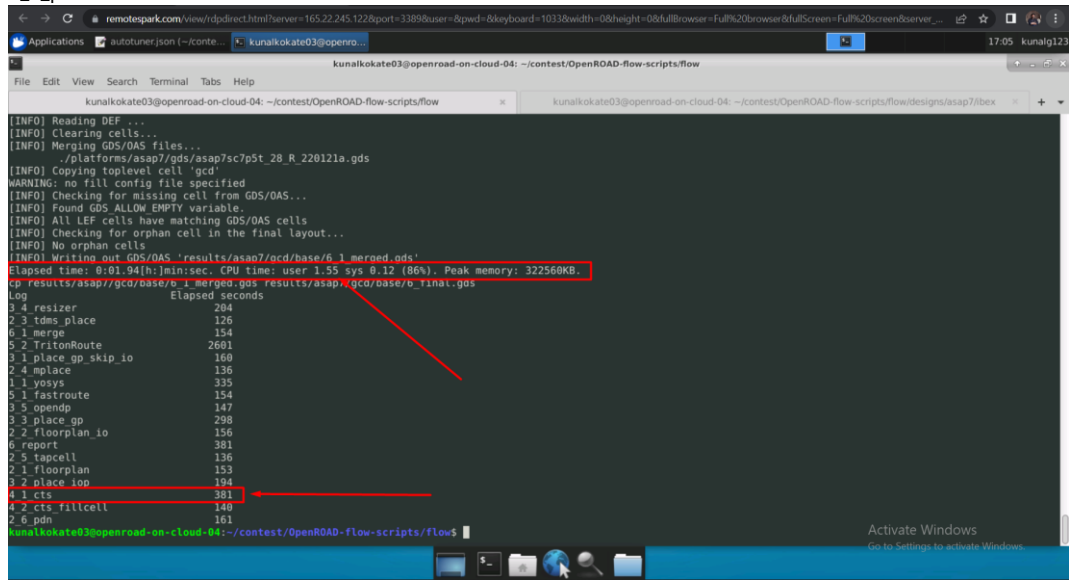
### GCD design

#### Overall Performance time

**Elapsed time: 0:01.94** [h:]min:sec. **CPU time: user 1.55** sys 0.12 (86%). Peak memory: 322560KB.

cp results/asap7/gcd/base/6\_1\_merged.gds results/asap7/gcd/base/6\_final.gds

Log	<b>Elapsed seconds</b>
3_4_resizer	204
2_3_tdms_place	126
6_1_merge	154
5_2_TritonRoute	2601
3_1_place_gp_skip_io	160
2_4_mplace	136
1_1_yosys	335
5_1_fastroute	154
3_5_opendp	147
3_3_place_gp	298
2_2_floorplan_io	156
6_report	381
2_5_tapcell	136
2_1_floorplan	153
3_2_place_iop	194
<b>4_1_cts</b>	<b>381</b>
4_2_cts_fillcell	140



## Timing report from 4\_1\_cts.log

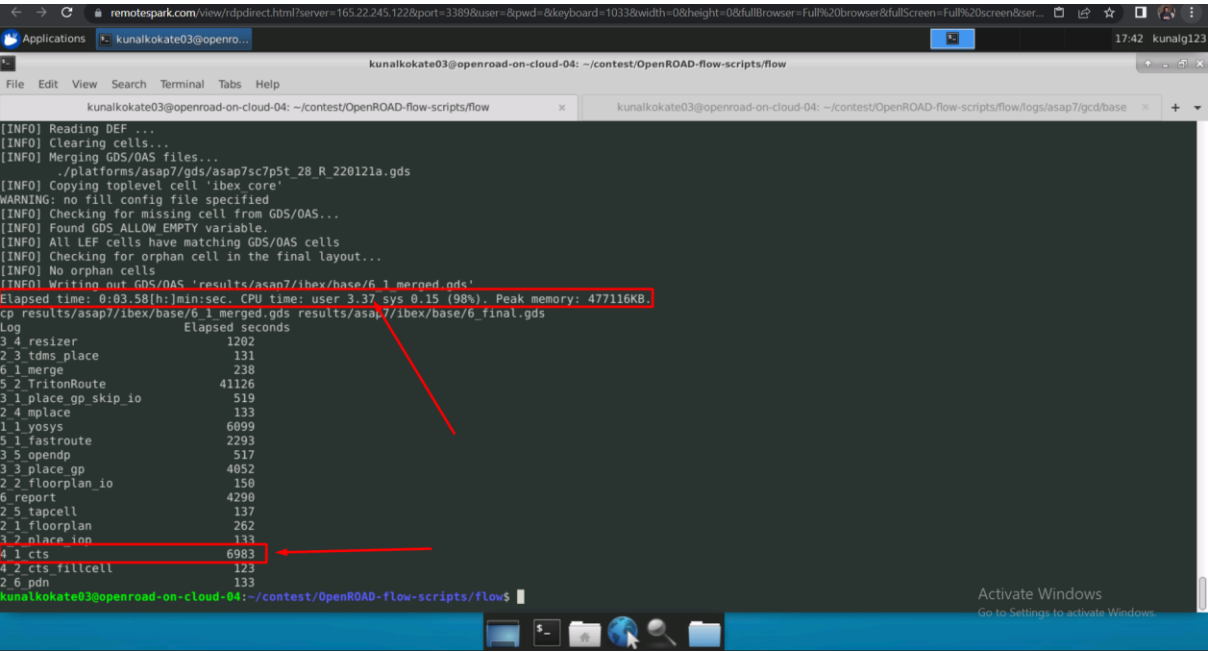
**Elapsed time: 0:06.21[h]:min:sec. CPU time: user 5.47 sys 0.06 (88%). Peak memory: 196980KB.**

# IBEX Design

## Overall Performance time

**Elapsed time: 0:03.58[h:]min:sec. CPU time: user 3.37 sys 0.15 (98%). Peak memory: 477116KB.**

Log	Elapsed seconds
3_4_resizer	1202
2_3_tdms_place	131
6_1_merge	238
5_2_TritonRoute	41126
3_1_place_gp_skip_io	519
2_4_mplace	133
1_1_yosys	6099
5_1_fastroute	2293
3_5_opendp	517
3_3_place_gp	4052
2_2_floorplan_io	150
6_report	4290
2_5_tapcell	137
2_1_floorplan	262
3_2_place_iop	133
<b>4_1_cts</b>	<b>6983</b>
4_2_cts_fillcell	123
2_6_pdn	133



## Timing report from 4\_1\_cts.log

**Elapsed time: 1:56.23[h:]min:sec. CPU time: user 116.06 sys 0.17 (100%). Peak memory: 296996KB.**

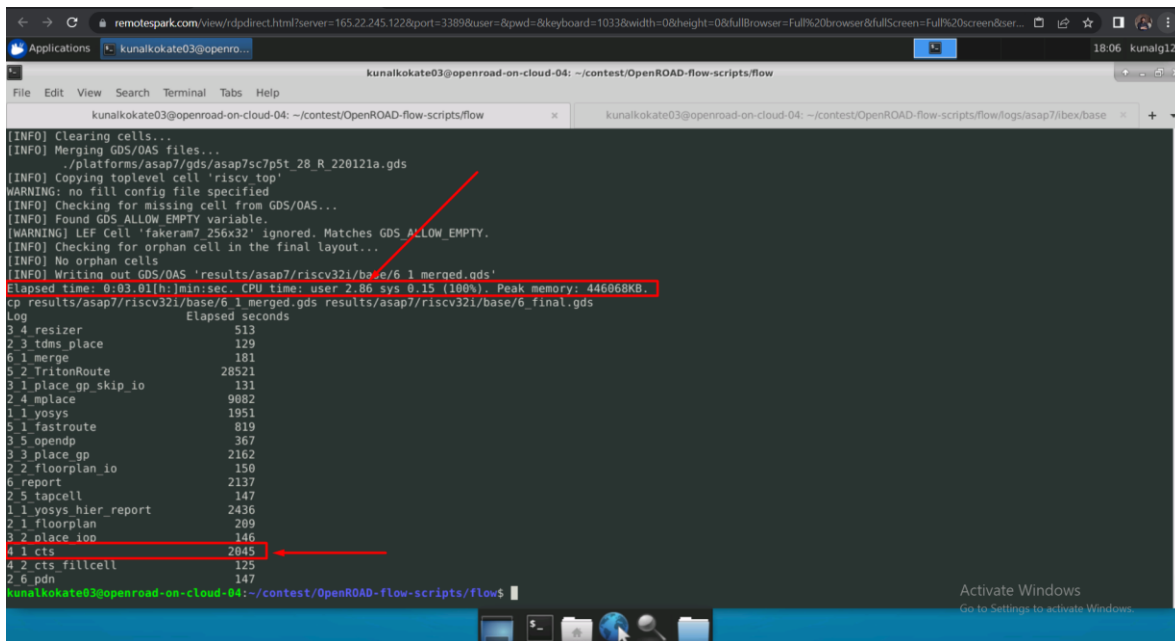
# RISCV32i Design

## Overall Performance time

**Elapsed time: 0:03.01**[h:]min:sec. **CPU time: user 2.86** sys 0.15 (100%). Peak memory: 446068KB.

cp results/asap7/riscv32i/base/6\_1\_merged.gds results/asap7/riscv32i/base/6\_final.gds

Log	Elapsed seconds
3_4_resizer	513
2_3_tdms_place	129
6_1_merge	181
5_2_TritonRoute	28521
3_1_place_gp_skip_io	131
2_4_mplace	9082
1_1_yosys	1951
5_1_fastroute	819
3_5_opendp	367
3_3_place_gp	2162
2_2_floorplan_io	150
6_report	2137
2_5_tapcell	147
1_1_yosys_hier_report	2436
2_1_floorplan	209
3_2_place_iop	146
<b>4_1_cts</b>	<b>2045</b>
4_2_cts_fillcell	125
2_6_pdn	147



```
[INFO] Clearing cells...
[INFO] Merging GDS/OAS files...
./platforms/asap7/gds/asap7sc7p5t_28_R_220121a.gds
[INFO] Copying toplevel cell 'riscv_top'
WARNING: no fill config file specified
[INFO] Checking for missing cell from GDS/OAS...
[INFO] Found GDS ALLOW_EMPTY variable.
[WARNING] LEF Cell 'fakera7_256x32' ignored. Matches GDS ALLOW_EMPTY.
[INFO] Checking for orphan cell in the final layout...
[INFO] No orphan cells
[INFO] Writing out GDS/OAS 'results/asap7/riscv32i/base/6_1_merged.gds'
Elapsed time: 0:03.01[h:]min:sec. CPU time: user 2.86 sys 0.15 (100%). Peak memory: 446068KB.
cp results/asap7/riscv32i/base/6_1_merged.gds results/asap7/riscv32i/base/6_final.gds
Log
Elapsed seconds
3_4_resizer 513
2_3_tdms_place 129
6_1_merge 181
5_2_TritonRoute 28521
3_1_place_gp_skip_io 131
2_4_mplace 9082
1_1_yosys 1951
5_1_fastroute 819
3_5_opendp 367
3_3_place_gp 2162
2_2_floorplan_io 150
6_report 2137
2_5_tapcell 147
1_1_yosys_hier_report 2436
2_1_floorplan 209
3_2_place_iop 146
4_1_cts 2045
4_2_cts_fillcell 125
2_6_pdn 147
```

## Timing report from 4\_1\_cts.log

**Elapsed time: 0:34.05**[h:]min:sec. **CPU time: user 33.93** sys 0.11 (99%). Peak memory: 296856KB.