DKK -> Salvin Or. & Dugar barrer Shivalal Aust Explain the addressing modes of 3051 with example Ans In 8051, thou we six types of addressing mode (1) Immediate addressing mode. (2) Register addressing mode. (3) Direct addressing mode. (4) Register Andisect adolessing made (5) Indexed Addressing mode. (6) Amplied Addressing mode. (1) Immediate addressing mode > In Immediate addressing mode data is provided immediately after the of code. examply > MOVA, # OAFH. MOV R3, # 45H; MOV DPTR, # FEOOH; In these instructions the # symbol is used for immediate data. (2) Register addressing mode - In the register addressing mode the source or distination data should be persent in a register (RO toR7). examples > MOVA, RS; MOV R2, #45H; MOVRO, A; Direct Addressing mode - In the direct addressing moder the source or destination address is specified by using &-bit data in the instruction. example MOV 80H, R6; MOVRZ, 45H' MOVRO, OSH;

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(4) Register indirect addressing mode - In this mode. the source or destination address is given inthe register The RD and RI are used for 8-bit addresses, and PPTR is used for 16-bit addresses, no other ougistors can be used for addressing purposes. example MOVOESH, GRO', MOV a DPTR, A; In the instruction, the regented is used for ougister indirect addressing. (5) Indexed addressing mode -> In the Indexed addressing mode, the source memory can only be accessed from program memon, only. eximply > MOVCA, GA + PC MOV CA, GA+ DPTR (6) Implied addressing mode -> In the implied addressing mode, there will be a single operand. These types of instruction can work on specific sugisters only. example - RLA: SWAPA', What is the 8051 operating clock constal frequency in MHZ.

Anso 12 MHz.

On =

What is the size of RAM and ROM in 8051? Ous -

305 1 micro controller is designed by Intel in 1981. It is an 8-bit mien Controller. It is built ceith 40 pins DIP (Dual inline package), 4KB of ROM storage and 128 bytes of RAM storage, 2 16-bit Homers.

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Ques- List the features and draw the block diagram of

Ans ->

Sos I micro controller is designed by Antel in 1981.

It is an 8-bit micro controller. It is built

with 40 pins DIP (Dual in line package), 4 kB of

ROM storage and 128 bytes of RAM estorage,

2 16-bit timers. It consists of are four parallel

8-bit ports, which are programmable as well as

addressable as per the veguinement. An on-chip

crystal oscillator is integrated in the micro controller

chaving crystal frequency of 12 MHz.

In the following diagram, the system bus Connects all the supporting derices to the CPU. The gystem bus Connects bus Consists of an 8-bit data bus, a 16-bit address bus and bus control signals. All other clinices like program memory, ports, data memory, serial interface, interrupt Control, simers, and the CPU are all interfaced together through the system bus.

Timer Country External 1 nde rouble 4KB INTO on-chip INTI 128 bytes ROM Intersupt K on-chip Input Timer (for program Control RAM Times 0 CPU OSC. Bus 4I oPort Contra +12+ Serial Post 4 50 30 MHZ Address Data TXD RXD

	Official
Grand C	oistource
COS	Micro Controller's Internal Blocks ->
6 6 5	CPU (ALU, Registous, Oscillator) (lock, Buscantoul) RAM (Dada memory ROM program memory I/o ports Timus (Orintors Serial ports Internifits.
(1 <u>us</u> -)	Discuss the Various SFRs of 8051.
frs∋	The Internal RAM or Data mimony of the 8051 micro Controller is divided into four hypes > Cremeral purpose vergisters, Bit addressable Registers, Register banks and Special function very sters or SFRS.
\$	The 8051 micro Controller Special function vegisteres our used to program and control different hardware peripherals like Timers, serial port, I/O ports etc. Out of these 128 memory locations (80H to FFH), there are Only 21 locations that are actually assigned to SFRs. Each SFR has one byte address and also a unique name which specifies like purpose.
=)	List of 8051 micro Controller special function vegistus -> A, B, DPL, DPH, IE, IP, PO, P1, P2, P3, PCON, PSW, SCON, SBUF, SP, TMOD, TCON,

TLO, THO, TLL, THI

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	Nome of the Regist	
	A or Acc	Accomulator
2,	B	B Register (for Arithmetic)
3,	DPH	Addressing external memory.
4,	DPL	Addressing external memory.
S,	IE	Internift Enable Control.
6,	IP	Internity building.
7,	PO	Posit O latch
8,	PI	Port 1 lateh
9,	P 2	Port 2 latel.
10,	P 3	Port 3 lateh.
11:	PCON	Power Control
12,	PSW	Program Status word.
13,	SCON	serial Port Control.
14,	SBUF	Sprial part data buffer.
15,	SP	stack pointer.
16,	TMOD	Times Country Mode Control
17,	TCON	Times Country Control.
	TLO	
19.	THO	Times a Low byte.
	TL1	Timer of high byte
21.	TH1	Timer 1- lous byte
X	Y	Timer 1 high byte.
extra Just	classify the di	Afterint group of SFR's of sost micro controlling
Ansa	The 21 Speci	al function exogéstere are categorized
	into person	armite The step sters are rategorized
(1)	Math or CPU	Rogistures: A B
(2)	Status Roomster	: PSW (Program states (word)
(3)	Pointy Repietes	Derna (Pringram strikes (word)
	-giste	s; DPTR(Dada pointer - DPL , DPH), and
(4)	TID hard A-	SP (Stack Pointer)
(1)	110 bost 70.	Trus - 10 P2 P3.
		$\frac{\text{Speckeron to}}{\text{(Posto) (Posts) (Posts)}}$

	Date / / Page No Shivalal
(5)	TMOD, IE and IP.
(6)	Peripheral Oata Registers; TLO, THO, TLI, The and SBUF.
M(1)=	(arite on 805) morrow to add the Contents of

R5 of beark 3 to R3 of beark 1. Save the result dus write a program to copy the value of Ro of banko to Ro of Bank 1, R1 of Bank 2 and R2 of

Banks

		Pag	ge No. Shivalal
Mus =	Exploiin the RAM	structure of 8051	in detail?
	addressable memony vegristers), another succepisters) area. Ou bit - addressable SF	one for viegistus locations, stacks (pout is the SFR (Specio t of these 21 locations R locations.	panks bit general purpose I function
/	2051 provides four	register bank.	
	Address Range	Regrister Bank	
	00H to 07H	Rigistin Banko	
	08H to 0FH	Register Bank 1	
	10H to 17H	Register Bank 2	
	18H to 1FH	Register Bank 3	
20	Right Bank area	rgenization coll OTH OTH OTH LOHI 18H	Register Register Register Register Register Register Register
4	M		benk3

			Date / / Page No. Shivalal	- (
	A vegister bank			+
	RO			7
	R1.			
	R2			
	R3			
	R4			
	RS			_
	R6		•	
	R7			
				_
7	X		XXX	_
(Iwa	Explain the difference	e beh	ween Micro processor & Micro Contro	-6
Anna	Micro processor		pi'cro contrally	Lu.
Lis .		hore the	. At is a Controlling device	
-	memory and Ilo cor	nponent	wherein the memory and	
	are connected exte	mally	. I/o component are present internally.;	
			· ·	ج
4	The circuit us comple	ex due	(4+ is present on chip)	
	to external co	mechan	. Is The circuit is less Complex.	
1.		<u> </u>	124+ cam be used us ith a	
7:		n compac	panfact system.	=
1	system.	1	> 9+ is efficient.	
<u></u>	It is not efficien	1.	31 43	
		r) Be is of		
L,	registers.	this floor	4 It does not have a zero	
	It has a zerosta	0.09	is It does not have a zero estatus flag.	
L	41	used in	4 94 is generally used in	
			trashing machines - and	_
	personal Computers		washing machines, and air conditioners.	_
				_

		Shivala
(w *	Explain the pin diagram in defail? and draw it	of 8051 micon Comball
	in defail? and draw it	2
•		
Ans 0)	8051 micro Controller ha	o to pins. the pin dia
	of sos 1 micro Controller do	oks as follows >
	P1-0 -1	40 Vec
	P1.1 = 2	30 PO.0
	P1.2 = 3.	327 PO-1
	P1.3 =4	37D PO.2
	P1.4 FS 8051	36 PO·3
	P1.5 46	35 PO.4
	P1.6 47	347 PO.S
	P1.7 = 8	337 PO-6
	RST 19,	32 PO-7
	(RXD) P3.0 = la,	317 EA NPP
2	(TXD) P3.1 [11]	30 ALE PROU
	INTO) P3-2 [12.	297 PSEN
()	INTI) P3-43 [13]	
	(TO) P3.4 - 14.	28] P2.7 (A15)
	(T1) P3.15=15.	27 7 /2.6 (A14)
	(WR) P3-6 = 16	267 P2.5 (A13)
		257 P2.4 (A12)
		247 P2-3 (A11)
	XTALZ 18	23 P 2.2 (A10)
	XTALLE 19	22 P2-1 (A9)
	(1HD = 20	21 J P2-0 [A8]
	19	

· Pins 1 to 8 -> These pins are formounds Port 1.
This port does not serve any other functions.

· P.ing -> It is a RESET pin, which is used to
Reset the micon Controller to its initial value.)

· Pin 10 to 17 -> These pins are bronon as Port 3.

This port serives some functions like interrupts,

timer in put, Control sognals, Serial Communication

- Signals RXD and TXD.

· Pins 18 & 19 -> These fins are used for interfacing on external crystal to get the system clock.

· Pin 20 - This pin provides the power Suppley to the Circuit. (GND)

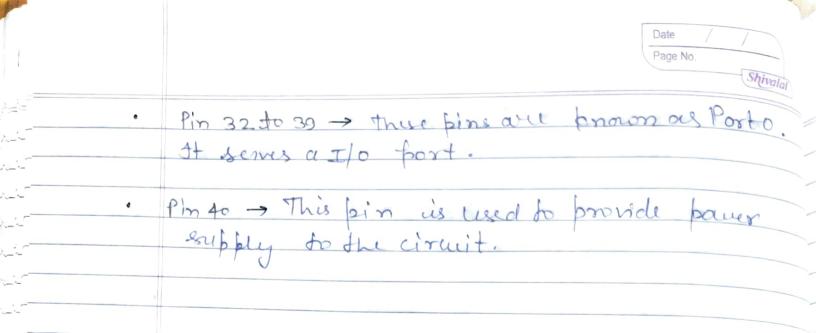
Pins 21 to 28 -> These pins are fanon as Port 2. ic.

It serves as I/O port.

Pin 29 → This is PSEN pin which stands for forgram store Enable. It is used to read a signal from the external forgram memory.

Pin 30 -> (EA) => This is EA pin which stands for external access imput. It is used to enable stable the memory infer facing.

Pin31 -> This is ALE pin, which stands for Address latch Enable. It is used to dimultiplex the address - data signal of port.



Minos-3 Syllabus -> · Micro Controller 3 RAM Structure (Bank 1, Bank 2) A Sevial Communication or Port -> Explain. ddocssing mode.