VLSI LAB

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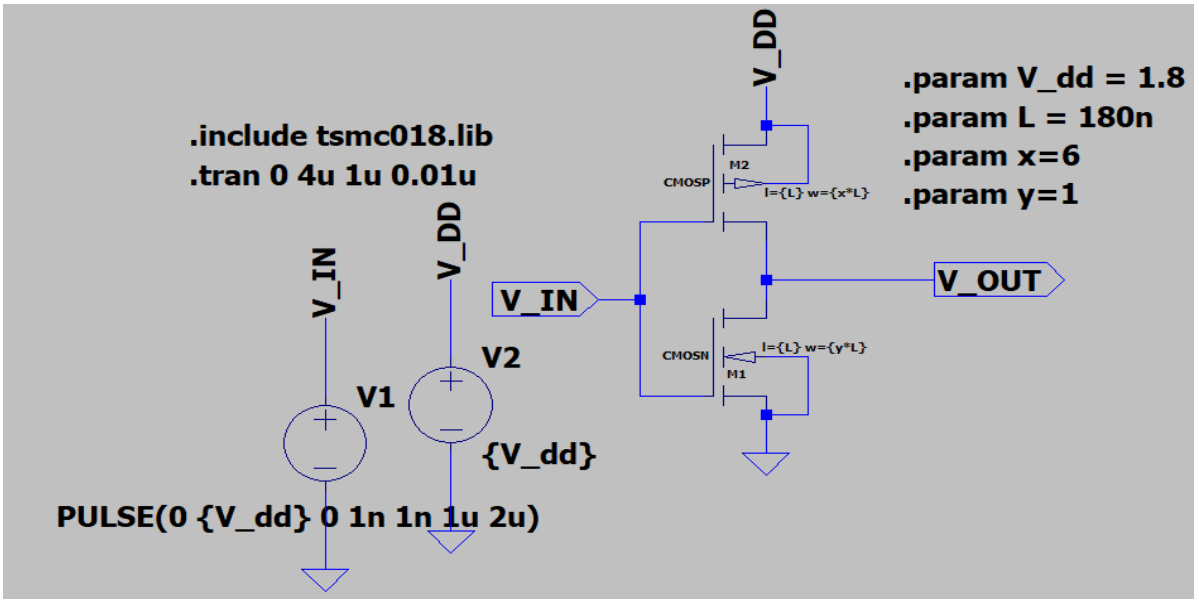
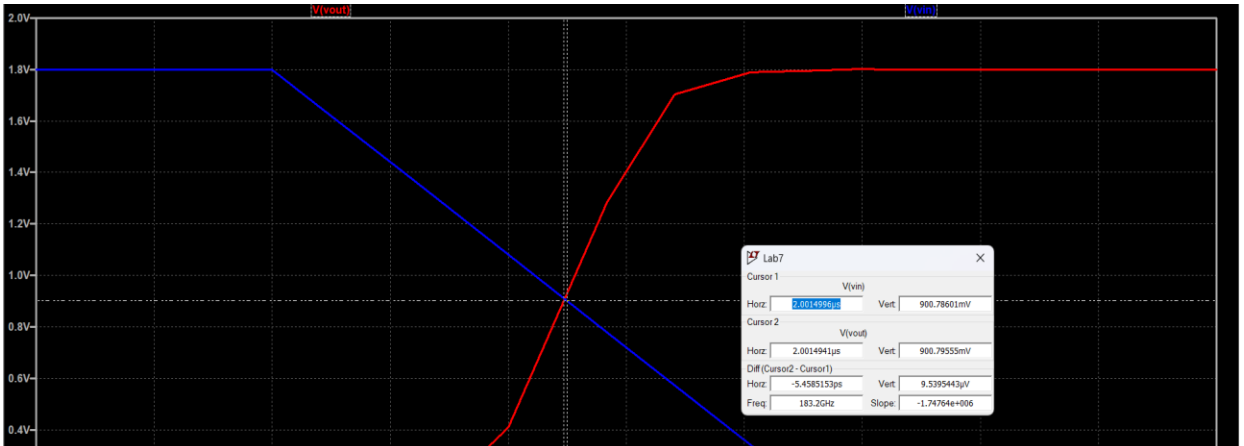
Objective 1:

- *Design an inverter chain to drive a load capacitance of 10 pF. Find the input capacitance of the stage-1 inverter and then design the chain such that the overall propagation delay is minimum.*

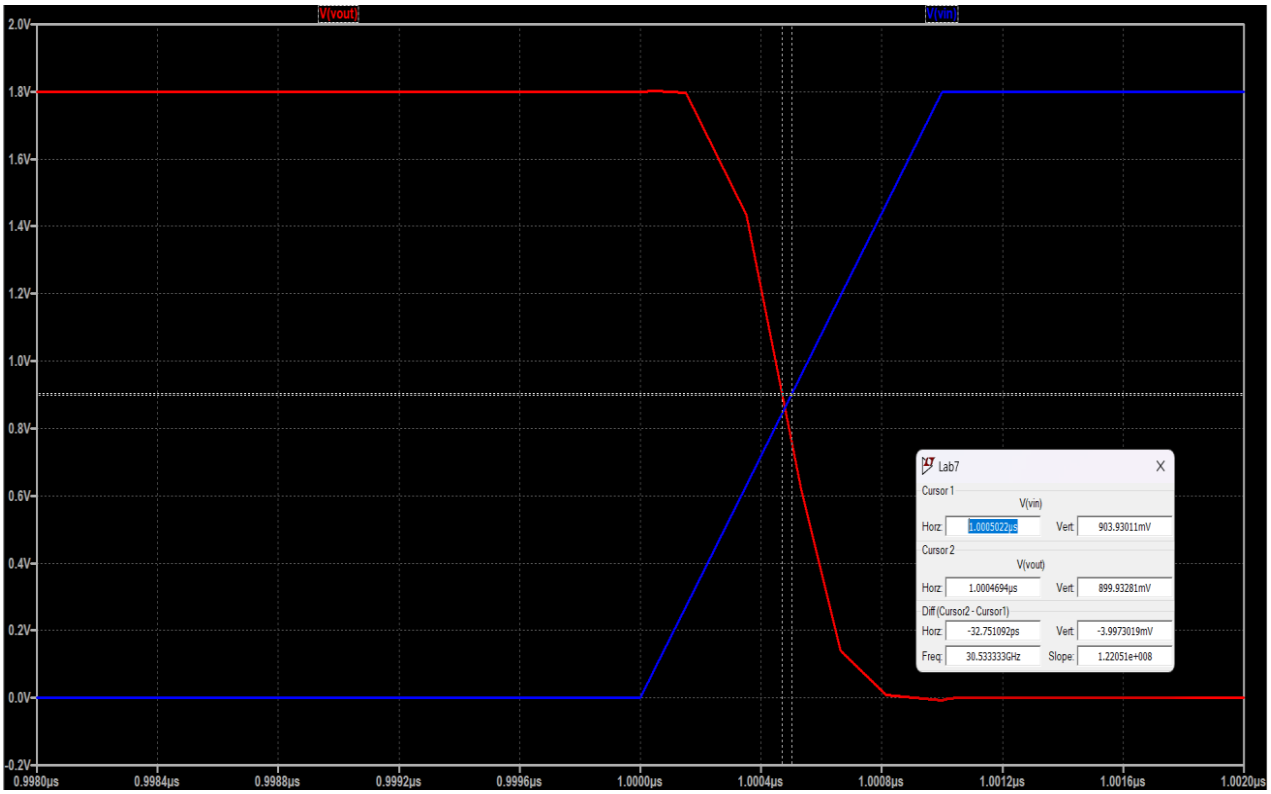
Circuit Diagram:



Stage – 1 CMOS inverter without external capacitor



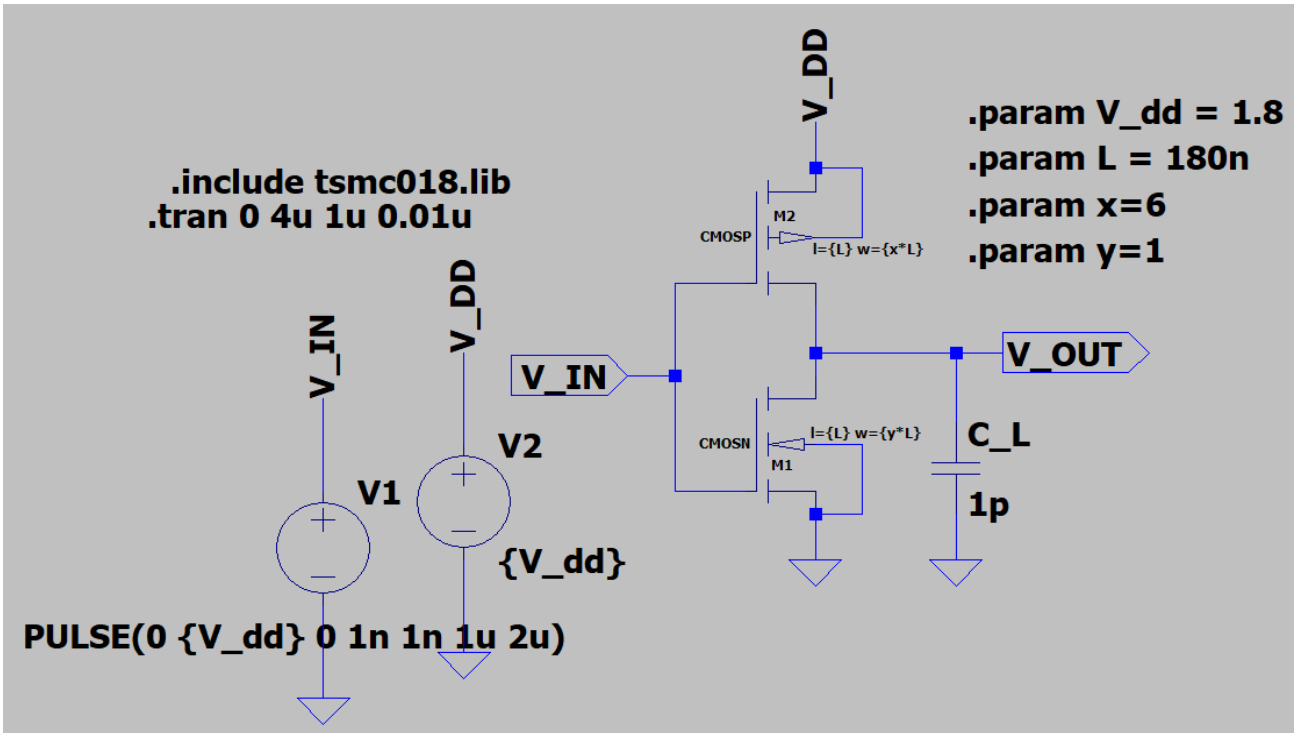
Propagation delay low to high (T_{PLH} = 5.4585153ps)



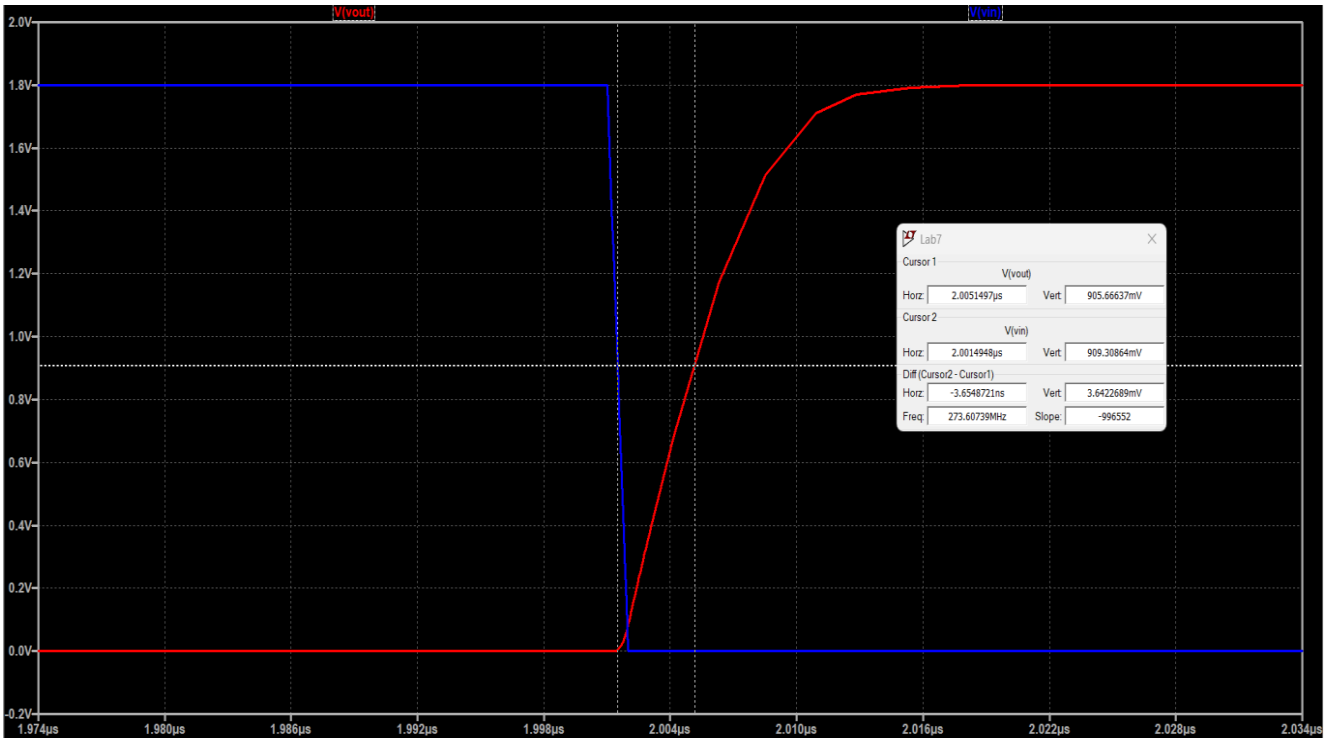
Propagation delay high to low (T_{PHL} = 32.751092ps)

Intrinsic delay (T_{p0}) = (T_{PLH} + T_{PHL})/2 = 19.1048035ps

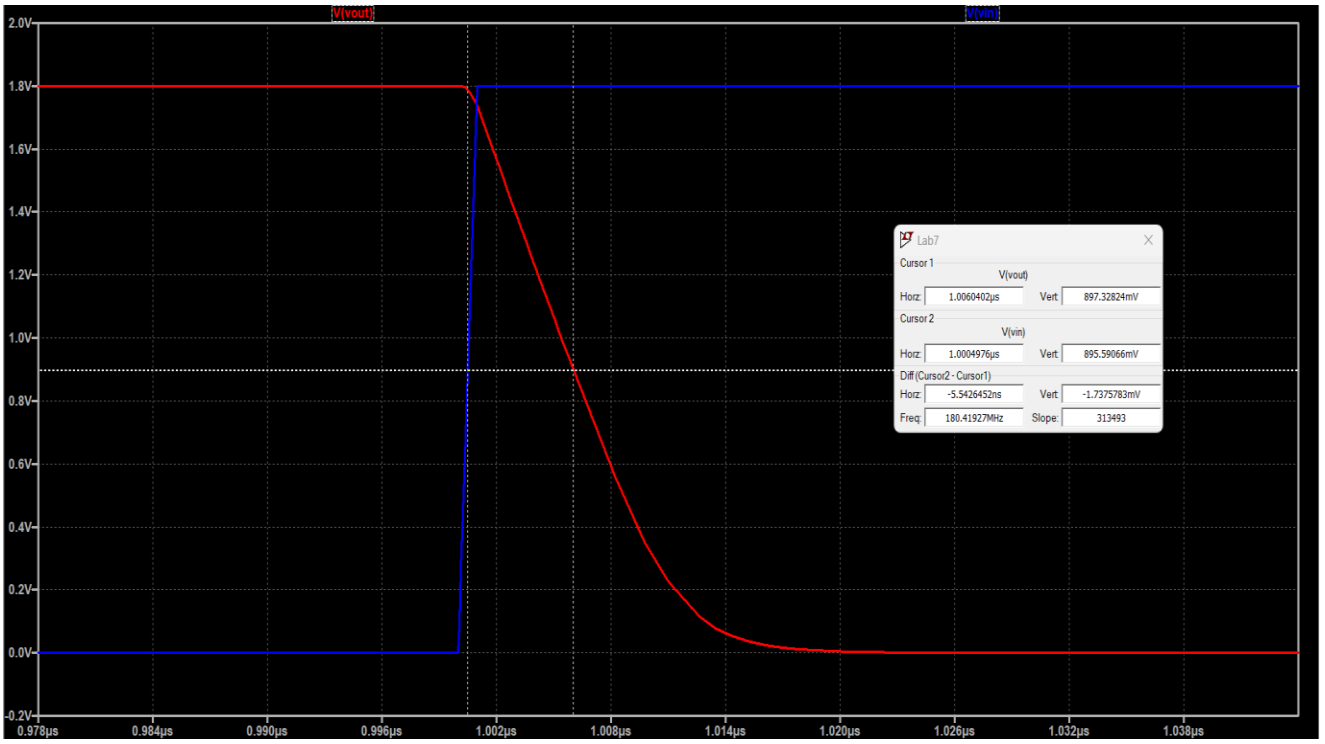
Circuit Diagram:



Stage – 1 CMOS inverter with external capacitor of 1pF



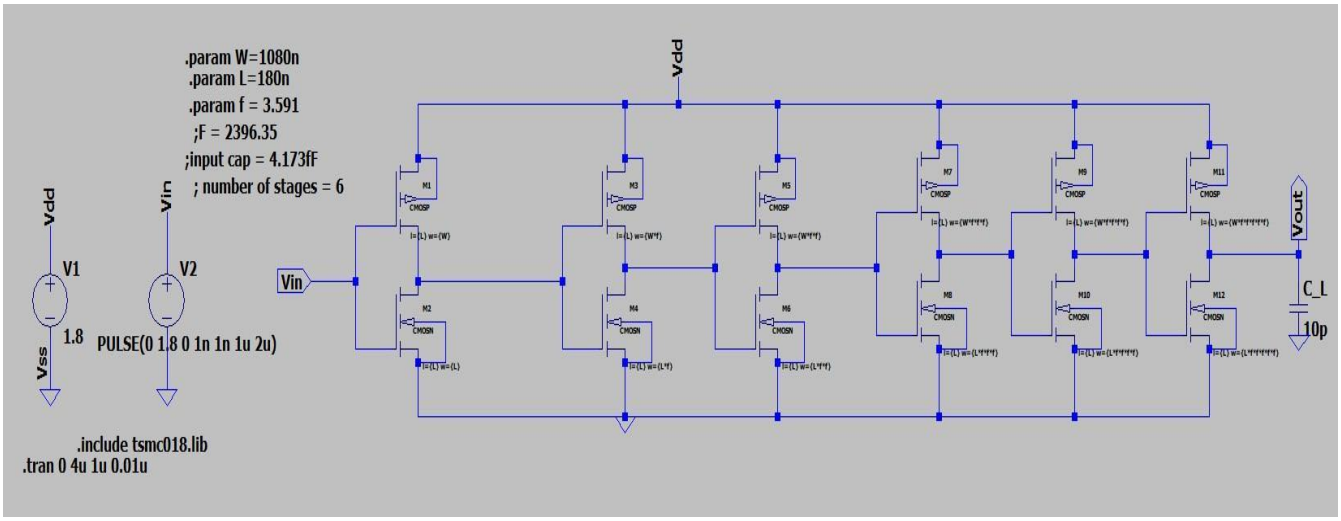
Propagation delay low to high (T_{PLH} = 3.654872ns)



Propagation delay high to low (T_{PHL} = 5.5426452ns)

Propagation delay (T_p) = (T_{PLH} + T_{PHL})/2 = 4.5987586ns

Circuit diagram:



CMOS Inverter chain with load capacitance of 10pF

Input Capacitance of CMOS inverter ***(C_{in}) = 4.171669 fF***

external capacitance ***(C_L) = 10pF***

Overall fanout ***(F) = C_L / C_{in} = 2396.35***

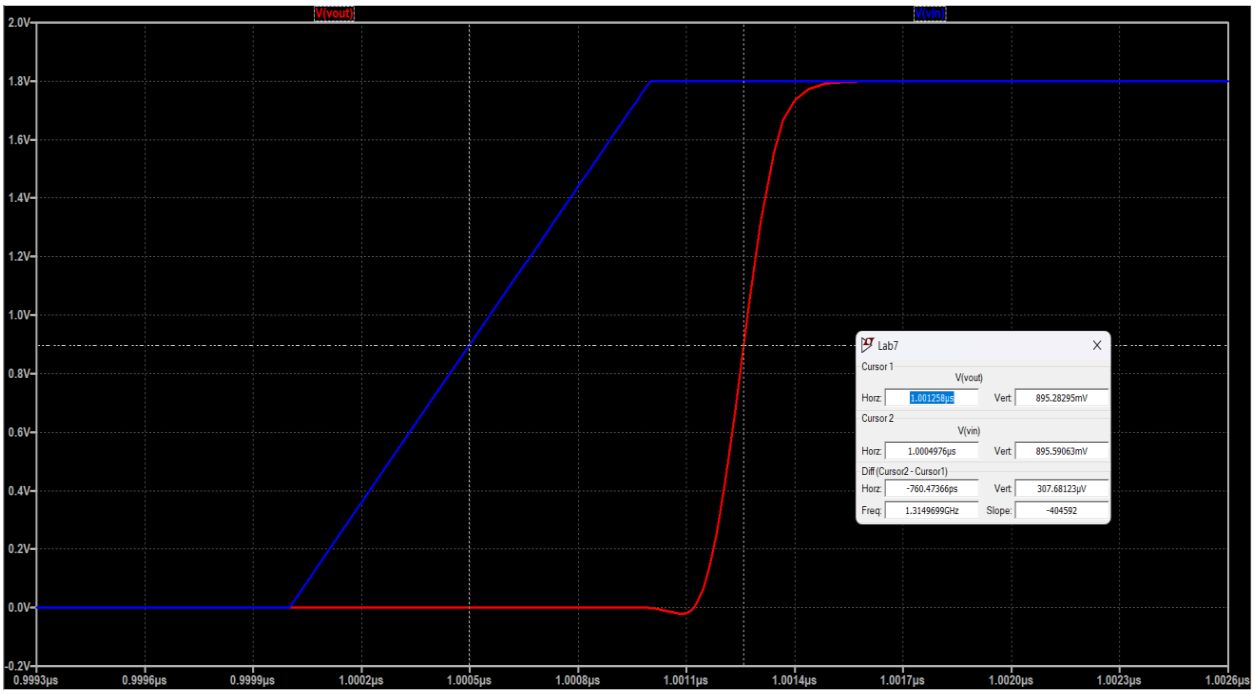
Since γ = 1, single stage effective fanout ***(f) = 3.591***

Number of stages, ***N = ln(F)/ln(f) = 6*** *(integer value) [Since $F = f^N$ for minimum delay]*

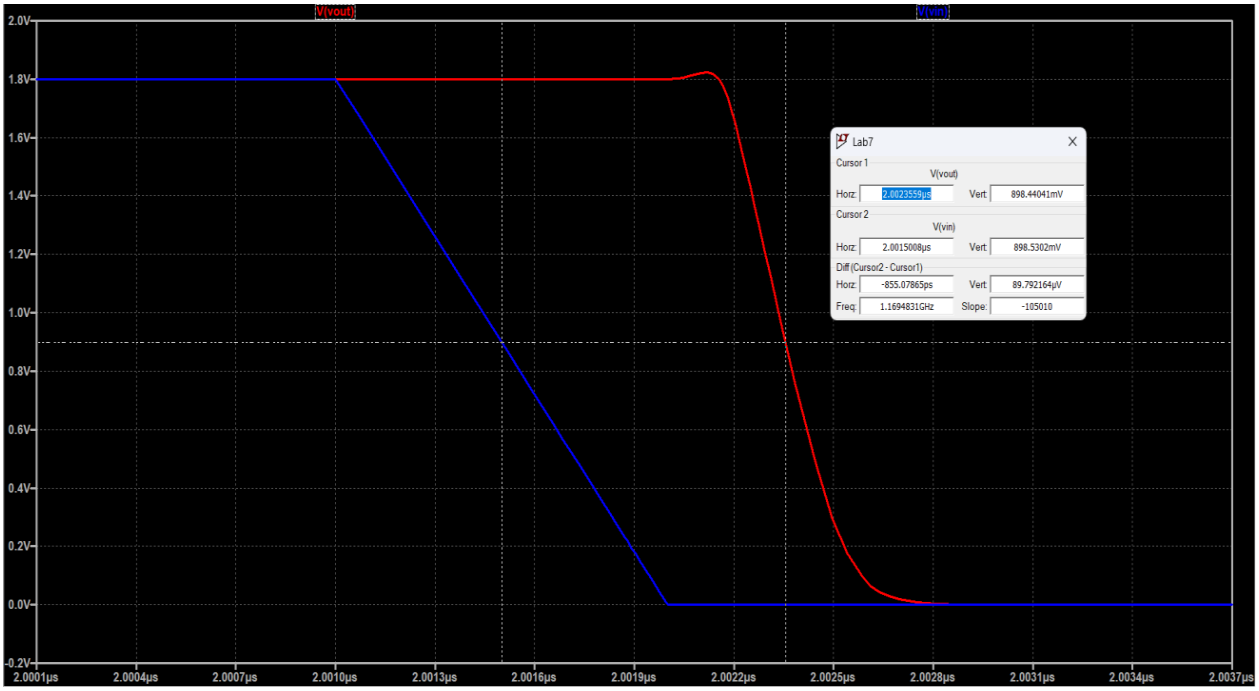
Sizes of each inverter:

The lengths of all the MOSFETs of all stages in the CMOS inverter chain are same and equal to 180nm.

Stage of CMOS inverter	***PMOS width (nm)***	***NMOS width (nm)***
1	*1080*	*180*
2	*1080 * f*	*180 * f*
3	*1080 * f^2*	*180 * f^2*
4	*1080 * f^3*	*180 * f^3*
5	*1080 * f^4*	*180 * f^4*
6	*1080 * f^5*	*180 * f^5*



Propagation delay low to high (T_{PLH} = 760.47366ps)

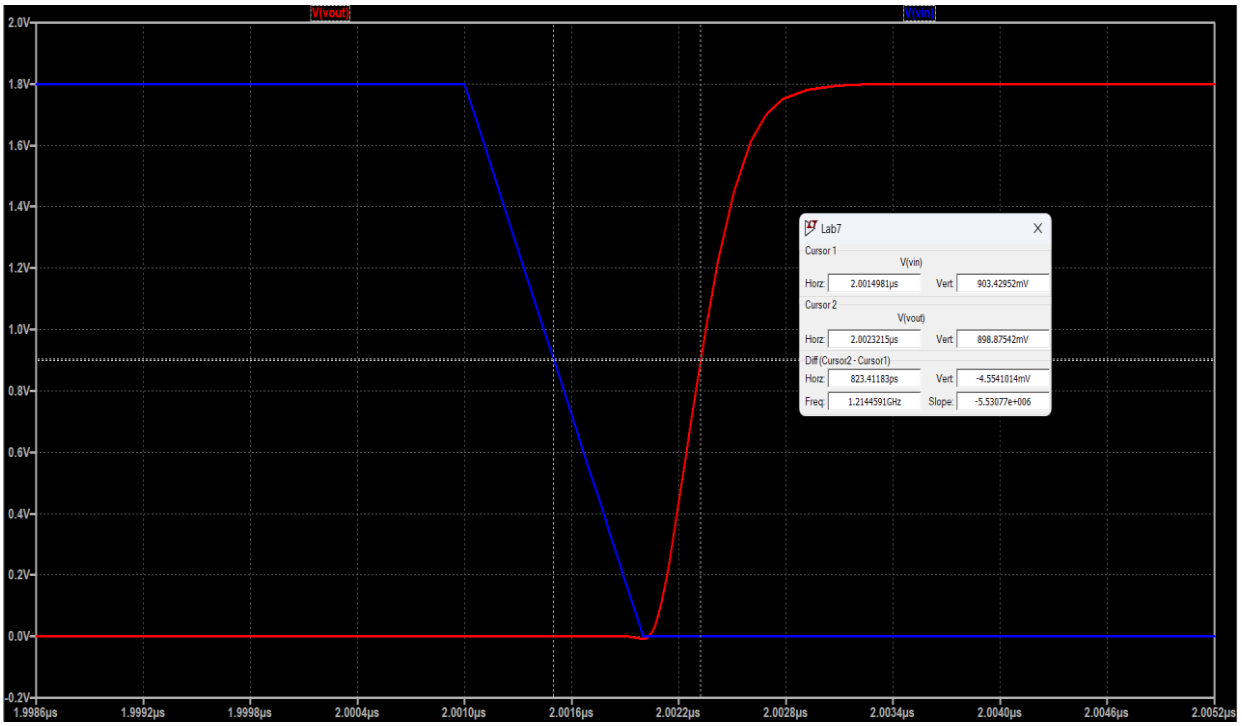


Propagation delay high to low (T_{PHL} =855.07865ps)

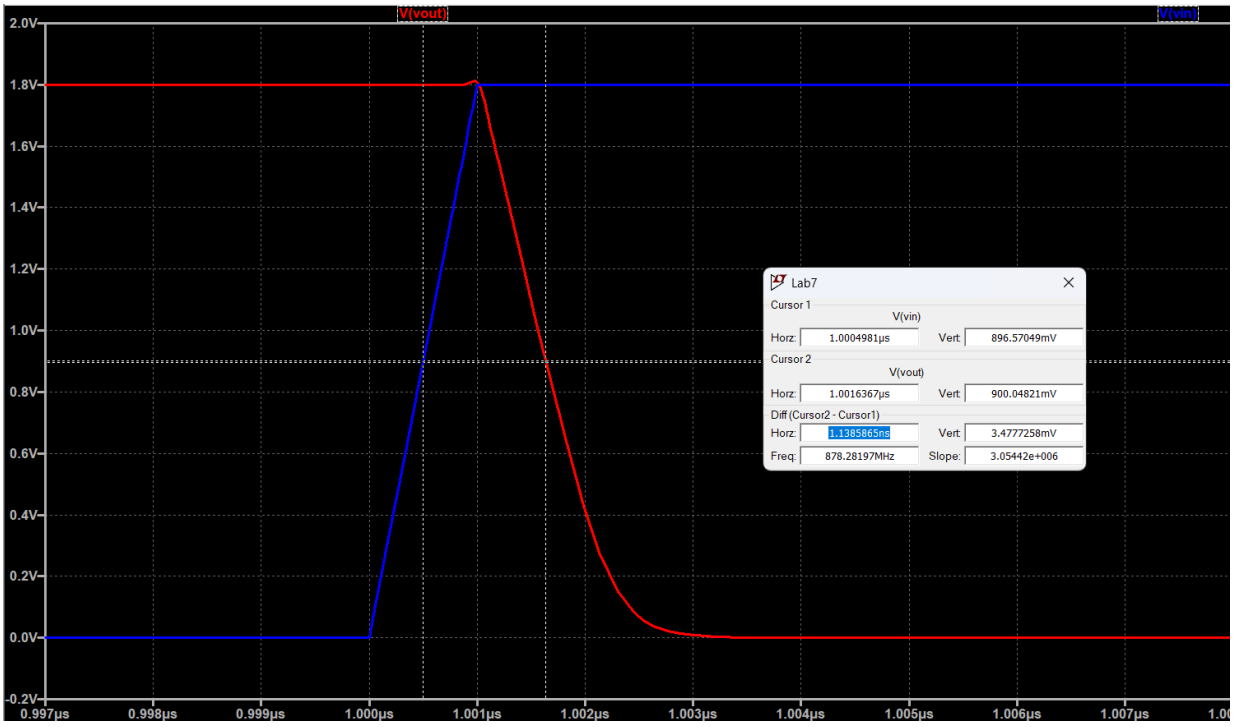
Minimum total delay of CMOS inverter chain (T_p) = (T_{PLH} + T_{PHL})/2 = 807.77613ps

- *To conform whether the obtained N (number of CMOS inverters) value (which is 6 according to our obtained plots and calculations) is optimal or not for obtaining minimum delay, we have checked for cases N = 5 and N = 7 and found the total delay of inverter chain.*

For 5 stage CMOS inverter chain:



Propagation delay low to high (T_{PLH} = 823.41183ps)

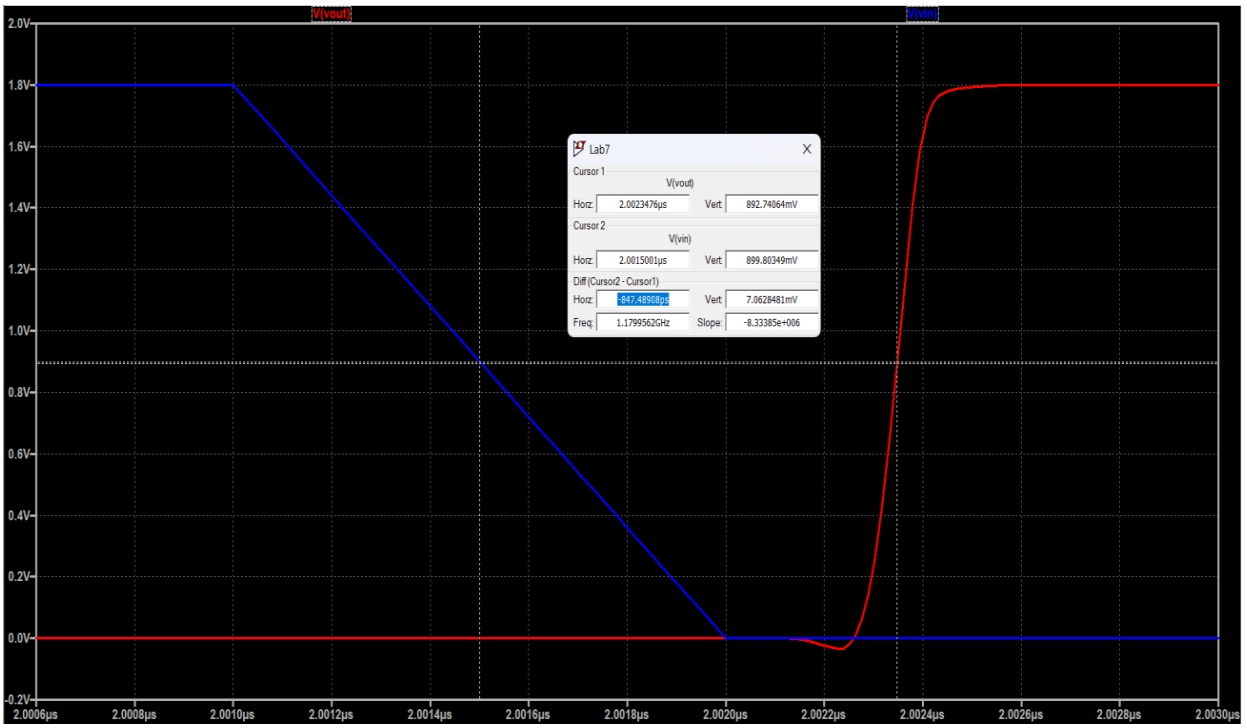


Propagation delay high to low (T_{PHL} =1.138586ns)

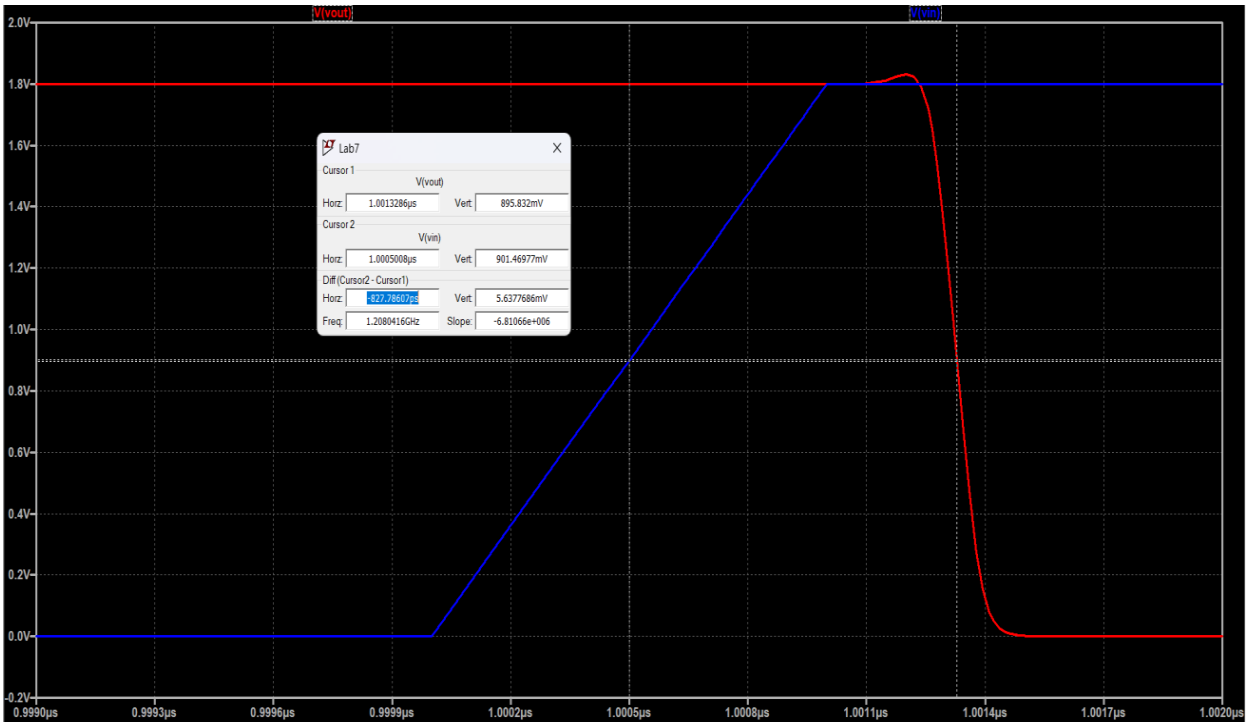
Propagation delay (T_p) = (T_{PLH} + T_{PHL})/2 = 980.9985ps

 which is greater than 807.77613ps (Minimum total delay of CMOS inverter chain).

For 7 stage CMOS inverter chain:



Propagation delay low to high (T_{PLH} = 847.48908ps)



Propagation delay high to low (T_{PHL} = 827.78607ps)

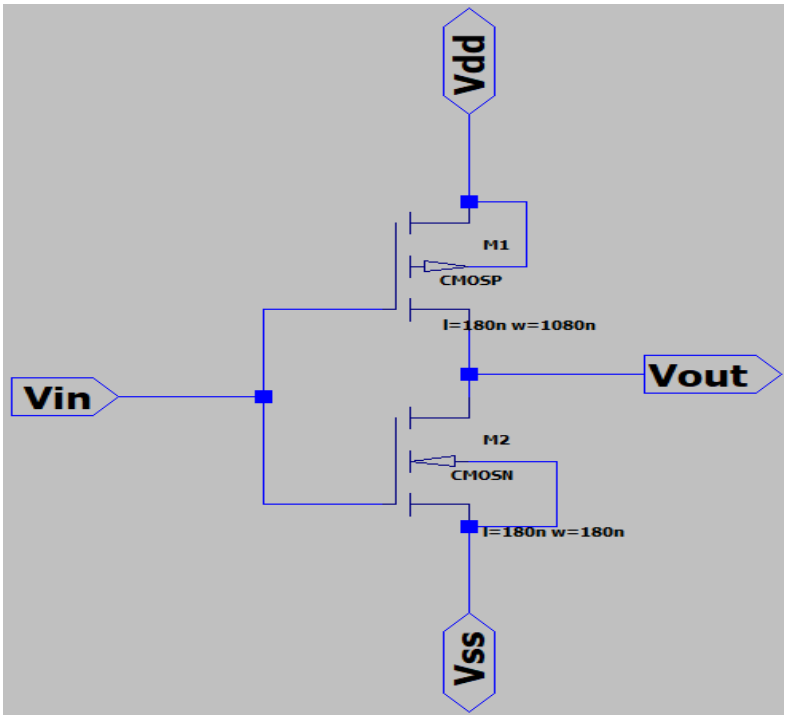
Propagation delay (T_p) = (T_{PLH} + T_{PHL})/2 = 837.637575ps

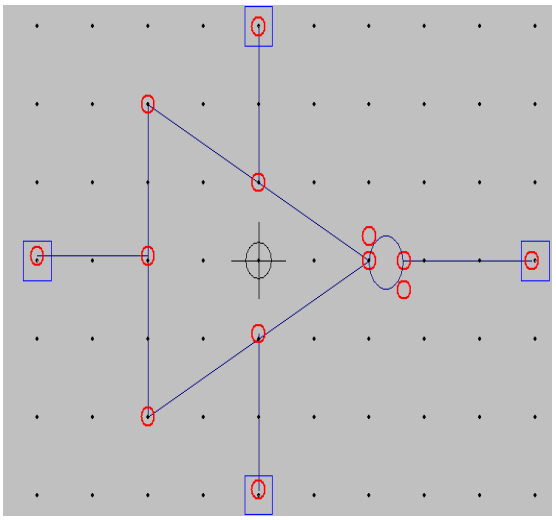
 which is greater than 807.77613ps (Minimum total delay of CMOS inverter chain).

Objective 2:

- *Design a ring oscillator (having 5 or 7 stages). Estimate the oscillation frequency (f) of the ring oscillator. Show that, f = 1/(2*n*tpd), where, n is the number of stages, tpd is the delay of a single inverter.*

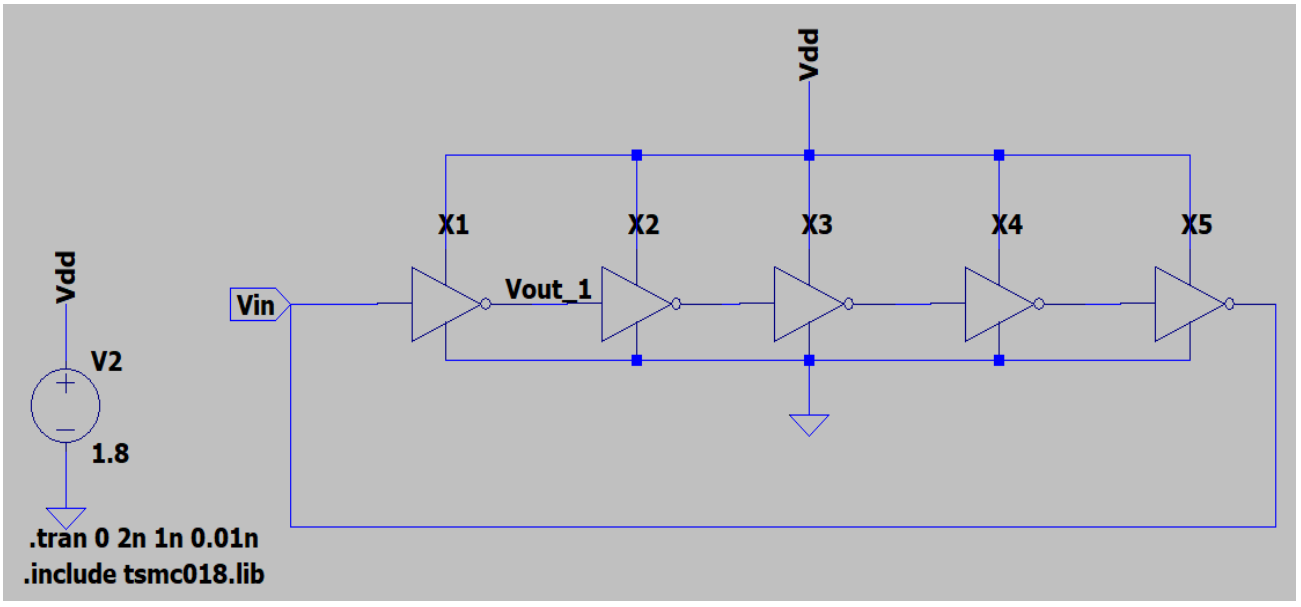
Circuit Diagram:

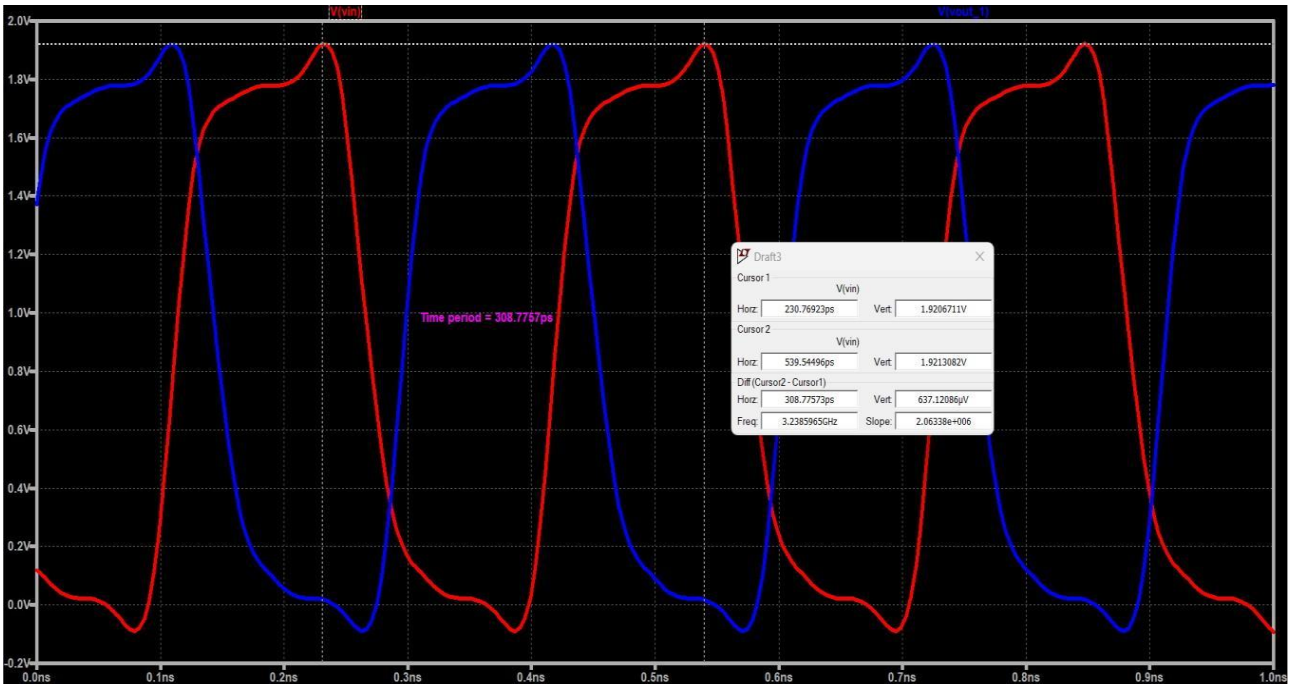




We have designed a LT spice schematic symbol for CMOS inverter with the sizes of the MOSFETs as said in objective (at which we get symmetrical VTC curve) with parameters Vin, Vout, Vdd, Vss.

Ring oscillator of 5 identical CMOS inverters





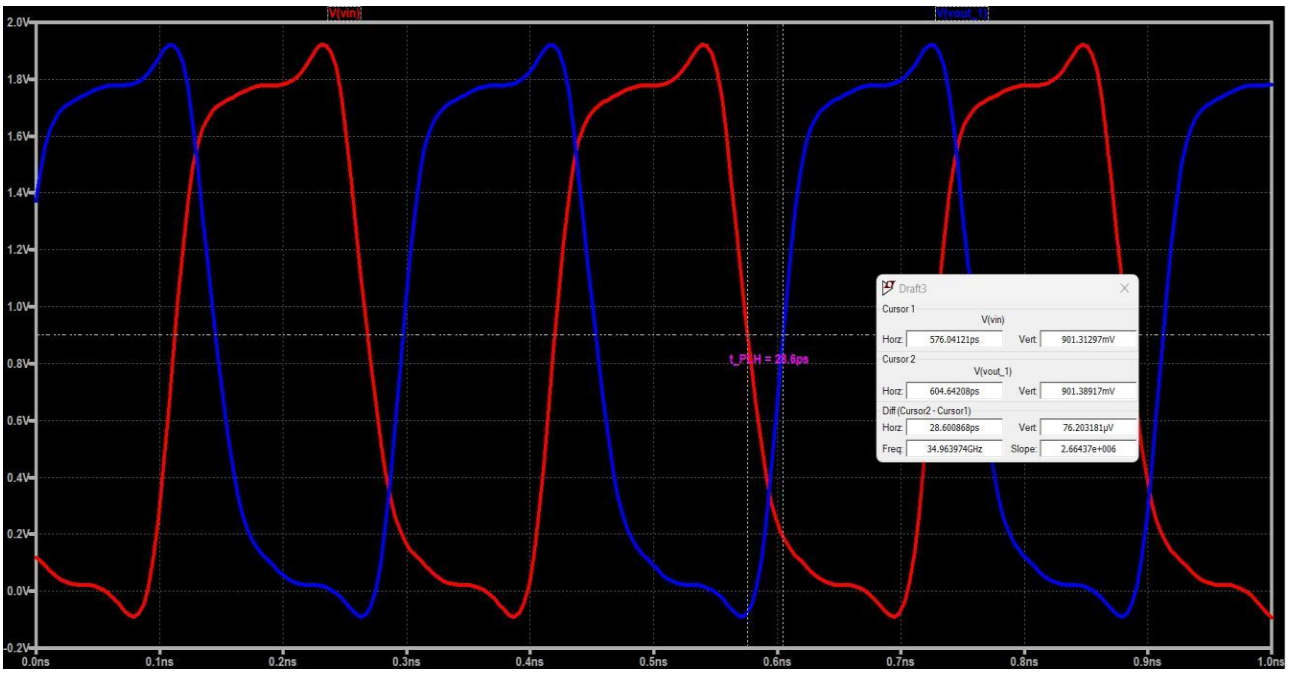
Oscillation period (T) = 308.7757ps

Frequency of ring oscillator = 1/T = 3.2386 GHz

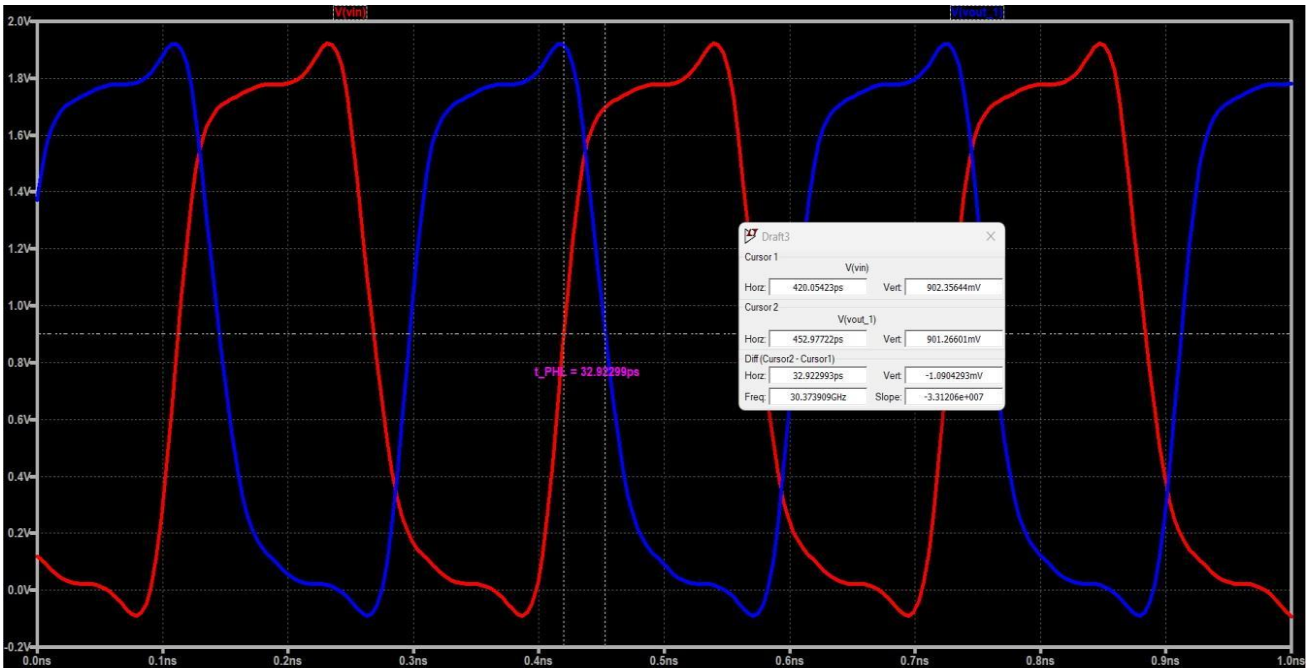
Number of stages (N) = 5

*Theoretical value delay of the single stage (T_s) = T / (2*N) = T/10 = 30.87757ps*

- *For verifying this we plotted output of the first inverter X1 (Vout1) which is now a single stage and measured propagation delay (T_p).*



Propagation delay low to high (T_{PLH} = 28.600868ps)



Propagation delay high to low (T_{PHL} = 32.922993ps)

Propagation delay (T_p) = (T_{PLH} + T_{PHL})/2 = 30.76193ps

Simulated value of delay of single stage (T_p) = 30.76193ps

*Percentage of error = {(T_s – T_p) / (T_s)} * 100 = 0.3745 %*

Discussions:

Objective – 01

a) *To find the input capacitance (C_{in}) of an inverter, we first calculated the intrinsic delay (T_{P_o}) of the inverter without connecting any load capacitance. Then, we connected a load capacitance (C_{ext}) at the output terminal and calculated the total propagation delay (T_P). The input capacitance (C_{in}) is then calculated using the above equation.*

b) *The Input Capacitance (C_{in}) of our designed CMOS inverter comes out to be 4.171669 fF.*
c) *A load capacitance of 10 pF is present at the output terminal of the CMOS inverter chain.*
d) *Let f_i be the fanout of i^{th} stage of inverter in a chain of inverters having N stages. We have, $F = f_1 f_2 \ldots f_N$.*
e) *For maximum performance, i.e., minimum delay, we should have $f_i = f_j \; \forall \, i, j$.*

Let us say, for maximum performance, $f_i = f \; \forall \, i$. We have, $\boldsymbol{F = f^N}$.

Objective – 02:

a) *A **ring oscillator** is a device composed of an odd number of NOT gates in a ring, whose output oscillates between two voltage levels, representing true and false.*
b) *The NOT gates, or inverters, are attached in a chain and the output of the last inverter is fed back into the first.*
c) *A circular chain composed of an even number of inverters cannot be used as a ring oscillator. The last output in this case is the same as the input.*
d) *However, this configuration of inverter feedback can be used as a storage element, it is the basic building block of static random-access memory (SRAM).*
e) *In a ring oscillator, because a single inverter computes the logical NOT of its input, it can be shown that the last output of a chain of an odd number of inverters is the logical NOT of the first input.*
f) *The final output is asserted a finite amount of time after the first input is asserted and the feedback of the last output to the input causes oscillation.*

g) *To increase the frequency of oscillation, we can either make the ring from a smaller number of inverters (with about the same power consumption) or we can increase the supply voltage, which increases the current consumed, thereby reducing the time to charge the load capacitance and hence the propagation delay through the chain of stages, increasing the frequency of the oscillation.*

h) *In a physical device, no gate can switch instantaneously. In a device fabricated with MOSFETs, for example, the gate capacitance must be charged before current can flow between the source and the drain. Thus, the output of every inverter in a ring oscillator changes within a finite amount of time after the input has changed.*

i) *Let us have 'N' NOT gates, each having a propagation delay of* T_d*. Suppose at t = 0, we have 0V at the output, which is also input to the chain of inverters. So, output of the first stage at t =* T_d *is 1V, output of the second stage at t =* $2T_d$ *is 0V, and finally, output of the* N^{th} *stage at t =* NT_d *is 1V. This 1V at the output again requires* NT_d *time to reach the output as 0V. Thus, we obtain the total Time Period of the Ring Oscillator =* $2*N*T_d$