VLSI LABORATORY [EC39004]
LAB REPORT - 6

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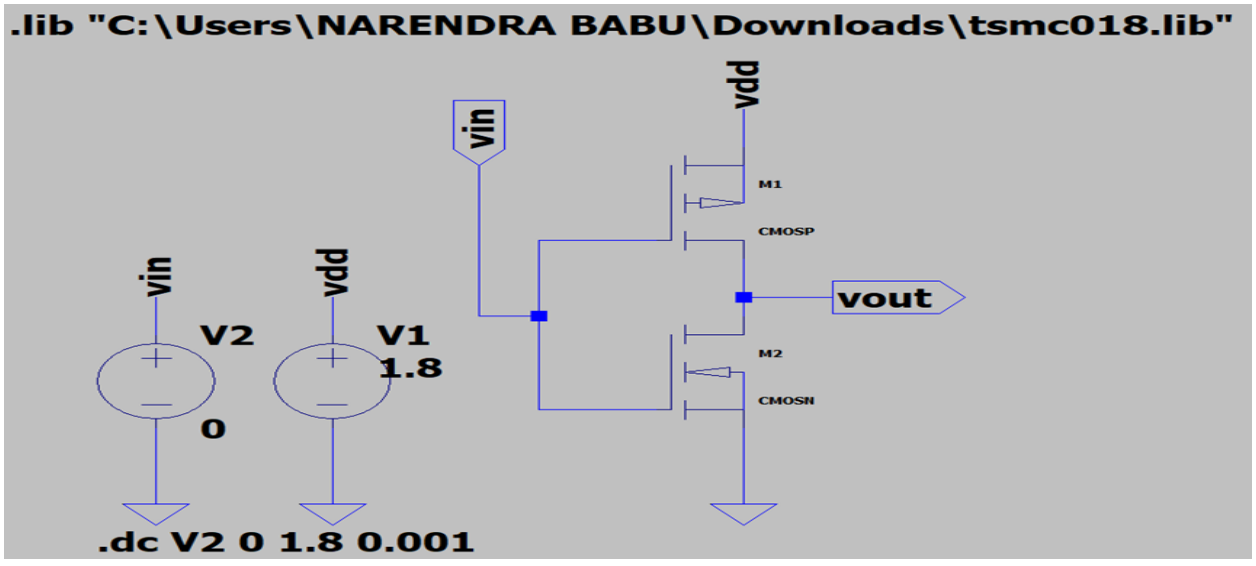
Objective-1:

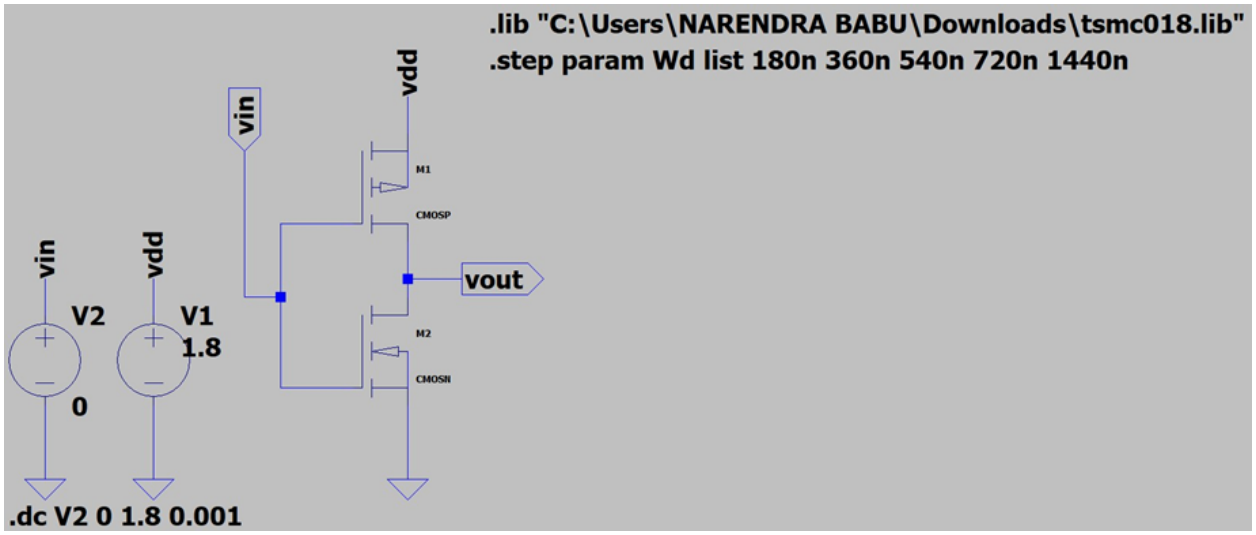
Design a CMOS inverter and plot its VTC using LTSpice. Investigate the effect of PMOS and NMOS widths on the VTC and the switching threshold. What is the impact of VDD on the VTC (check even when VDD < |VTh|)? Plot the current characteristics of a CMOS inverter.

Circuit Diagrams:

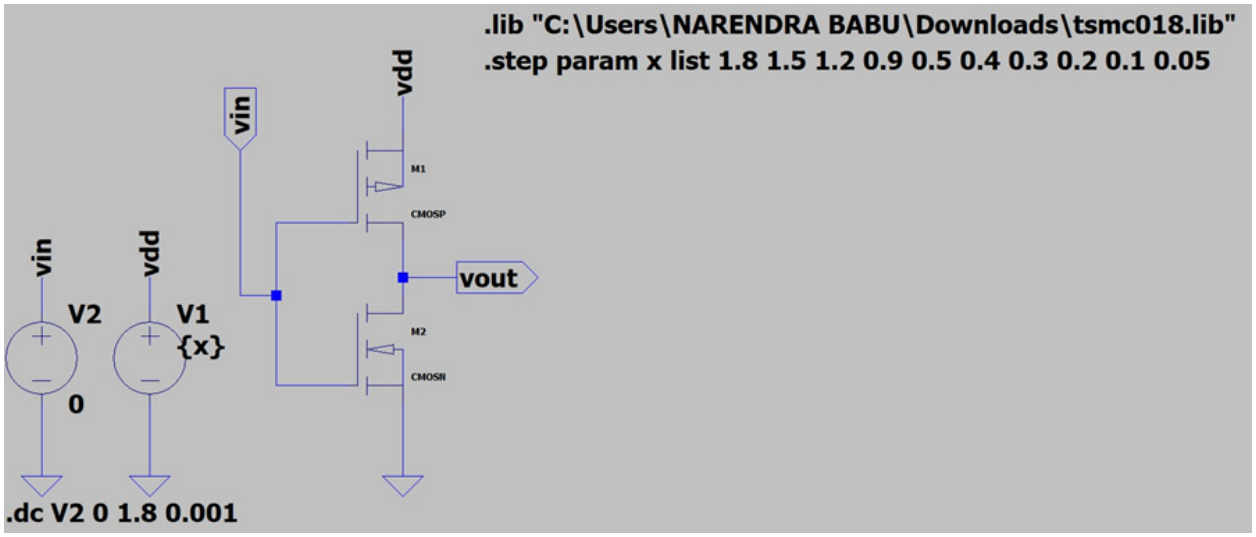
a)For plotting the VTC



b)For investigating the effects of PMOS and NMOS widths on the VTC and the switching threshold

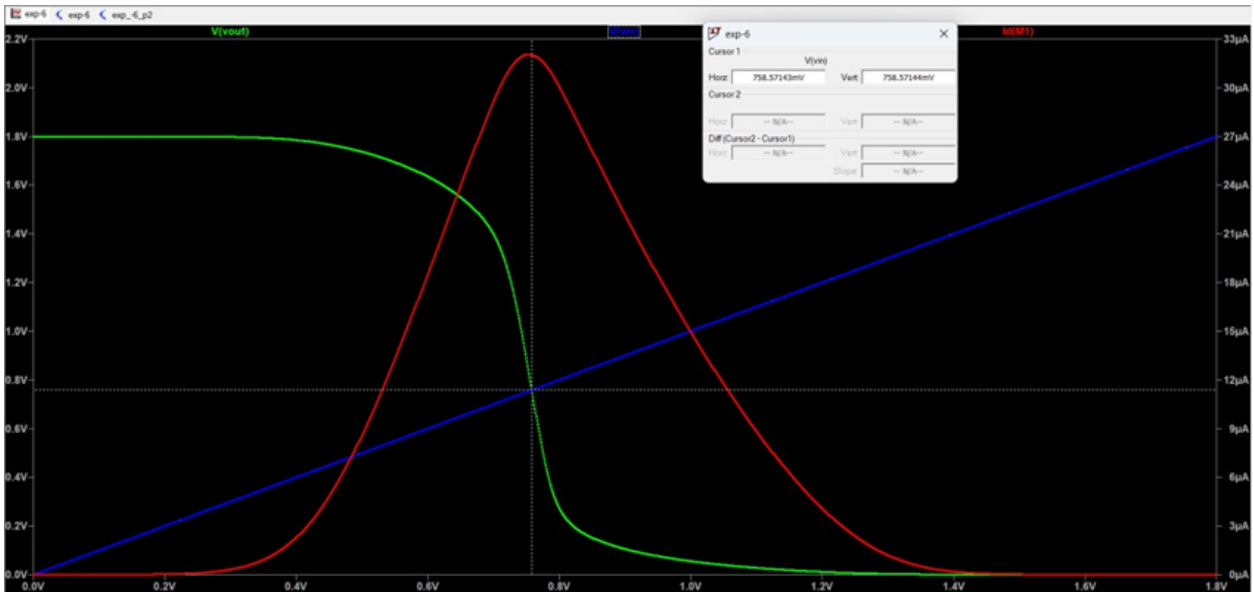


c) For checking the impact of VDD on the VTC



Plots and Observations:

a) Plotting the VTC of the inverter

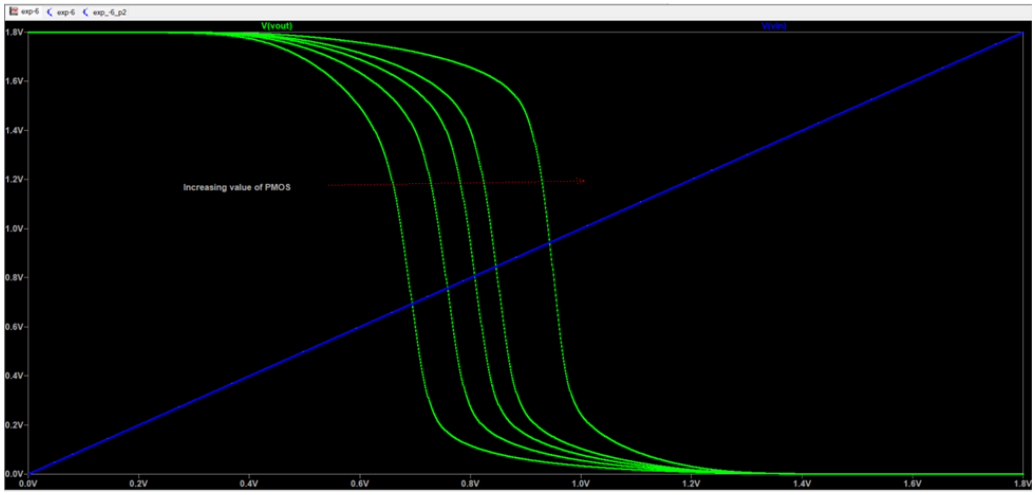


· *The PMOS width = 360 nm and NMOS width = 180nm*

· *We can see that for these widths the VTC is not symmetric, that is, the switching threshold voltage is not at 0.9 (=vdd/2)*

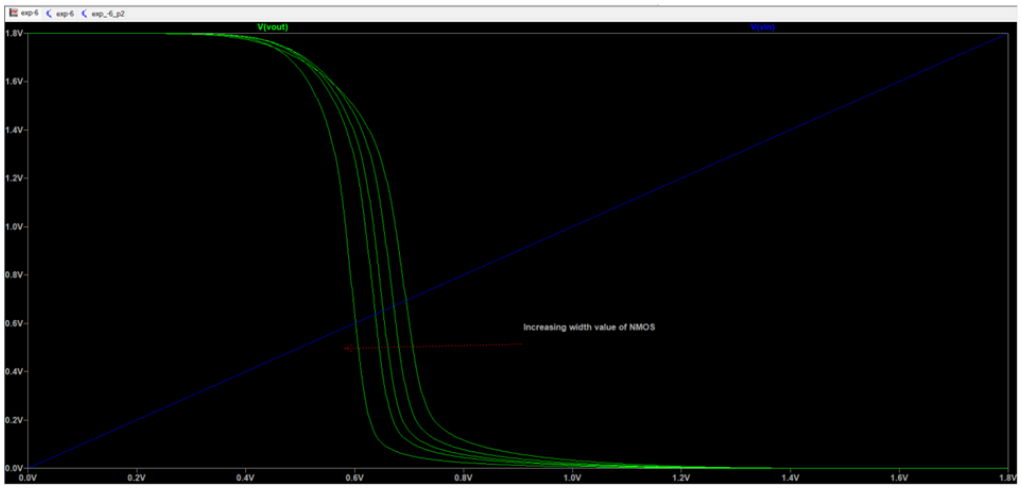
·*The current characteristics of the inverter are also plotted here and we observe that the Short-circuit current is maximum at the switching threshold voltage*

b)Effect of device widths on the VTC and the switching threshold



· *The NMOS has been fixed to 180nm while the PMOS width is varied*

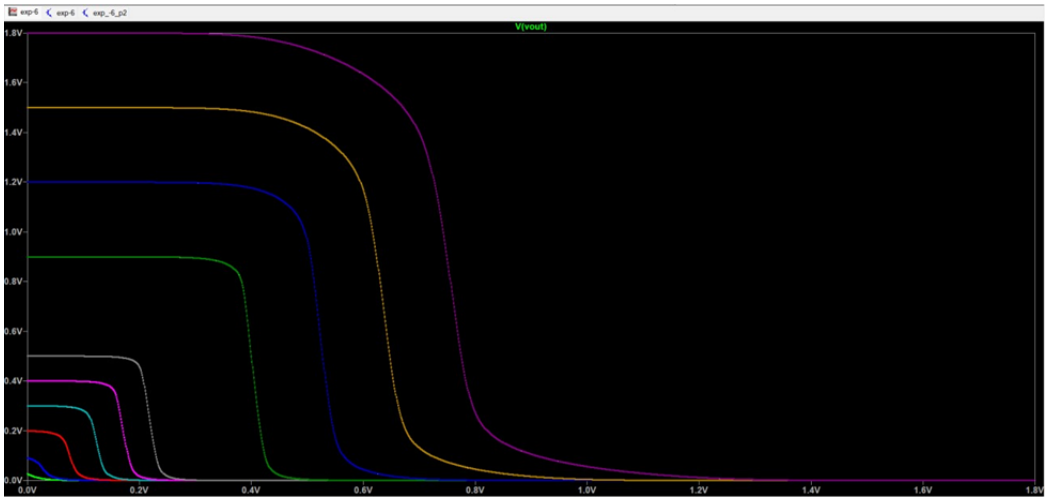
· *Increase in width of the PMOS is making the VTC shifts to right*



· *The PMOS has been fixed to 180nm while the NMOS width is varied*

· *Increase in width of the NMOS is making the VTC shift to left*

c) Impact of VDD on the VTC



· *We can see that decreasing Vdd leads to shrinking of the VTC in both dimensions*

· *The inverting behavior is retained even when Vdd < |Vth| because of subthreshold conduction*

·*But Vdd below 0.1V (Vdd < 0.1V), we cannot see the inverting property.*

· *We also observe that the gain in the transition region increases as we decrease Vdd*

·*But below a certain point, the gain in the transition region start falling again*

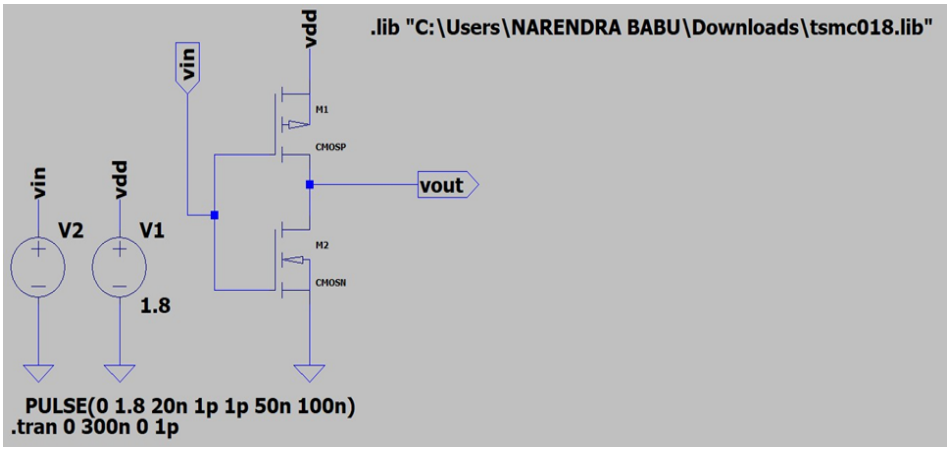
· *Due to the shrinking of the VTC, we can say that the noise margin of the inverter keeps decreasing as the VDD decreases.*

Objective-2:

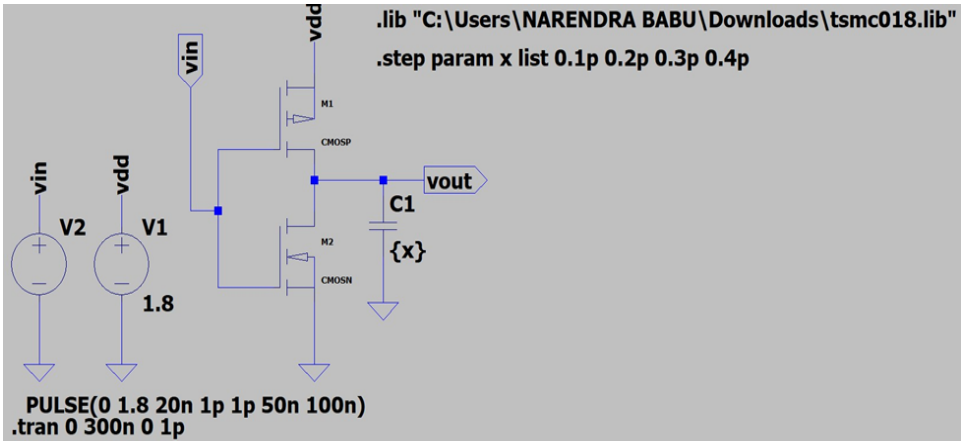
For the CMOS inverter, estimate its propagation delay when no load is connected. Examine the effect of the PMOS/NMOS ratio on the propagation delay. Find the PMOS/NMOS ratio for which the delay is minimum. Now, could you connect a variable load capacitor at the output node and investigate the delay?

Circuit Diagrams:

a)Circuit for estimating and checking the impact of PMOS/NMOS ratio on propagation delay without a load capacitor

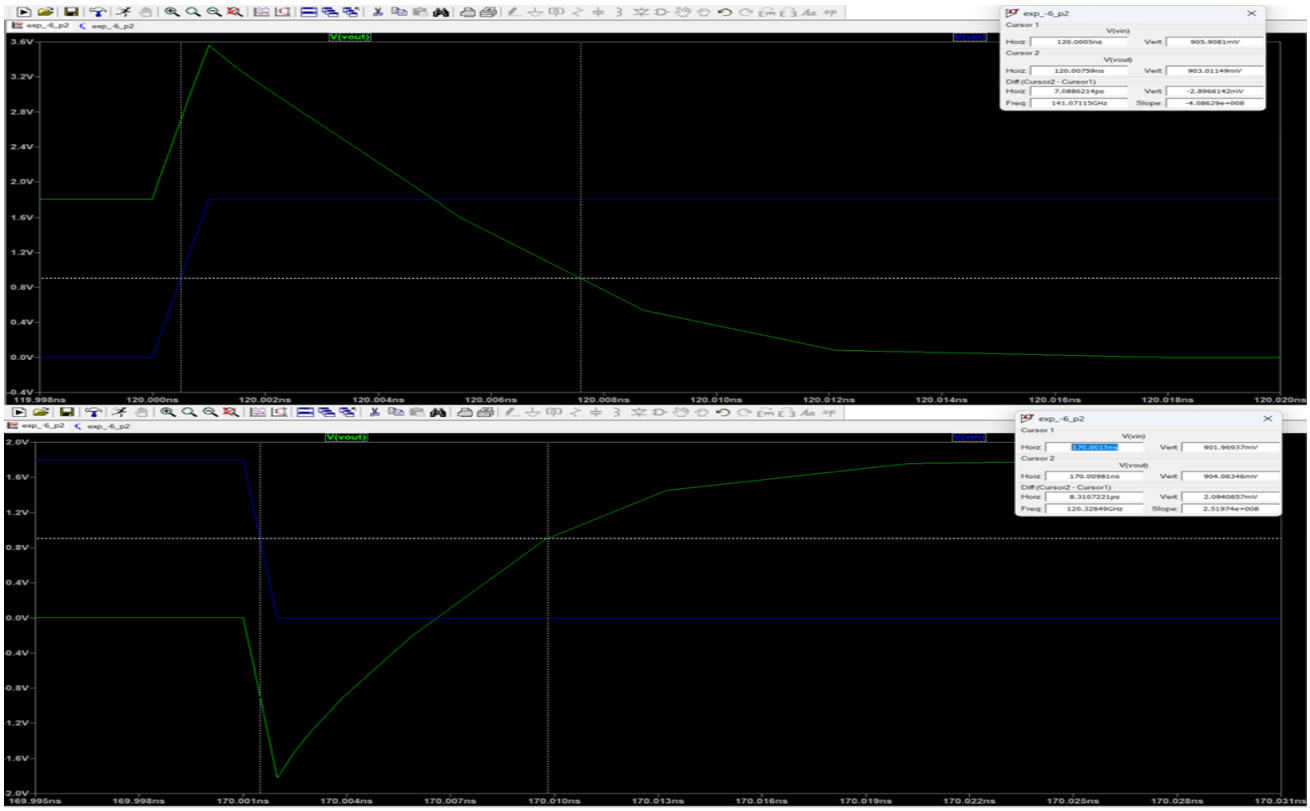


b)Circuit for observing the impact of a load capacitor on the propagation delay



Plots and Observations:

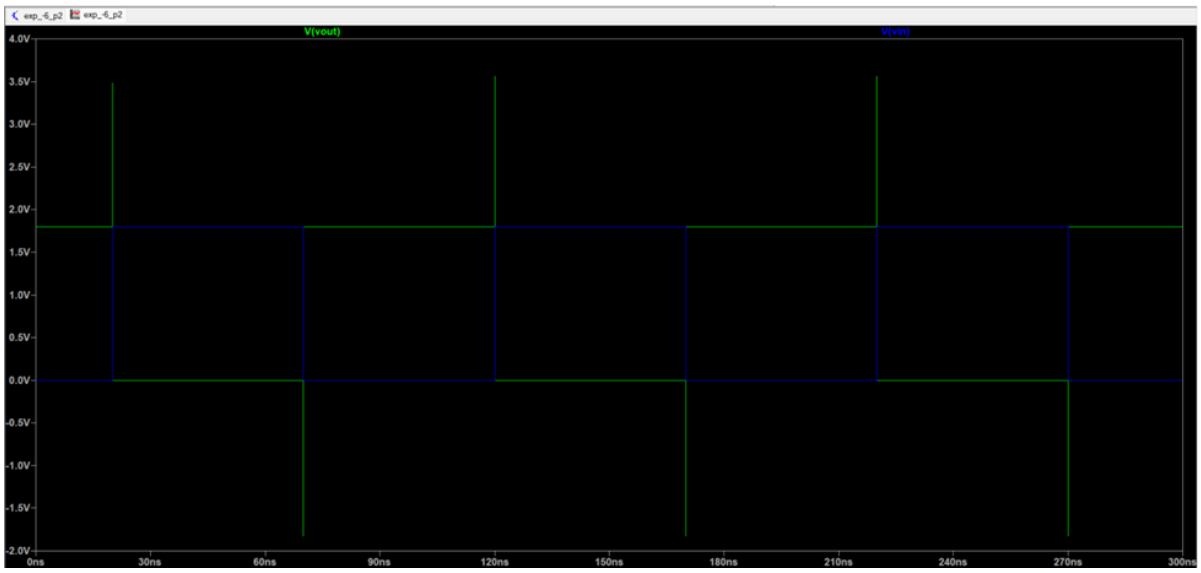
a)Plots for estimating the propagation delay without any external cap:



· For the above experiment we have taken Wp = 360 nm, Wn = 180 nm and Lp = Ln = 180nm.

· *In the above plot blue signal represents the input signal and the green signal represents the output signal.*

· *We know that propagation delay is defined as the average of time difference between input low to high and output, time difference between input high to low and output when they are vdd/2*
· *The time delay for input low to high (tlh) = 7.08ps and the time delay for input high to low (thl) = 8.31ps*
· *From the above plot we can say that the time delay for the given CMOS inverter is average of tlh and thl [(tlh + thl)/2] = 7.695ps.*
· *Now even if we change the W/L ratio of the PMOS or NMOS, the intrinsic time delay won't change (there will be very small change)*
· *We can observe some kinks (small peaks as shown in below figure) at the positive edges in the output signal.*



b) *Plots for observing the impact of external cap on tp:*

·*W and L values of the PMOS and NMOS are made as before. Red output signal represents cap 0.1pF, 0.2pF, 0.3pF, 0.4pF respectively.*

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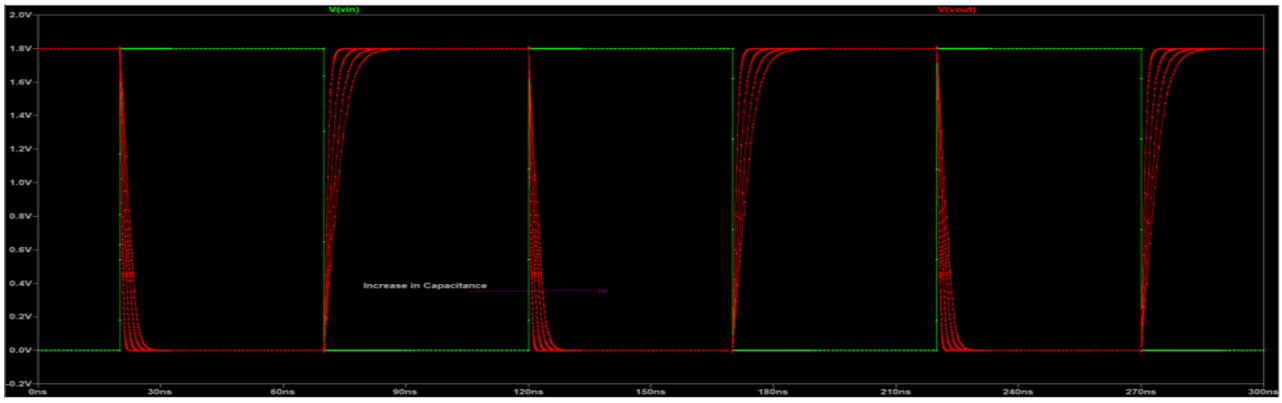

Therefore, from the above plot we can say that as the external capacitance increases, time delay will also increase because cout increases and, Tp = 0.69(Reqp + Reqn)*cout/2.*

Discussions:

<u>Objective-1:</u>

· Initially we took Wp = 360 nm, Wn = 180 nm and Lp = Ln = 180nm, for these values, the switching threshold (Vt) is around 0.758V, so to get a symmetric VTC we need to shift our VTC to right.

·The switching threshold (Vt) will increase if Kp > Kn, i.e., VTC will shift right side if Wp increases, and Vt will decrease if Kp < Kn, i.e., VTC will shift left side if Wn increases.

· At Wp = 1160 nm, Wn= 180nm, the switching threshold Vt = Vdd/2 (remaining all dimensions are the same).

·The short circuit current through the inverter is maximum at Vt, because at this point both PMOS and NMOS are in saturation and a direct current flows between VDD and GND.

·This current is the reason for the short circuit power loss and it is around 30uA, when Vdd = 1.8, but if you decrease the Vdd, then this current will also decrease, which decreases the power dissipation.

·Even when Vdd goes below Vth, we will get some current in the order of pA, which is referred to as the subthreshold leakage current. This current lets us still obtain inverter action.

Objective-2:

·Even without any external capacitor, we will be having some propagation delay in our output due to the self-capacitance of the CMOS inverter. This delay is also known as intrinsic delay
· The intrinsic delay of a CMOS inverter is given by the expression: Tp = 0.69(Reqp + Reqn)*Cself/2.*

·The intrinsic delay of an inverter is independent of the W/L ratio of PMOS or NMOS. Because Cself is directly proportional to W/L and Req is inversely proportional to W/L, they cancel each other

· In the propagation delay plot we can observe that there are kinks (small peaks), at both the positive and negative edges of the output signal, i.e., output voltage goes above Vdd and goes below 0 V, for a small interval.

· If we increase the rise and fall time in the input signal, then there will be some time for the voltage across the cap to change and hence the peaks amplitude will decrease.

· As, you increase the external capacitance of the inverter, the C_{out} will increase and hence propagation delay will increase