VLSI LABORATORY [EC39004]
LAB REPORT - 8

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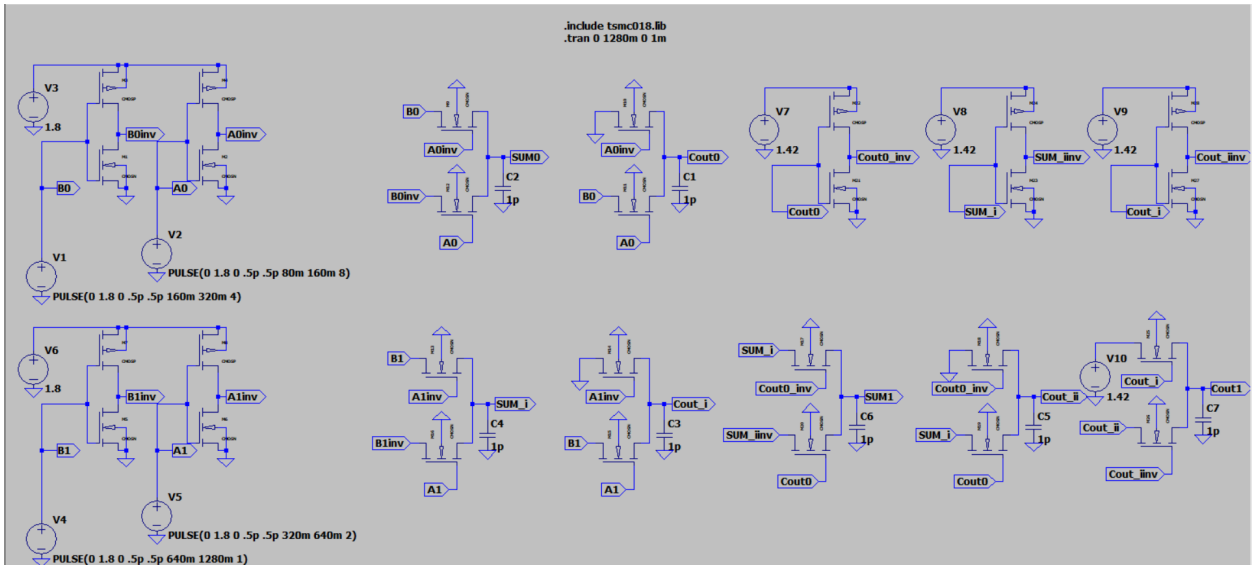
OBJECTIVE:

1) Implement 2 bit adder using pass transistors

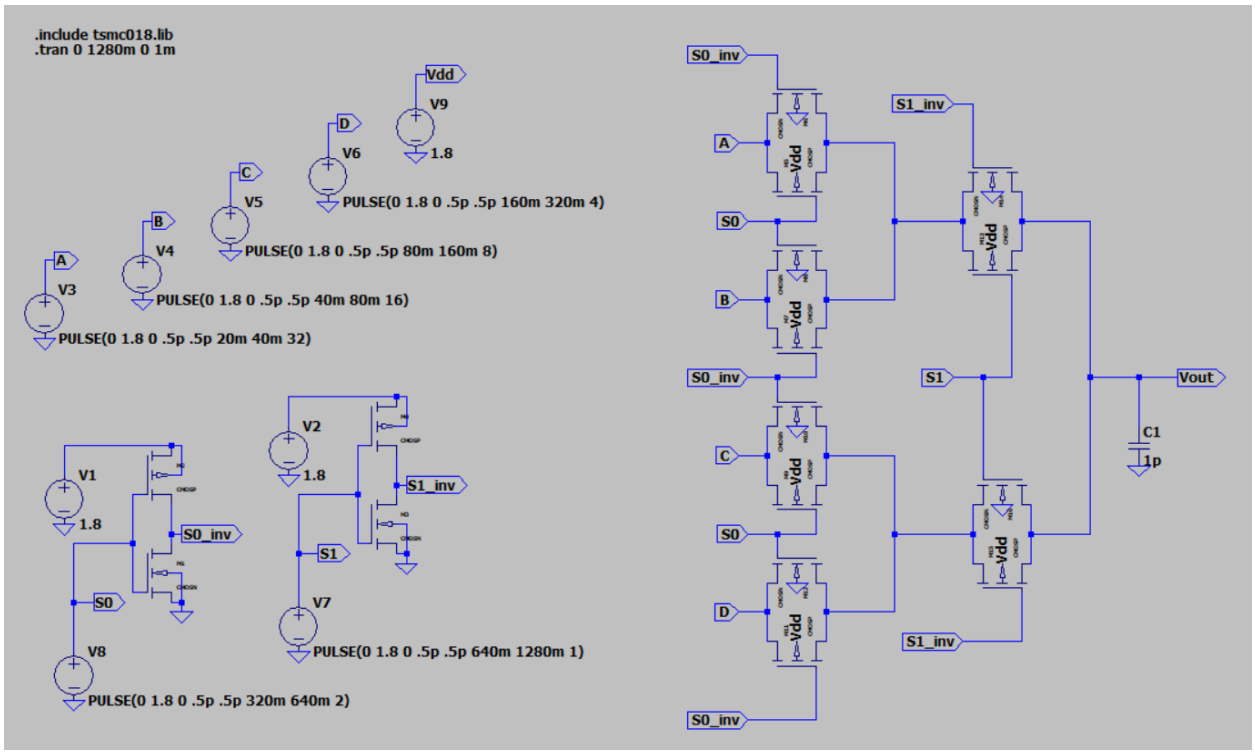
2) Implement 4:1 mux using transmission gates

CIRCUIT DIAGRAMS:

- ***2 Bit Adder (Pass Transistors)***

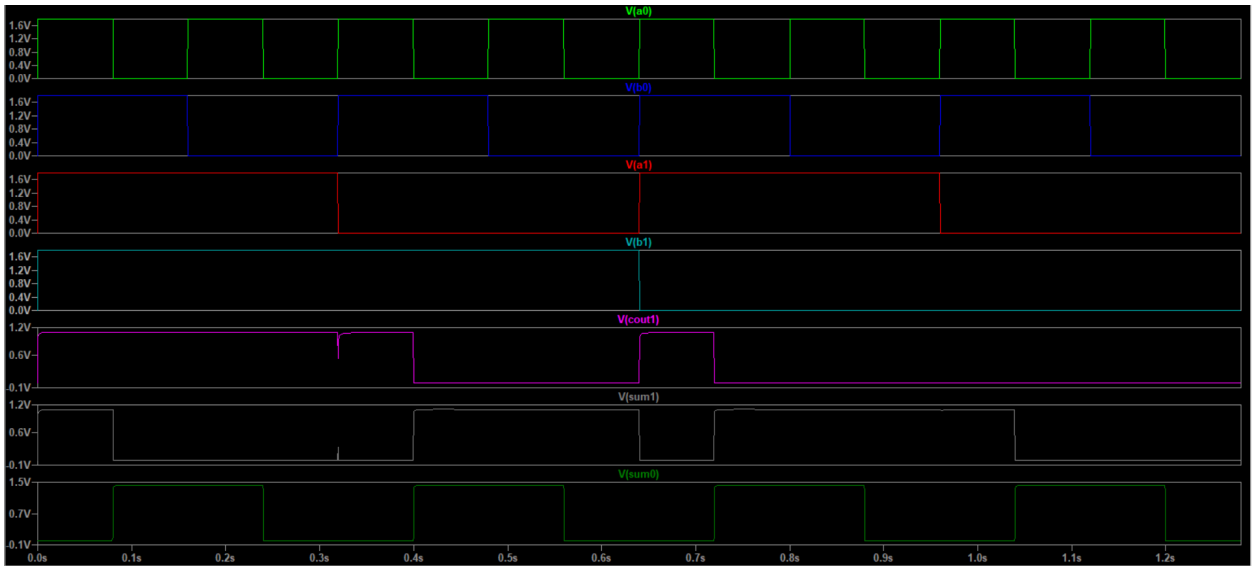


- ***4:1 MUX (Transmission Gates)***

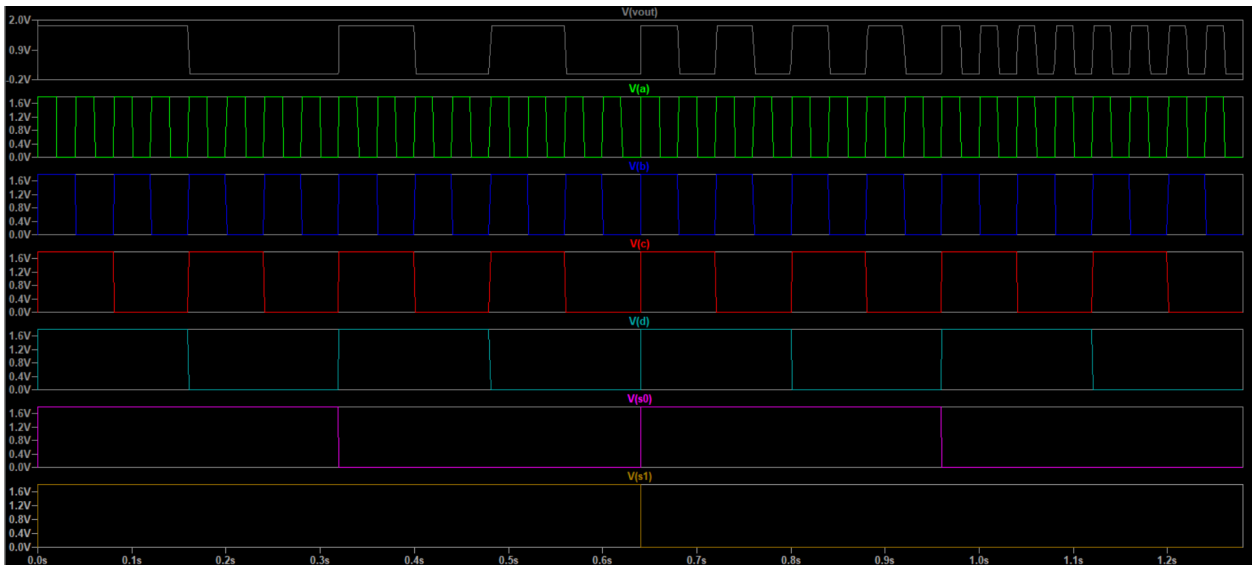


OUTPUT WAVEFORMS:

- ***2 Bit Adder (Pass Transistors)***



- ***4:1 MUX (Transmission Gates)***



DISCUSSION:

1. 2 Bit Adder (Pass Transistors)

- *In order to implement a 2bit full adder, we will make use of a 1bit half adder circuit which consists of an AND to give carry output and XOR gate to give sum output.*
- *We will need 2half adders and an OR gate to realize a 1bit full adder.*
- *So, in total, we need 3half adders and an OR gate to realize 2bit full adder.*
- *In order to realize the AND, XOR, OR gates, we are going to use pass transistor logic(PTL).*
- *Pass Transistor Logic (PTL) are generally superior to CMOS circuits interms of delay and power consumption.*
- *As we observe in the output waveform plots, the values of Sum0, Sum1, Cout1 are accurate to the expected values.*

  Sum0 = A0 ^ B0

  Sum1 = A1 ^ B1 ^ Cout0

  Cout1= A1 . B1 + Cout0 . (A1 ^ B1)
- *We observe that, there is still a bit of loss at each PTL gate level transmission.*
- *Initially our input was at Vdd=1.8V. After the first stage of half adder, we see a fall in Vmax which is now close to 1.42V, we can see in the plot for Sum0.*
- *For Sum1 and Cout1, the maximum voltage value goes further down to around 1.1V.*
- *In order to obtain inverted voltages for some of the pins, we are still using static CMOS logic, where the Vdd level is set according to the input's max voltage.*
- *We see small fluctuations in Sum1 and Cout1, which is most probably caused because of the different levels of max voltage for input pins(1.8V) and 1st stage pins(1.42V).*

2. 4:1 MUX (Transmission Gates)

- *We realize 4:1 MUX using 3' 2:1 MUX, where we have 4input bits and 2 select bits.*
- *Our 4:1 MUX will send one of the 4 input bits as output bit according a specific select bit combination.*
- *In our circuit, if select line is 00, Vout = A, if 01, Vout = B, if 10 Vout = C, if 11 Vout = D.*
- *We can write this in the form of a boolean logic,*

  Vout = A . S0' . S1' + B . S0 . S1' + C . S0' . S1 + D . S0 . S1
- *As we can observe the output waveform, we can clearly see the multiplexer working correctly.*
- *We implemented this circuit using transmission gates which are generally used in these analog multiplexers and bilateral switches.*
- *The advantage of this logic is that it can be implemented using less transistors compared to traditional CMOS logic, but this logic consumes more power.*