Year/Sem	Seat no.	Subject	Date	Sign	Page no.
SE / IV R2019	RWM4181	Microprocessor	10/06/21	Kunj	1/6

Question no.:- Q. 2(A)

-> Interrupt is the method of creating a temporary halt during program execution and allows peripheral devices to access the microprocessor. The microprocessor responds to that interrupt with an ISR (Interrupt Service Routine), which is a short program to instruct the microprocessor on how to handle the interrupt.
The types of interrupts present in 8086 microprocessors are as follows:-

1] Hardware Interrupt.
2] Software Interrupt.

1] Hardware Interrupt:- Hardware interrupt is caused by any peripheral device by sending a signal through a specified pin to the microprocessor. The 8086 has two hardware interrupt pins, i.e. NMI and INTR. NMI is a non-maskable interrupt and INTR is maskable interrupt having lower priority. One more interrupt pin associated is INTA called interrupt acknowledge.

2] Software Interrupt:- Some instructions are inserted at the desired position into the program to create interrupts. These interrupts instructions can be used to test the working of various interrupt handlers. Types:- (i) Normal interrupts and (ii) Exception.

(P.T.O.)

Year/Sem	Seat no.	Subject	Date	Sign	Page no.
SE / IV R2019	RWM4181	Microprocessor	10/06/21	Kunj	2/6

Question no. :- Q.2(A)

Interrupt vector table:- Interrupt vector table on 8086 is a vector that consists of 256 total interrupts placed at first 1 kb of memory from 0000h to 03ffh, where each vector consists of segment and offset as a lookup or jump table to memory address of bios interrupt service routine (f000h to ffffh) or dos interrupt service routine address, the call to interrupt service routine address, the call is similar to far procedure call. The size of for each interrupt vector is 4 bytes (2 word in 16 bit), where 2 bytes (1 word) for segment and 2 bytes for offset of interrupt service routine address.

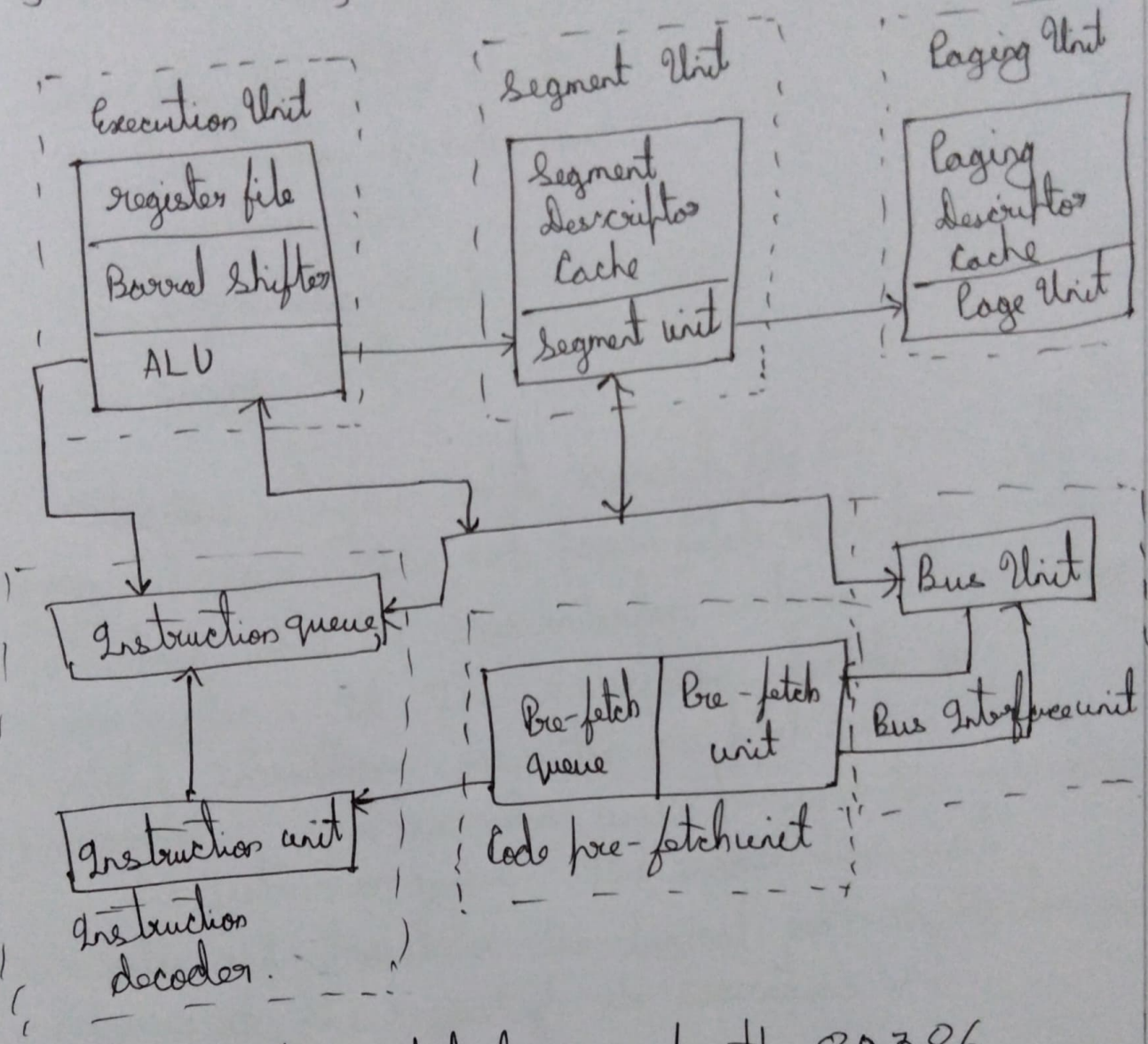
Year/Sem	Seat no.	Subject	Date	Sign	Page no.
SE/IV R2019	RWM4181	Microprocessor	10/06/21	Kuri	3/6

Question no.: Q.2(D)

→ Attribute	8086	80386	Pentium
Processor size	16 bit	32 bit	32 bit
Data bus size	16 bit	32 bit	64 bit
Address Bus size	20 bit	32 bit	32 bit
Physical memory	1 MB	4 GB	4 GB
Segmentation	Yes	Yes	Yes
Paging	No	Yes	Yes
Protection	No	Yes	Yes
Pipeline level	2 stage	3 stage	5 Stage
Brand prediction	No	No	Yes
Cache	No	Yes	Yes
On Chip L1 Cache	No	No	Yes, 16KB
Out of order execution	No	No	No.
Year of Release	1978	1985	1993

Year/Sem	Seat No.	Subject	Date	Sign	Page No.
SE / IV R2019	RWM4181	Microprocessor	10/06/21	Kunj	4/6

Question no. : Q. 2 (E)



→ The internal architecture of the 80386 includes six functional units that operate in parallel. The parallel operation is called as pipeline processing. Also, the six functional units of 80386 architecture are :

1] Bus Interface Unit.

Year / Sem	Seat No.	Subject	Date	Sign	Page no.
SE / IV R2019	RWM4181	Microprocessor	10/06/21	Kunj	5/6

Question no.: Q.2(E)

2] Code Pre-fetch Unit
3] Instruction decoder unit
4] Execution Unit
5] Segmentation Unit
6] Paging Unit.

The Bus interface unit connects the 80386 with memory and I/O. The code pre-fetch unit pre-fetches instructions when the bus interface unit is not executing the bus cycles. The instruction decode unit translates instructions from the pre fetch queue into microcode. The execution unit processes the instructions from the instruction queue. The segmentation unit calculates and translates the logical address into linear addresses at the request of the execution unit.

Year/Sem	Seat no.	Subject	Date	Sign	Page no.
SE/IV R2019	RWN4181	Microprocessor	10/06/21	Kunj	6/6

Question no.:- Q.2(F)

→ Operating modes of 80386 are as follows:-

1] Real Mode:- Unlimited direct software access to all memory, I/O address & hardware.

2] Protected Mode:- (i) It allows system software to use features such as virtual memory, paging and safe multi-tasking designed to increase an operating system's control over application software. (ii) It begins executing instruction in real mode. (iii) It starts after the system software sets up several descriptor tables and enables the Protection Enable (PE) bit in the control register 0.

3] Virtual Mode:- Allows the execution of real mode applications that are incapable of running directly in protected mode.

4] Paging:- Organize the available physical memory in to 4 kb size each, under segmented memory.